The DAQ Status of JadePix3

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September 14, 2020
JadePix3 Weekly Meeting

Outline

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The Status of Firmware

Checked logic:

1. DAC70004 ILA timing
   - SYNC signal logic fixed
   - BUSY signal set high as active, and it's monitored by IPbus. (DAC status is checked before sending next command).
2. JadePix3 SPI ILA timing
   - Data sequence was wrong, this bug has been fixed.
   - MOSI is not clean: around the active spi data, there are some useless data exists, and the SCLK is low. This bug has been fixed.
   - Not tested MISO yet.

Unchecked logic:

1. Jadepix3 configuration ILA timing
2. Jadepix3 rolling shutter mode ILA timing
3. Jadepix3 Global shutter mode ILA timing

Outline

Software Status

- Structure and logic are optimized. See more details in code repository.

Summary and Outlook

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1. Finished FW and SW of chip control logic, and they are under testing via vivado ILA.

Outlook

1. Discussion on data readout logic...