Jadepix3 FW and SW Status

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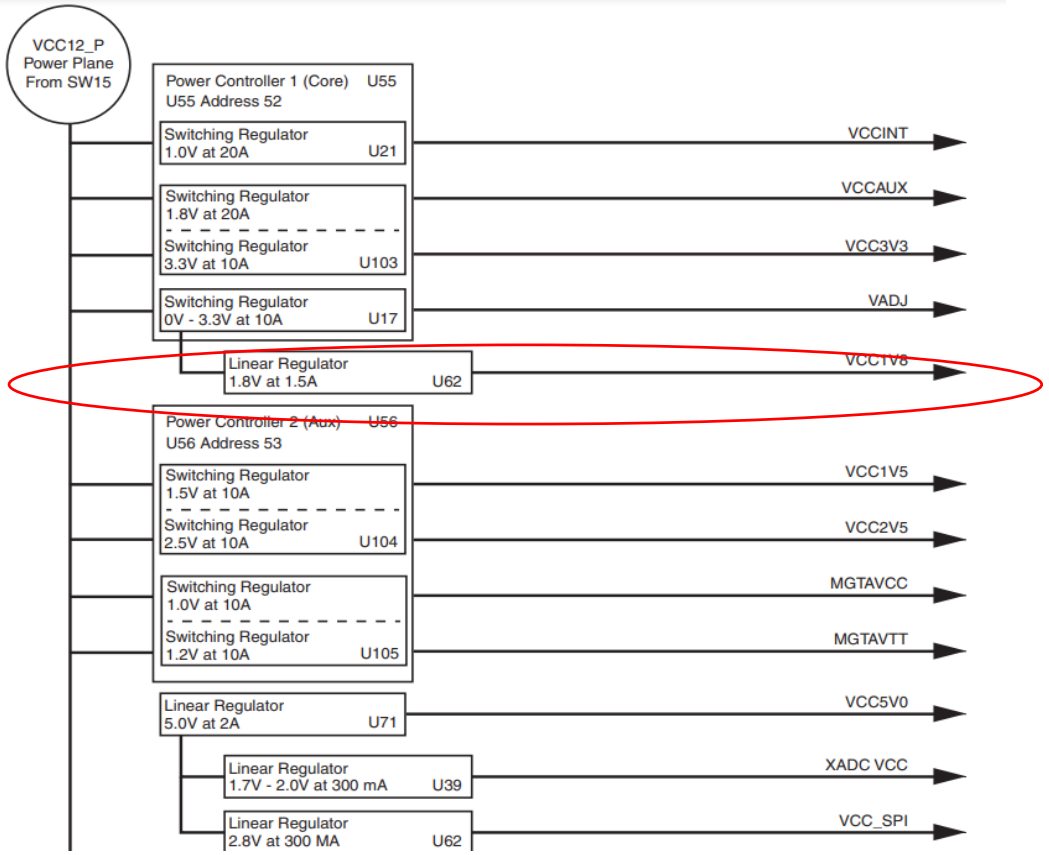
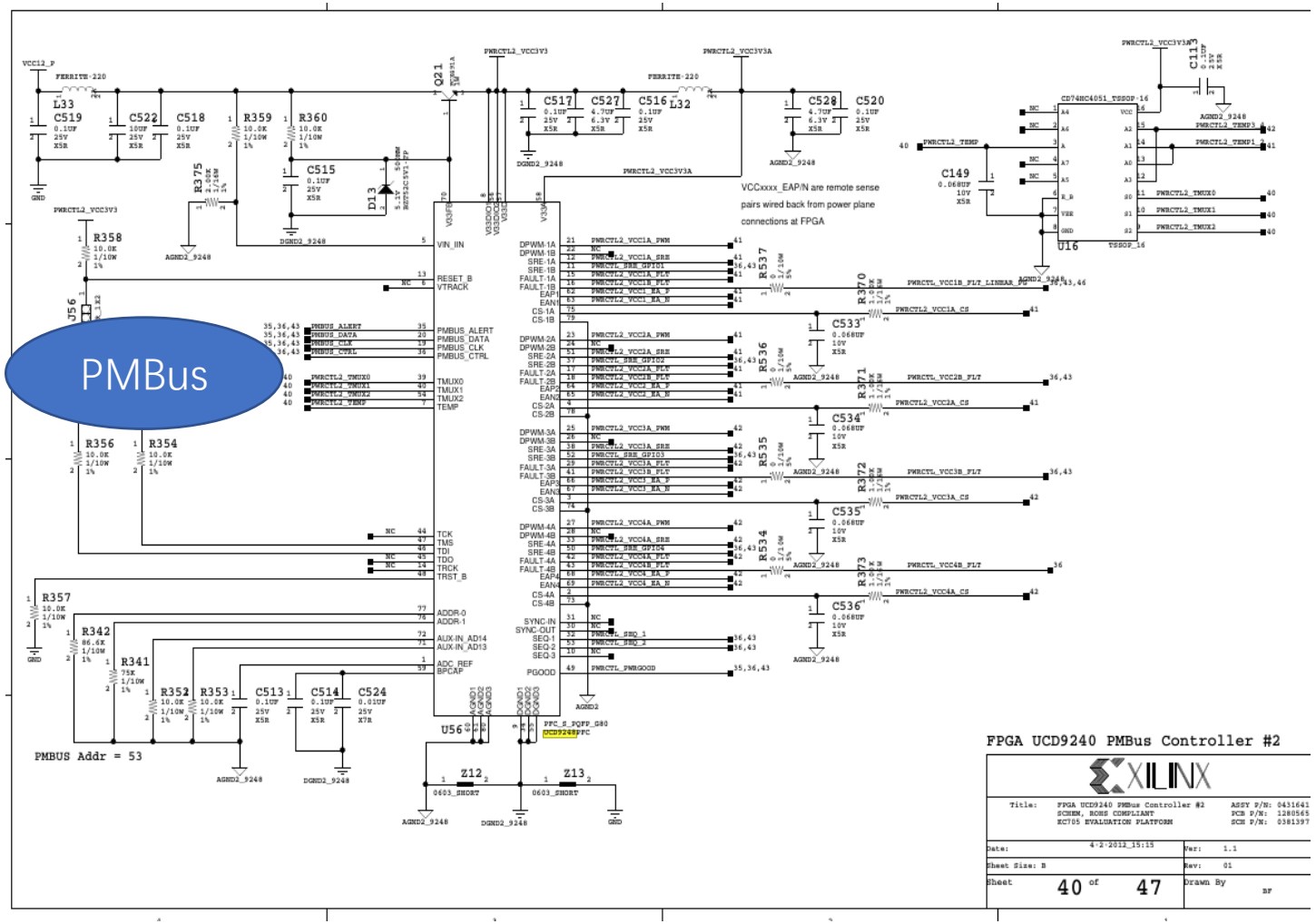
FPGA VADJ





UCD9248： Digital PWM System Controller
PTD08A010W: DIGITAL POWERTRAI MODULE

FMC VADJ Adjustment

FMC_VADJ Voltage Control

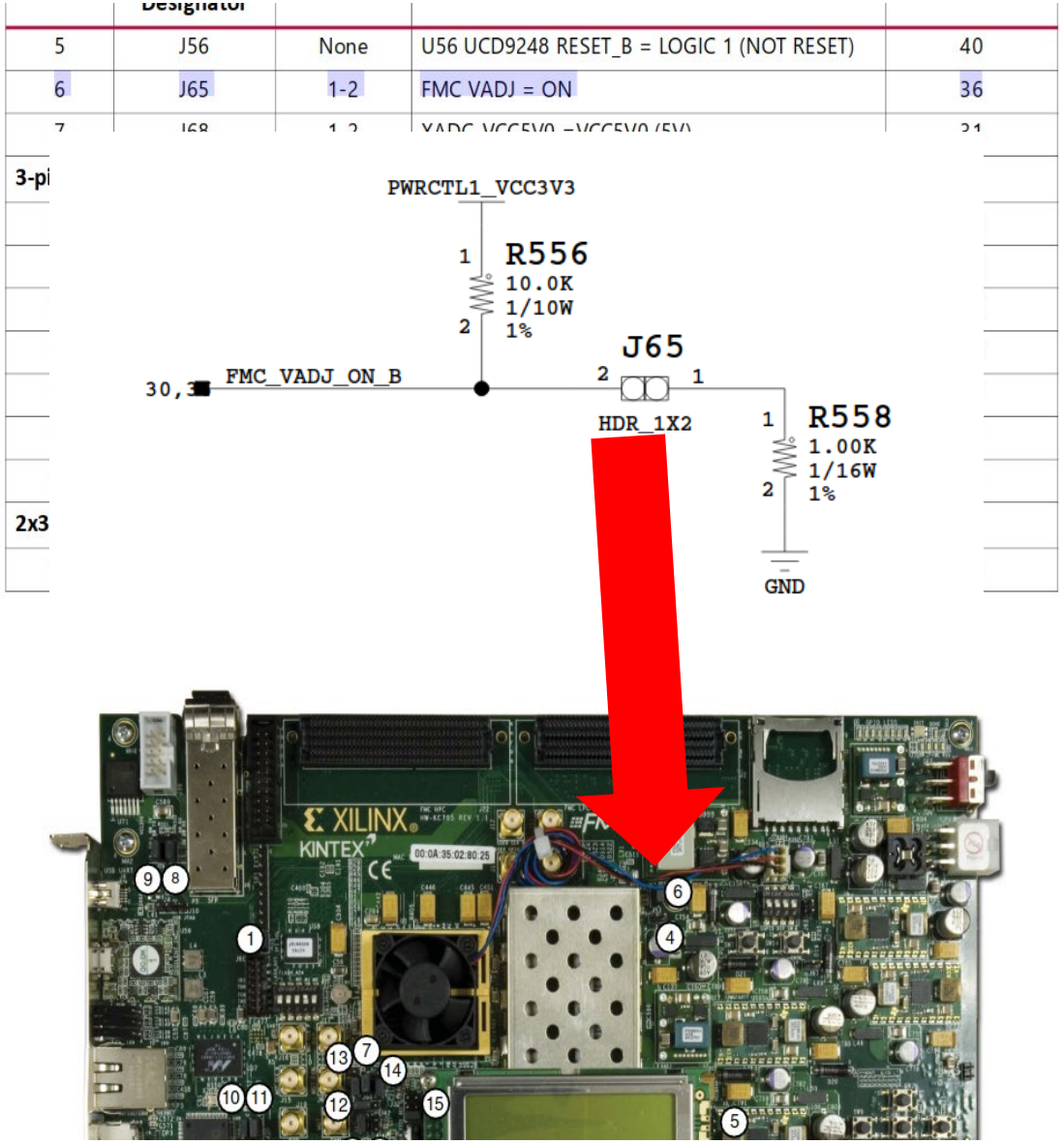
The FMC_VADJ rail is set to 2.5V. When the KC705 board is powered on, the state of the FMC_VADJ_ON_B signal wired to header J65 is sampled by the Texas Instruments UCD9248 controller U55. If a jumper is installed on J65, signal FMC_VADJ_ON_B is held low, and the TI controller U55 energizes the FMC_VADJ rail at power on.

Because the rail turn on decision is made at power on time based on the presence of the J65 jumper, removing the jumper at J65 after the board is powered up does not affect the 2.5V power delivered to the FMC_VADJ rail and it remains on.

A jumper installed at J65 is the default setting.

If a jumper is not installed on J65, signal FMC_VADJ_ON_B is High, and the KC705 board does not energize the FMC_VADJ 2.5V at power on. In this mode you can control when to turn on FMC_VADJ and to what voltage level (1.8V - 3.3V). With FMC_VADJ off, the FPGA still configures and has access to the TI controller PMBUS (on bank 32) along with the FMC_VADJ_ON_B signal (on bank 15 pin J27). The combination of these allows you to develop code to command the FMC_VADJ rail to be set to something other than the default setting of 2.5V. After the new FMC_VADJ voltage level has been programmed into TI controller U55, the FMC_VADJ_ON_B signal can be driven Low by the user logic and the FMC_VADJ rail comes up at the new FMC_VADJ voltage level. Installing a jumper at J65 after a KC705 board powers up in this mode turns on the FMC_VADJ rail.

For Texas Instruments fusion tools documentation describing PMBUS programming for the UCD9248 digital power controller, see [Ref 20].



UG810: KC705 Evaluation Board for the Kintex-7 FPGA

FMC VADJ Adjustment

USB-GPIO

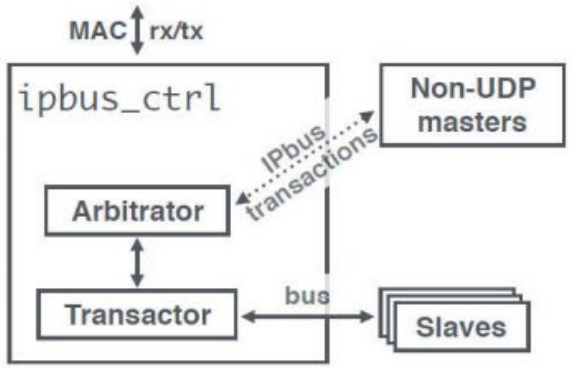
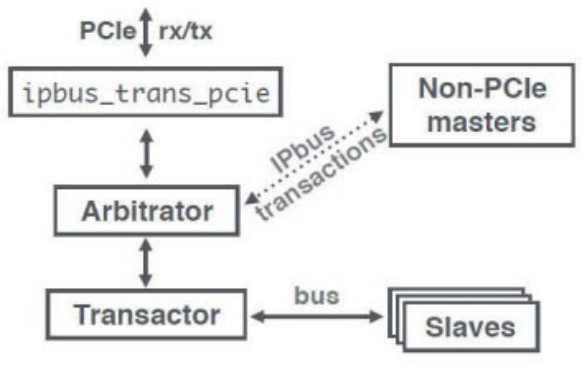
- Three methods to adjust:
  - 1. TI USB-GPIO. (~900 CNY)
    - Digikey: https://www.digikey.cn/products/zh?WT.z_header=search_go&keywords=%20USB-TO-GPIO%20
    - Manual: https://www.xilinx.com/Attachment/KC705_Power_Controllers_Reprogramming_Steps.pdf)
  - 2. PMBus programing, via software of firmware. Complex and not safe!
  - 3. ~~Resistor replacement, ugly and not safe!~~

Data Link Upgrade, IPbus-FIFO -> IPbus-PCIe

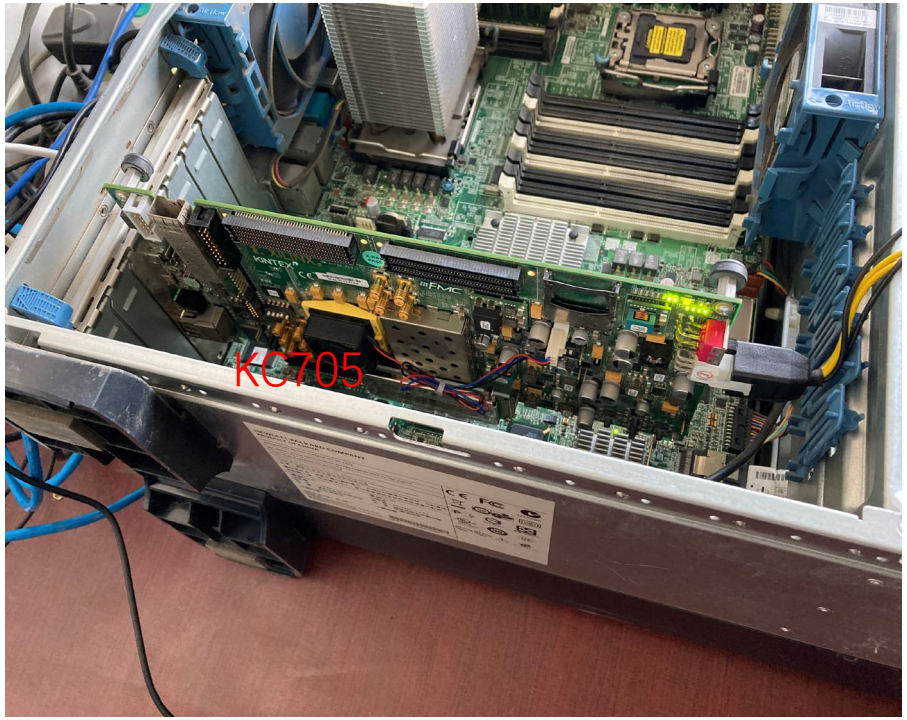
Ethernet vs PCIe: User point of view

	Ethernet	PCIe

SW	`using namespace uhal;`
	`HwInterface hw("chtcp-2.0://…");`
	
	`auto x = hw.getNode("reg1").read();`
	`auto y = hw.getNode("reg2").read();`
	`hw.dispatch();`
	
	`cout << "reg1 = " << x << endl;`
	`cout << "reg2 = " << y << endl;`
		`using namespace uhal;`
		`HwInterface hw("ipbuspcie-2.0://…");`
		
		`auto x = hw.getNode("reg1").read();`
		`auto y = hw.getNode("reg2").read();`
		`hw.dispatch();`
		
		`cout << "reg1 = " << x << endl;`
		`cout << "reg2 = " << y << endl;`

FW		

Slide courtesy: T. Williams



0. IPbus_PCIe link pass
1. IPbus PCIe link + UDP link
2. IPbus PCIe link only