Status of CEPC HCAL

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CEPC Day

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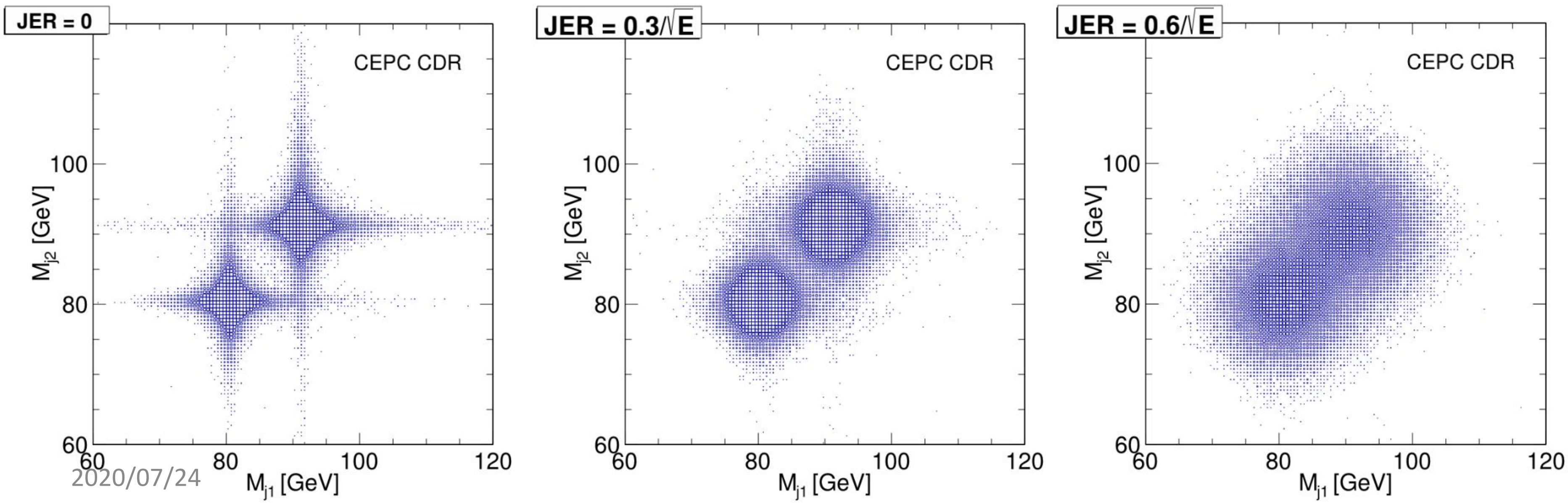
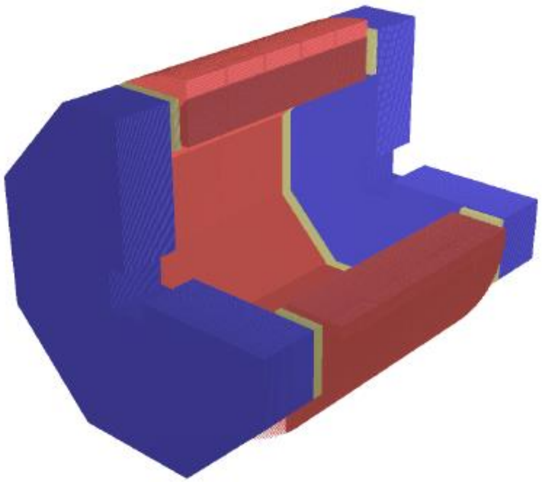
Requirements of CEPC Calorimeters

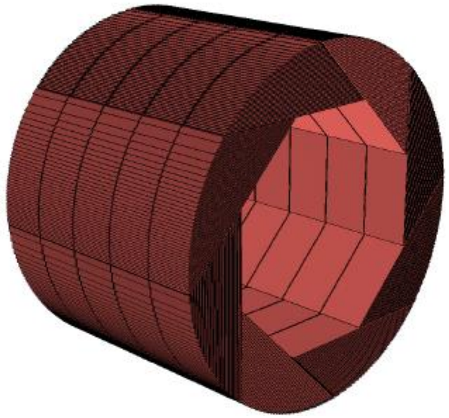
Physics process	Measurands	Detector subsystem	Performance requirement
$ZH, Z \to e^+e^-, \mu^+\mu^-$ $H \to \mu^+\mu^-$	$m_H, \sigma(ZH)$ $\mathrm{BR}(H \to \mu^+\mu^-)$	Tracker	$\Delta(1/p_T) =$ $2 \times 10^{-5} \oplus \frac{0.001}{p(\mathrm{GeV}) \sin^{3/2}\theta}$
$H \to b\bar{b}/c\bar{c}/gg$	$\mathrm{BR}(H \to b\bar{b}/c\bar{c}/gg)$	Vertex	$\sigma_{r\phi} =$ $5 \oplus \frac{10}{p(\mathrm{GeV}) \times \sin^{3/2}\theta} (\mu\mathrm{m})$
$H \to q\bar{q}, WW^*, ZZ^*$	$\mathrm{BR}(H \to q\bar{q}, WW^*, ZZ^*)$	ECAL HCAL	$\sigma_E^{\mathrm{jet}}/E =$ $3 \sim 4\%$ at 100 GeV
$H \to \gamma\gamma$	$\mathrm{BR}(H \to \gamma\gamma)$	ECAL	$\Delta E/E =$ $\frac{0.20}{\sqrt{E(\mathrm{GeV})}} \oplus 0.01$

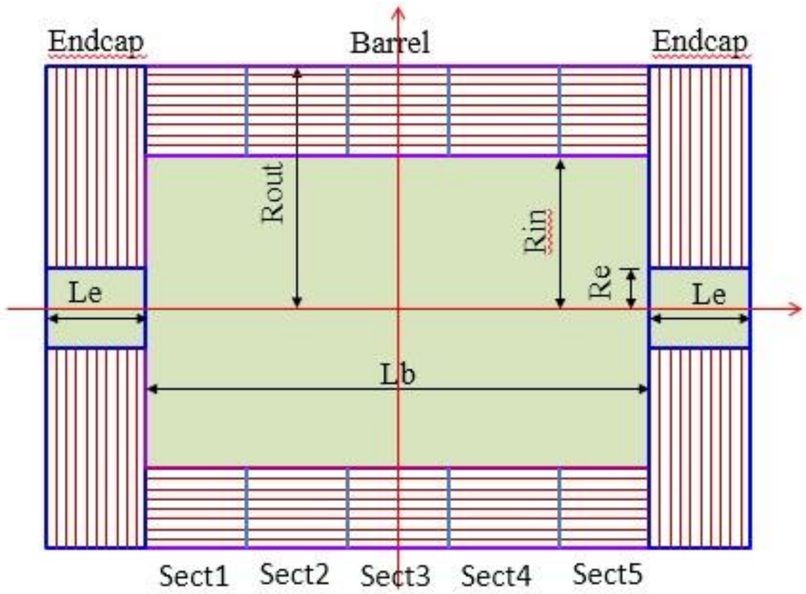


CEPC HCAL: Geometry and Layout

SDHCAL

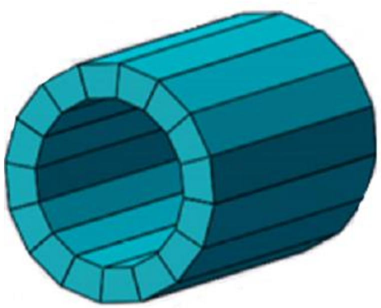




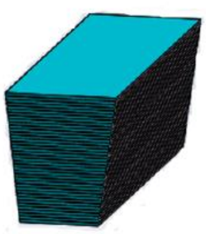


AHCAL

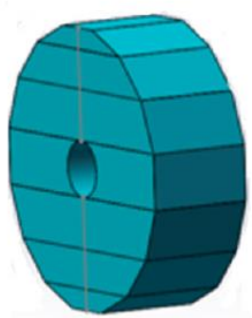
AHCAL barrel



AHCAL super module



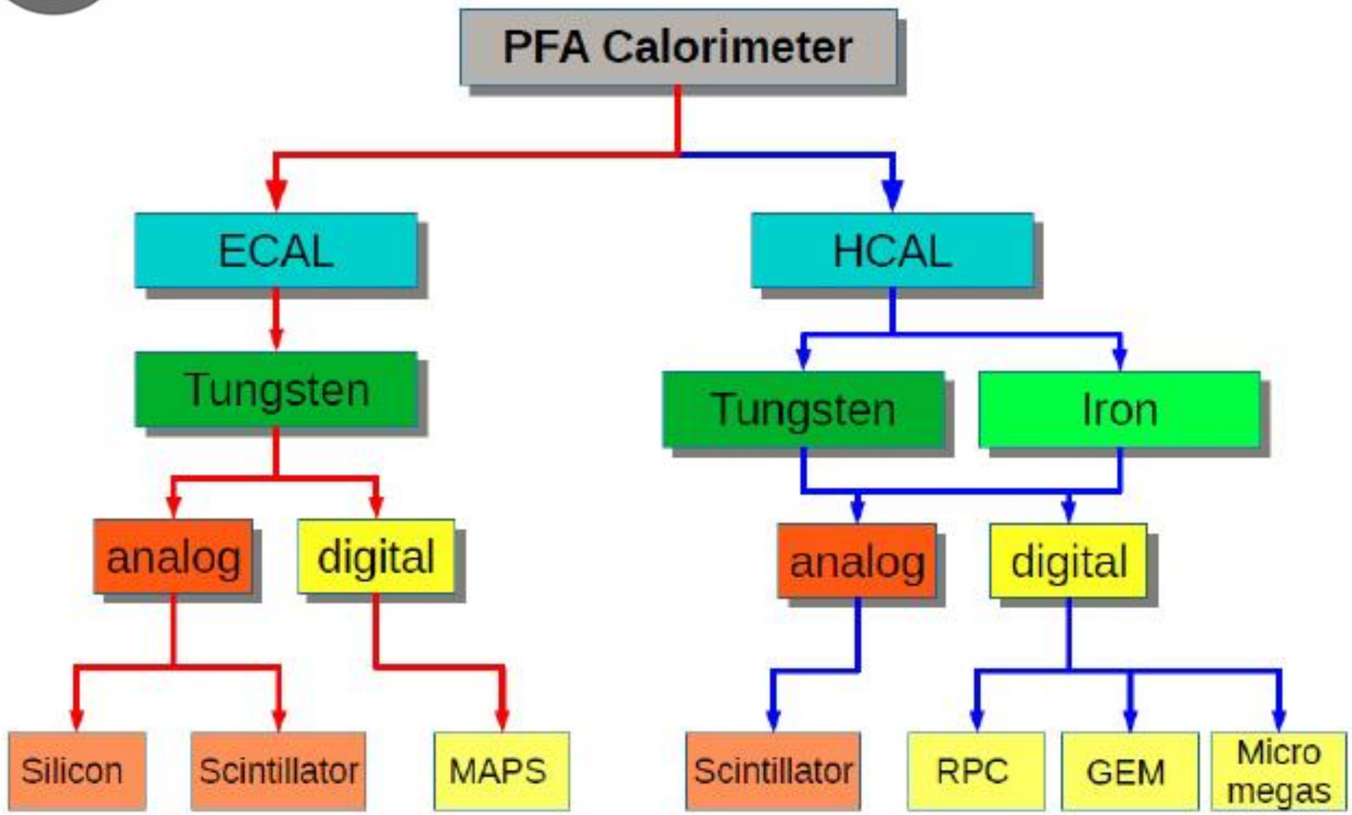
AHCAL endcap



- Inner radius in X-Y plane R_{in} = 2300mm
- Outer radius R_{out} = 3340mm
- Inner & outer of HCAL endcap in Z-axis are 2670mm and 3710mm

PFA Calorimeters

https://twiki.cern.ch/twiki/bin/view/CALICE/CalicePapers



AHCAL: Scintillator + SiPM
SDHCAL: RPC & MPGD

Outline

■Status of AHCAL

- Measurements of new NDL SiPMs
- Light output and uniformity test of AHCAL tiles
- Assembly of scintillator testing platform
- Testing of KLauS chips

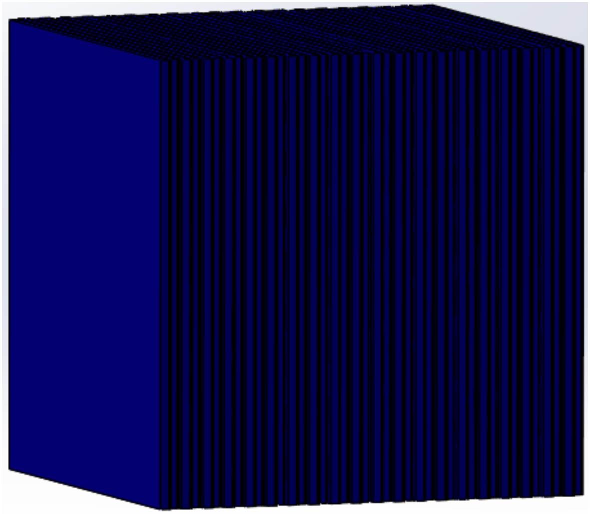
■Status of SDHCAL

- TMVA-ParticleID with TB data
- 5D HCAL with position(x,y,z), energy and timing
- GRPC Construction and Test

CEPC AHCAL Prototype

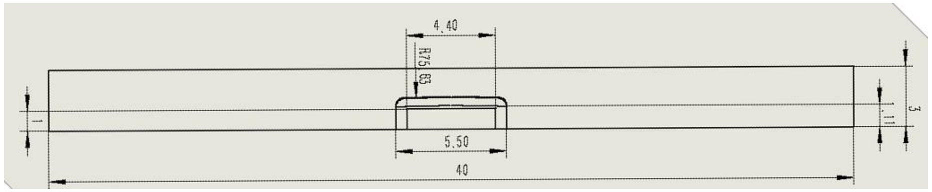
Requirement of JER

$$\frac{\sigma}{E} = \frac{60\%}{\sqrt{E}} \oplus 3\%$$

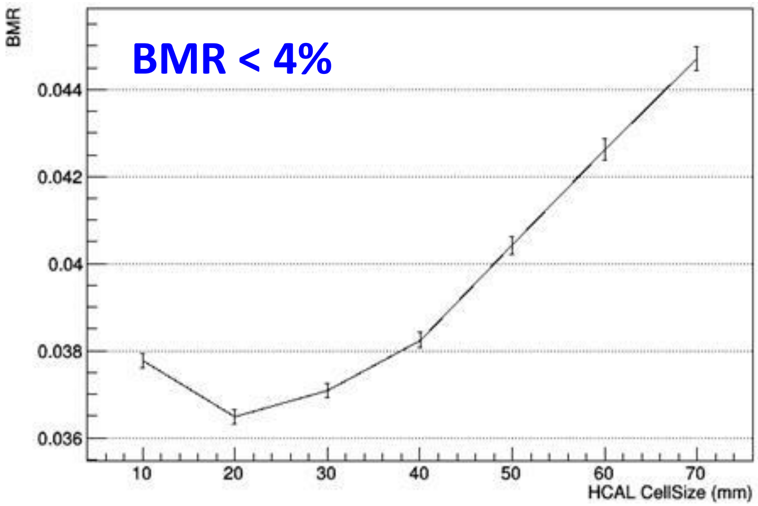


- Absorber: 2 cm Stainless steel ($0.12\lambda_I$, $1.14X_0$);
- Sensitive detector : Scintillator (cell: 4x4cm^2);
- SiPMs: HMAMMATSU vs NDL;
- About 40 layers, readout channels: 12960
- Dimension: 72 cm*72 cm (cell: 4x4cm^2)

- **New structure of 4cm x 4cm x 3mm**



BMR: Boson Mass Resolution at di-jet
BMR*sqrt(2) = Jet Energy Resolution

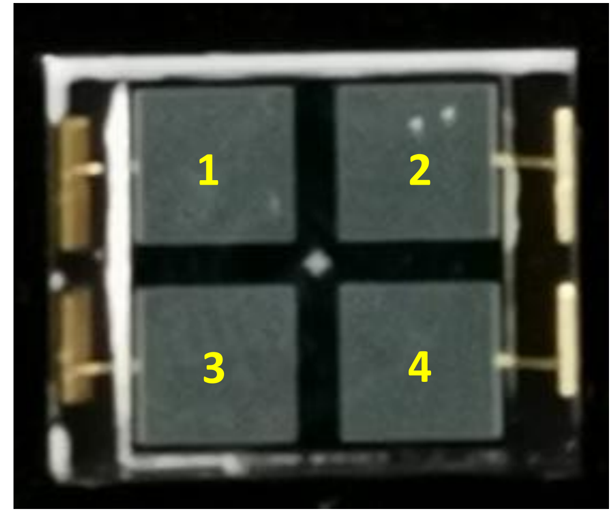


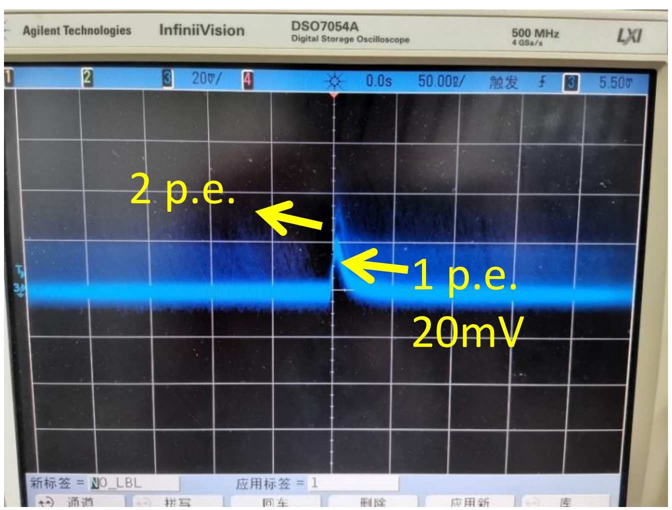
BMR - HCAL Cell Size

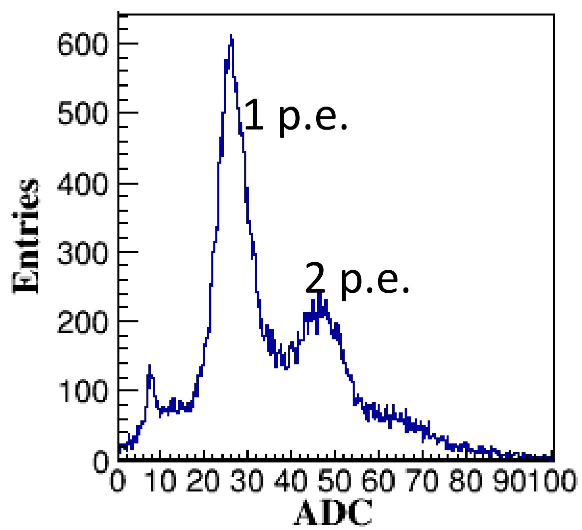
SiPM: NDL 22-1313-15S

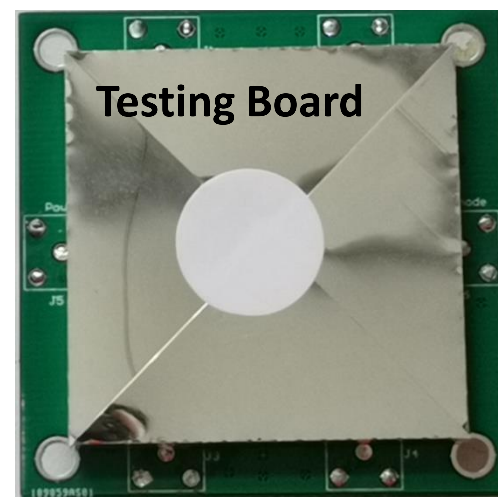
- To get more light output combined with new design of AHCAL tiles of 4x4cm^2.

Breakdown[V]	19
PDE@400nm [%]	45
Transverse dimension [mm^2]	4.45×3.65
Thickness [mm]	0.95
Number of Pixel	7400×4





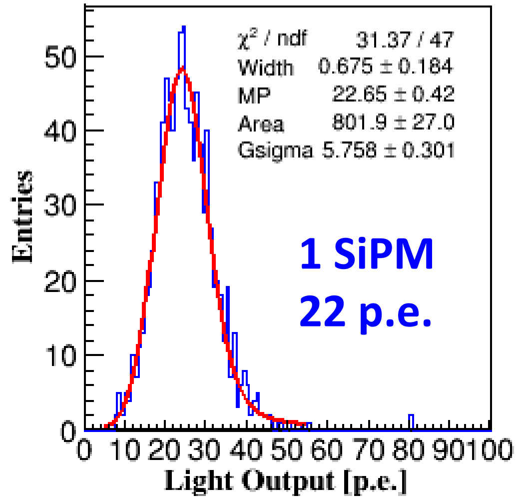


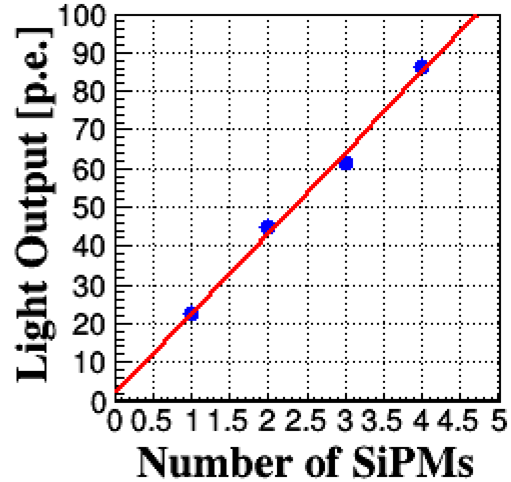


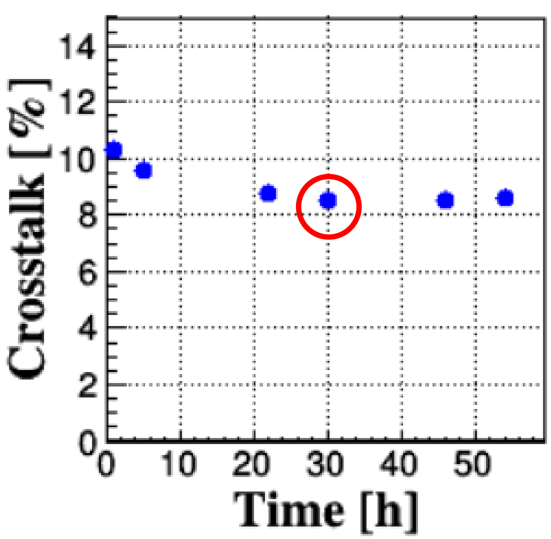
SiPM: Light Output

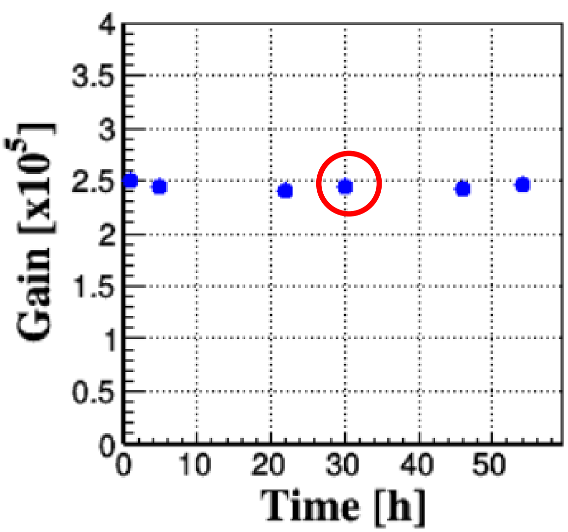
Testing parameters

- **Voltage: 23V**
- **Scintillator:**
  Thermal polymerization
- **SiPMs: NDL 22-1313-15S**









Stable point:

- Gain:2.44× 10^5
- DCR:330,574 Hz
- CT: 8.5%
- Dark current:1.48 uA

SiPM: Comparison of NDL

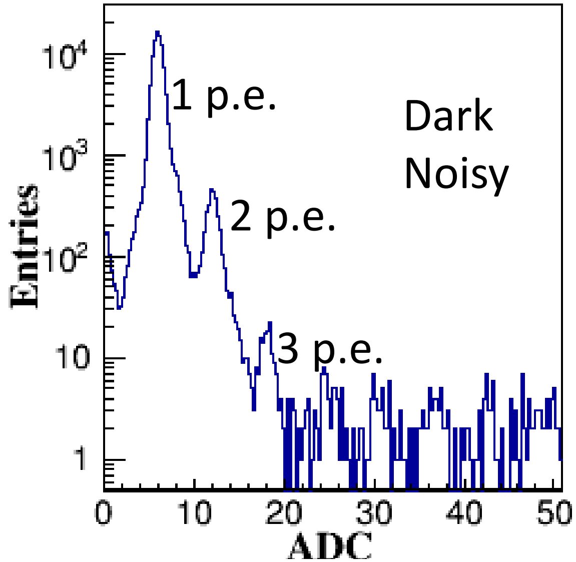
Company	NDL				
Type	1010C	3030C	125	15	**22-15**
Active area[mm^2]	1	9	1	1	1.69
Pixel number	10000	90000	6400	4300	7400
Breakdown[**V**]	27.5	27.5	21.5	19.5	19
Overvoltage[**V**]	6.5	6.5	3	4	4
Dark counts[**kHz**]	550	5150	470	380	330
Crosstalk[**%**]	4.4	8	8.1	9.7	8.5
Gain[10^5]	1.295	1.3	1.91	3.01	2.44

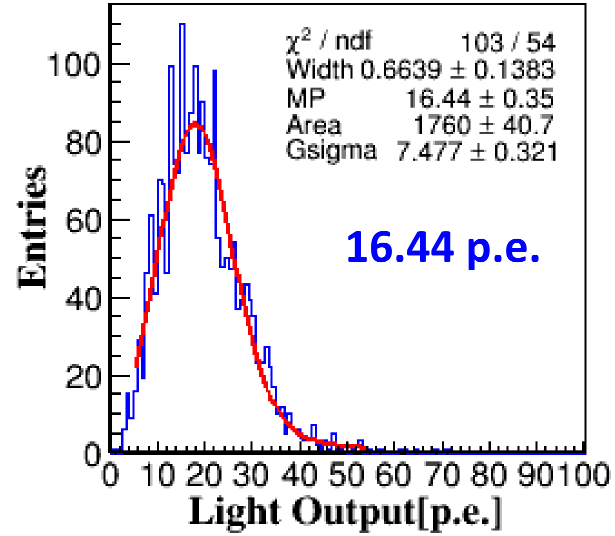
➔ Comparing with NDL 1010-15, new type NDL SiPM 22-1313-15S decreases of Crosstalk , DCR and Gain !

SiPM: Comparison with HAMAMATSU

13360-1325PE

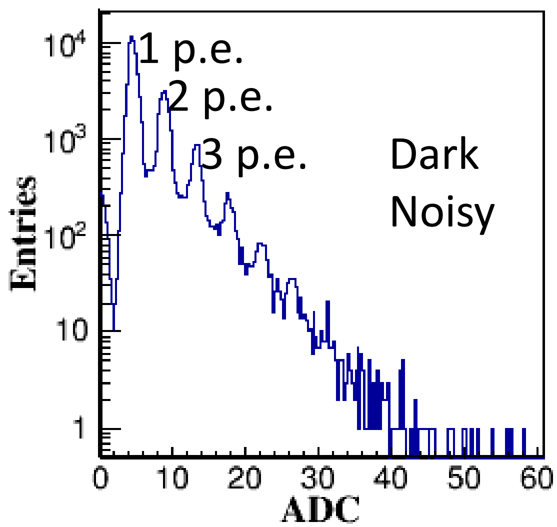
- Voltage: 58V
- Scintillator: Thermal Polymerization
- Light ouput: 16.4 p.e.

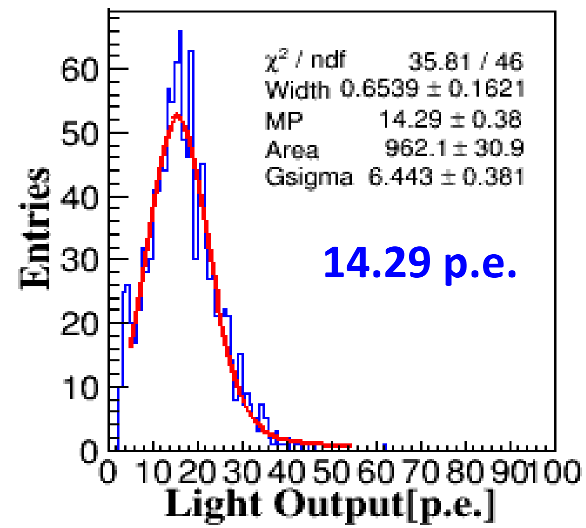




12571-025P

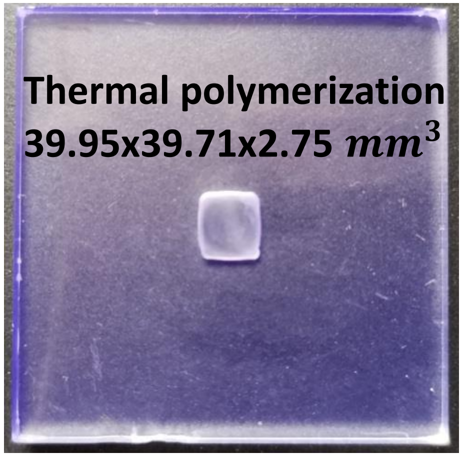
- Voltage: 67.4V
- Scintillator: Thermal Polymerization
- Light output: 14.3 p.e.

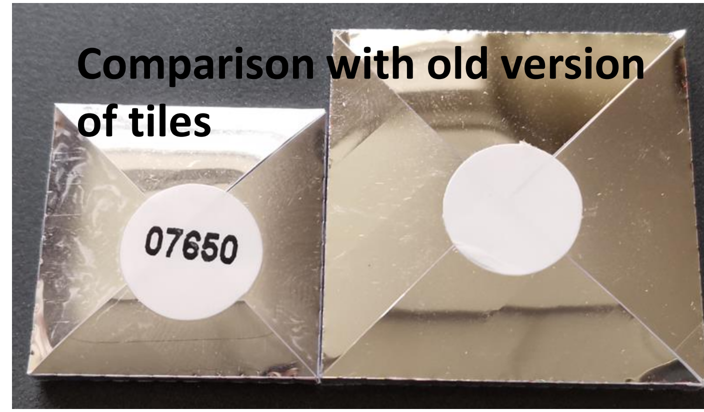




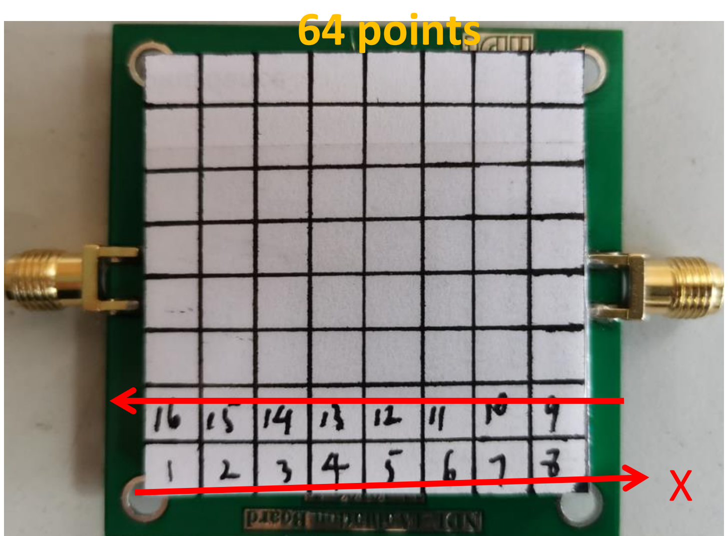
NDL-22-1313-15S has light output: 22 p.e.

Scintillator: Uniformity Test

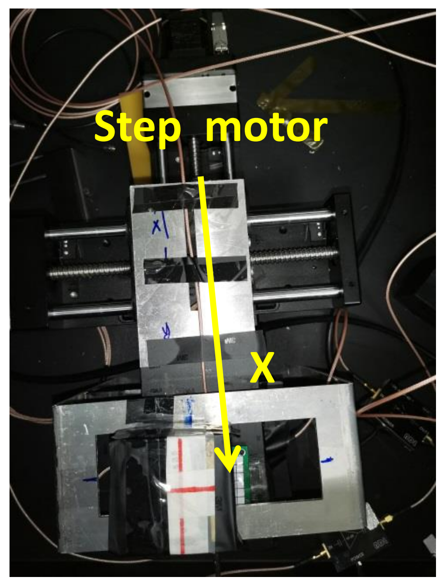


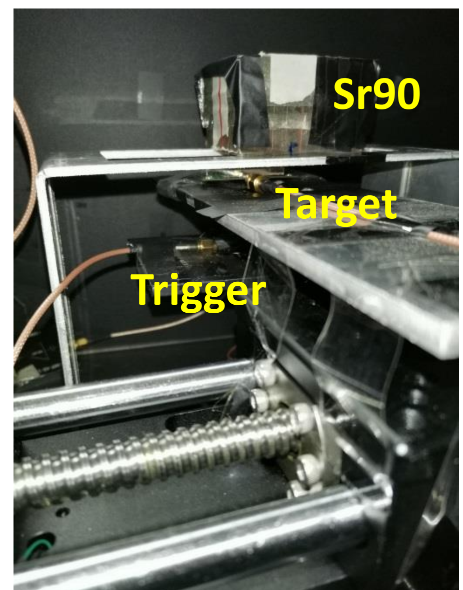


Uniformity testing region



apparatus

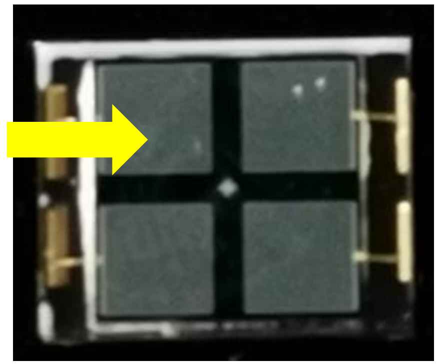




Scintillator(PS): Uniformity of Tiles

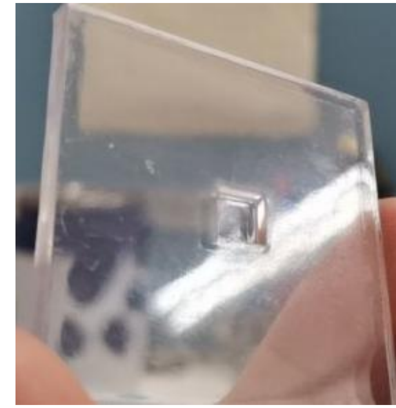
Injection molding scintillators within a batch (Polystyrene)

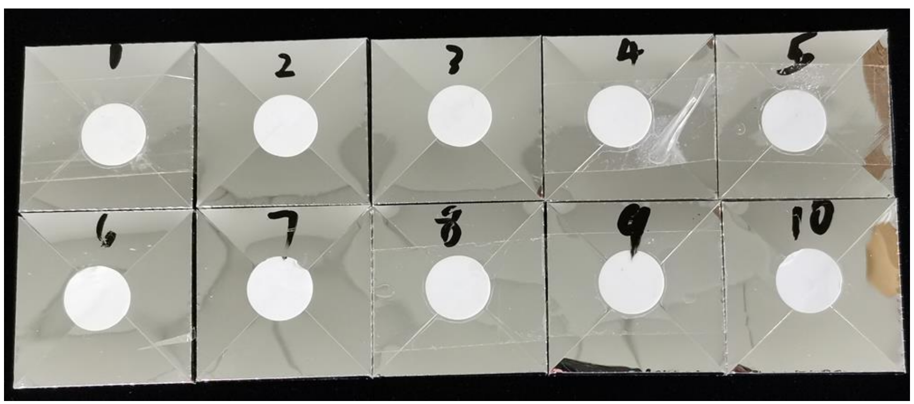
- Number of SiPM: 1
- Voltage:23V
- Tiles: PS

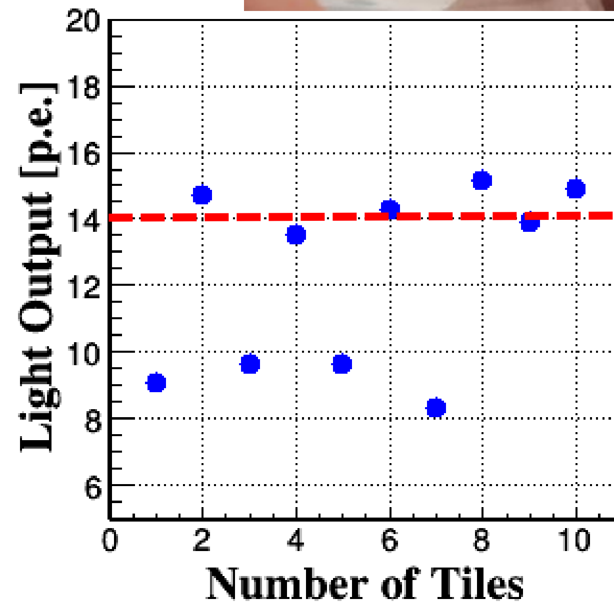


Injection craft:

- Massive production
- High efficiency
- Consistency





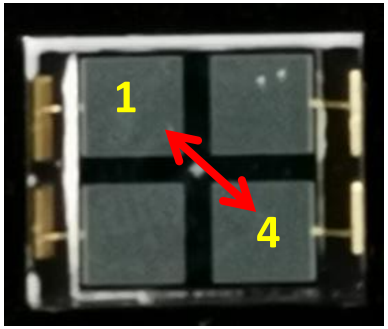


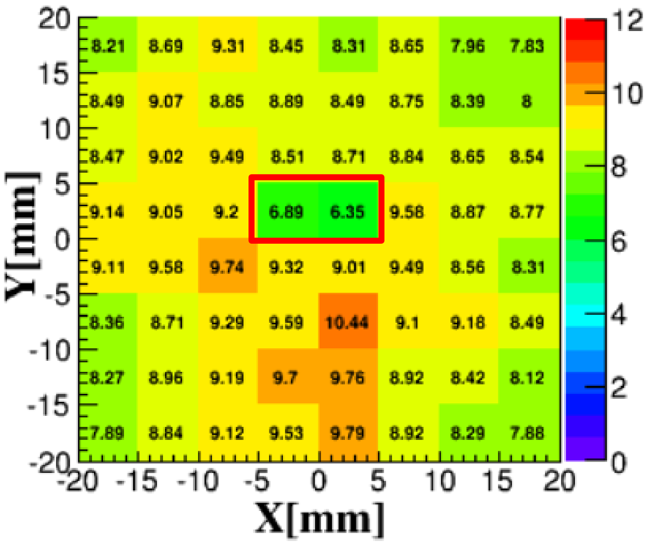
■ **Two obviously different light output within a same batch of PS tiles.**

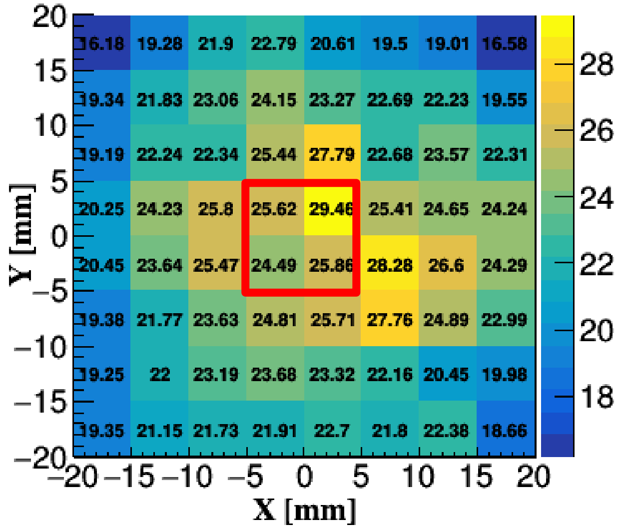
Light Output Uniformity within a Tile

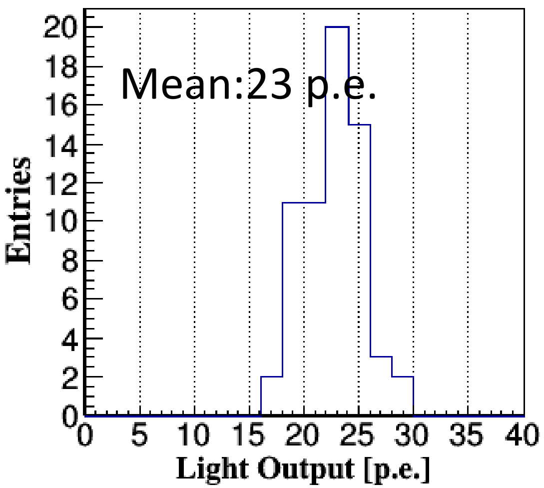
- SiPM: NDL-1010C
- Voltage: 33V
- Scintillator : TP tile

NDL-22-1313-15S
- Voltage: 23V
- Scintillator: PS tile





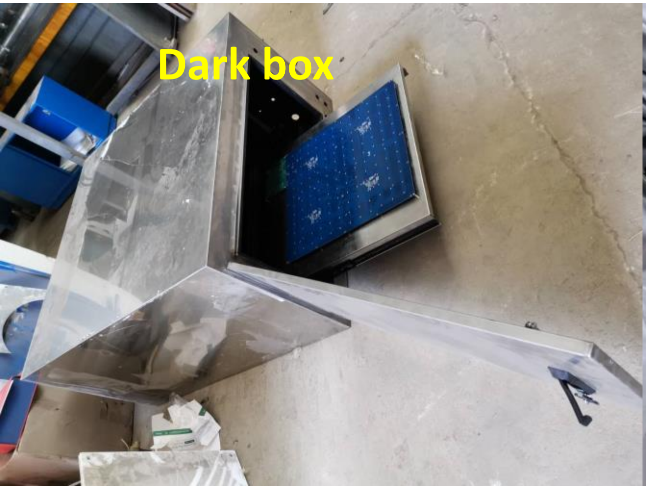


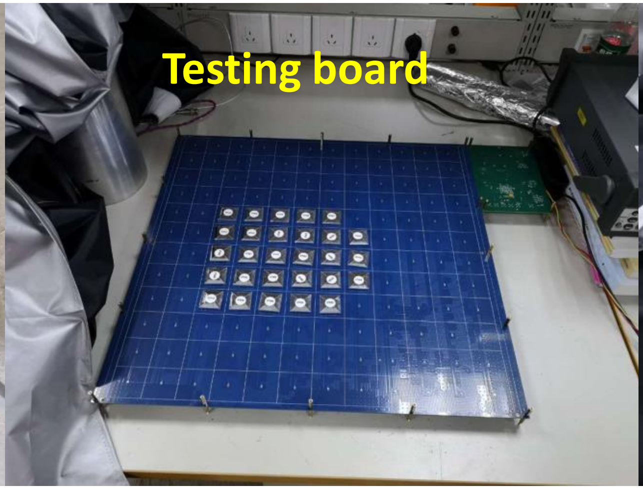


- **Light output is uniform in cavity of tiles read out by 2 diagonal SiPMs.**

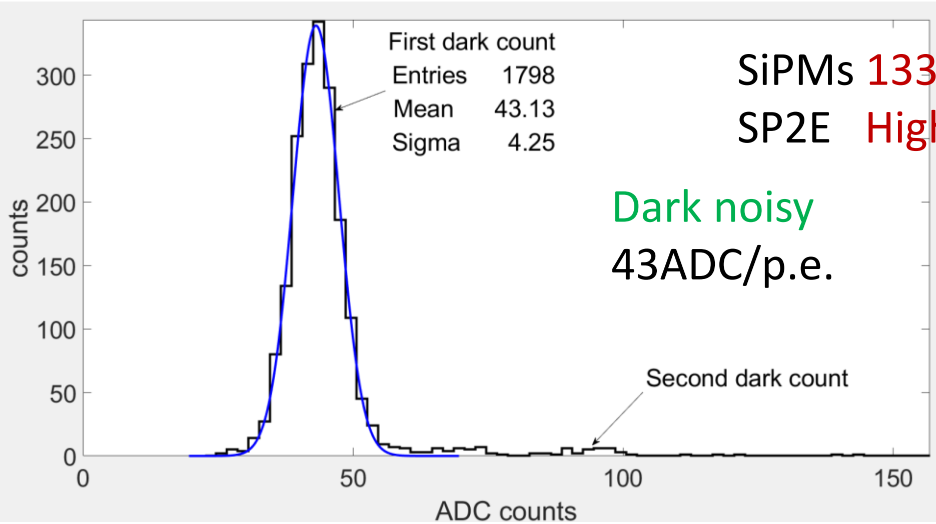
Scintillator Testing Platform (STP)

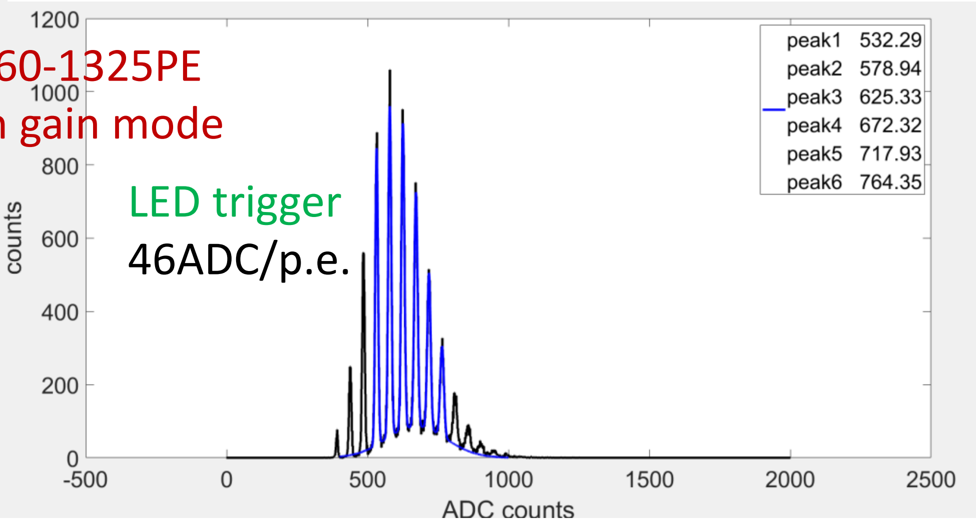
STP of AHCAL Quickly check the uniformity among detector cells





SiPMs 13360-1325PE
SP2E High gain mode



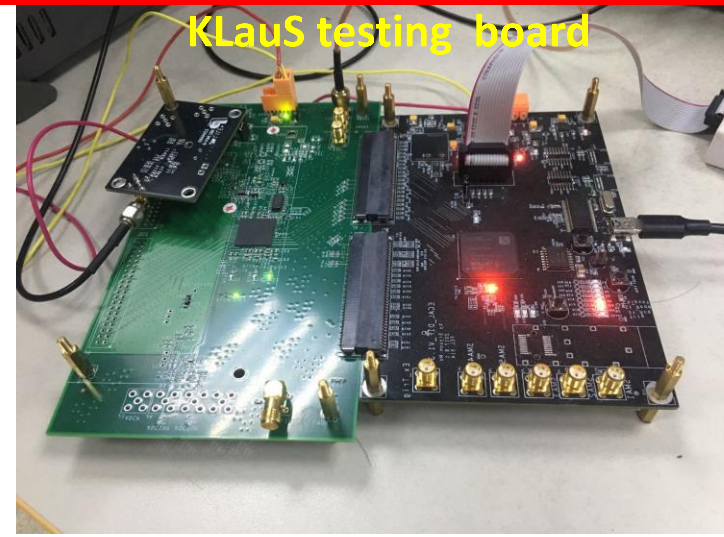


KLauS Chips

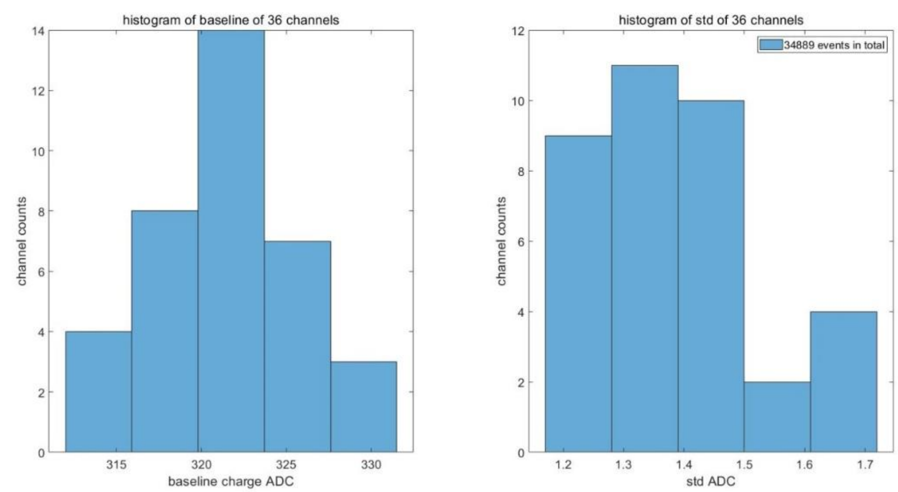
KLauS vs SPIROC2 (SP2)

- Used in AHCAL
- By **University Heidelberg**, **Omega**
- Transistor: 180nm （SP2 350nm）
- Power consumption： full operation 3.6mW
  sum = 3.6mW * 36 chns = 130mW （SP2 ≈300mW）
- Auto/Ext Trigger
- 36 channels
- Dynamic Range： 450pC（SP2 320pC）
- Pe/Noise Ratio = 35 （SP2 11）
- ADC： 10/12bits
- 4 Gain modes (SP2 2 gain modes)
- Dead time 500ns (SP2 ~ms)

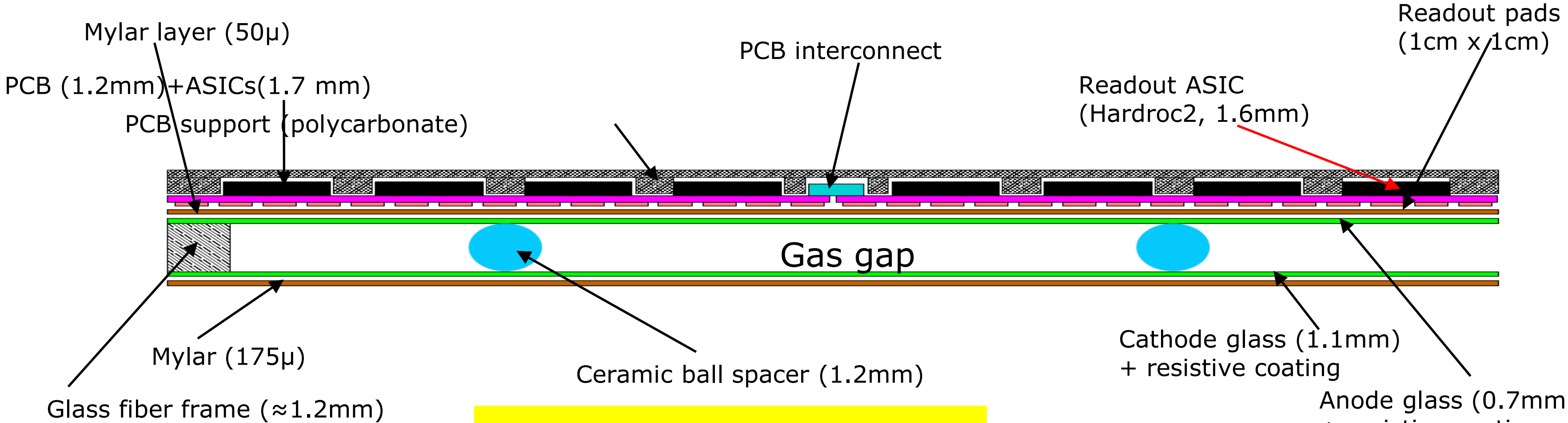
✓ **The KLauS testing board can work now.**



Baseline and Std. distribution

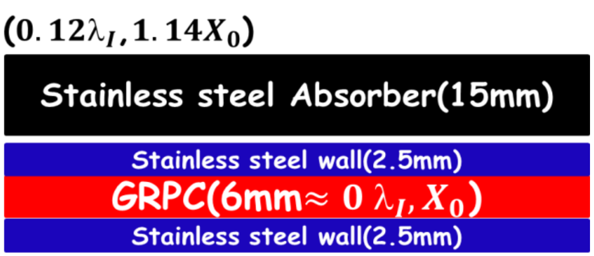


SDHCAL based on RPC

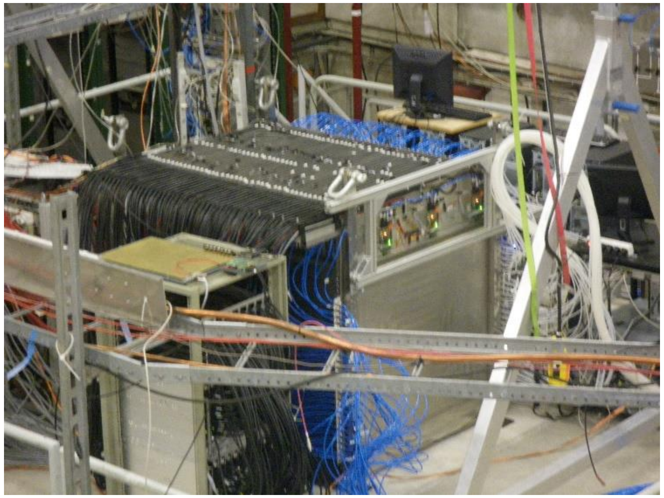


Large GRPC R&D

- ✓ Negligible dead zone
- ✓ Large size: 1 x 1 m²



SDHCAL prototype
Size: 1m x 1m x 1.4m
No. of layers: 48
Cell size: 1cm x 1cm
No. of channels: 440K
Power: 1mW/ch

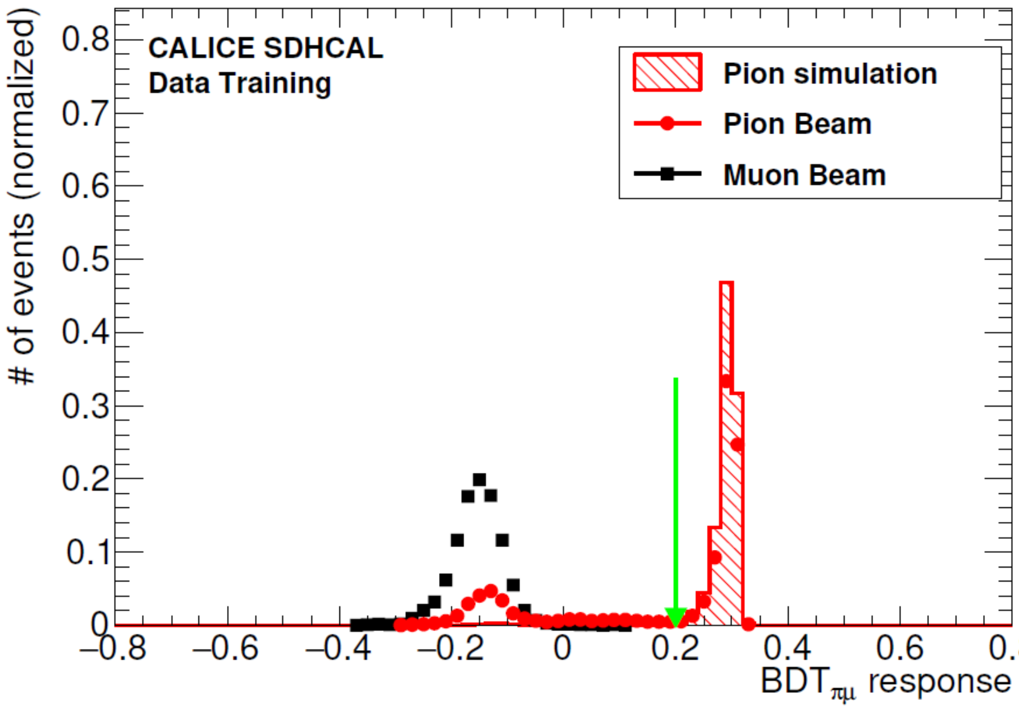


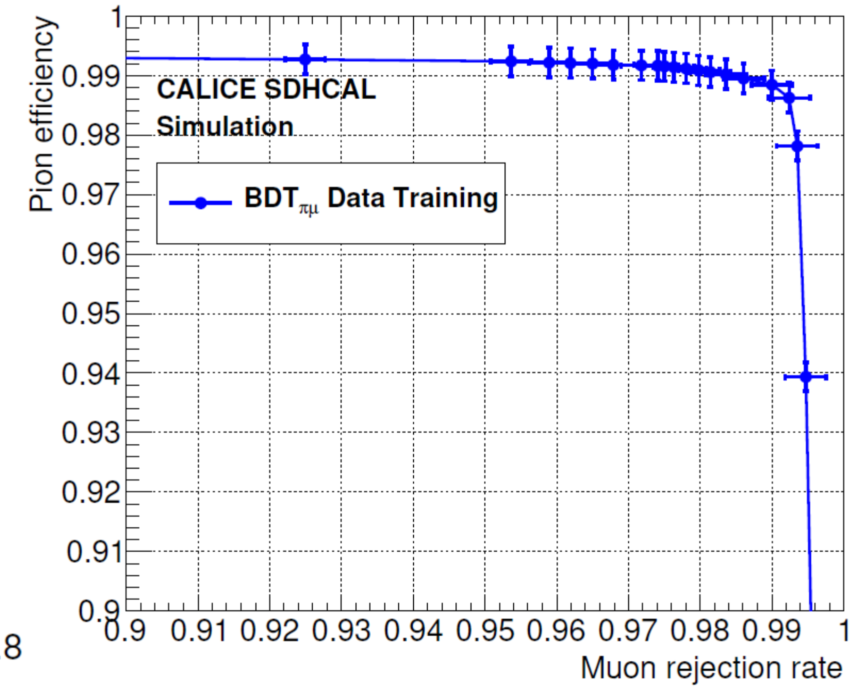
ASIC HARDROC (64 ch)
3-threshold: 110fC, 5pC, 15pC

SDHCAL TB: Particle identification

➢ **Apply BDT to SDHCAL TB data analysis**

SJTU+IPNL, arXiv:2004.02972
Accepted by JINST



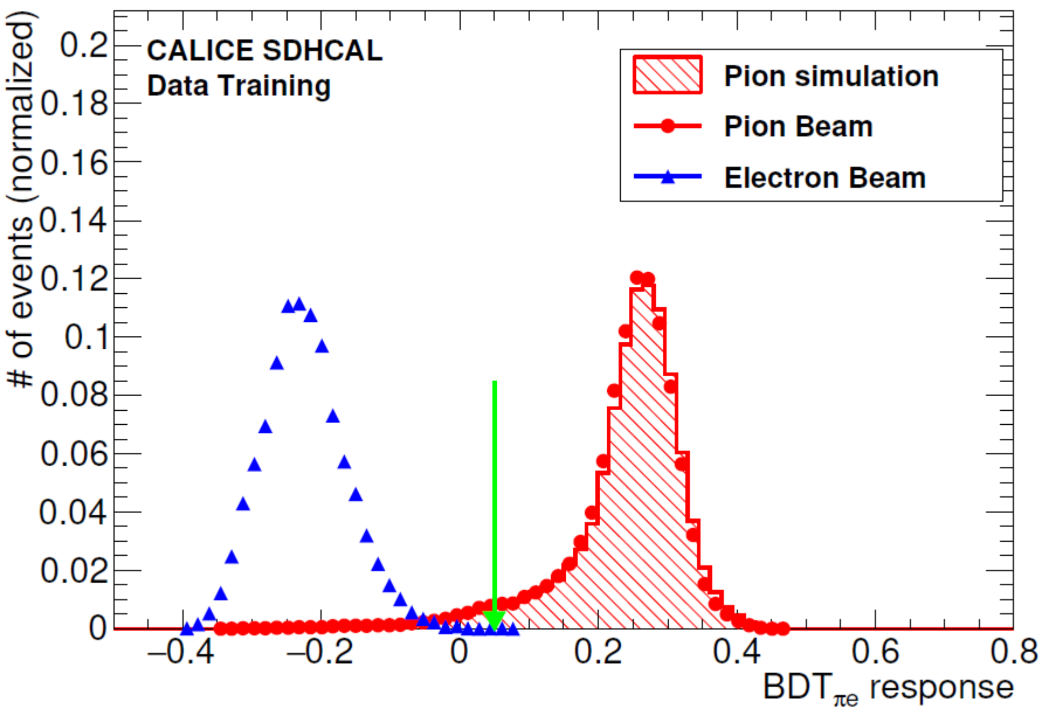


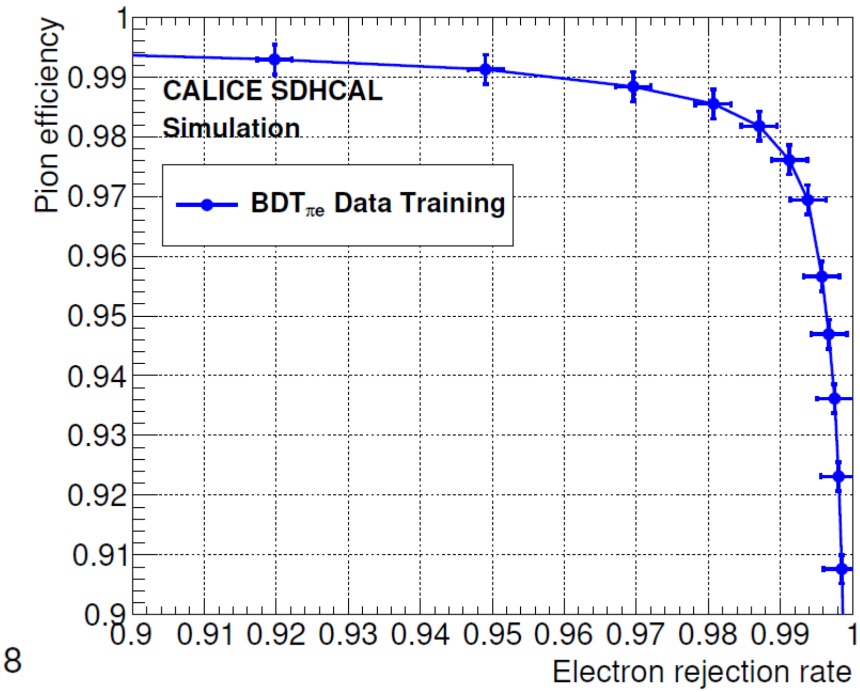
➔ **BDT helps to improve the hadron/e/mu PID, purify TB samples.**
➔ **Keep 98% of pion efficiency and to reject >99.4% of mu.**

SDHCAL TB: Particle identification

SJTU+IPNL, arXiv:2004.02972
Accepted by JINST

- ➢ **Apply BDT to SDHCAL TB data analysis**





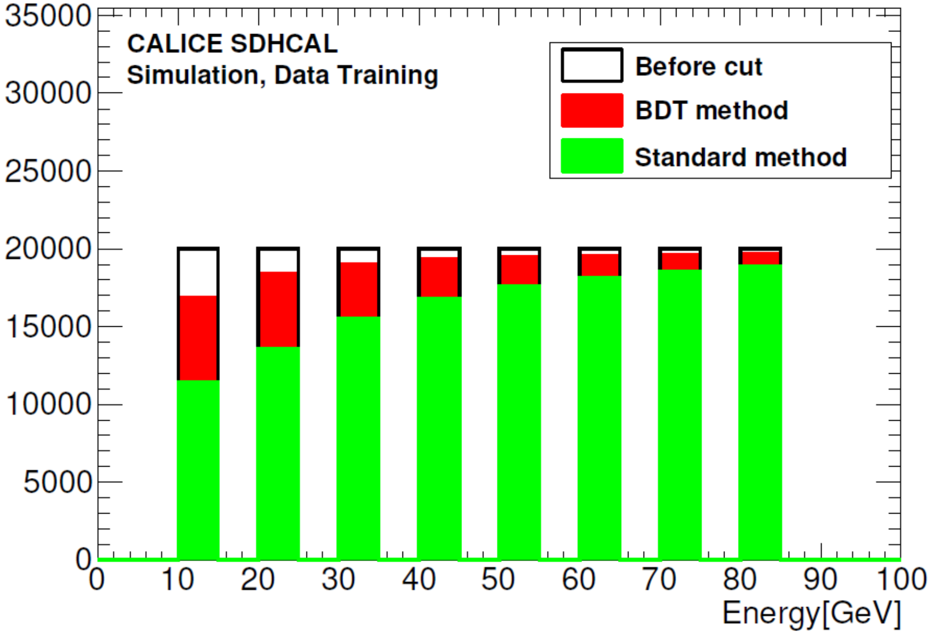
➔BDT helps to improve the hadron/e/mu PID, purify TB samples.
➔Keep 98% of pion efficiency and to reject >99% of electron.

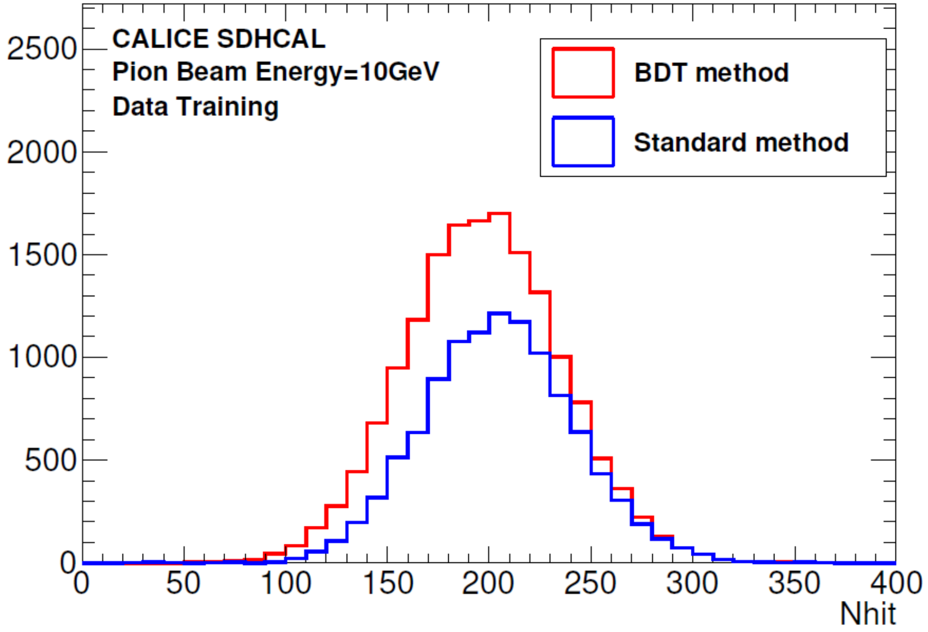
SDHCAL TB: Particle Identification

- Apply BDT to SDHCAL TB data analysis

SJTU+IPNL, arXiv:2004.02972
Accepted by JINST

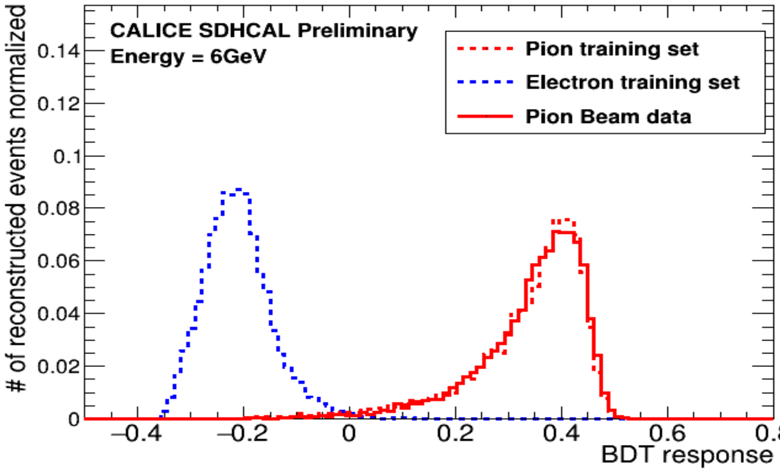
→ **BDT significantly enhance pion selection efficiency of TB samples comparing to standard method, especially at energy up to 40 GeV.**

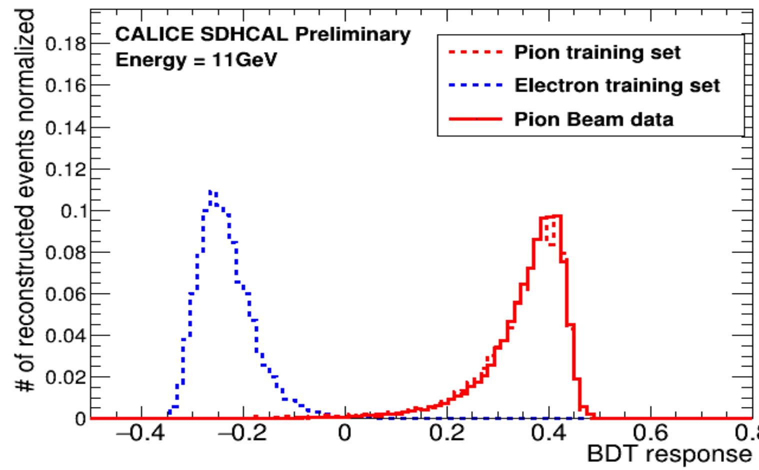


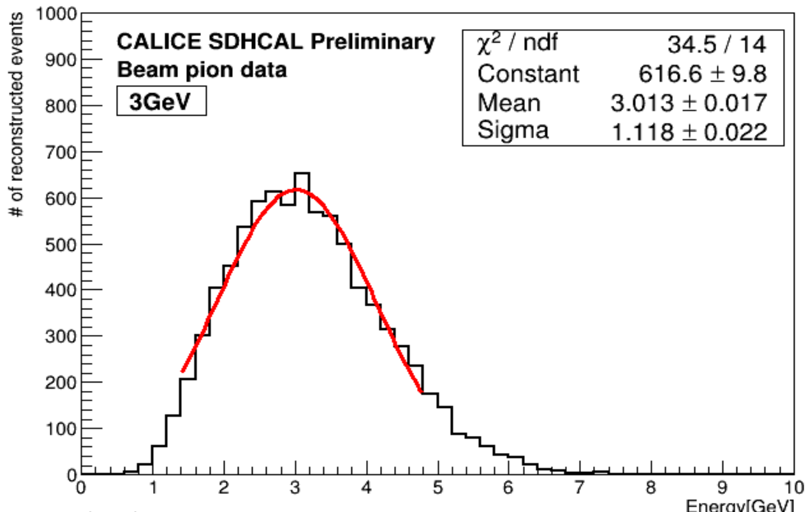


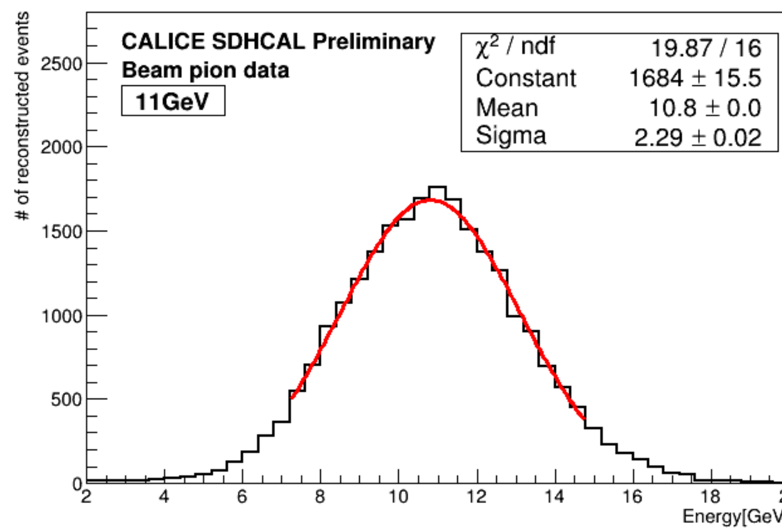
SDHCAL TB: Low Energy

- ➔ **SDHCAL TB at CERN using low energy (3-11 GeV) pion beam.**
- ➔ **Data and MC simulation for pion samples agree well**



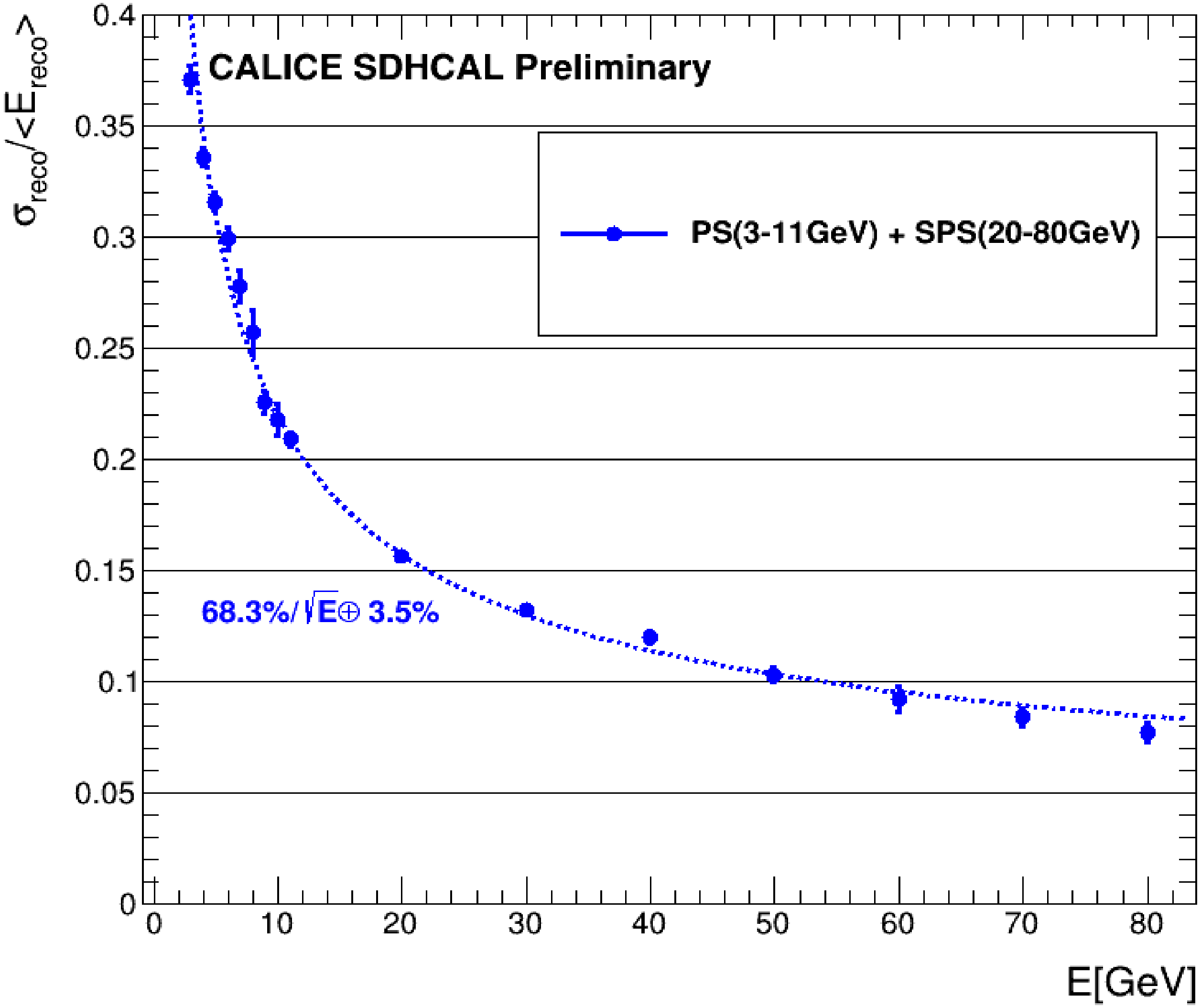






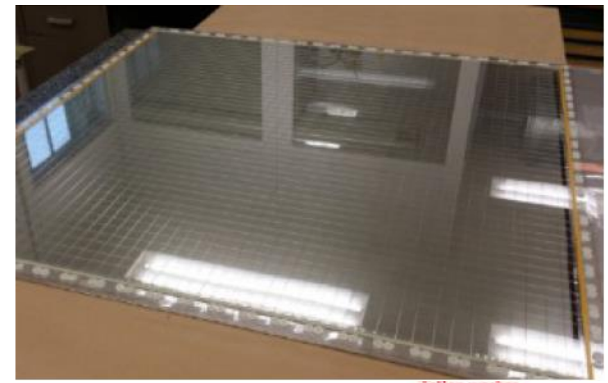
SDHCAL TB: Energy Resolution

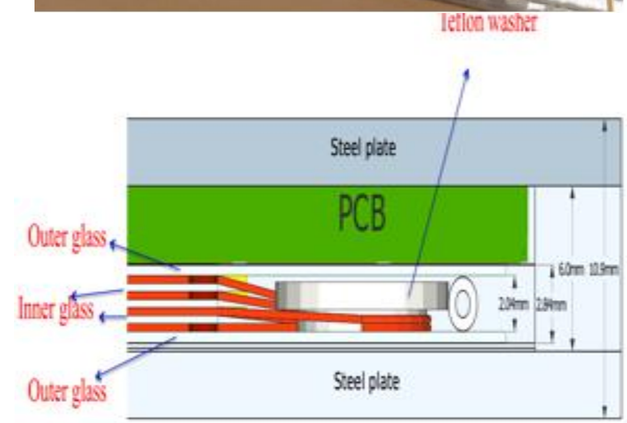
SJTU+IPNL, CALICE note under preparation

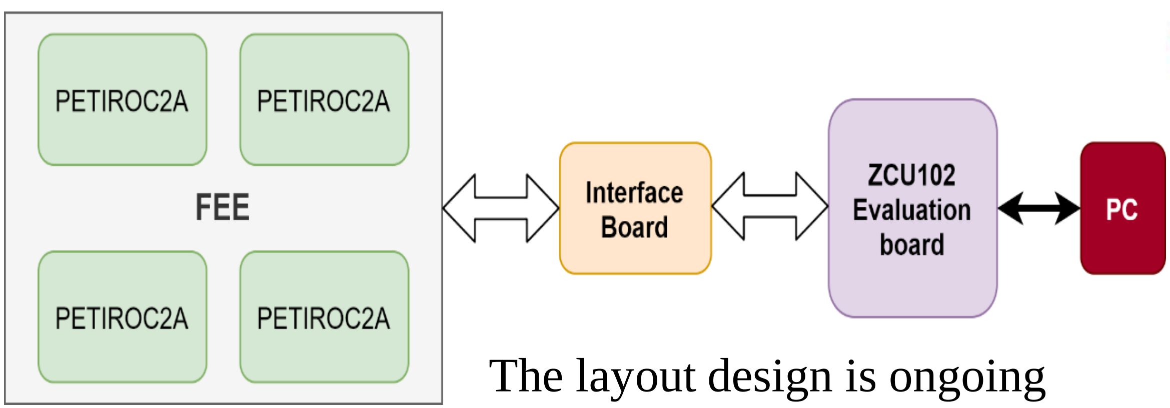


SDHCAL: New Design with 5D

- Purpose: five dimension (5D) SDHCAL:
  - Energy, position (X, Y, Z), timing
- Add MRPC layers in SDHCAL prototype
  - Same size as standard RPC
- Front-end board for MRPC readout
  - Charge and timing measurement simultaneously
  - **PETIROC2A** (32 channels, size: 2.8x2.8cm2)
  - < 20ps time jitter

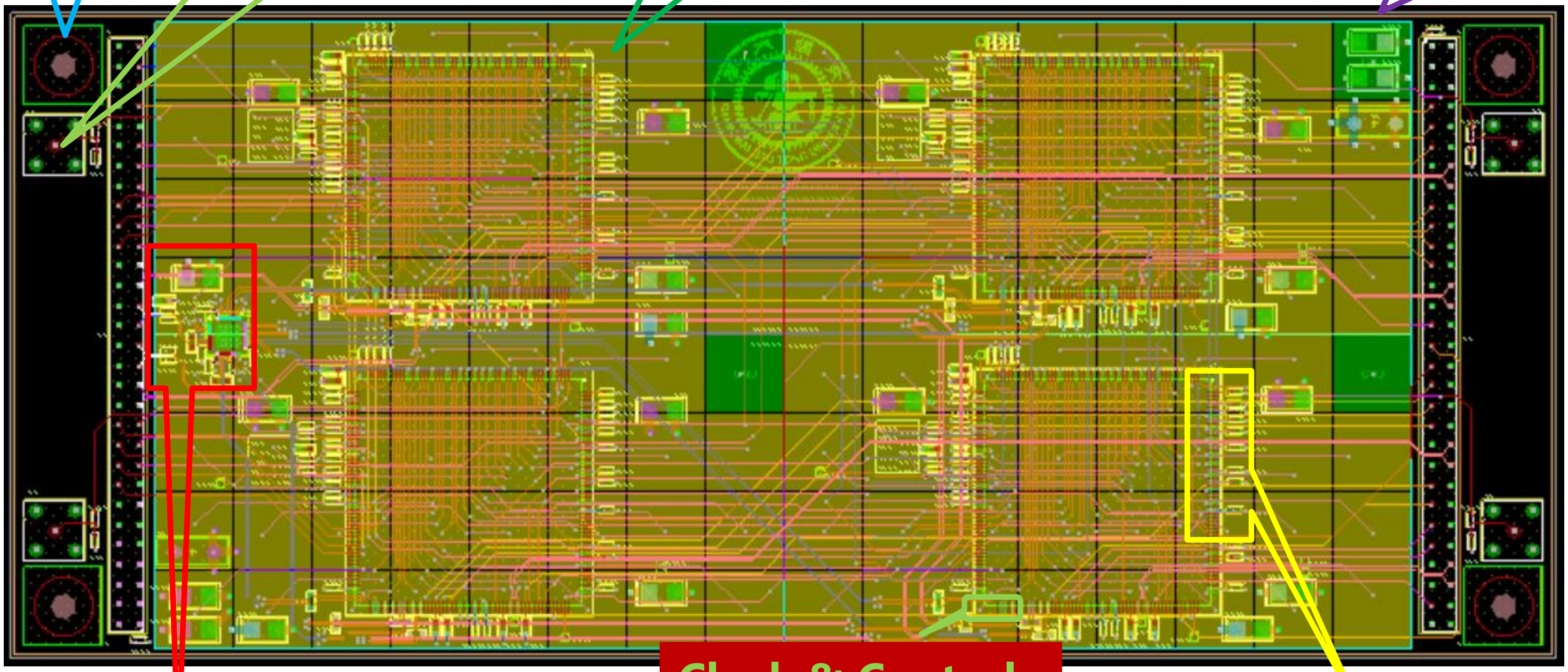






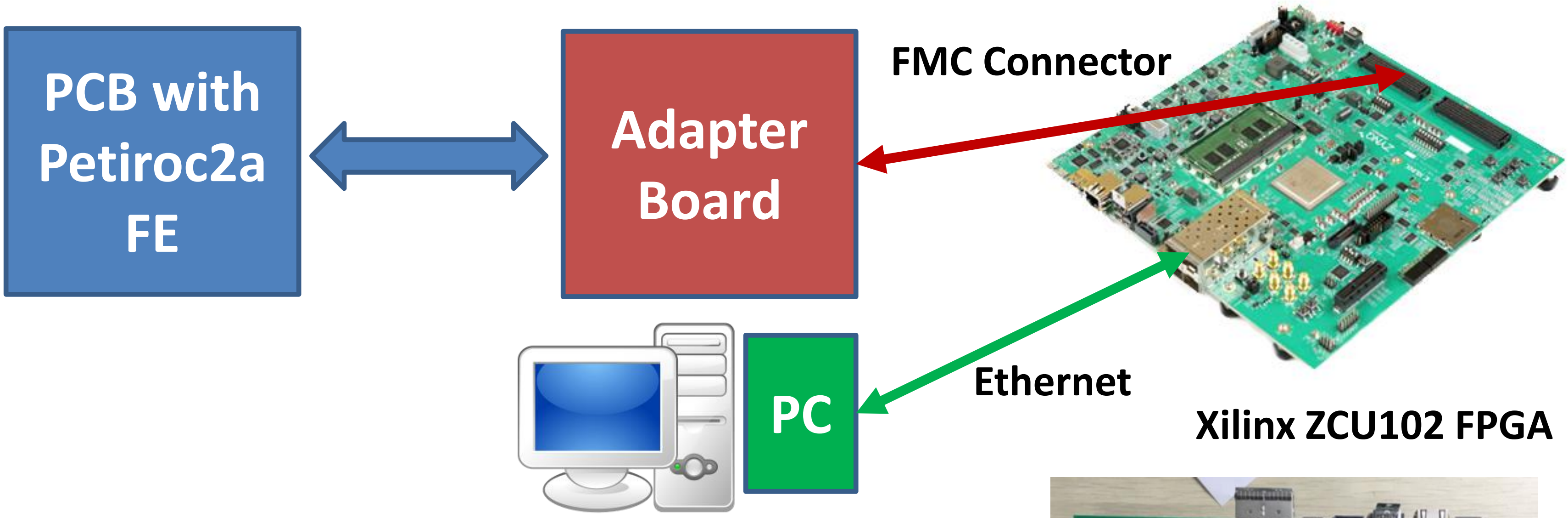
The layout design is ongoing

Design of PCB with Petiroc2A by SJTU



PCB layout with Petiroc2A
Size: 19.7cm x 8.2cm

Readout System for Petiroc2A based PCB

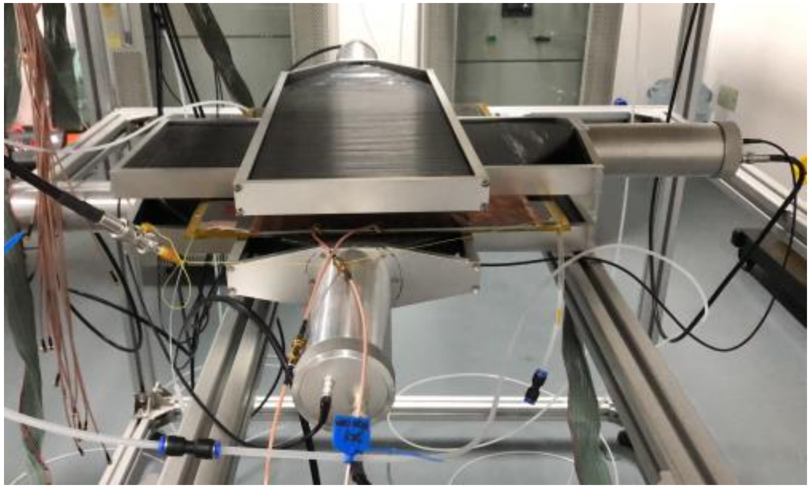


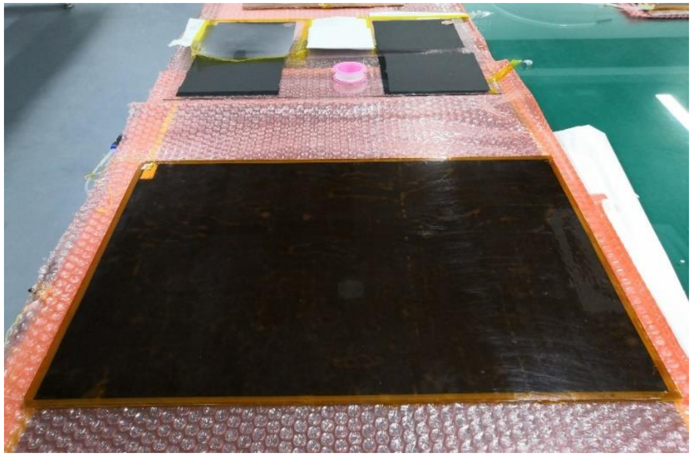
Xilinx ZCU102 has been purchased, readout system is under development.

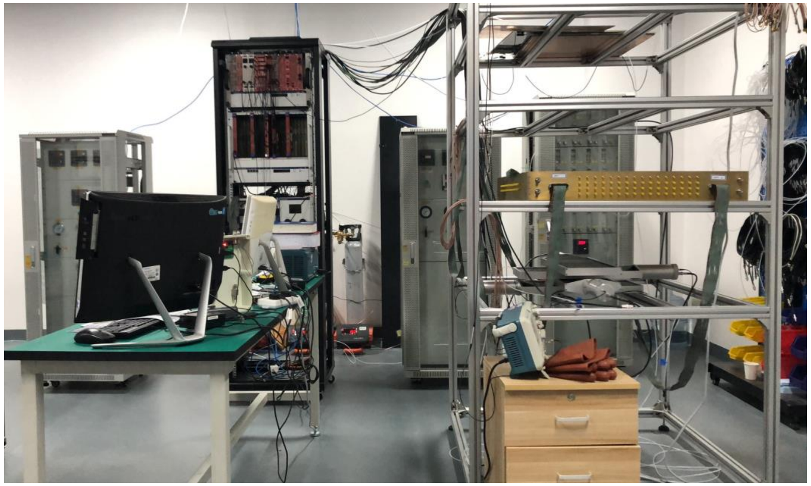
https://www.xilinx.com/products/boards-and-kits/ek-u1-zcu102-g.html

GRPC Construction and Test

GRPC construction in Cleanroom







- Now: RPC size 35cm×50 cm
- Next step: Large size RPC 1m×1m

Summary and Future Plan

AHCAL

- The scintillator cell size is 4cmx4cmx3mm and the light output of both PS and TP tiles can satisfy our requirement.
- New NDL SiPMs 22-1313-15S looks promising
- PS tile production, wrapping, testing is under preparation

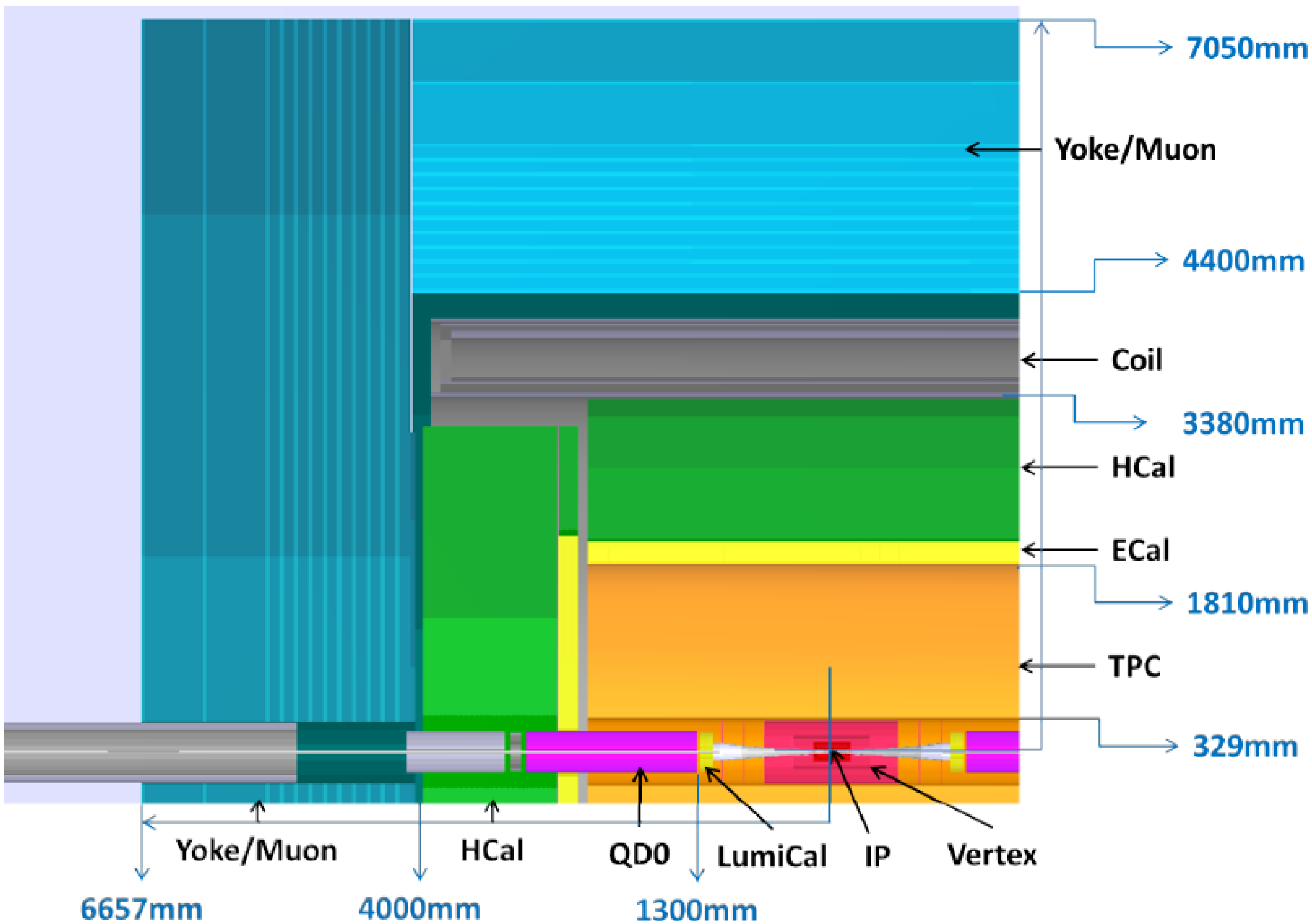
SDHCAL

- TMVA-BDT improves PID for SDHCAL TB data samples
- Design of FEE and PCB with PETIROC2A for MRPC 5D measurements is ongoing
- Construction and test of GRPC is ongoing

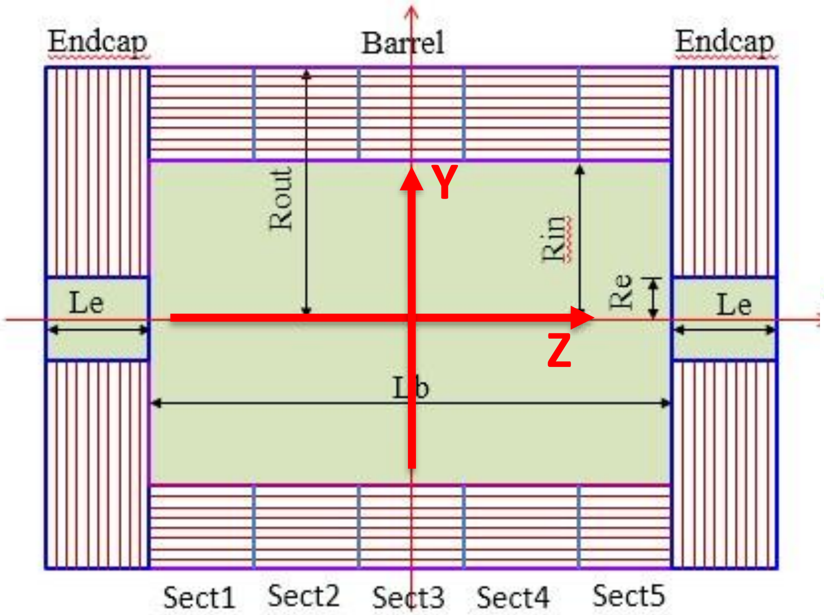
Thanks for your attention !

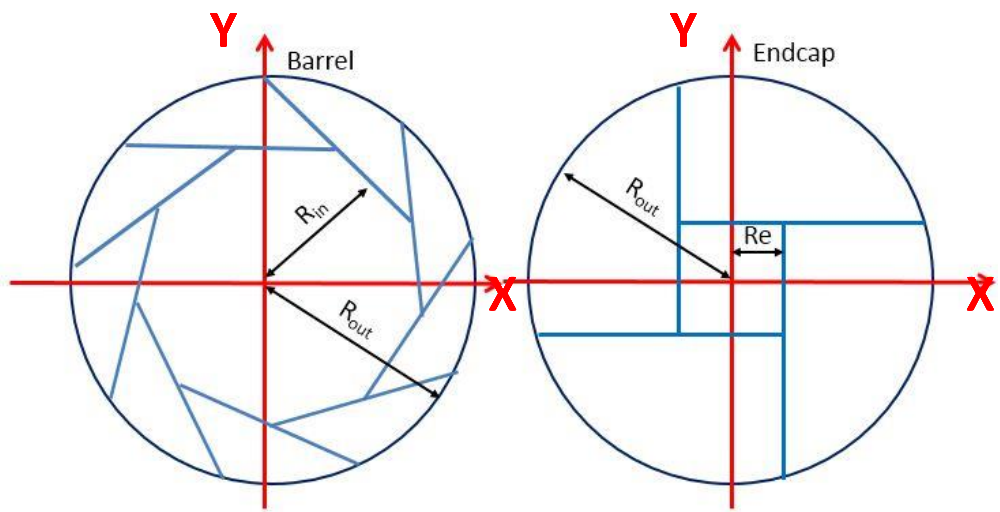
Backup

Schematic of CEPC Detector

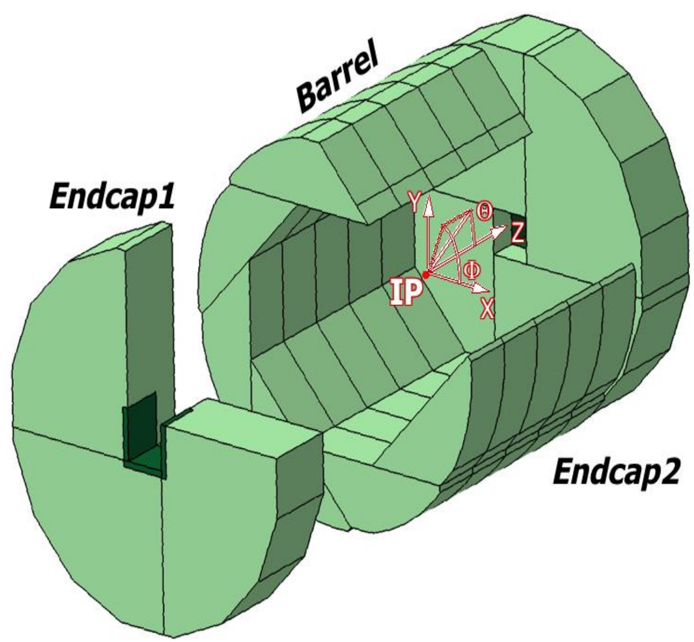


CEPC HCAL Geometry



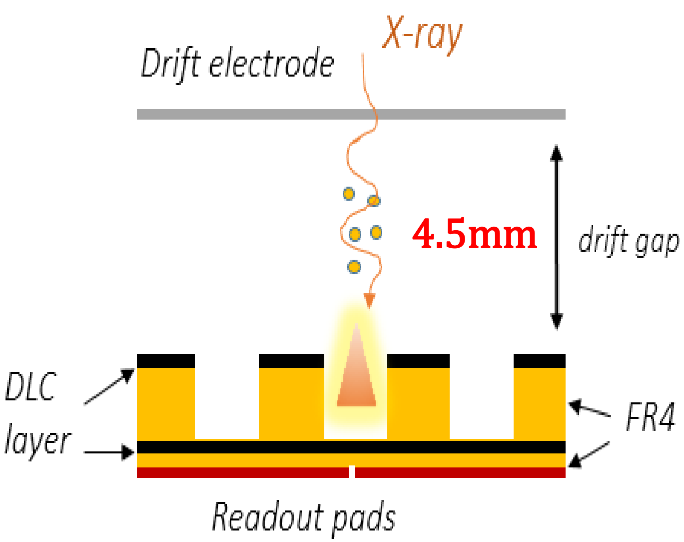


- Inner radius in X-Y plane R_{in} = 2300mm
- Outer radius R_{out} = 3340mm
- Inner & outer of HCAL endcap in Z-axis are 2670mm and 3710mm

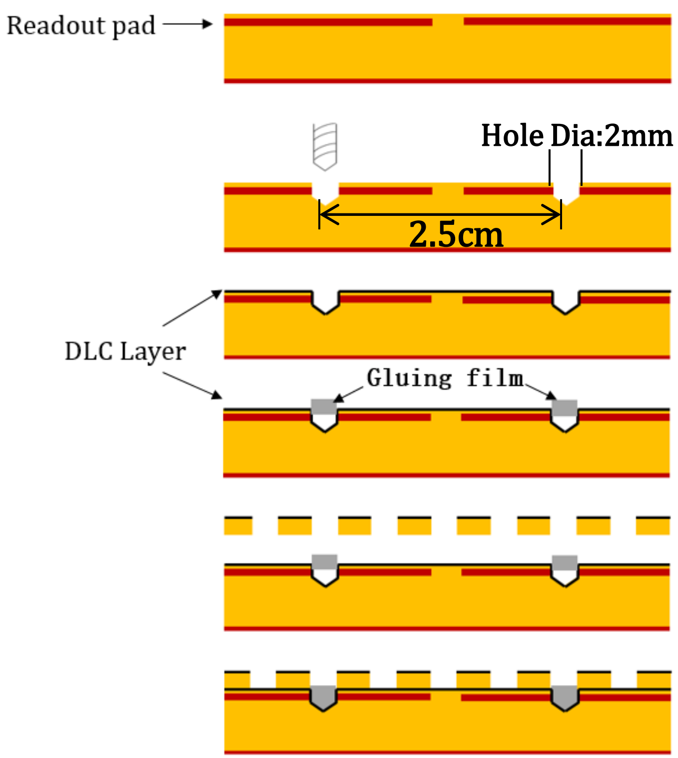


RWELL Detector development

RWELL: Resistive WELL



a) Hole Diameter: 500μm
b) Pitch: 1mm
c) Thickness: 400μm
d) Sensitive area: 25cm× 25cm



From USTC group

DLC deposition and Thermal bonding

- Key issues for RWELL:
  1. **Resistive layer-DLC(Diamond like carbon)**
  2. **Bonding method**

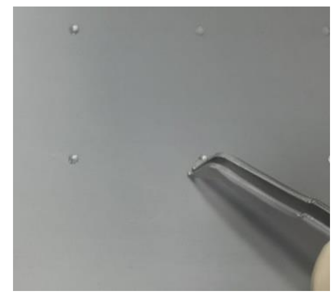
DLC is deposited on a PCB substrate by the magnetron sputtering method

Sample Clamping
↓
Vacuum Pumping
↓
Sample Pre-treating
↓
Deposition
↓
Cooling in Vacuum
↓
Sample taking down

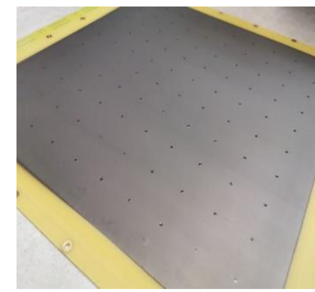
A DLC-coating Readout Board

Surface resistivity :>100MΩ/SQ

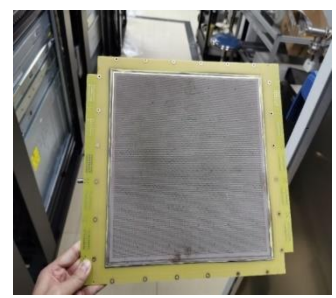
DLC deposition procedure



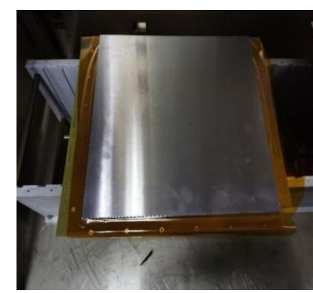
Step 1，Place the gluing film



Step 2，Pre-heating



RWELL Detector

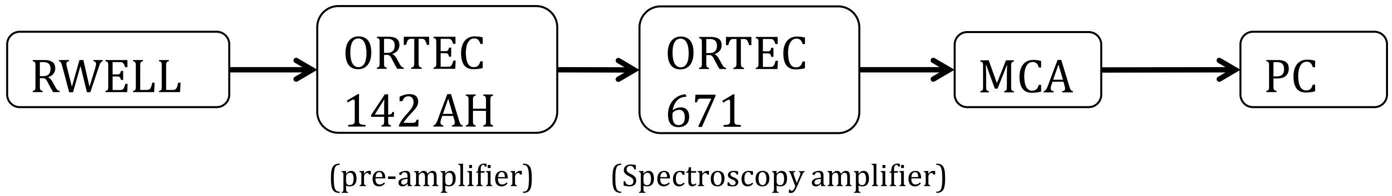


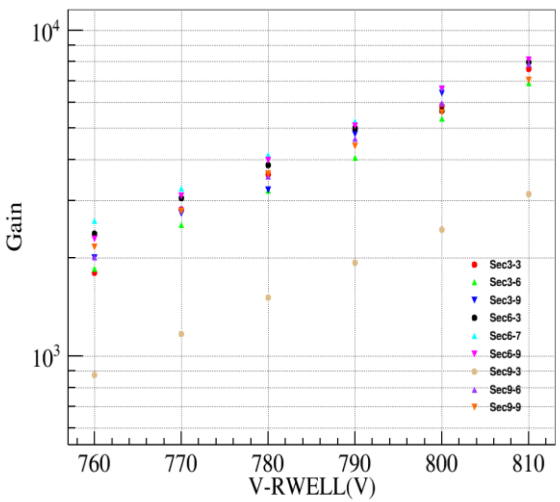
Step 3，Thermal boding

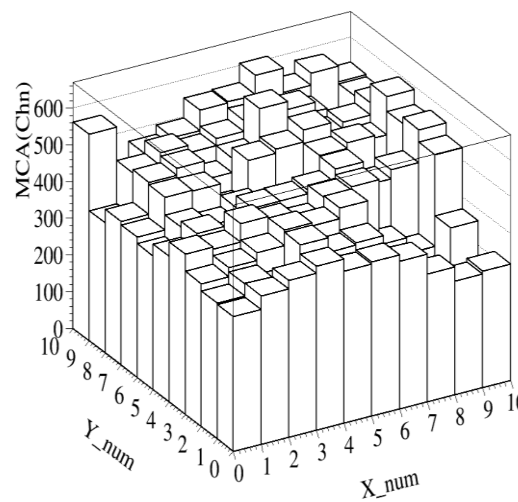
Thermal bonding procedure

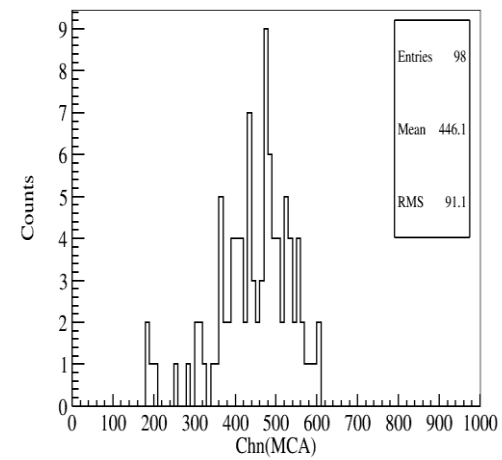
Gain Test

- Test setup :









Gain : ~8000

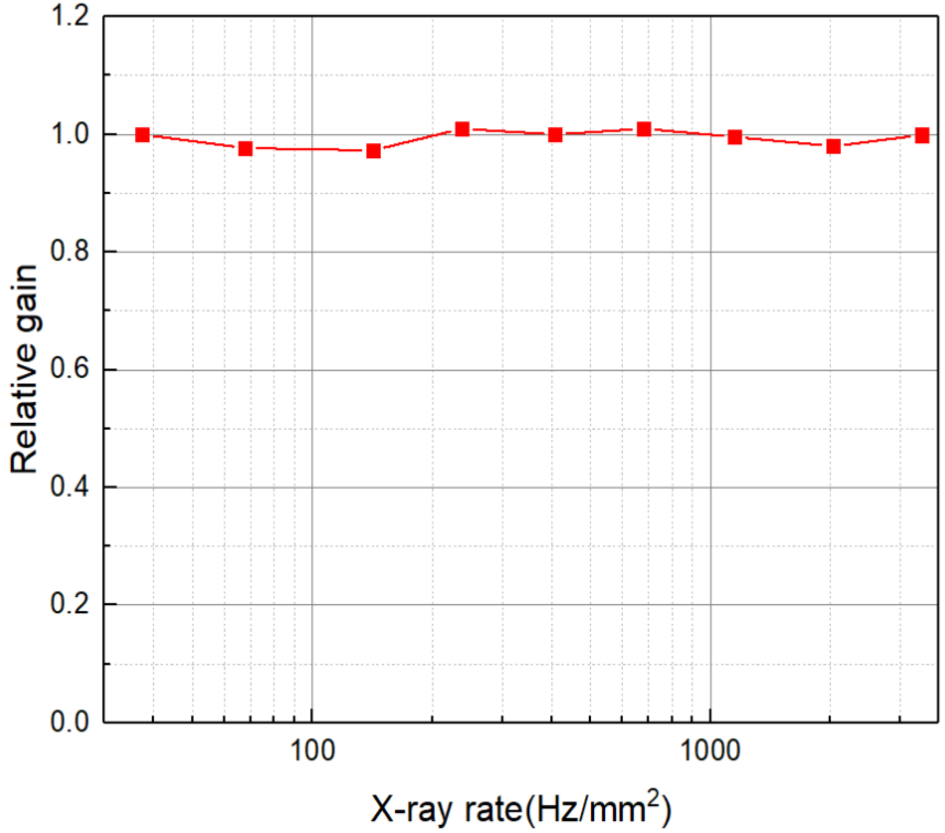
Gain uniformity :RMS/Mean ～20.4%

- Gain uniformity is not good. Possible reason:

  1. Gas flow
  2. Uniformity due to the thermal bonding procedure

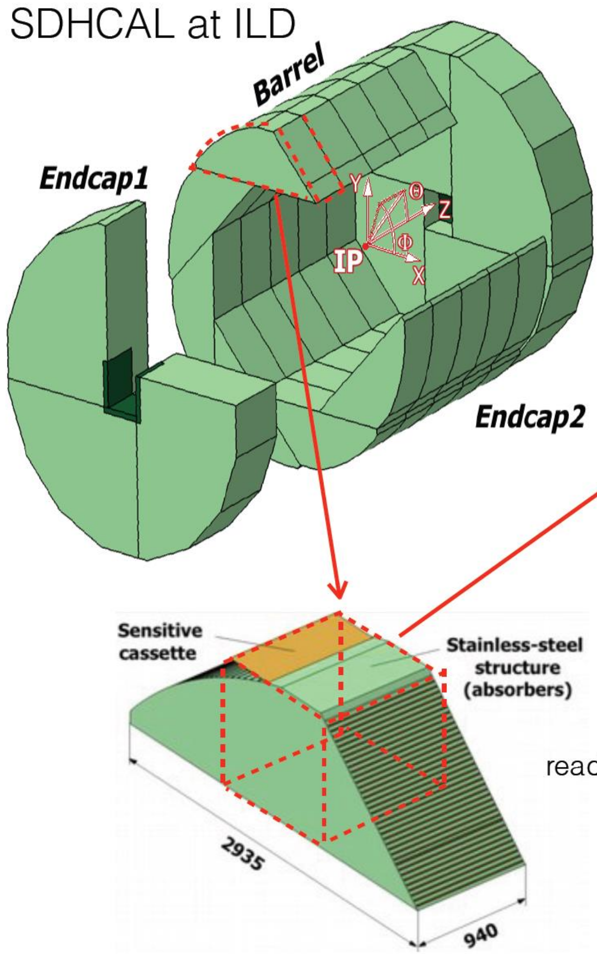
Rate Capability

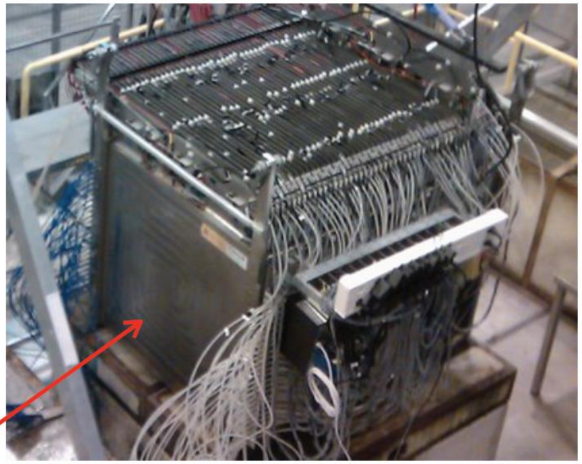
- RWELL is irradiated with 8 keV X-ray, and gain of the detector is almost no reduction@300kHz/cm^2 (Initial gain G0:～5500).



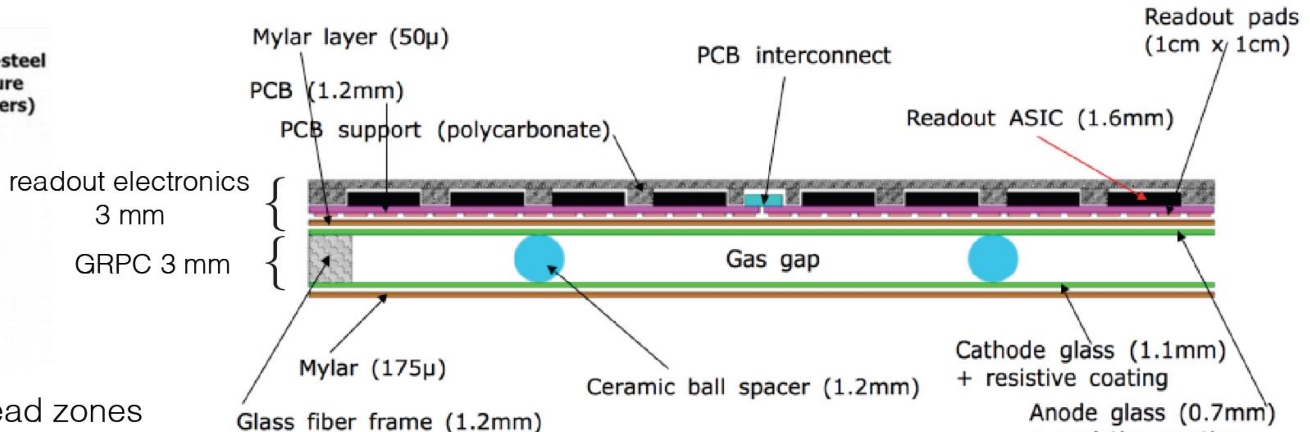
- Detector discharge while irradiated at a higher rate

SDHCAL based on RPC





- 48 layers, 6 λ_I
- GRPC (1×1 m^2)
- Cell pads:1×1 cm^2
- On each layer, ASIC: 12 x 12; 64 ch. on each ASIC; 9612 ch. in total
- Three thresholds readout (2 bits): (0.11, 5, 15) pC
- Power-pulsing electronics
- Self-supporting mechanical structure as absorber as well



- Very compact with negligible dead zones
- Eliminates projective cracks
- Minimizes separation of barrel and endcap

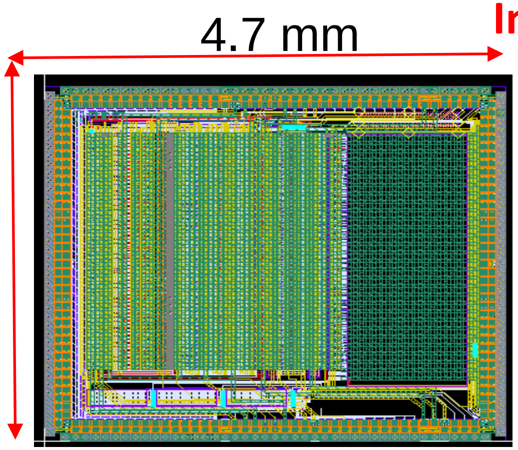
arXiv:1602.02276

JINST 10 (2015) P10039

Electronics Readout

Imad Laktineh (IPNL)

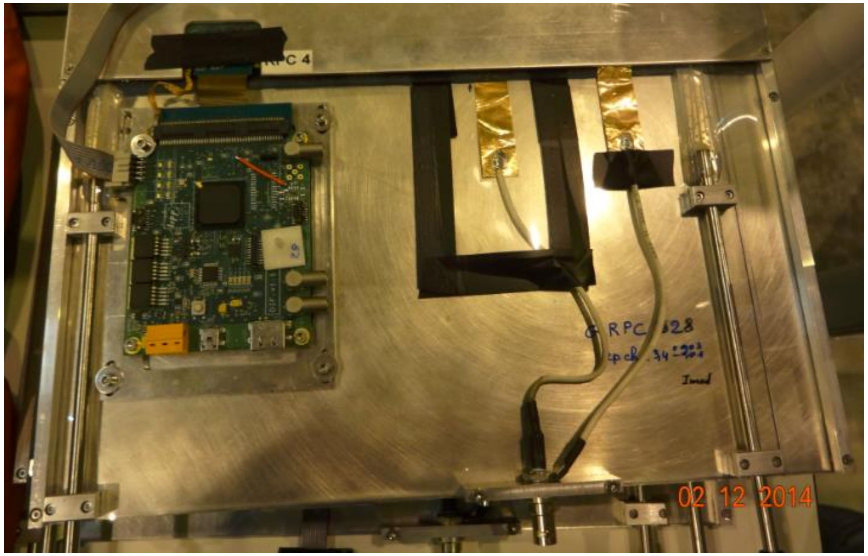
ASICs : HARDROC2
64 channels
Trigger less mode
Memory depth : 127 events
3 thresholds
Range: 10 fC-15 pC
Gain correction → uniformity



Printed Circuit Boards (PCB) were designed to reduce the cross-talk with 8-layer structure and buried vias.

Tiny connectors were used to connect the PCB two by two so the 24X2 ASICs are daisy-chained. $1 \times 1 m^2$ has 6 PCBs and 9216 pads.

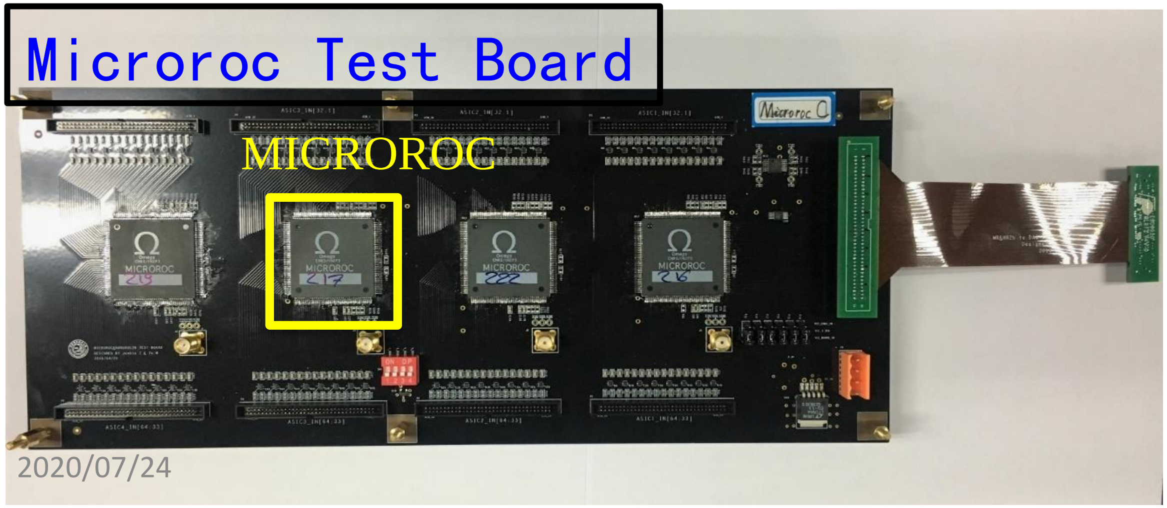
DAQ board (DIF) was developed to transmit fast commands and data to/from ASICs.



Readout ASIC

Readout ASIC	Channels	Dynamic Range	Threshold	Consumption
GASTONE	64	200fC	Single	2.4mW/ch
VFAT2	128	18.5fC	Single	1.5mW/ch
DIRAC	64	200fC for MPGD	Multiple	1mW/ch, 10μW/ch
DCAL	64	20fC~200fC	Single	——
HARDROC2	64	10fC~10pC	Multiple	1.42mW/ch,10μW/ch
MICROROC	64	1fC~500fC	Multiple	335μW/ch, 10μW/ch

Considered the multi-thresholds readout, dynamic range and power consumption, MICROROC is an appropriate readout ASIC



MICROROC Parameters

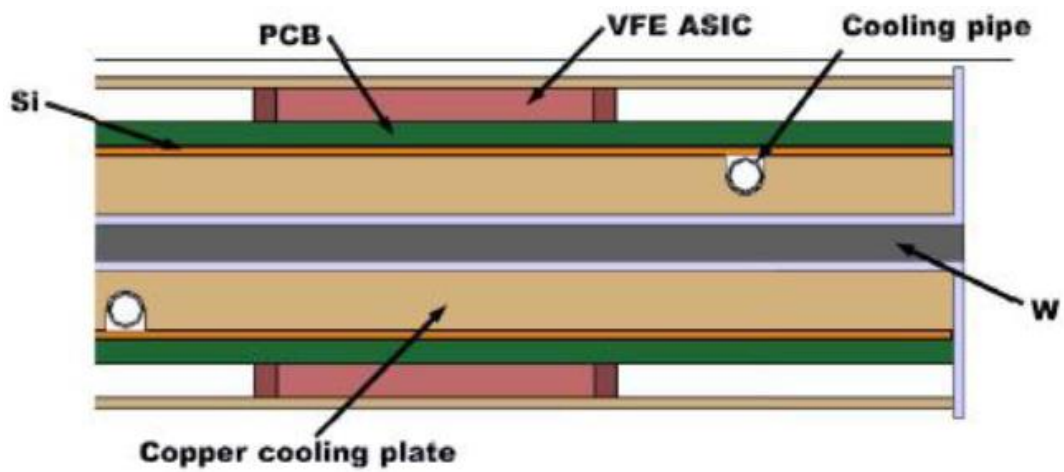
- Thickness: 1.4mm
- 64 Channels
- 3 threshold per channel
- 128 hit storage depth
- Minimum distinguishable charge:2fC

Active Cooling

- CEPC is designed to operate at continuous mode with beam crossing rate: 2.8×10^5 Hz. Power pulsing will not work at CEPC.
- Compare to ILD, the power consumption of VFE readout electronics at CEPC is about two orders of magnitude higher, hence it requires an active cooling
  - Evaporative CO_2 cooling in thin pipes embedded in Copper exchange plate.
  - For CMS-HGCAL design: heat extraction of 33 mW/cm^2, allows operation with 6×6 mm^2 pixels with a safety margin of 2
- To be modelled for Mokka simulation

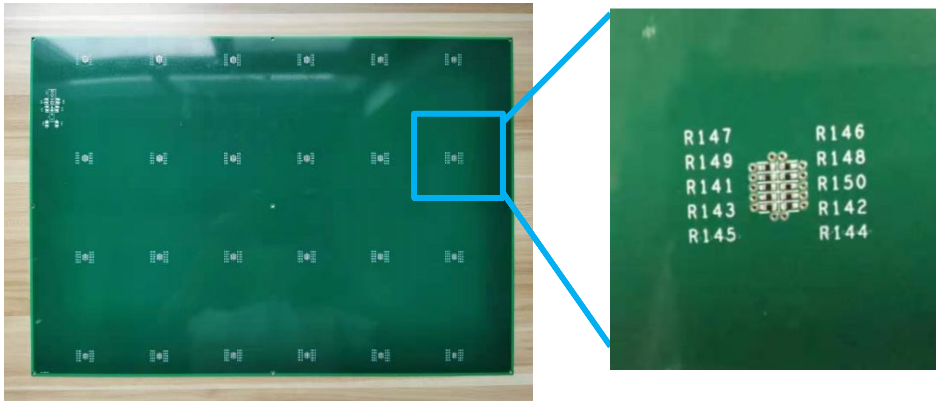
➔ Transverse view of the slab with one absorber and two active layers.

➔ The silicon sensors are glued to PCB with VFE chips, cooled by the copper plates with CO_2 cooling pipes.



Active Cooling Simulation and Test

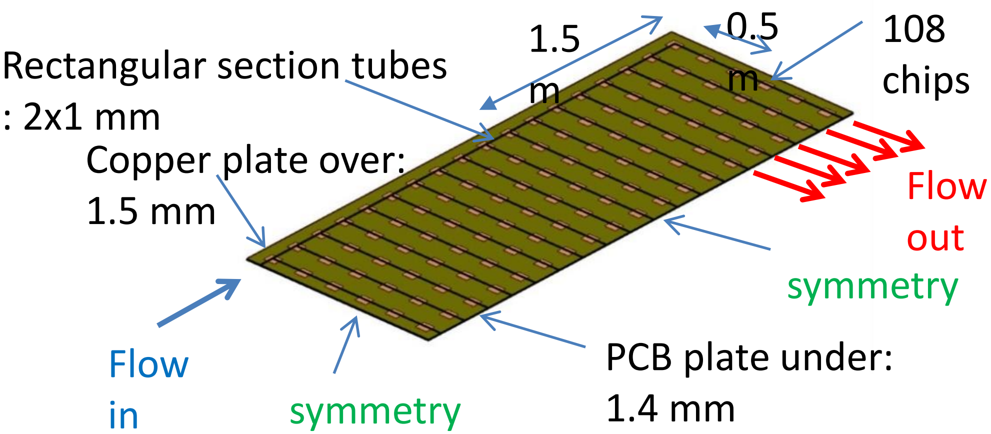
- Resistors: 4*6*10 per PCB
- Total resistance of a group of 10 parallel-connected resistors: 470Ω
- ASICs in SDHCAL: ~0.064W/chip
  ➔ ~5.5V on resistors
- Requirements for the power supply:
  - Voltage range: >0~5.5V
  - Output power: >1.536W/PCB
  - Adjustable/programmble



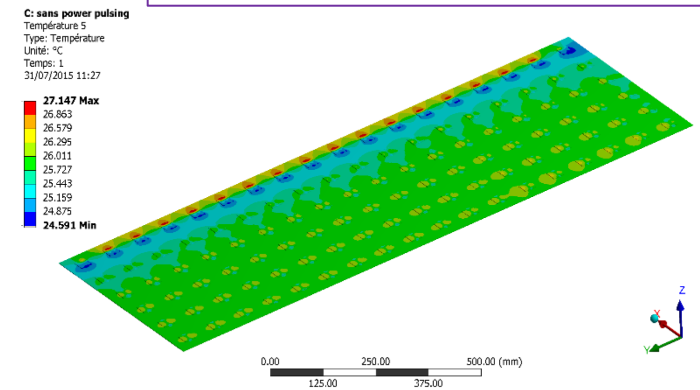
Resistance(Ω)	4.7k
Power rating(W)	0.0625(~17V)
Max operating voltage(V)	50
Max overload voltage(V)	100
Max operating T(℃)	155
Min operating T(℃)	-55
Temperature coefficient	±100ppm/℃

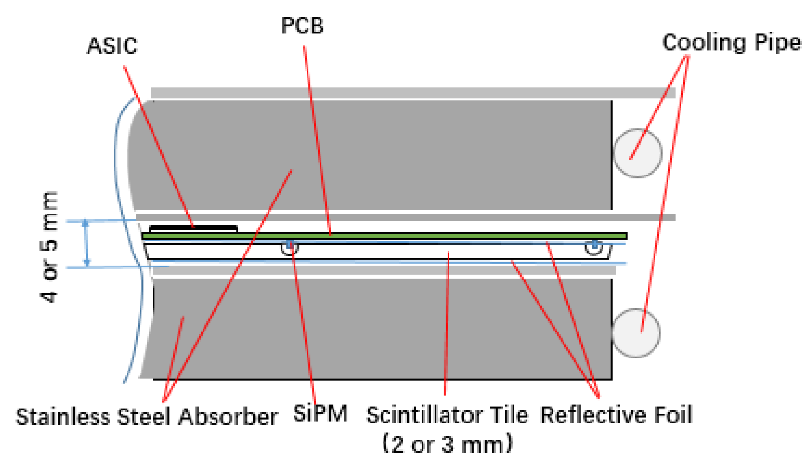
Active Cooling Simulation

Cooling maybe necessary if operating at continuous mode (CEPC)



27.147 (max) – 24.591 (min) =2.556 °C





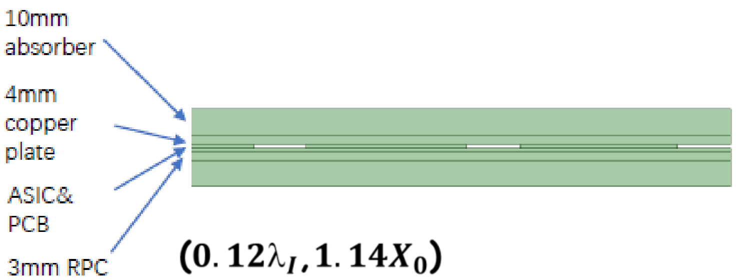
- A water-based cooling system inside copper tubes in contact with the ASICs to absorb excess heat.
- Temperature distribution in an active layer of the SDHCAL.

Water cooling : h = 10000 W/m²/k
Thermal load : 80 mW/chip

- For AHCAL, a water-based copper cooling system embedded in the stainless steel absorber.

Active Cooling Simulation

ANSYS Simulation of RPC+PCB With copper plate & water tubes



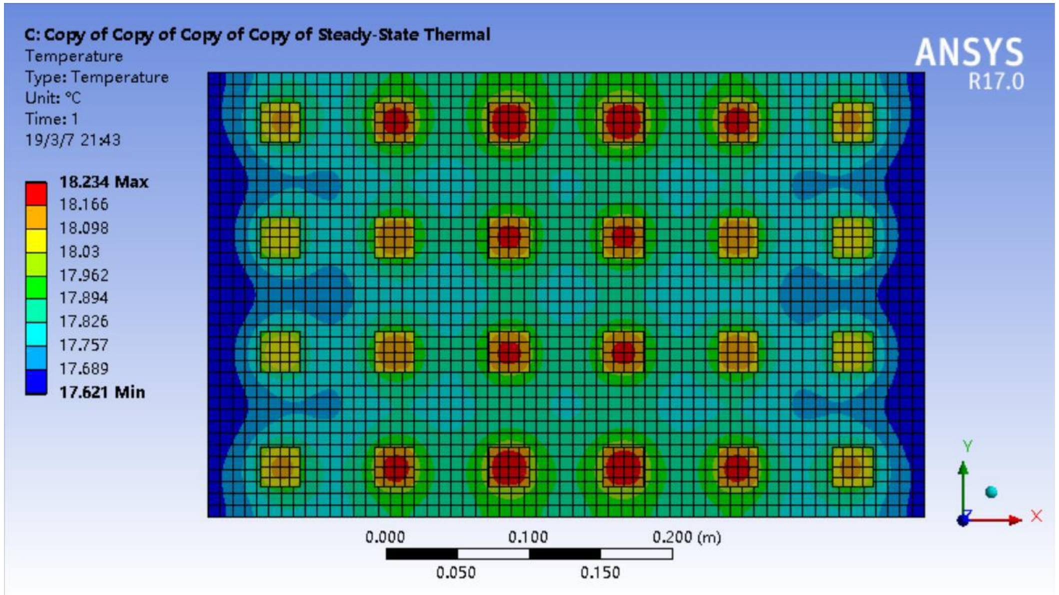
$(0.12\lambda_I, 1.14X_0)$

Stainless steel Absorber(15mm)

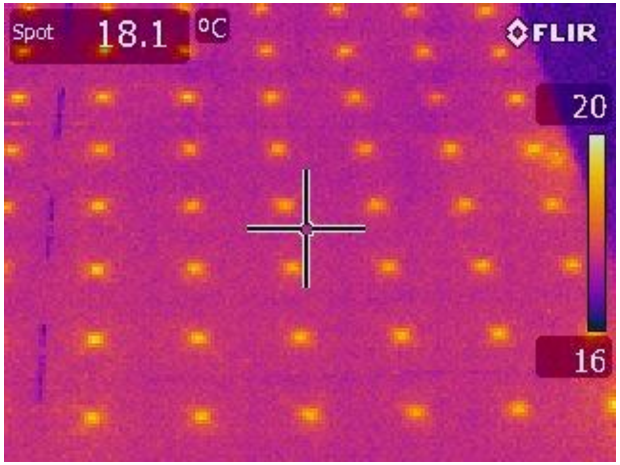
Stainless steel wall(2.5mm)

GRPC(6mm≈ $0\ \lambda_I, X_0$)

Stainless steel wall(2.5mm)



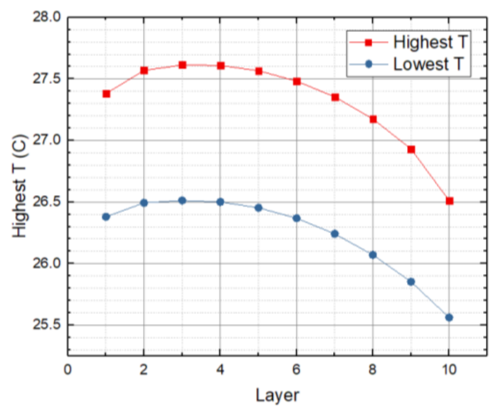
Temperature test of RPC+PCB



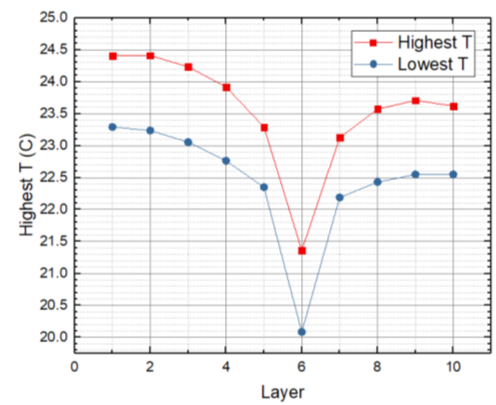
Active Cooling Simulation

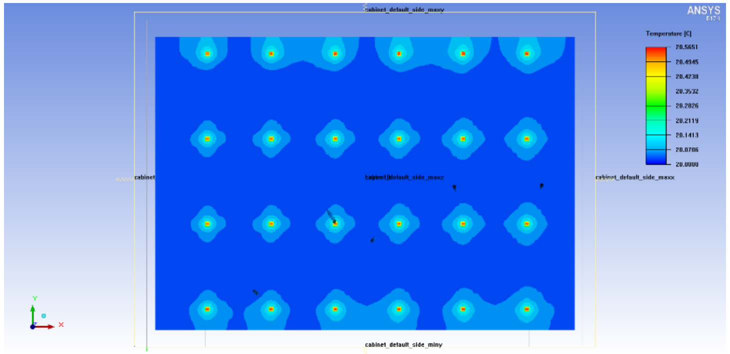
- 10 layers, flow rate: 1m/s
- With cooling at 6th layer:
- With cooling each layer:
  - uniform among layers
  - cooling power: ~1.53W/layer

no cooling

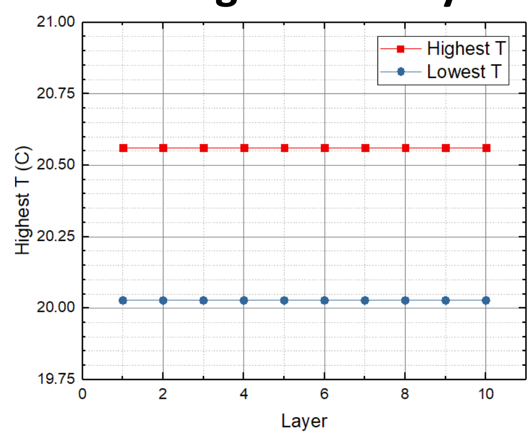


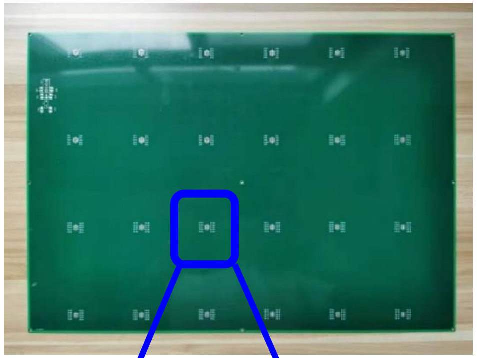
cooling at 6^{th} layer

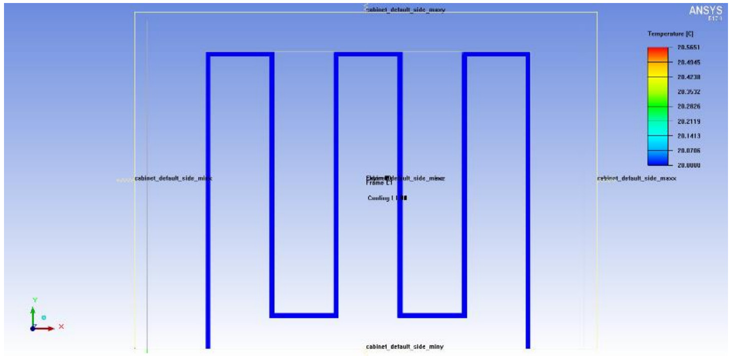




cooling at each layer







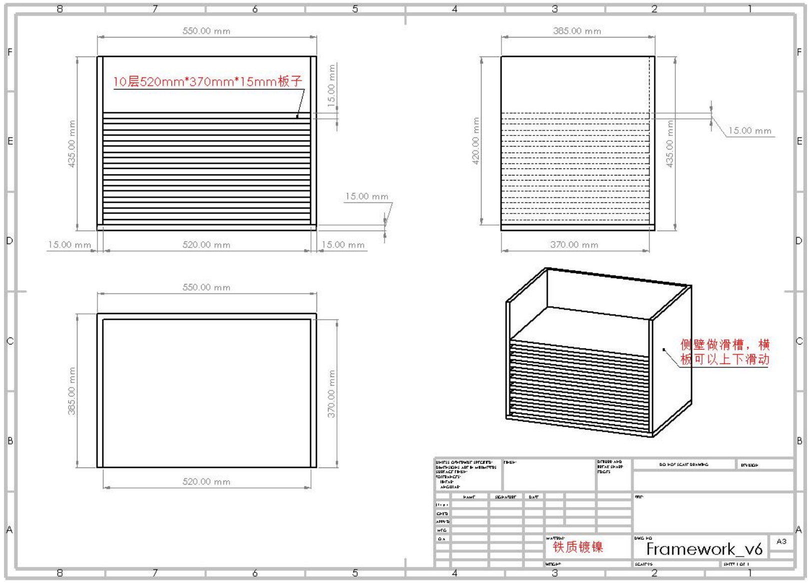
cooling pipes

PCB with resistors to mimic HARDROC ASIC heat source for cooling design and test.

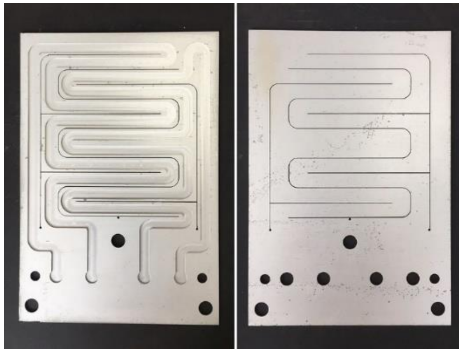
Active Cooling Module

- Cooling plates: water pipes imbedded in metal plates
  - cooling ability: ~kW/m^2
  - safety(water is not so good)
- Stainless steel
  - poor heat transmission
  - difficult to produce → high cost
  - can work as the absorber
- Aluminum
  - good heat transmission
  - easy to produce
  - 5 times the radiation length than steel

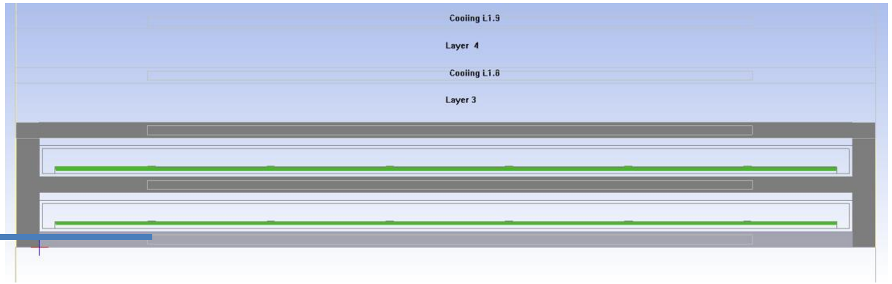
Cooling Test Module



Cooling plates



Cooling plate
PCB
RPC
Stainless steel



Schematic of CEPC Detector