iRPC 后端触发电子学进展





高能所触发组刘振安,赵京周 2020年8月11日 2020年LHC 探测器升级研讨会





- 课题任务
- 现状与进展

▶后端读出电子学设计及批量生产进展

▶在CERN 904楼2D 读出RPC联调取得巨大进展

▶iRPC后端固件开发

▶文章合作组审核通过

• 小结及后续计划





- 任务书验收名称及指标:
 - 一级径迹触发模式识别和海 量数据触发高速传输板
 - ≥32K/单板
 - 单路速率≥10Gbps
 - 单板速率≥400Gbps

- 触发电子学二期升级任务
 - 缪子端盖触发预处理的设 计建造
 - iRPC后端电子学的设计与 建造



iRPC后端系统与前端系统的基本框图





iRPC后端触发电子学设计



后端触发电子学板功能模块:

- Clock module
 - Fan out to FEE for temporary test
- Virtex-7 FPGA
 - GBT-FPGA
 - Process
- Kintex-7 FPGA
 - Clock manager for BEE
- MiniPODs
 - DAQ
 - SC
 - GBT links
 - 36 GTH, 11.3Gbps/ch





iRPC后端触发电子学板测试



iame of	TX RX	Status	Bits	Errora	BER	BERT Reset	TX Pattern		RX Pattern	OFE Enabled	Inject Error	TXReset	RX Reset	RX PLL Sta	TX PLL St.	Loopback M	iode	TX Polant
4 Link Group						Reset	PRBS 7-bit	¥	PRBS 7-bit ~	2	Inject	Reset	Reset			None	v	
S Link 0	MGT_X0Y28/TX MGT_X0Y28/RX	11,300 Gbps	4.643E14	0E0	2.154E-15	Reset	PRBS 7-bit	~	PRBS 7-bit ~	2	Inject	Reset	Reset	Locked	Locked	None	~	
% Link 1	MGT_X0Y29/TX MGT_X0Y29/RX	11.300 Gbps	4.643E14	0E0	2.154E-15	Reset	PRBS 7-bit	¥	PRBS 7-bit ~	1	Inject	Reset	Reset	Locked	Locked	None	÷	
% Link 2	MGT_X0Y30/TX MGT_X0Y30/RX	11,300 Gops	4.643E14	0E0	2.154E-15	Reset	PRBS 7-bit	¥	PRBS 7-bit ~	2	Inject	Reset	Reset	Locked	Locked	None	~	
% Link3	MGT_X0Y31/TX MGT_X0Y31/RX	11.300 Gops	4.643E14	0E0	2.154E-15	Reset	PRBS 7-bit	v	PRBS 7-bit 🛩	12	Inject	Reset	Reset	Locked	Locked	None	¥	
% Link 4	MGT_X0Y32/TX MGT_X0Y32/RX	11.300 Gbps	4.643E14	0E0	2.154E-15	Reset	PRBS 7-bit	¥	PRBS 7-bit ~	2	Inject	Reset	Reset	Locked	Locked	None	v	2
% Link5	MGT_X0Y33/TX MGT_X0Y33/RX	11.300 Gbps	4.643E14	OED	2.154E-15	Reset	PRBS 7-bit	v	PRBS 7-bit ~	2	Inject	Reset	Reset	Locked	Locked	None	v	
% Links	MGT_X0Y34/TX MGT_X0Y34/RX	11,300 Gops	4.643E14	0E0	2.154E-15	Reset	PRBS 7-bit	*	PRBS 7-bit v	2	Inject	Reset	Reset	Locked	Locked	None	v	
% Link 7	MGT_X0Y35/TX MGT_X0Y35/RX	11.300 Gbps	4.643E14	0E0	2.154E-15	Reset	PRBS 7-bit	v	PRBS 7-bit ~	1	Inject	Reset	Reset	Locked	Locked	None	¥	
% Link8	MGT_X0Y36/TX MGT_X0Y36/RX	11.300 Gbps	4.643E14	0E0	2.154E-15	Reset	PRBS 7-bit	÷	PRBS 7-bit ~	2	Inject	Reset	Reset	Locked	Locked	None	v	
S Link 9	MGT_X0Y37/TX MGT_X0Y37/RX	11.300 Gbps	4.643E14	0E0	2.154E-15	Reset	PRBS 7-bit	~	PRBS 7-bit ~	2	Inject	Reset	Reset	Locked	Locked	None	×	
S Link 10	MGT_X0Y38/TX MGT_X0Y38/RX	11.300 Gops	4.643E14	0E0	2.154E-15	Reset	PRBS 7-bit	~	PRBS 7-bit ~	2	Inject	Reset	Reset	Locked	Locked	None	¥	
% Link 11	MGT_X0Y39/TX MGT_X0Y39/RX	11.300 Gbps	4.643E14	0E0	2.154E-15	Reset	PRBS 7-bit	¥	PRBS 7-bit ~	2	Inject	Reset	Reset	Locked	Locked	None	÷	
S Link 12	MGT_X1Y16/TX MGT_X1Y16/RX	11.300 Gbps	4.643E14	OED	2.154E-15	Reset	PRES 7-bit	v	PRBS 7-bit ~	2	Inject	Reset	Reset	Locked	Locked	None	÷	
% Link 13	MGT_X1Y17/TX MGT_X1Y17/RX	11.300 Gbps	4.643E14	0E0	2.154E-15	Reset	PRBS 7-bit	~	PRBS 7-bit ~	2	Inject	Reset	Reset	Locked	Locked	None	÷	
% Link 14	MGT_X1Y18/TX MGT_X1Y18/RX	11.300 Gbps	4.643E14	OEO	2.154E-15	Reset	PRBS 7-bit	~	PRBS 7-bit ~	2	Inject	Reset	Reset	Locked	Locked	None	Ψ.	
% Link 15	MGT_X1Y19/TX MGT_X1Y19/RX	11.300 Gbps	4.643E14	0E0	2.154E-15	Reset	PRBS 7-bit	v	PRBS 7-bit ~	2	Inject	Reset	Reset	Locked	Locked	None	v	
% Link 16	MGT_X1Y20/TX MGT_X1Y20/RX	11.300 Gops	4.643E14	0E0	2.154E-15	Reset	PRBS 7-bit	×	PRBS 7-bit ~	2	Inject	Reset	Reset	Locked	Locked	None	v	
% Link 17	MGT_X1Y21/TX MGT_X1Y21/RX	11.300 Gbps	4.643E14	OED	2.154E-15	Reset	PRBS 7-bit	÷	PRBS 7-bit ~	2	Inject	Reset	Reset	Locked	Locked	None	v	
% Link 18	MGT_X1Y22/TX MGT_X1Y22/RX	11.300 Gbps	4.643E14	0E0	2.154E-15	Reset	PRBS 7-bit	÷	PRBS 7-bit ~	2	Inject	Reset	Reset	Locked	Locked	None	~	
% Link 19	MGT_X1Y23/TX MGT_X1Y23/RX	11.300 Gbps	4.643E14	0E0	2.154E-15	Resot	PRBS 7-bit	v	PRBS 7-bit ~	2	Inject	Reset	Reset	Lacked	Locked	None	v	
% Link 20	MGT_X1Y24/TX MGT_X1Y24/RX	11.300 Gaps	4.643E14	0E0	2.154E-15	Reset	PRBS 7-bit	\sim	PRBS 7-bit ~	2	Inject	Reset	Reset	Locked	Locked	None	~	
% Link 21	MGT_X1Y25/TX MGT_X1Y25/RX	11.300 Gaps	4.643E14	0E0	2.154E-15	Resot	PRBS 7-bit	.4	PRBS 7-bit ~	2	Inject	Reset	Reset	Locked	Locked	None	v	
% Link 22	MGT_X1Y26/TX MGT_X1Y26/RX	11.300 Gbps	4.643E14	0E0	2.154E-15	Reset	PRBS 7-bit	~	PRBS 7-bit ~	2	Inject	Reset	Reset	Locked	Locked	None	×	
% Link 23	MGT_X1Y27/TX MGT_X1Y27/RX	11,300 Gbps	4.643E14	0E0	2.154E-15	Reset	PRBS 7-bit	v	PRBS 7-bit v	2	Inject	Reset	Reset	Locked	Locked	None	v	
% Link24	MGT_X1Y28/TX MGT_X1Y28/RX	11,300 Gops	4.643E14	0E0	2.154E-15	Reset	PRBS 7-bit	÷	PRBS 7-bit v	2	inject	Reset	Reset	Locked	Locked	None	v	
% Link 25	MGT_X1Y29/TX MGT_X1Y29/RX	11.300 Gops	4.643E14	0E0	2.154E-15	Reset	PRBS 7-bit	.4	PRBS 7-bit ~	2	Inject	Reset	Reset	Locked	Locked	None	~	
% Link 26	MGT_X1Y30/TX MGT_X1Y30/RX	11.300 Gaps	4.643E14	0E0	2.154E-15	Reset	PRBS 7-bit	¥	PRBS 7-bit ~	2	Inject	Reset	Reset	Locked	Locked	None	~	
% Link 27	MGT_X1Y31/TX MGT_X1Y31/RX	11.300 Gbps	4.643E14	060	2.154E-15	Reset	PRBS 7-bit	¥	PRBS 7-bit v	1	Inject	Reset	Reset	Locked	Locked	None	×	
% Link 28	MGT_X1Y32/TX MGT_X1Y32/RX	11.300 Gbps	4.644E14	0E0	2.154E-15	Reset	PRBS 7-bit	¥	PRBS 7-bit ~	2	Inject	Reset	Reset	Locked	Locked	None	Ψ.	
% Link 29	MGT_X1Y33/TX MGT_X1Y33/RX	11.300 Gbps	4.644E14	0E0	2.154E-15	Reset	PRBS 7-bit	¥	PRBS 7-bit ~	1	Inject	Reset	Reset	Locked	Locked	None	~	
% Link 30	MGT_X1Y34/TX MGT_X1Y34/RX	11.300 Gops	4.644E14	0E0	2.154E-15	Reset	PRBS 7-bit	v	PRBS 7-bit v	×.	Inject	Reset	Reset	Lacked	Locked	None	¥	
% Link 31	MGT_X1Y35/TX MGT_X1Y35/RX	11.300 Gaps	4.644E14	0E0	2.154E-15	Reset	PRBS 7-bit	¥	PRBS 7-bit ~	2	Inject	Reset	Reset	Locked	Locked	None	w.	
S Link 32	MGT_X1Y36/TX MGT_X1Y36/RX	11.300 Gops	4.638E14	0E0	2.156E-15	Reset	PRBS 7-bit	¥	PRBS 7-bit v	2	Inject	Reset	Reset	Locked	Locked	None	~	
% Link 33	MGT_X1Y37/TX MGT_X1Y37/RX	11.300 Gaps	4.638E14	0E0	2.156E-15	Reset	PRBS 7-bit	¥	PRBS 7-bit ~	2	Inject	Reset	Reset	Locked	Locked	None	~	
% Link 34	MGT_X1Y38/TX MGT_X1Y38/RX	11,300 Gbps	4.638E14	0E0	2.1566-15	Reset	PRBS 7-bit	~	PRBS 7-bit ~	2	Inject	Reset	Reset	Locked	Locked	None	~	
% Link 35	MGT_X1Y39/TX MGT_X1Y39/RX	11.300 Gaps	4.638E14	OED	2.156E-15	Reset	PRBS 7-bit	~	PRBS 7-bit ~	2	Inject	Reset	Reset	Locked	Locked	None	~	
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后端触发电子学板测试结果:

- 单通道达到 11.3Gbps 满足验收指标 ≥10Gbps
- 单板: 406.8Gbps (36ch*11.3Gbps/ch) 满足验收指标单板≥400Gbps



iRPC后端触发电子学板小批量生产进展



iRPC后端触发电子学板生产 情况:

- PCB板已经完成;
- 主要芯片FPGA已经到 国内;
- 其余芯片已经全部下单, 并部分到货。





二维读出探测器的联调

- •为什么二维读出?
 - CMS二期升级将采用双端读出的前端电子学(A方案)
 - 但法国合作者的进度一再拖延
 - 故跟RPC合作组讨论决定联调采用B方案,即二维读出的电子学
- •困难
 - •二维读出的电子学有经过甄别器输出到TDC输入
 - •我们必须基于甄别器输出,设计FEE前端读出电路 (数据汇总板GBF。见下页)

前端数据汇总板设计



根据需要临时开发的 汇总板

- Kintex-7 FPGA:
 - GBT-FPGA,
 - TDC-FPGA,
 - Rising&Falling Edge, 2.5ns
- E-link Interface:
 - 32 pairs of LVDS input
- SMA Interface:
 - External clock input from BEE
- Trigger Interface:
 - Pulse Generator or Scintillator
- QSFP:
 - 4-channel optical module, GBT link





904楼探测器联调测试



- FEE(ASIC)-X
- FEE(ASIC)-Y
- 触发
 - Scintillator
 - Timer
- GBF前端板
 - Data-Collector
- BEE 后端板
- 控制 PC
- 参加人员

CERN: 曹鹏程, 寇含君, 刘振安 北京: 赵京周, 宋嘉宁, 陶嘉, 龚文煊



904楼探测器联调测试



- iRPC 2D chamber
 - X 16 strips, 3 dead
 - Y 10 strips, 1 dead
- Trigger: Timer/Scintillator

- one BEE board
- two Data Collector boards
 - 16 inputs each
- One server for SC and DAQ



904楼探测器联调测试结果





2020/8/11

iRPC探测器FEE数据模拟



- 前端电子学模拟
 - 出发点
 - iRPC双端读出前端电子学板 目前无法联调
 - 实验室缺乏实际的前端板和 探测器来验证后端电子学系 统可行性
 - 解决方案
 - 模拟iRPC探测器击中情况产 生一个数据源: 根据TDR提供 的iRPC参数模拟产生数据文 件
 - FEE emulator: 模拟前端电子 学功能,与后端进行交互



iRPC前后端固件开发



- 前端电子学打包、发送
 - FEE根据event rate读取模拟数据并加入bcn信息, bcn间隔与event rate相关;
 - 数据依次进入mux FIFO、transmission FIFO,通过GBT链路发送给BEE;
- •后端电子学接收解码、簇查找
 - 数据接收后放入demux FIFO;
 - 解码后的数据按簇查找算法进行簇查找,给出中心条号,使用查找表给出 击中角度φ和半径r;



iRPC读出电子学原型系统架构设计示意图

RPC合作组对工作的认可



- PRC合作组负责人Gabriella对 触发组的工作认可:
 - 1.RPC后端电子学系统做的ATCA 的原型设计
 - 2. iRPC后端电子学板的设计和原型系统的搭建
 - 3. 在CERN 904 原型系统的搭建 及与探测器的联调测试



Università degli Studi di Bari Politecnico di Bari Gabriella Pugliese Associate Professor Dipartimento Interateneo di Fisica Via Amendola 174, Bari Italy Tel. +390805442346 Email Gabriella.pugliese@doa.infn.it

To whom it may concern

As project manager of the RPC subsystem of the CMS experiments at CERN, I certify the progress made by the group of the Institute of High Energy Physics, Chinese Academy of Sciences (IHEP), under the supervision of Prof. Zhen-An Liu. Within the RPC upgrade program for HL-LHC phase, the IHEP group is responsible of developing the new Backend for the present RPC system and for the new RPC stations to be installed at high eta region of CMS. These stations, RPC 3/1 and 4/1, will be equipped with a new generation Resistive Plate Chambers (RPC) detectors (iRPC). In detail, the following milestones have been fulfilled:

≻ Early 2019:

- IHEP proposal for a new RPC backend system
- HEP modular ATCA prototype development for the proposal
- Serenity joint work recommendation

≻ Middle 2019:

- Development of uTCA board for iRPC backend/off-detector electronics
- · Development of iRPC backend demonstration setup
- ≻ Early 2020:
 - Development and validation of a backend system at CERN in 904 Laboratory
 - Joint test between Backend and an iRPC detector prototype equipped with a new FEB electronics.
 - Chamber test with cosmic muons and validation of the Backend system.

I would like to express my congratulation with the great progress done and successfully results obtained.

In case you need more information feel free to contact me.

Yours sincerely,

Gamille Puplione

发表文章1篇



- •关于iRPC电子学读出文章1篇,CMS合作组审核通过。
- RDTM已接收。

文章在RPC合作组内审核通过(邮件)

Hi Pengcheng,

Yes, from the RPC side the approval is over. Thank you for your accurate work. Now we are waiting for a Muon decision. I think a Muon group reviewer should be already assigned. Best! Roumyana Roumyana Mileva Hadjiiska
 To: Pengcheng Cao; Sijin Qian

Cc: 🗐 Borislav Pavlov

- You forwarded this message on 16/07/2020 11:16.

Hi Pengcheng,

```
Yes, from the RPC side the approval is over.
Thank you for your accurate work.
Now we are waiting for a Muon decision.
I think a Muon group reviewer should be already assigned.
Best!
Roumyana
```

文章在Muon合作组内审核通过(邮件)

Dear all,

All my editorial comments have been suitably dealt with and I approve going to the next step, whatever that is, and if it is really required for me to say so.

Regards, Richard

 Richard Breedon [breedon@physics.ucdavis.edu] In response to the message from Pengcheng Coo, Thu 16/07 To: Pengcheng Coo, Thu 16/07 To: Source State Pengcheng Coo, Thu 16/07 Coo State State Pengcheng Coo, Thu 16/07 Coo State Pengcheng Coo, State State Pengcheng Peng

Dear all,

All my editorial comments have been suitably dealt with and I approve going to the next step, whatever that is, and if it is really required for me to say so. Regards, Richard

文章在CMS出版委员会内审核通过(邮件)

Dear Jesus, PubComm has no objections if the relevant conveners agree with the author list (and content, of course). Best wishes, Claudia

Claudia Wulz
 Ter (ii) Issa Purta Pelaye
 Ga (ii) Cetra Lawrence (iii) East Simple Andre (iii) Indiard Intendors (iii) Pengtheng Cet. (iii) Roumyana Mines Hadjiske (iii) Sjin Qan
 -You replied on 18/07/2020 13:50.
 Dear Jesus,

PubComm has no objections if the relevant conveners agree with the author list (and content, of course). Best wishes, Claudia

Noname manuscript No. (will be inserted by the editor)

Research and Development of the Readout

- Electronics System for the Improved Resistive Plate
- Chambers in CMS

P. Cao^{1,2}, Z.-A. Liu^{1,2}, J. Zhao^{1,2} J. Tao^{1,2}, H. Kou^{1,2}, J. Song^{1,2}, W. Gong², A. Fagot^a, M. Gul^a, 7 C. Roskas^a, M. Tytgat^a, N. Zaganidis^a, S. Fonseca De Souza^b, A. Santoro^b • F. Torres Da Silva De Araujo^b A. Aleksandrov^c, R. Hadjiiska^c, P. Iaydjiev^c, M. Rodozov^c, M. Shopova^c, 12 G. Sultanov^c, A. Dimitrov^d, L. Litov^d, B. Pavlov^d, P. Petkov^d, A. Petrov^d, S.J. Qiane, D. Hanf, Y. Wangf, C. Avilas, A. Cabreras, C. Carrillos, M. Segura^g, S. Aly^h, A. Mahrous^h, A. Mohamed^h, Y. Assran^{hh,hhh}, " C. Combaretⁱ, M. Gouzevitchⁱ, G. Grenierⁱ, F. Lagardeⁱ, I.B. Laktinehⁱ, » H. Mathezⁱ, L. Mirabitoⁱ, K. Shchabloⁱ I. Bagaturia^j, D. Lomidze^j, I. Lomidze^j, L.M. Pant^k, V. Bhatnagar^l, R. Gupta^l, R. Kumari¹, M. Lohan¹, J.B. Singh¹, V. Amoozegar^m, B. Boghrati^{m,n}, H. Ghasemy^m, S. Malmir^m, M. Mohammadi Najafabadi^m 7 M. Abbresciaº, A. Gelmiº, G. Iaselliº, S. Lezki^o, G. Pugliese^o, L. Benussi^p, » S. Bianco^p, D.Piccolo^p, F. Primavera^p, » S. Buontempo⁹, A. Crescenzo⁹, G. Galati^q, F. Fienga^q, I. Orso^q, L. Lista^q, » S. Meola^q, P. Paolucci^q, E. Voevodina^q, A. Braghieri^r, P. Montagna^r, M. Ressegotti^r, C. Riccardi^r, P. Salvini^r, P. Vitulo^r, S.W. Cho^s, » S.Y. Choi^s, B. Hong^s, K.S. Lee^s, " J.H. Lims, S.K. Parks, J. Goht,tt. » T.J. Kim^t, S. Carrillo Moreno^u, » O. Miguel Colin^u, F. Vazquez Valencia^u, « S. Carpintevro Bernardino^v,

4 J. Eysermans^v, I. Pedraza^v,



小结与后续计划



- iRPC后端触发电子学板小批量生产进展顺利。触发电子 学板指标满足验收指标。
- 2020年1-3月在CERN完成了二维读出探测器的联调测试, 取得巨大成功。
- 实验结果显示高能所iRPC后端系统基本功能正确,数据 读出可靠。证明高能所设计的方案基本可行。文章正在 发表中。
- RPC合作组对触发组的工作做了认可。
- iRPC后端系统,期待与法国iRPC 双端读出FEE联调。
- 依据联调结果决定最终量产计划与明年安装时间