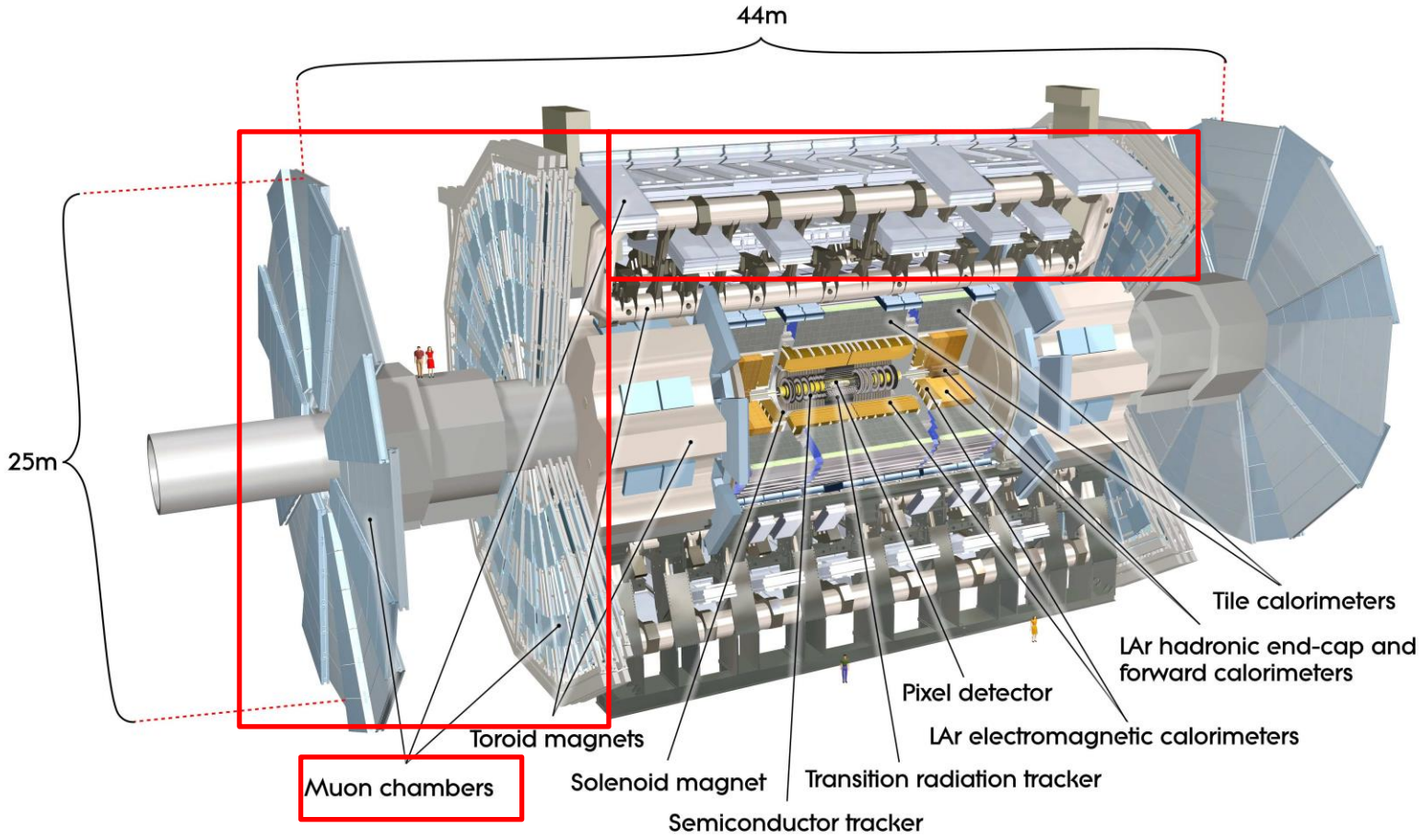
TDC ASIC Design for MDT in ATLAS Phase II Upgrade

Yuxiang Guo August 12th, 2020
University of Science and Technology of China
University of Michigan

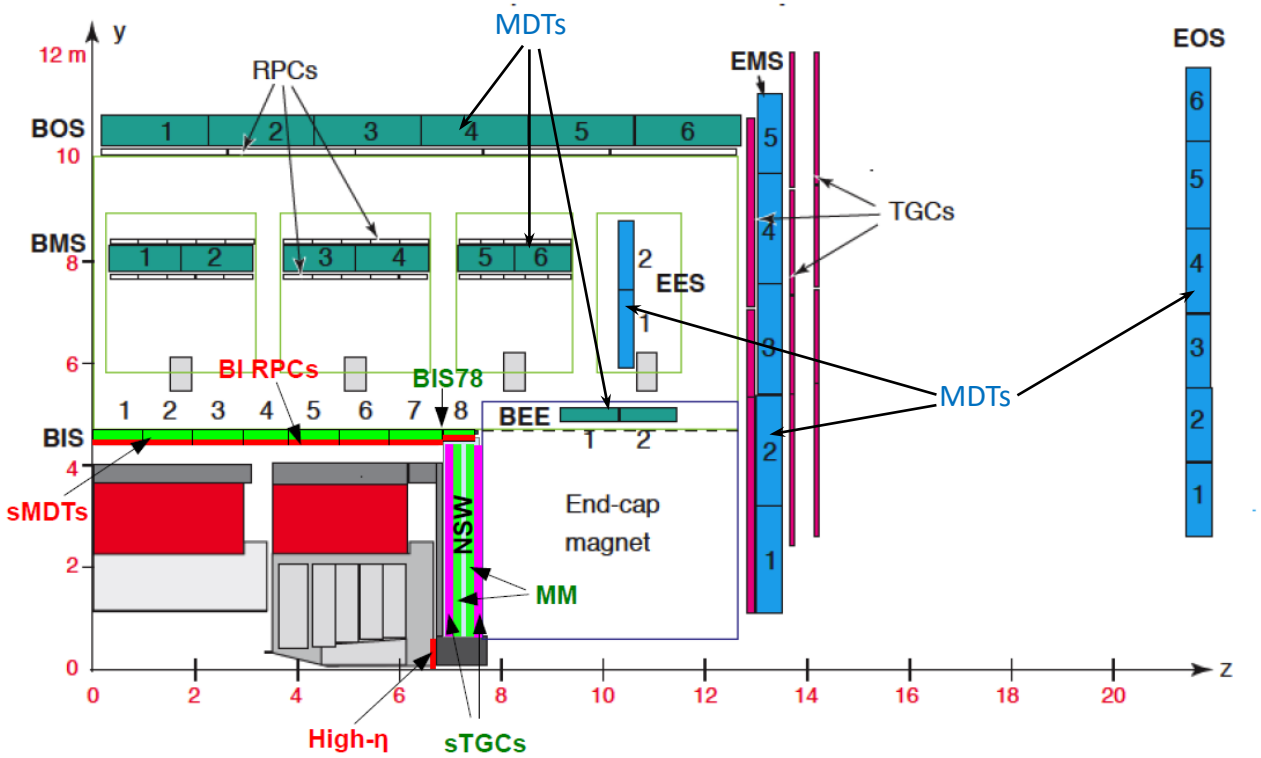
Outline

- Introduction
- TDC ASIC design
- Testing of the TDC
- Summary

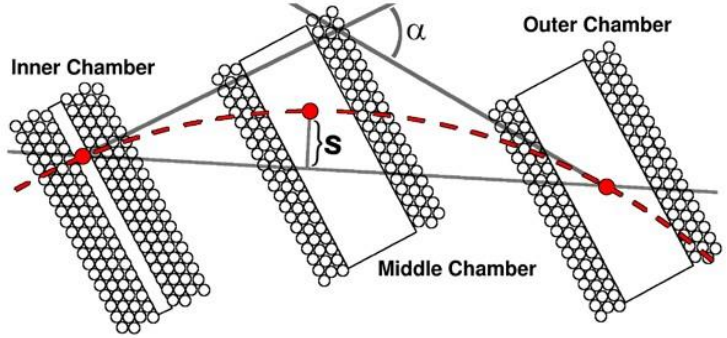


ATLAS Monitored Drift Tube (MDT) Detector

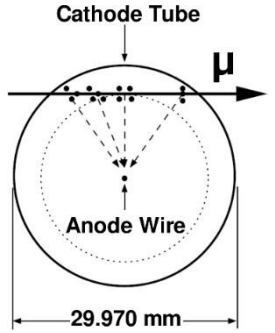
- ATLAS muon spectrometer is mainly used for muon triggering, identification and momentum measurement;
- Provides a standalone transverse momentum measurement (10% at 1 TeV), mainly by the Monitored Drift Tube (MDT) chambers;

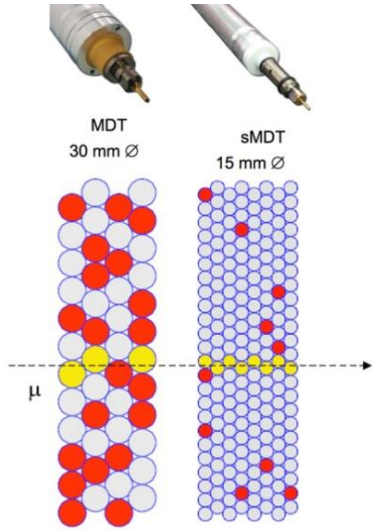


R-Z views of the Phase-II ATLAS muon spectrometer layout (small sector)



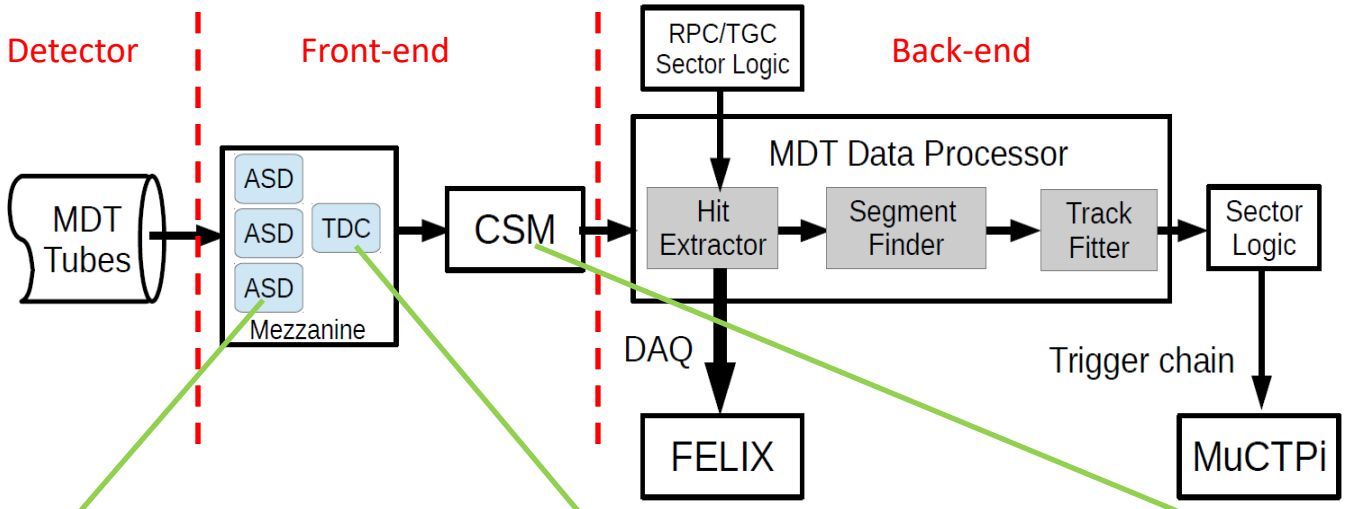
3-station MDT chambers to measure transverse momentum





MDT Frontend Electronics Upgrade

- Monitored Drift Tube(MDT) in the current system is only used for precision readout;
- After the Phase II upgrade, MDT information will be used also at the first-level trigger;
- MDT electronics needs to cope with the new ATLAS TDAQ scheme.



Block diagram of the MDT trigger and readout electronics for HL-LHC runs

ASD

- Lower peaking time delay;
- larger sensitivity and higher SNR for a minimum charge of 5fC.

TDC

- 0.78ns binsize, 102.4us dynamic range;
- Triggerless working mode;
- 320Mbps *2 output data rates.

CSM

- lpGBT: 320Mbps *36 input e-links;
- 10.24Gbps *2 output optical links.

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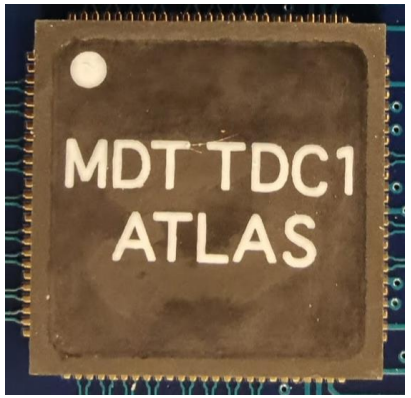
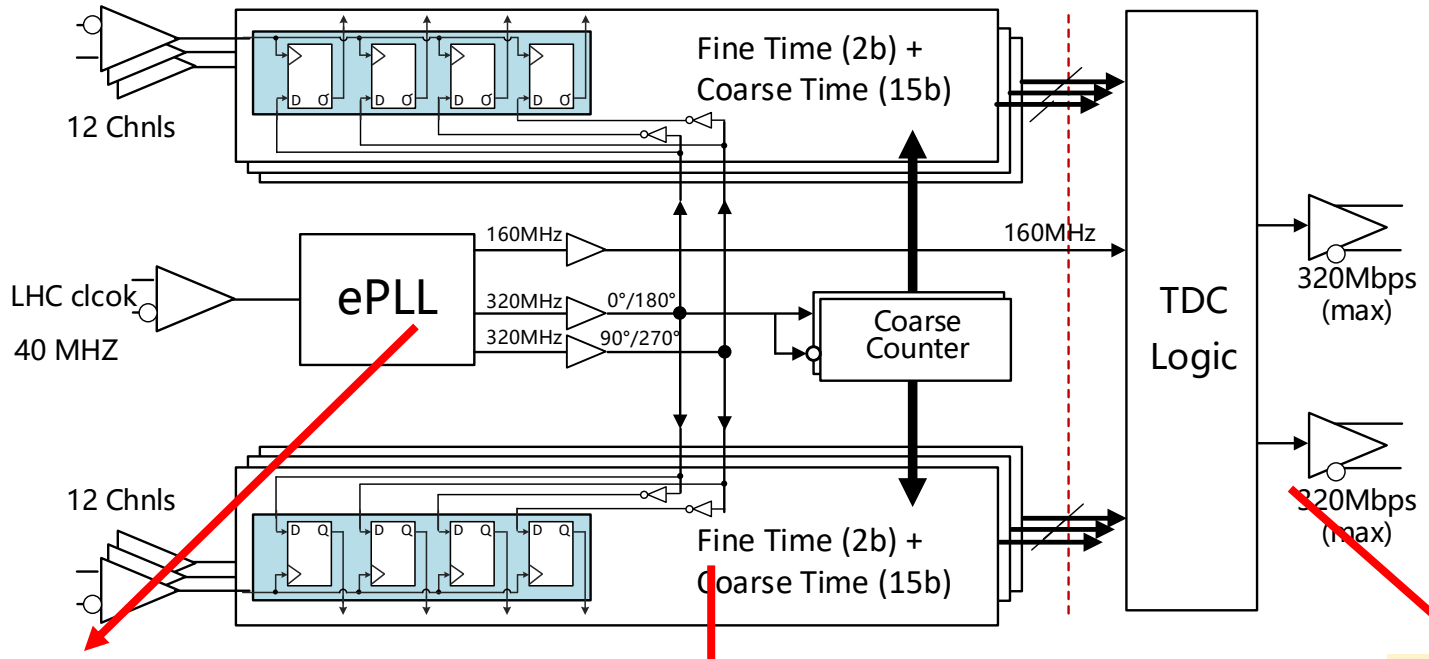
Timeline of the new TDC ASIC



Nov. 2016 → Dec. 2018 → Jan. 2020

- 1st Version
  - ✓ 0.13 µm CMOS GF
  - ✓ QFN100
  - ✓ Rising/Falling/Pair measurement
  - ✓ Triggerless mode
  - ✓ 24 input channels
  - ✓ 320Mbps*2 output
  - ✓ 355mW @1.5V
- 2nd Version
  - ✓ 0.13 µm CMOS TSMC
  - ✓ QFN100
  - ✓ Sampling circuits optimized
  - ✓ Triggered mode implemented
  - ✓ 250mW @1.2V
- 3rd Version
  - ✓ 0.13 µm CMOS TSMC
  - ✓ BGA144
  - ✓ TMR implemented
  - ✓ Minor bugs fixed
  - ✓ 257mW @1.2V

Architecture of the new TDC ASIC



The schematic diagram of the TDC ASIC*

Part 1: ePLL (extended Phase-locked loop)
- Migrate from CERN ePLL

Part 2: Timing Circuit:
- Timing unit: fine time + coarse time
  - 4 clock phase time Interpolator
  - Coarse time(15bit) + fine time(2bit)
  - 0.78 ns bin
- Optimization in power consumption

Part 3: TDC logic:
- Full feature logic
  - Triggerless operation { Pair Mode / Edge Mode
  - Trigger operation { Pair Mode / Edge Mode
  - Output protocol
  - High speed interface

Part 4: Interface
- Serial outputs
- Configuration
- Reference clocks
- TTC

*Y. Liang et al., Design and performance of a TDC ASIC for the upgrade of the ATLAS Monitored Drift Tube detector. NIM-A, 939, 10-15 (2019).

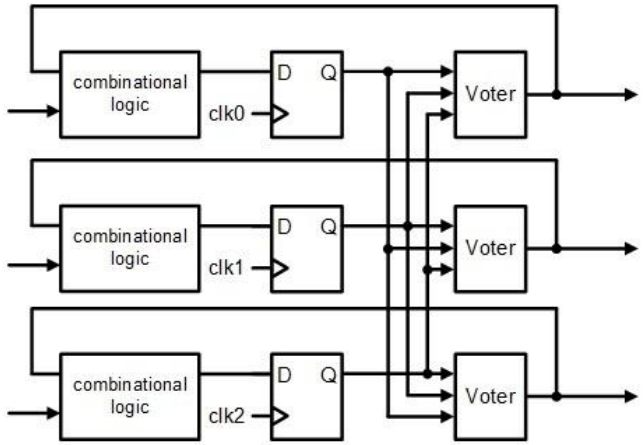
Radiation Tolerance Requirement

Radiation-tolerance criteria with safety factors for the BIS78 region

	SRL	SFsim	SFldr	SFlot	RTC
TID (krad)	5.6	1.5	1.5	2	25.2
NIEL(10^{11}n/cm^2)	13.2	2	1	2	52.8
SEE(10^{11}n/cm^2)	2.24	2	1	2	8.96

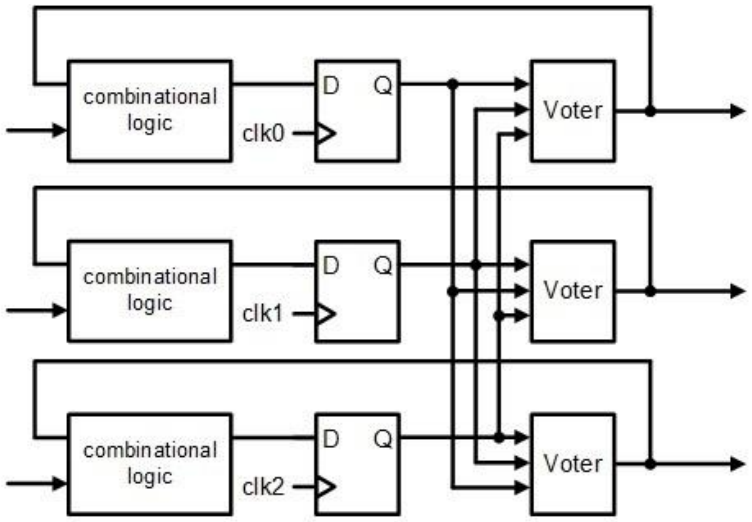
- NIEL: Modern CMOS integrated circuits are insensitive to displacement damage.
- TID: 25krad is insignificant for the 130nm CMOS techonology.
- SEE: Recoverable (SET, SEU) and non-recoverable (latch-up, burnout, gate rupture)

For Recoverable SEE, Triple Module Redundancy (TMR) is effective!



TMR with 3 voters and individual combinational logic

TMR Implementation

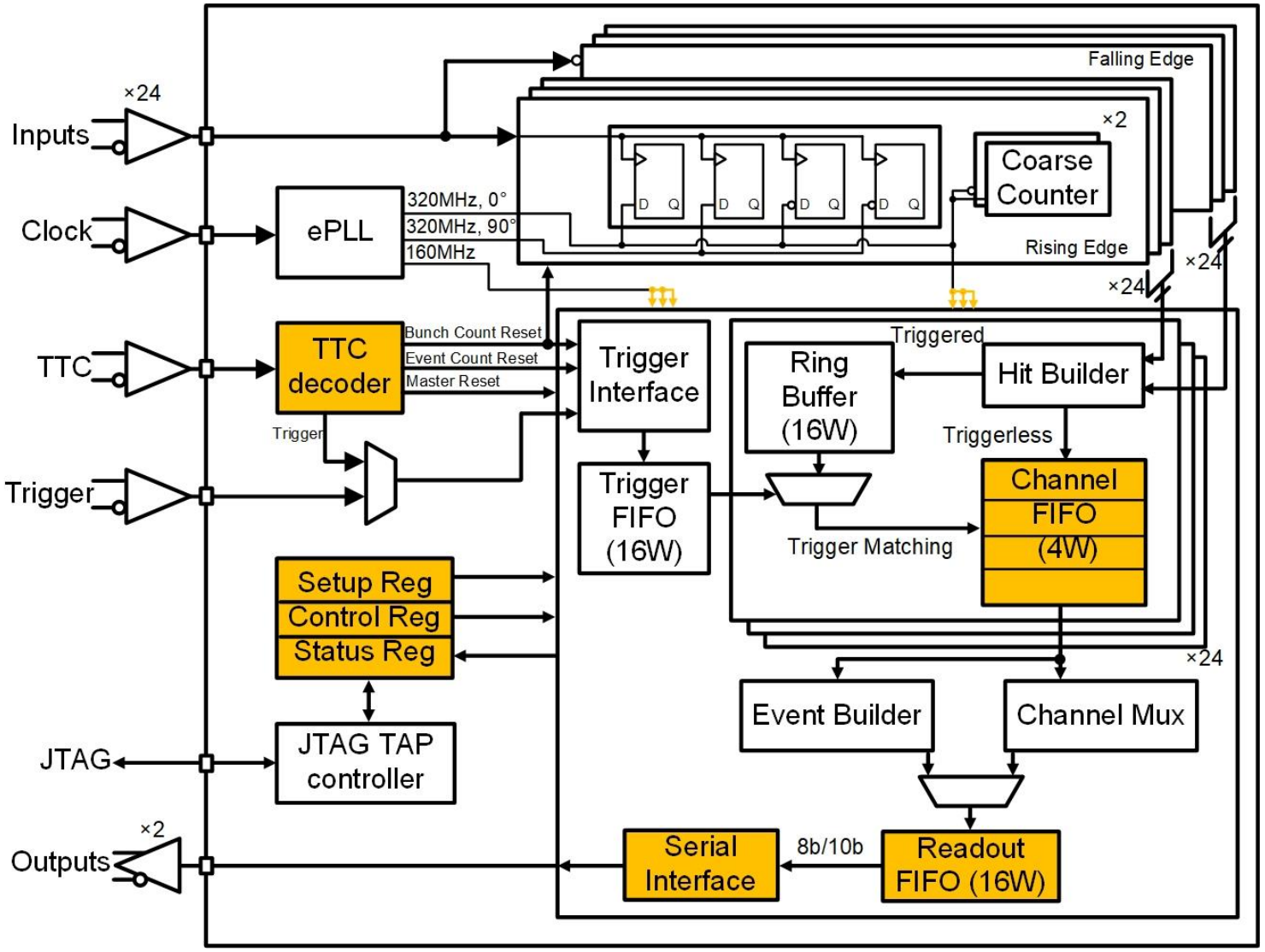


TMR with 3 voters and individual combinational logic

Power Consumption	TDC V1 Measured (mW)	Full TMR Estimated (mW)
Digital	146	438
Analog	104	104
Total	250	542

- A 3 times power consumption in the digital logic is expected if TMR is implemented fully! Power consumption is not acceptable, let alone die area…
- Solution: TMR only implemented in critical logic blocks.

TMR Implementation



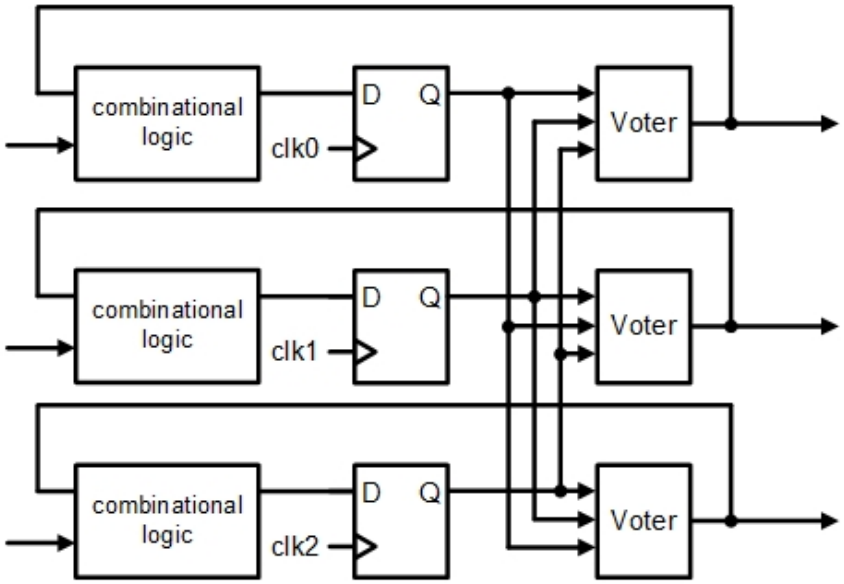
Block diagram of the new TDC ASIC with TMR implemented (Yellow)

Idea: Protect the working flow/mode, not timing information for one hit!

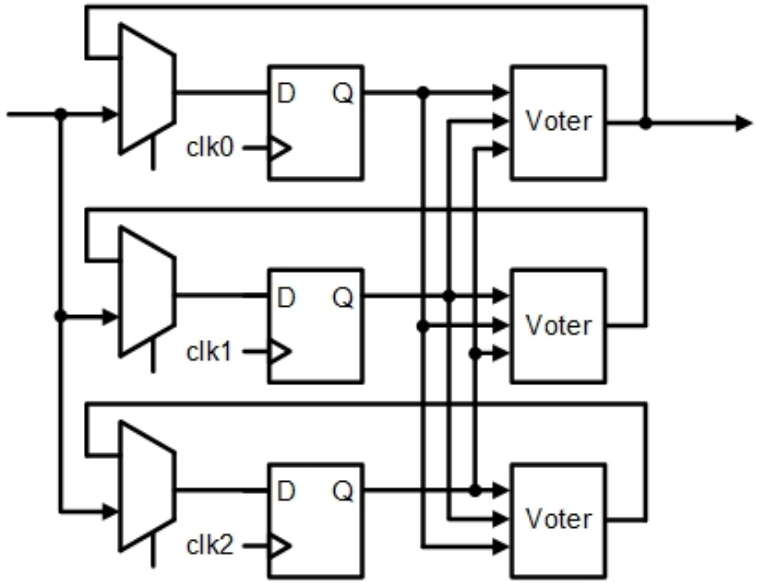
Four different TDC logic categories:

- Sampling logic
- Memory logic
- Flow control logic
- Configuration logic

TMR Implementation



(a) TMR with 3 voters and individual combinational logic



(b) TMR with data scrubbing

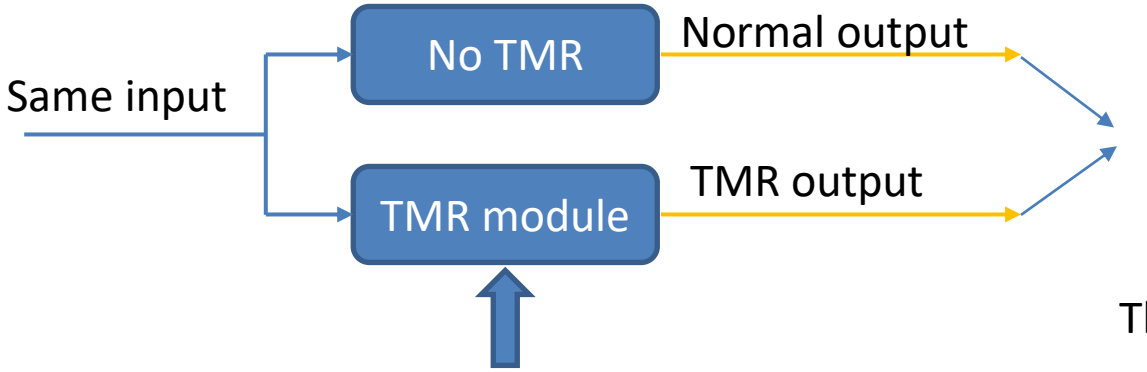
Flow control logic TMR cell

- Internal state machine, FIFO pointers

Configuration logic TMR cell

- External JTAG input

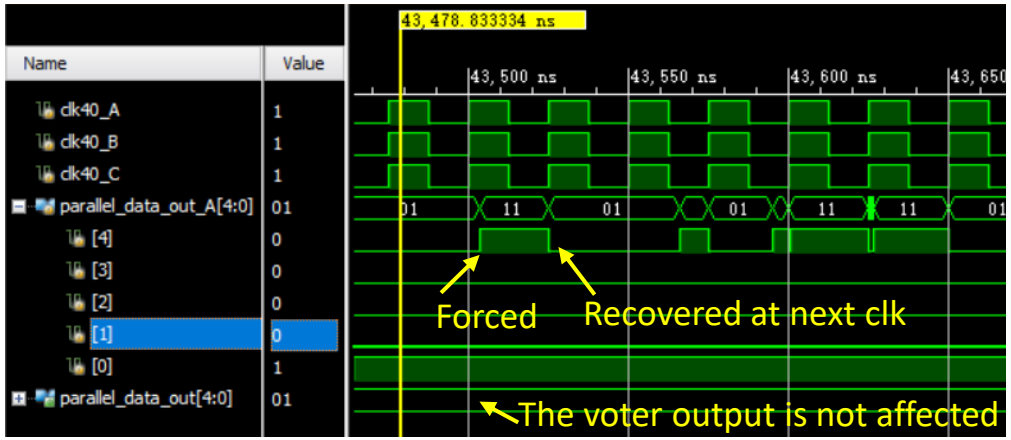
TMR block behavioral simulation



Monitor the outputs and check if they are equal to each other

Three different ways to simulate SEU:

- Change 1 clk frequency -> clock glitches
- Shut down 1 of the 3 clks -> clock miss
- Force register to reverse -> register upset



At43503.56563ns common_setup_with_TMR_inst.TTC_setup.parallel_data_out_A[4] force to 1
At 43503.56662ns common_setup_with_TMR_inst.TTC_setup.parallel_data_out_A[4] released
At43566.06563ns common_setup_with_TMR_inst.TTC_setup.parallel_data_out_A[4] force to 1
At 43566.06662ns common_setup_with_TMR_inst.TTC_setup.parallel_data_out_A[4] released

Example for one register forced to be reversed

TDC Logic Digital Simulation (after place and route)

Triggerless Pair mode hit data

```
303859.00 ns Info: Channel 19, leading edge 0x04a4d (coarse time 0x1293, fine time 0x1), width 166, indicate b11
304297.00 ns Info: Channel 19, leading edge 0x04c76 (coarse time 0x131d, fine time 0x2), width 172, indicate b11
304719.00 ns Info: Channel 19, leading edge 0x04ea7 (coarse time 0x13a9, fine time 0x3), width 155, indicate b11
305125.00 ns Info: Channel 19, leading edge 0x050c9 (coarse time 0x1432, fine time 0x1), width 139, indicate b11
305531.00 ns Info: Channel 19, leading edge 0x052de (coarse time 0x14b7, fine time 0x2), width 109, indicate b11
305969.00 ns Info: Channel 19, leading edge 0x054d3 (coarse time 0x1534, fine time 0x3), width 168, indicate b11
306391.00 ns Info: Channel 19, leading edge 0x05705 (coarse time 0x15c1, fine time 0x1), width 154, indicate b11
309828.00 ns Info: Channel 20, leading edge 0x06820 (coarse time 0x1a08, fine time 0x0), width 175, indicate b11
310219.00 ns Info: Channel 20, leading edge 0x06a51 (coarse time 0x1a94, fine time 0x1), width 106, indicate b11
310656.00 ns Info: Channel 20, leading edge 0x06c3e (coarse time 0x1b0f, fine time 0x2), width 174, indicate b11
```

Triggerless Edge mode hit data

```
360010.00 ns Single hit leading mode test start=========================
364853.00 ns Info: Channel 0, edge 0x00244 (coarse time 0x0091, fine time 0x0), indicate b01
365228.00 ns Info: Channel 0, edge 0x00421 (coarse time 0x0108, fine time 0x1), indicate b01
365634.00 ns Info: Channel 0, edge 0x0063a (coarse time 0x018e, fine time 0x2), indicate b01
366009.00 ns Info: Channel 0, edge 0x0081f (coarse time 0x0207, fine time 0x3), indicate b01
366384.00 ns Info: Channel 0, edge 0x009f5 (coarse time 0x027d, fine time 0x1), indicate b01
366775.00 ns Info: Channel 0, edge 0x00be6 (coarse time 0x02f9, fine time 0x2), indicate b01
367181.00 ns Info: Channel 0, edge 0x00def (coarse time 0x037b, fine time 0x3), indicate b01
367603.00 ns Info: Channel 0, edge 0x01011 (coarse time 0x0404, fine time 0x1), indicate b01
```

- Typical path delay shown, also checked with min/max delay
- TMR registers checked after place and route to ensure the redundant registers are not removed during synthesis.

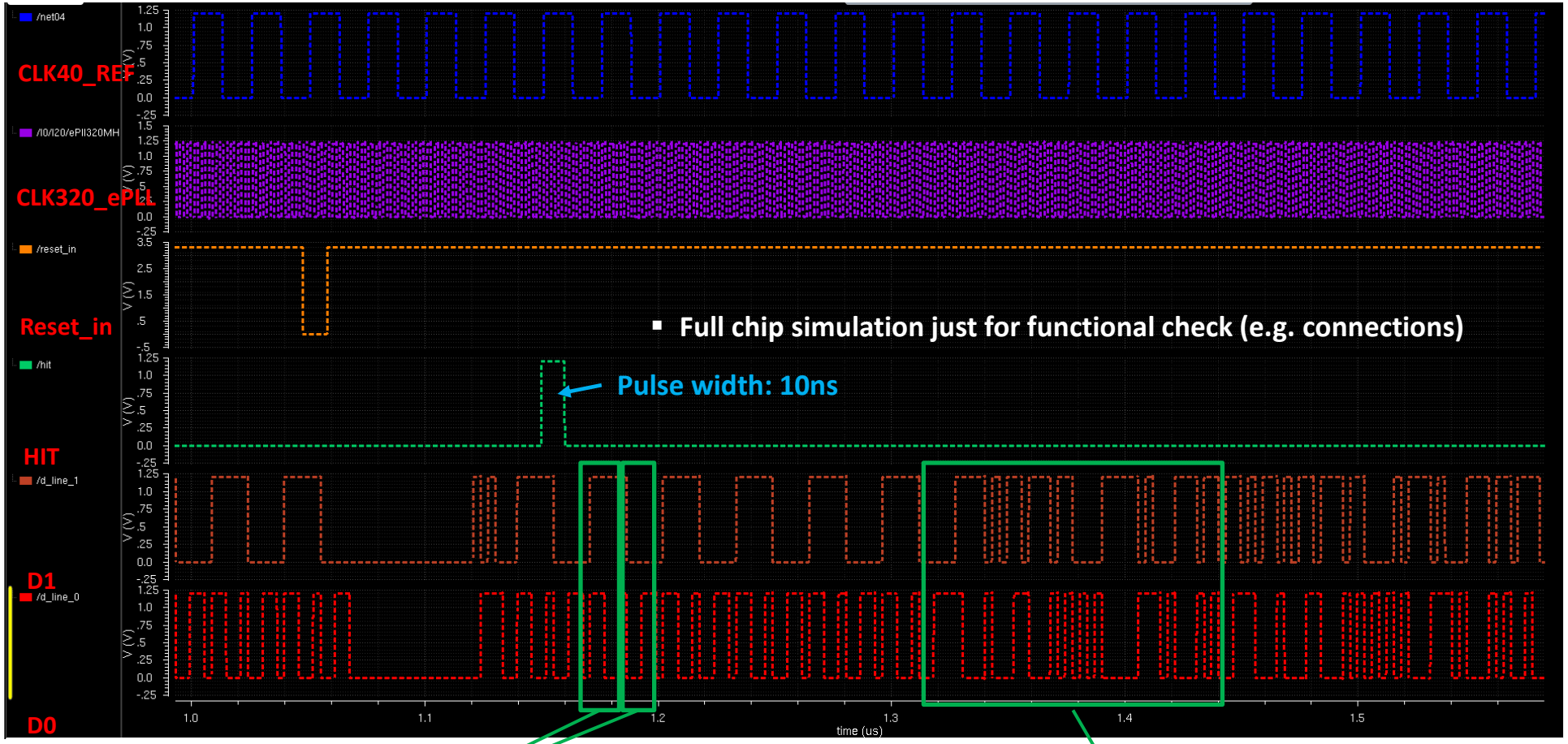
Trigger pair mode hit data

```
578000.00 ns Trigger matching test start=========================
586288.00 ns Info: event id: 0, bunch id: 0x036
586347.00 ns Info: Channel 23, leading edge 0x00554 (bunch id 0x02a,coarse time 0x0155, fine time 0x0), width 128, indicate b11
586409.00 ns Info: Channel 0, leading edge 0x00554 (bunch id 0x02a,coarse time 0x0155, fine time 0x0), width 128, indicate b11
586453.00 ns Info: HIt counter 2=========================
```

JTAG interface

```
110269.00 ns : JTAG ID_CODE check pass
110269.00 ns : Finish JTAG ID_CODE interface simulation
110269.00 ns : Start JTAG setup_0 interface simulation
113744.00 ns : JTAG setup_0 default check pass
117219.00 ns : JTAG setup_0 all 0s check pass
120694.00 ns : JTAG setup_0 all 1s check pass
124169.00 ns : JTAG setup_0 noramal operation check pass
124169.00 ns : Finish JTAG setup_0 interface simulation
```

Full chip Simulation (analog, 25°C, typical, 1.2V)



❑ Idle packet

- After alignment and 8b/10b decoding: **10111100 (K28.5)** which is the comma of triggerless edge mode.

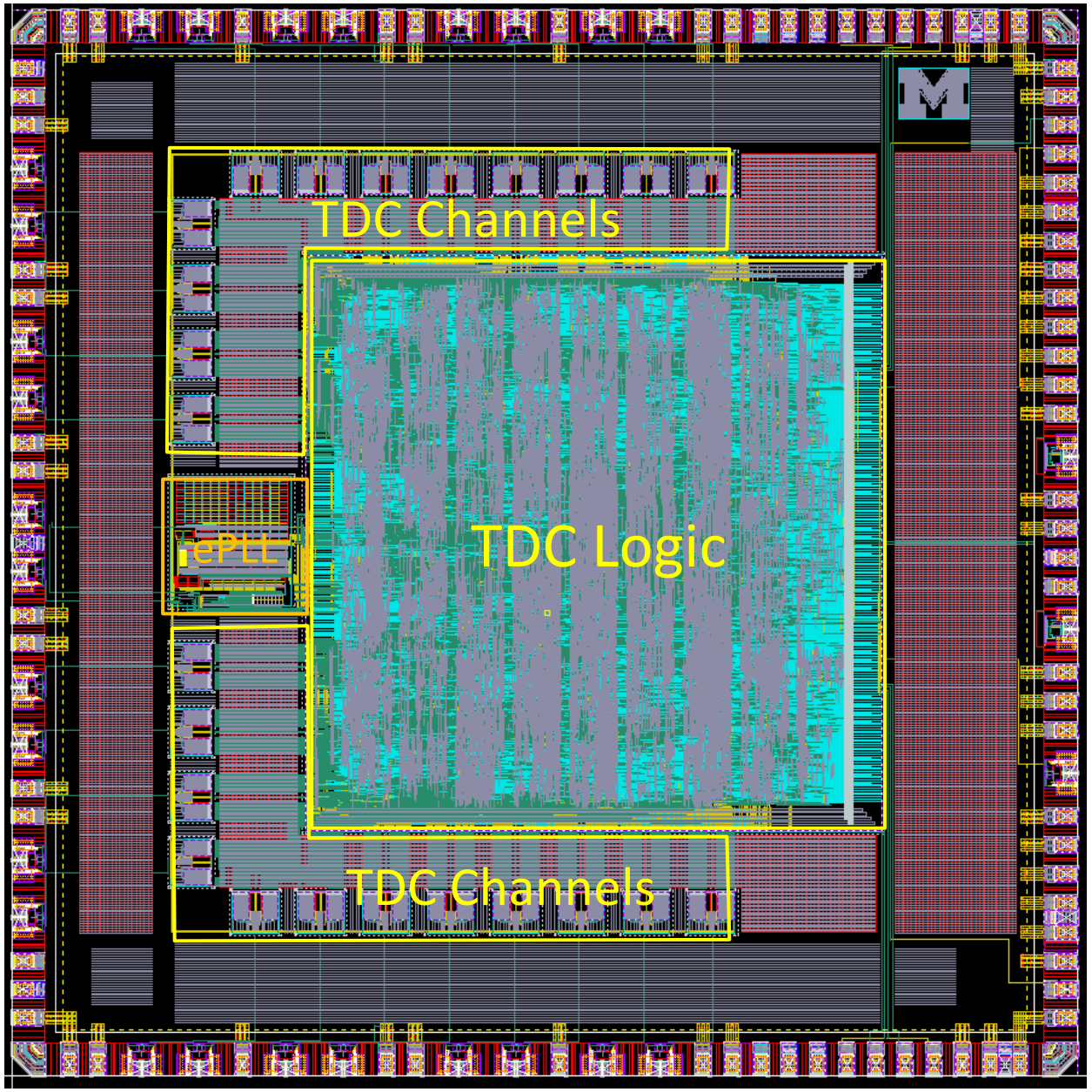
❑ Data packet (example as below)

- After alignment and 8b/10b decoding:

10111 11 0000000000110110 00001101

Chnl ID: #23	Edge Mode : Pair mode	Time MEAS.: 54*0.78n=42.12n	Pulse Width: 13*0.78n=10.14n

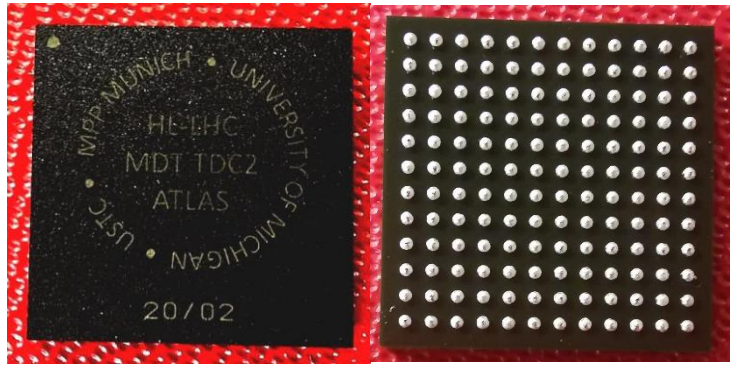
TDC ASIC Layout



Die Dimension
3.7 mm * 3.7 mm

	1	2	3	4	5	6	7	8	9	10	11	12	
A	GND	GND	CHNL7_P	CHNL6_P	CHNL5_P	CHNL4_P	CHNL3_P	CHNL2_P	CHNL1_P	CHNL0_P	TDO	TMS	A
B	CHNL8_P	CHNL8_N	CHNL7_N	CHNL6_N	CHNL5_N	CHNL4_N	CHNL3_N	CHNL2_N	CHNL1_N	CHNL0_N	Reset_in	TRST	B
C	CHNL9_P	CHNL9_N	GND	GND	GND	GND	GND	GND	GND	GND	TCK	TDI	C
D	CHNL10_P	CHNL10_N	GND	VDD_A	VDD_A	GND	GND	VDD_D	VDD_D	VDD_PST3	VDD_PST3	VDD_PST3	D
E	CHNL11_P	CHNL11_N	VDD_PST0	VDD_A	VDD_A	GND	GND	VDD_D	VDD_D	VDD_PST2	TDC_DOUT1_N	TDC_DOUT1_P	E
F	TDC_CLK_P	TDC_CLK_N	VDD_PST0	VDD_A	VDD_A	GND	GND	VDD_D	VDD_D	VDD_PST2	GND	GND	F
G	BCR_P	BCR_N	VDD_PST0	VDD_A	VDD_A	GND	GND	VDD_D	VDD_D	VDD_PST2	TDC_DOUT0_N	TDC_DOUT0_P	G
H	CHNL12_P	CHNL12_N	VDD_PST0	VDD_A	VDD_A	GND	GND	VDD_D	VDD_D	VDD_PST2	TTC_N	TTC_P	H
J	CHNL13_P	CHNL13_N	GND	VDD_A	VDD_A	GND	GND	VDD_D	VDD_D	VDD_PST1	VDD_PST1	VDD_PST1	J
K	CHNL14_P	CHNL14_N	GND	GND	GND	GND	GND	GND	GND	GND	GND	ASD_DIN	K
L	CHNL15_P	CHNL15_N	CHNL16_N	CHNL17_N	CHNL18_N	CHNL19_N	CHNL20_N	CHNL21_N	CHNL22_N	CHNL23_N	ASD_LOAD	ASD_DOUT	L
M	GND	GND	CHNL16_P	CHNL17_P	CHNL18_P	CHNL19_P	CHNL20_P	CHNL21_P	CHNL22_P	CHNL23_P	ASD_DOWN	ASD_TCK	M
	1	2	3	4	5	6	7	8	9	10	11	12	

BGA substrate pin assignment



TDC ASIC with a 12x12 BGA package (1mm pitch), received in Jan. 2020.

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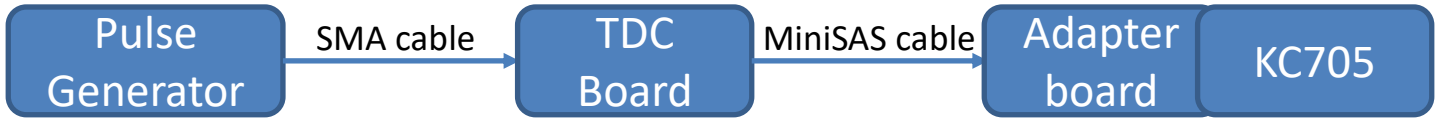
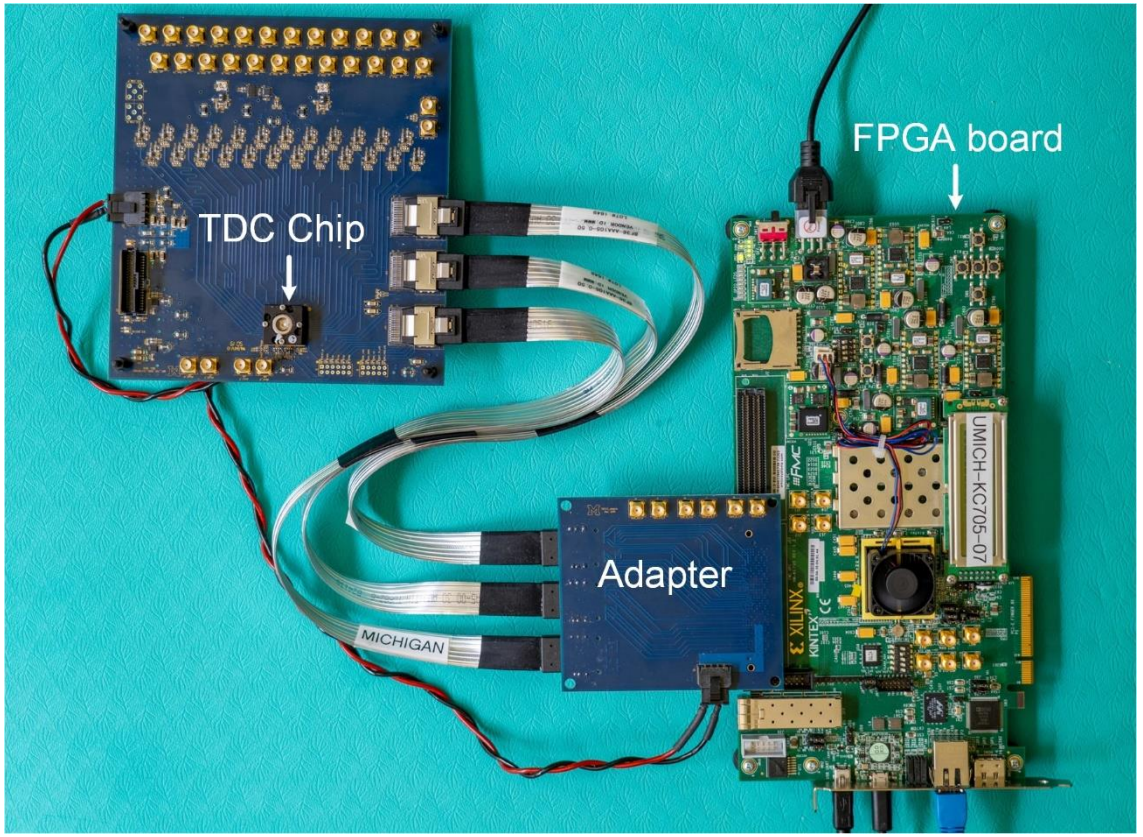
TDC Test Fixture



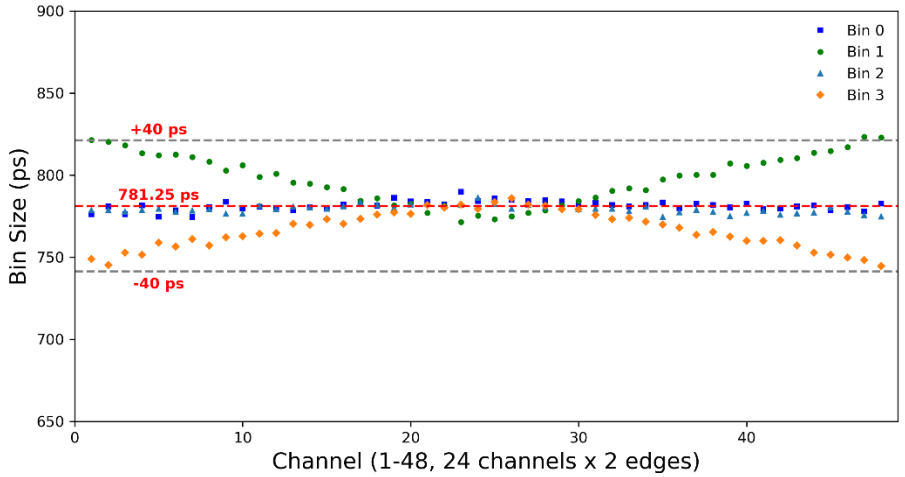
- Timing performance is tested using a pulse generator based on FPGA MMCM.



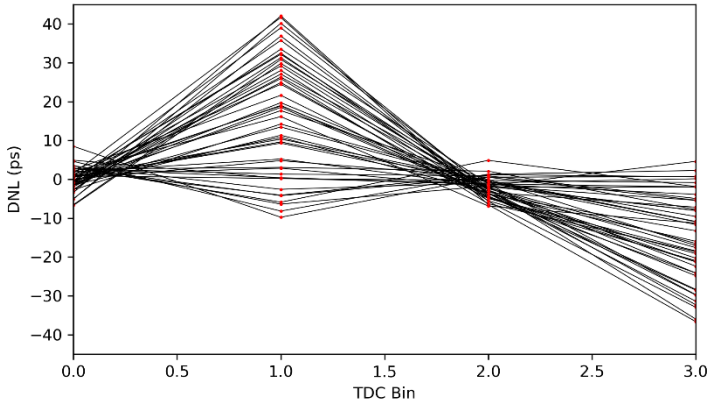
TDC test fixture

Performance of TDC bin size

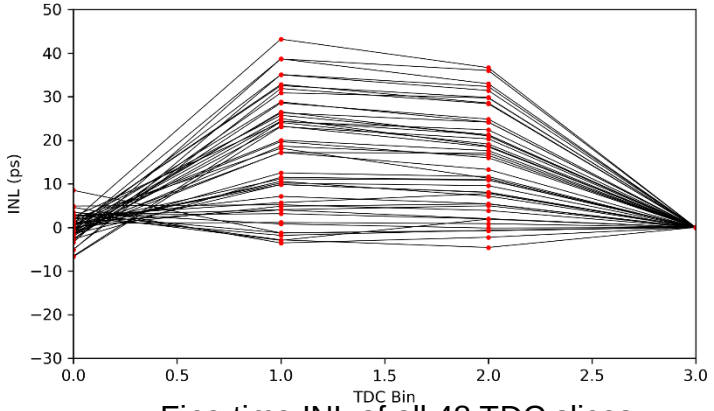
Code-density Test: Non-related input hit frequency



Fine-time bin size of all 48 TDC slices



Fine-time DNL of all 48 TDC slices

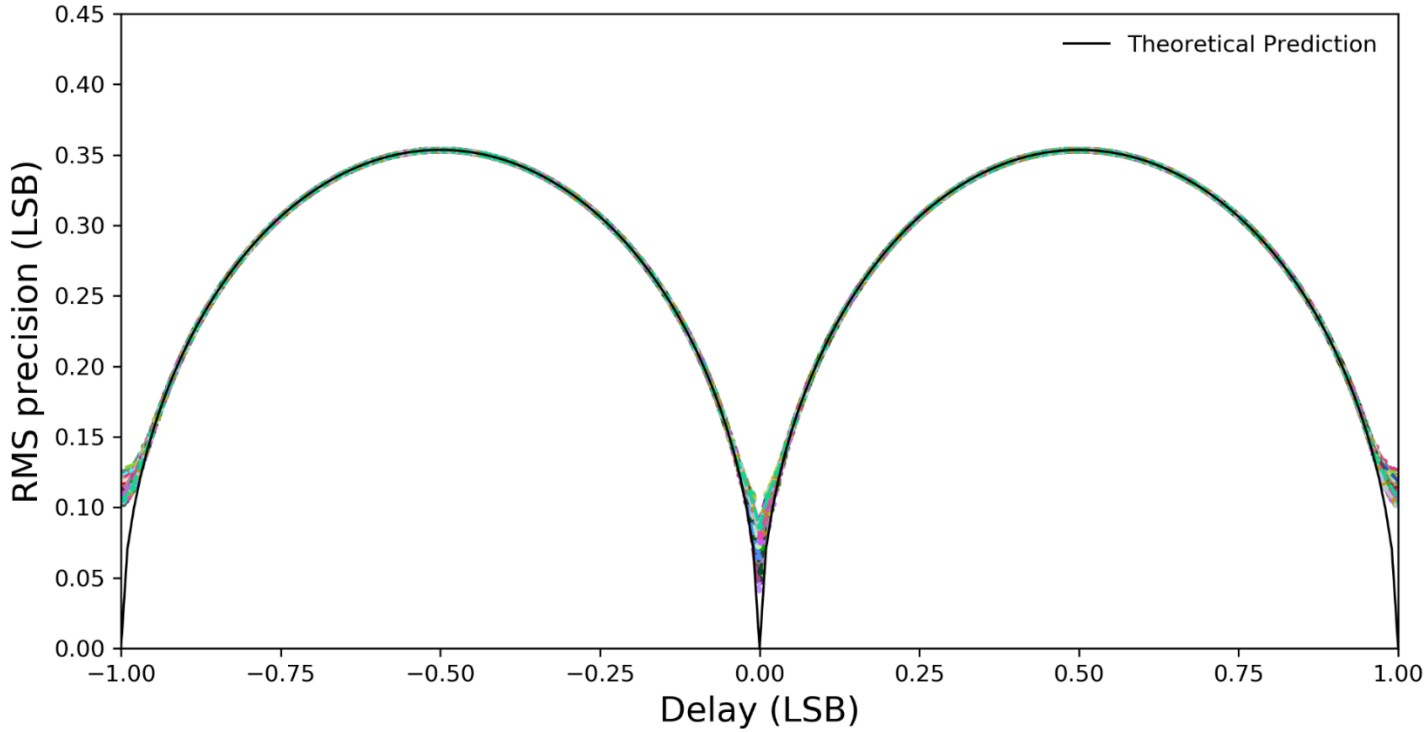


Fine-time INL of all 48 TDC slices

- Bin sizes for all 48 TDC slices have been measured (24 channels * rising and falling edges)
- Bin size variation ±40 ps, INL and DNL ±40 ps

Performance of TDC RMS

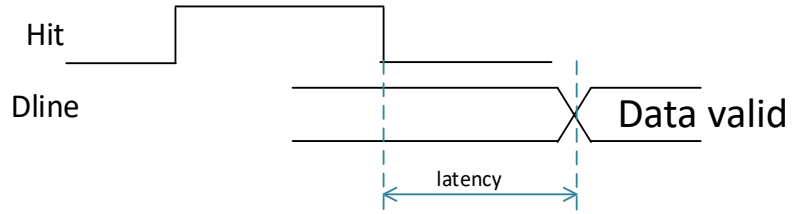
Path delay test



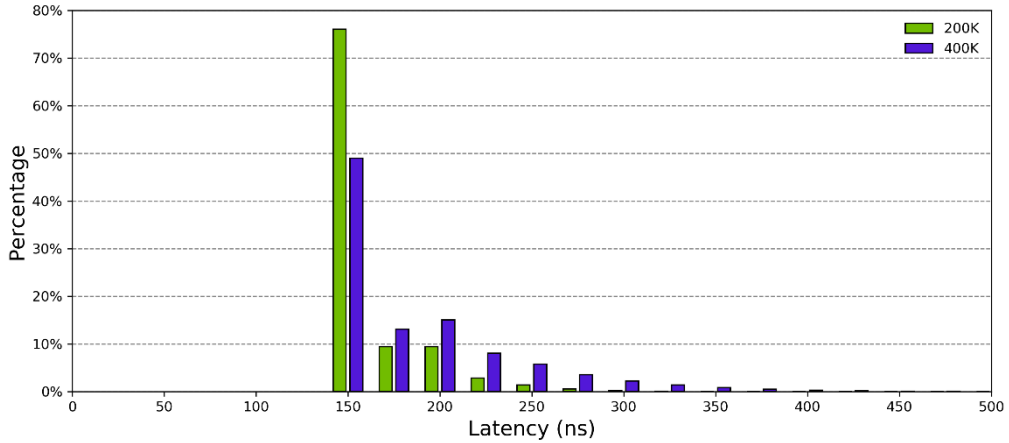
- The timing resolution effect due to the TDC design is ~10% of the LSB (~80 ps)
- The dominant contribution comes from the finite fine-time bin size (780/sqrt(12)=225 ps)
- The performances are similar to TDC1, indicating that the TMR and the BGA substrates do not make the performances degraded.

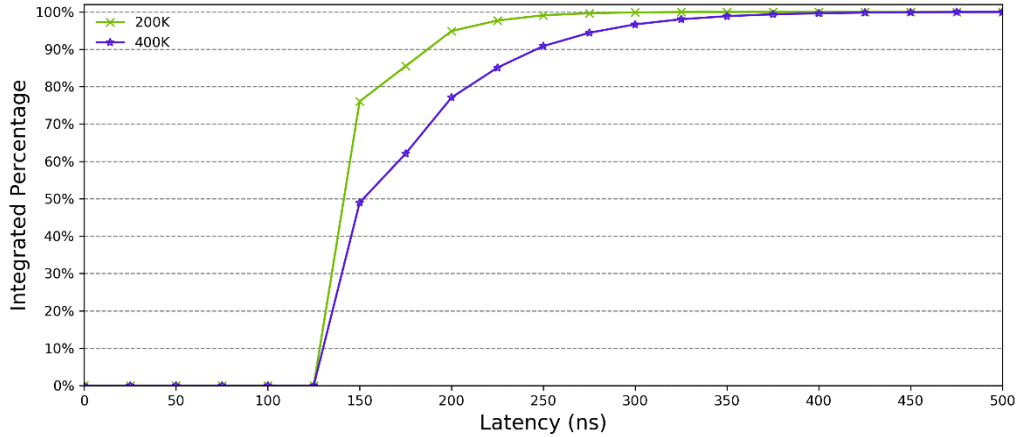
Performance of TDC latency

Trigger-less Latency



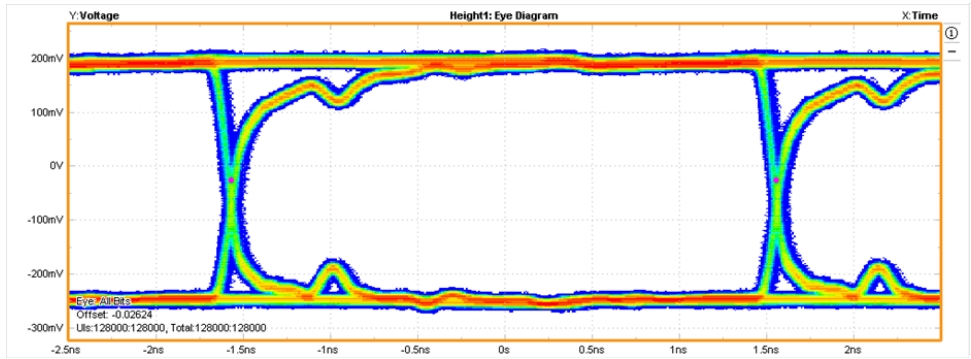
Latency definition here: From the trailing edge of input hit to the moment the corresponding data comes from output lines.



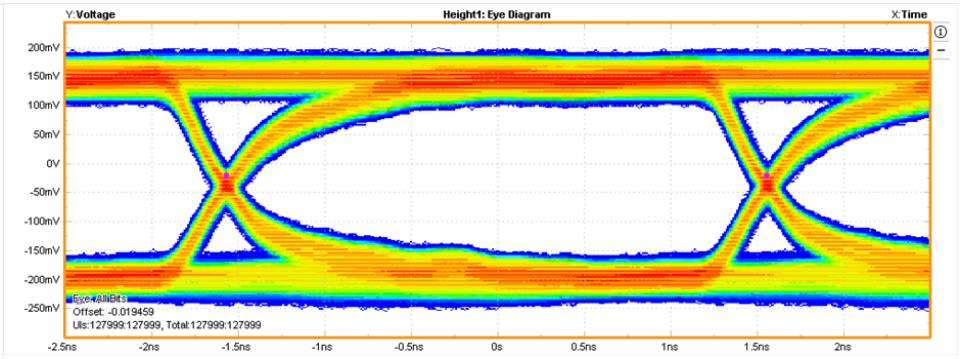


- Latency result for 200K/400K hit rate to all 24 channels.
- For 400K hit rate, after 350ns, 99% of the data was read out.

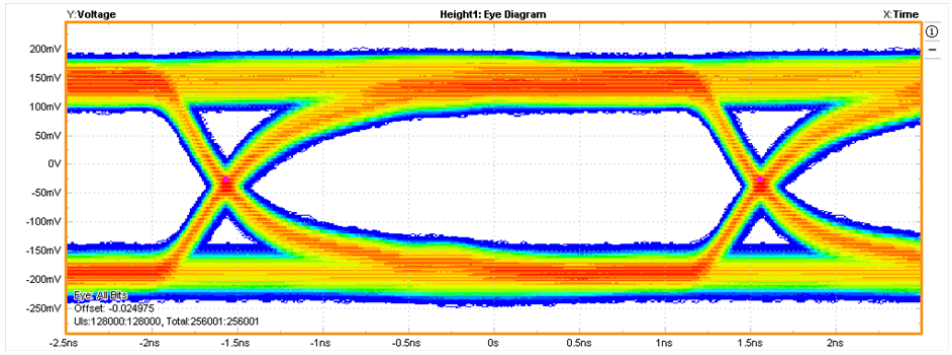
Performance of TDC output driver



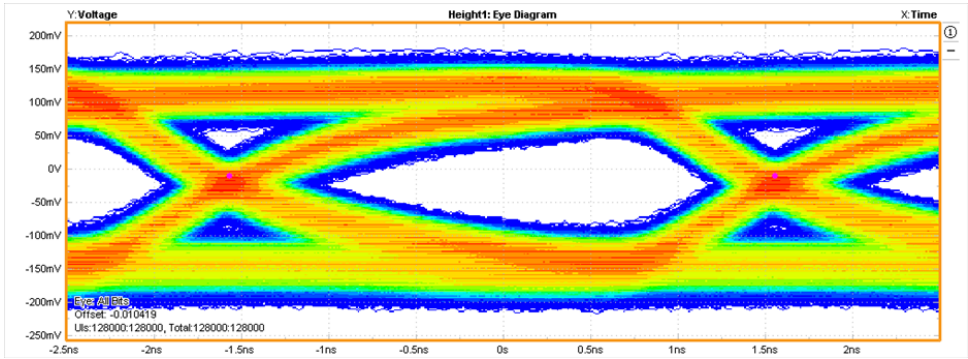
No cable



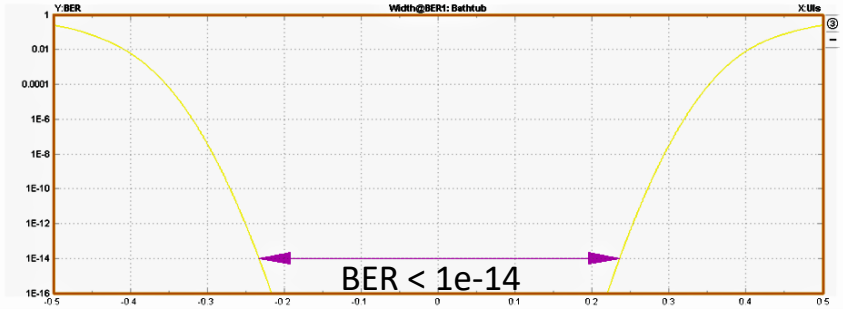
0.5m



1m



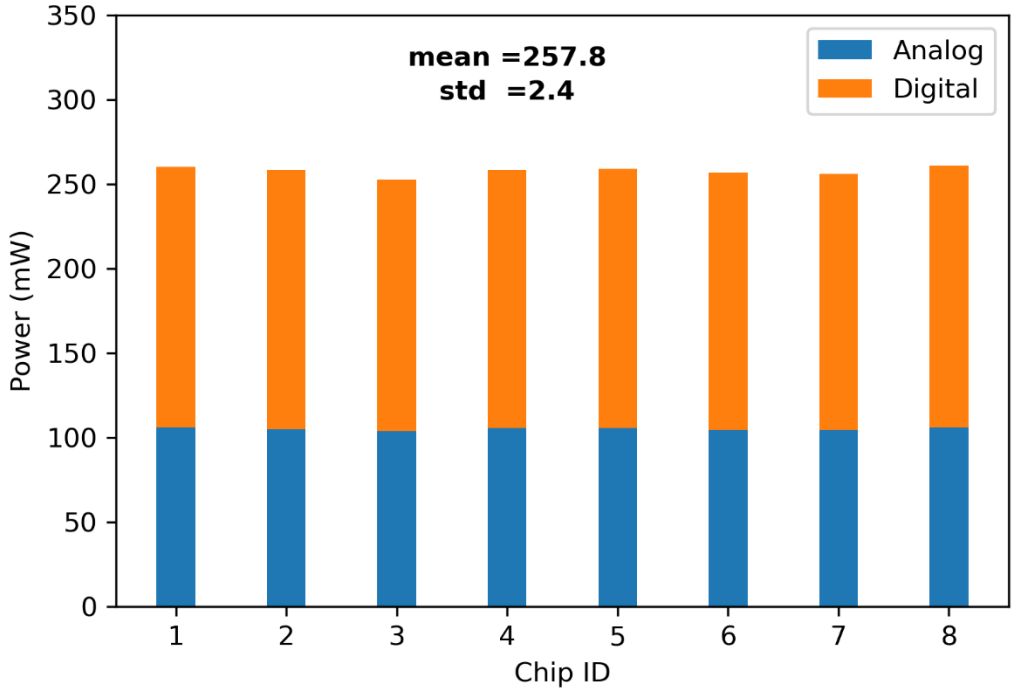
4m



Bathtub for 4m cable eye diagram

- Requirement: Bit error rate(BER) < 1e-14

TDC Power consumption



	TDC1 Measured (mW)	TDC2 Estimated (mW)	TDC2 Measured (mW)
Digital	146	153*	152.6
Analog	104	105.5*	105.2
Total	250	258.5*	257.8

***Estimated value is based on TDC1 measured/simulated power consumption ratio in typical corner.**

- 1.2V power supply, 0.2ohm resistor in series after LDO (chip voltage drop: 25mV max).
- Power consumption measured for trigger-less mode running with an input hit rate of 660 kHz per channel (Max rate that TDC could readout).

Summary

- A third version of the TDC ASIC with TMR protection for the upgrade of the ATLAS MDT detector at the HL-LHC has been designed in TSMC 130nm CMOS technology;
- Timing resolution and latency of the TDC is checked and satisfy the requirement, and the TDC power consumption is ~260mW compared to 350mW for the AMT ASIC;
- Radiation tests for TID and SEU will be performed in the near future, and joint tests with other parts of the MDT front-end electronics (ASD, CSM) will be performed once they are received;
- Engineering run of 22,000 dies will be placed after FDR in late 2020 or early 2021, if all future tests are passed.

Thank you!