Status of the TaichuPix chip for the high-rate CEPC Vertex Detector

Wei Wei

On behalf of the CEPC MOST2 Vertex detector design team

2020-08-21

Outline

- **TaichuPix1 chip design**
- **TaichuPix1 test status**
- **TaichuPix2 chip design**
- **Sensor TCAD simulation for TID**

Challenges and R&D activities on pixel sensors

- **Bunch spacing**
  - **Higgs: 680ns; W: 210ns; Z: 25ns**
  - **Meaning 40M/s bunches (same as the ATLAS Vertex)**
- **Hit density**
  - **2.5hits/bunch/cm^2 for Higgs/W; 0.2hits/bunch/cm^2 for Z**
- **Cluster size: 3pixels/hit**
  - **Epi- layer thickness：~18μm**
  - **Pixel size：25μm×25μm**
- **Hit rate: 120MHz/chip @W**

- **Two major constraints for the CMOS sensor**
  - **Pixel size: < 25μm* 25μm (σ~5μm)**
    - **aiming for 16μm*16μm (σ~3μm)**
  - **Readout speed: bunch crossing @ 40MHz**
- **None of the existing CMOS sensors can fully satisfy the requirement of high-rate CEPC Vertex Detector**
- **TID is also a constraint, 1~2.5Mrad/year is achievable**

	ALPIDE	ATLAS-MAPS (MONOPIX / MALTA)	MIMOSA
Pixel size	✔	X	✔
Readout Speed	X	✔	X
TID	X (?)	✔	✔

Main specs of the full size chip for high rate vertex detector

- **Bunch spacing**
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  - **Meaning 40M/s bunches (same as the ATLAS Vertex)**
- **Hit density**
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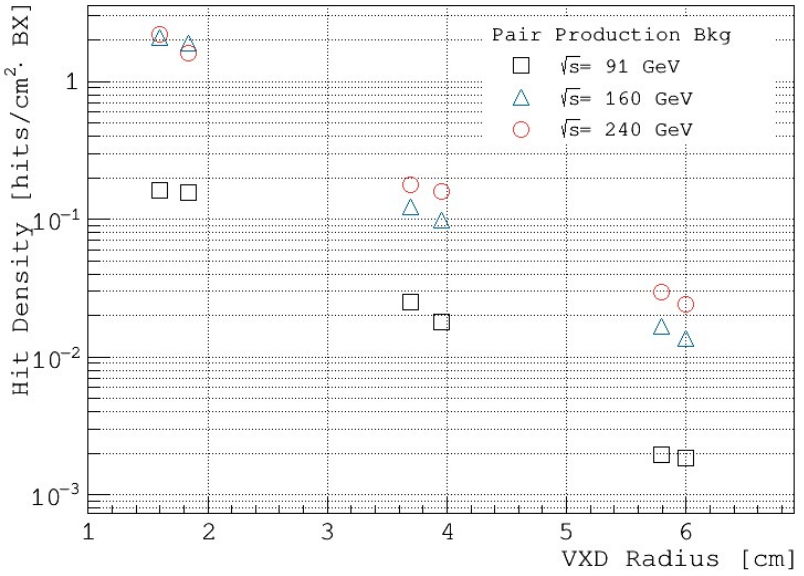
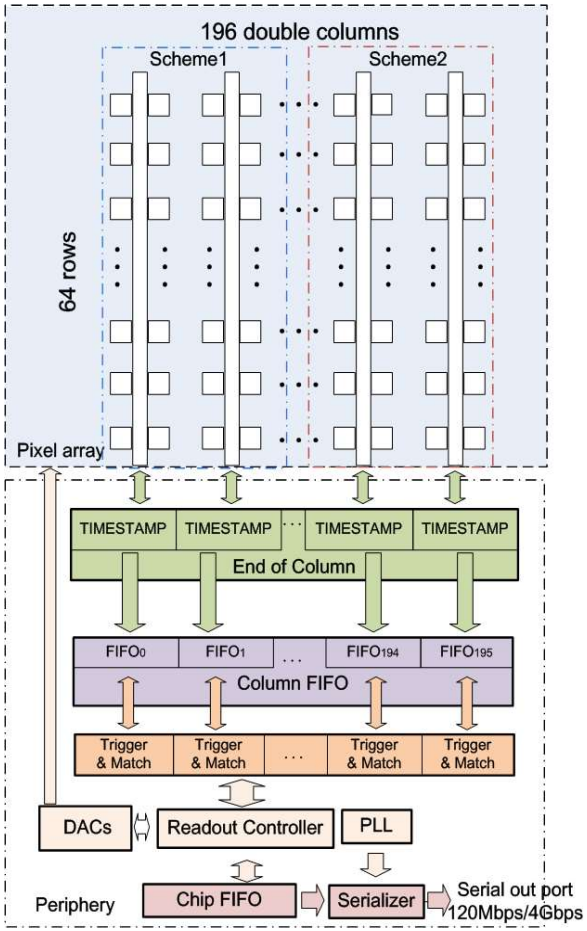
From the CDR of CEPC

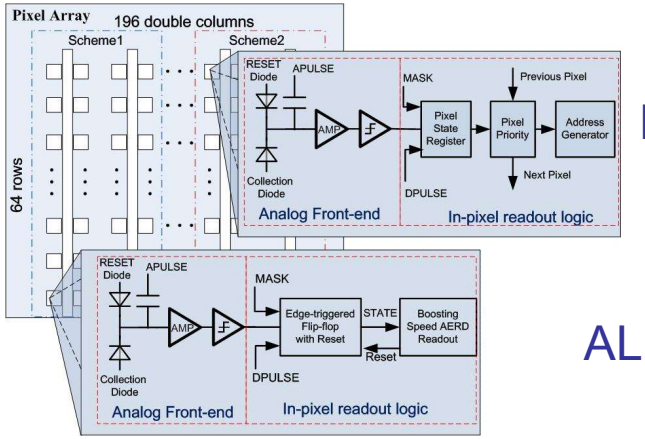


For Vertex	Specs	For High rate Vertex	Specs	For Ladder Prototype	Specs
Pixel pitch	<25μm	Hit rate	120MHz/chip	Pixel array	512row×1024col
TID	>1Mrad	Date rate	3.84Gbps --triggerless ~110Mbps --trigger	Power Density	< 200mW/cm^2 (air cooling)
		Dead time	<500ns --for 98% efficiency	Chip size	~1.4cm×2.56cm

New proposed architecture by TaichuPix



From Tianya Wu in User Manual



FE-I3-like Pixel

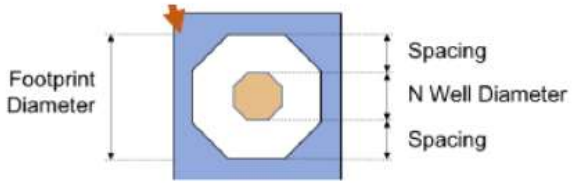
ALPIDE-like Pixel

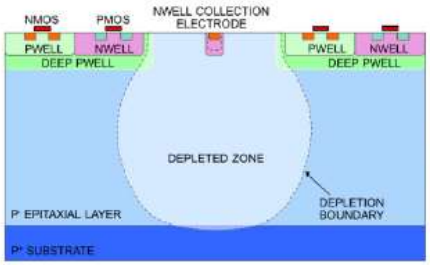
- **Similar to the ATLAS ITK readout architecture: "column-drain" readout**
  - **Priority based data driven readout**
  - **Modification: time stamp is added at EOC whenever a new fast-or busy signal is received**
  - **Dead time: 2 clk for each pixel (50ns @40MHz clk), negligible compared to the average hit rate**
- **2-level FIFO architecture**
  - **L1 FIFO: In column level, to de-randomize the injecting charge**
  - **L2 FIFO: Chip level, to match the in/out data rate between the core and interface**
- **Trigger readout**
  - **Make the data rate in a reasonable range**
  - **Data coincidence by time stamp, only matched event will be readout**

Sensing diode

Design of Sensor

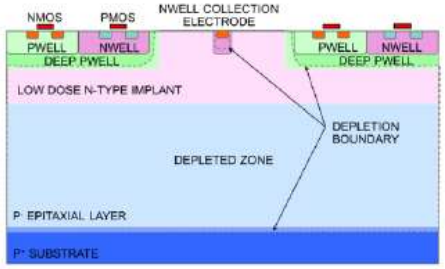
- **Goal: high Q/C (collected charge/sensor capacitance)**
  - **Small collection electrode → low C**
  - **High charge collection efficiency → high Q**
- **Process options:**
  - High resistivity sensitive layer (> 1 kΩ cm)
  - Deep p-well shielding n-well to allow full CMOS





Baseline process

no full depletion on pixel edges



Modified process

additional low doped n-layer

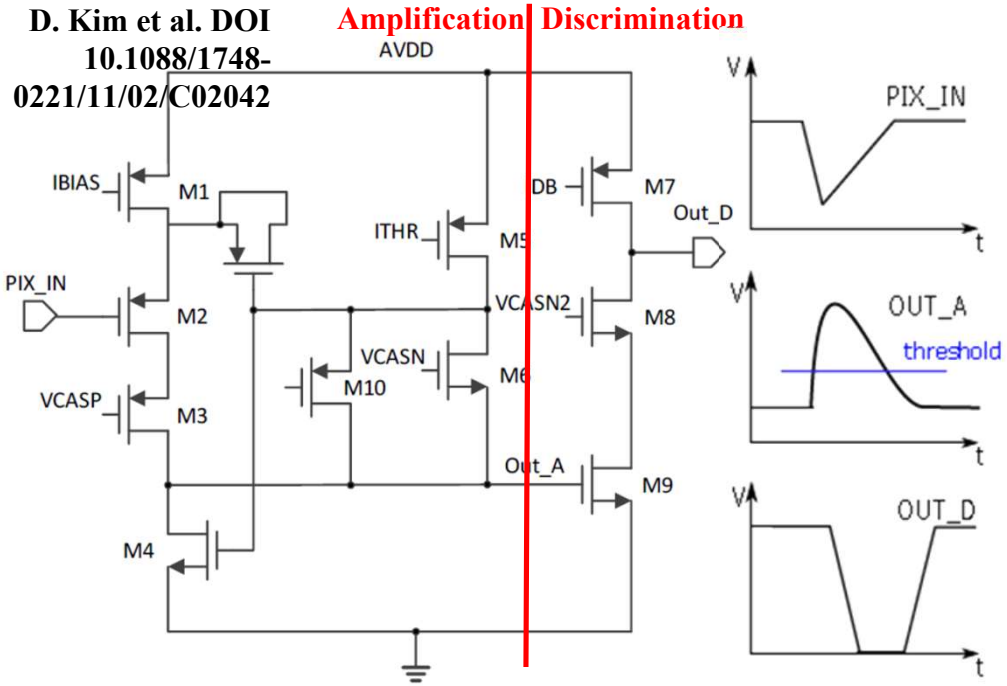
full depletion, faster charge coll. & better rad. tolerance

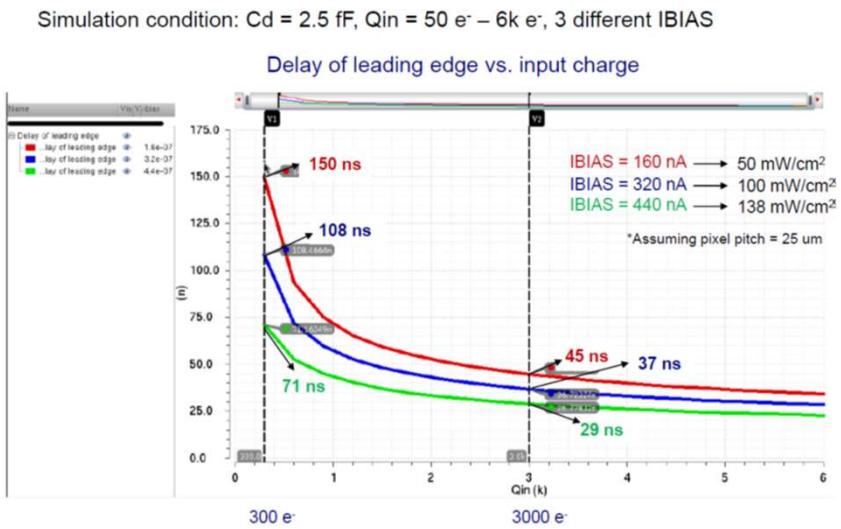
W. Snoeys et al.
DOI 10.1016/j.nima.2017.07.046

- **Design key points**
  - **Diode geometry optimization**, benefit from previous design (JadePix1)
    - 2-3 μm small electrode & large footprint
  - **Reverse bias** (~ 6V) ➔ reduce C & increase depletion volume

Pixel analog

D. Kim et al. DOI 10.1088/1748-0221/11/02/C02042

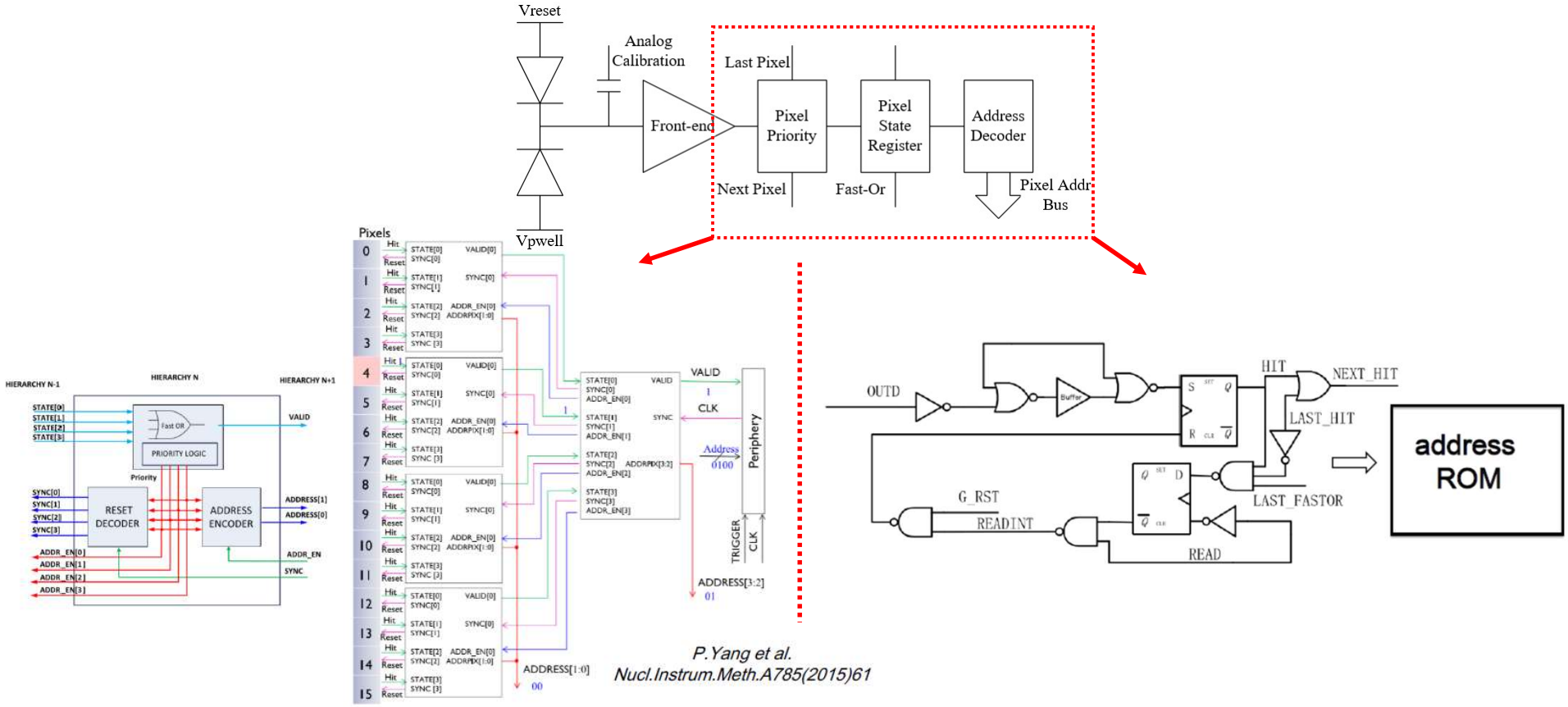




Y. Zhang for the CEPC Vertex MOST2 group meeting

- **Digital-in-Pixel scheme: in pixel discrimination & register**
- **Pixel analog is derived from ALPIDE (and benefit from MIC4 for MOST1)**
  - **As most of ATLAS-MAPS sensors' scheme**
- **Biasing current has to be increased, for a peaking time of ~25ns**
  - **Now in MOST1 ~2us peaking time was designed, too slow for 40MHz BX**
- **Consequence:**
  - **Power dissipation increased**
  - **Modified TJ process for ATLAS has to be used**
    - **With faster charge collection time, otherwise only fast electronics is of no meaning**

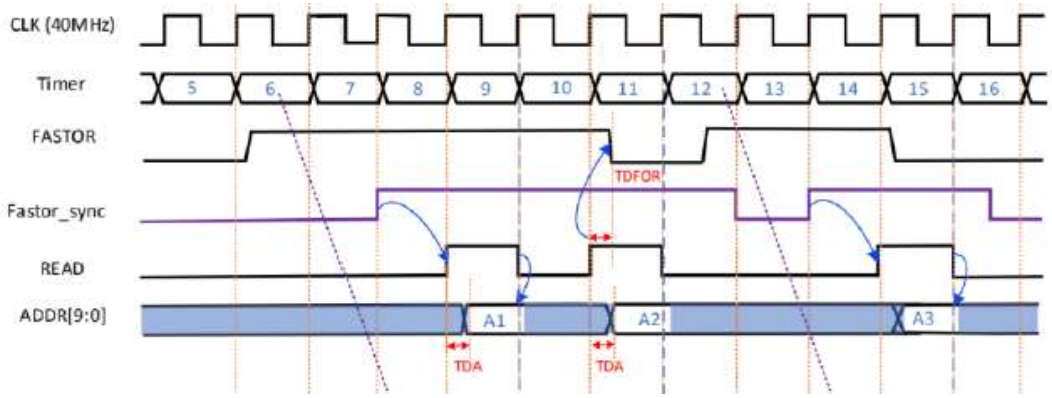
Pixel architecture – parallel digital schemes



- **Two parallel digital readout architectures were designed:**
  - **Scheme 1：ALPIDE-like: benefit from the proved digital readout in small pixel size**
  - **Scheme 2：FE-I3-like: benefit from the proved fast readout @40MHz BX (ATLAS)**

Design effort aiming for 40MHz BX on digital

- **ALPIDE-like scheme：**
  - **Fast-Or bus added to record the column hit time stamp**
  - **Boosting speed of the AERD (Address-Encoder & Reset-Decoder）**
    - **To shift the Fast-Or by a half of the clock cycle**
      - **More margin in the timing constraint of the periphery circuit**



Normal AERD

SS ; 1.6V ; 50°C	
Signal	Delay
FASTOR	14. 3ns
READ	14. 3ns
TDA	28ns
TDFOR	1. 3ns

Boost AERD

SS ; 1.6V ; 50°C	
Signal	Delay
FASTOR	14. 3ns
READ	14. 3ns
TDA	25. 5ns
TDFOR	1. 3ns

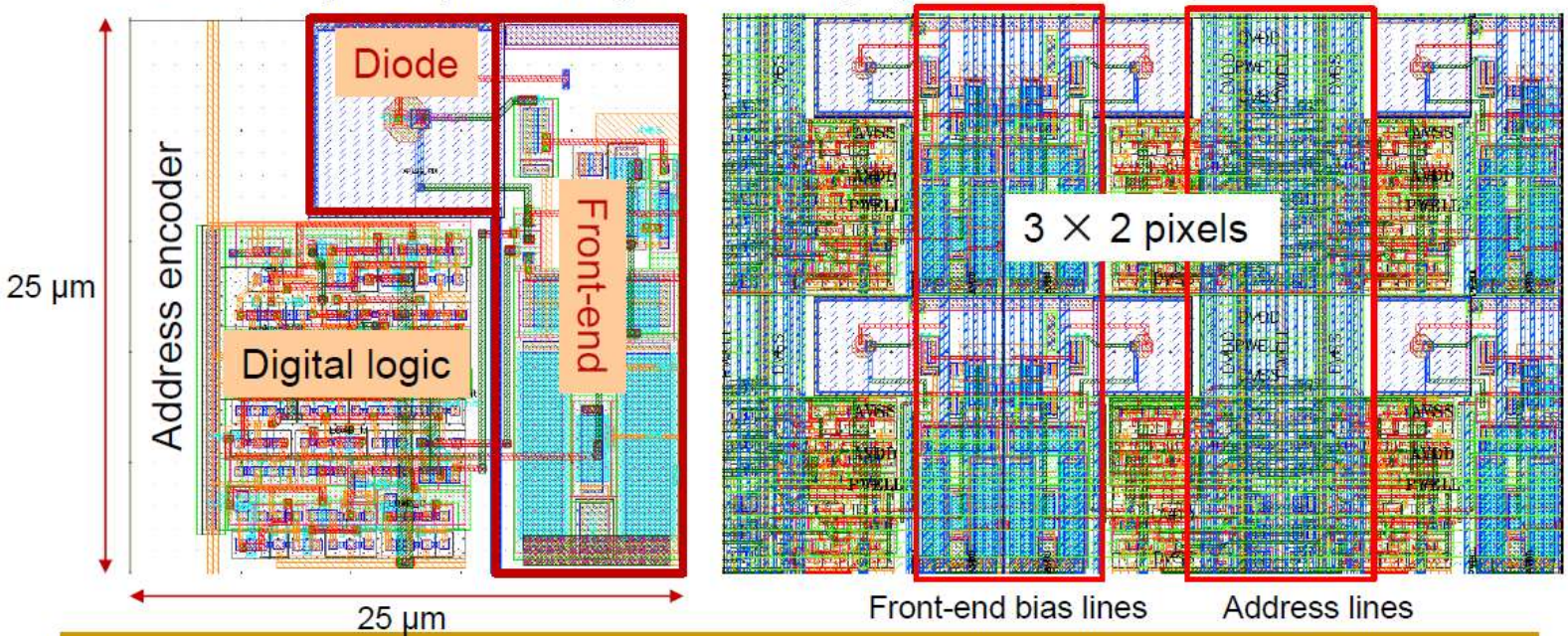
TY. Wu for the CEPC Vertex MOST2 group meeting

- **FE-I3-like scheme：**
  - **Simplify the pixel cell logic**
  - **All the logic gates were re-designed with fully customized layout**
    - **For smaller pixel size**

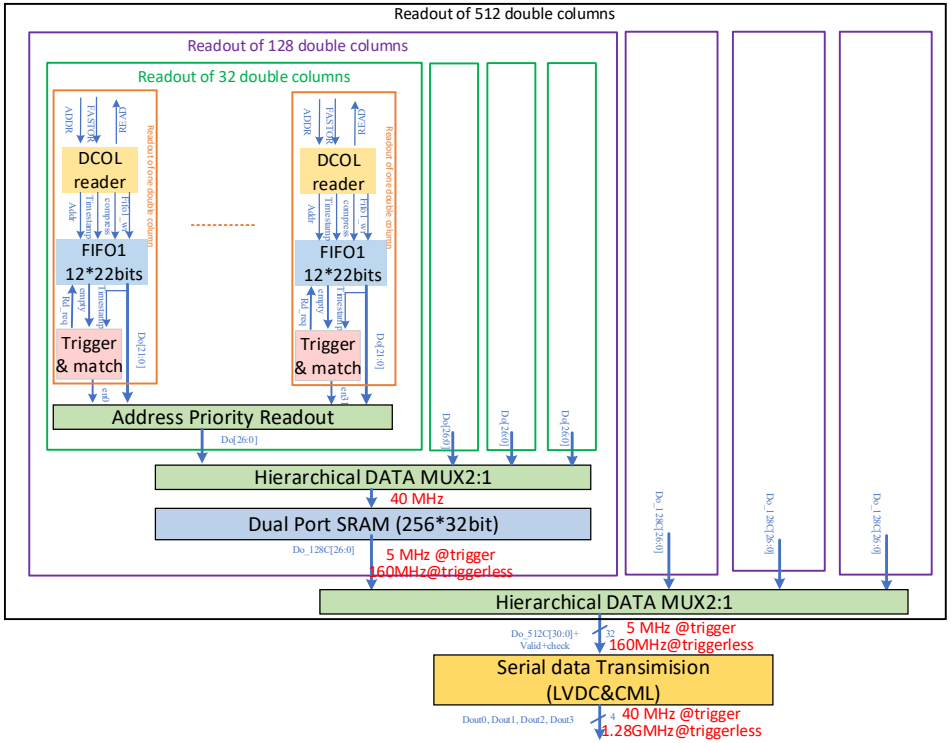
Pixel layout

Layout

- **Pixel size: 25 μm × 25 μm**
  - Sensor + Front-end occupy 45% pixel area
    - Smaller area possible
  - Shield from digital part to minimize crosstalk
  - Pixels are aside to separate analog and digital part
  - Two adjacent pixel analog share biasing signal routing



Full chip periphery logic design

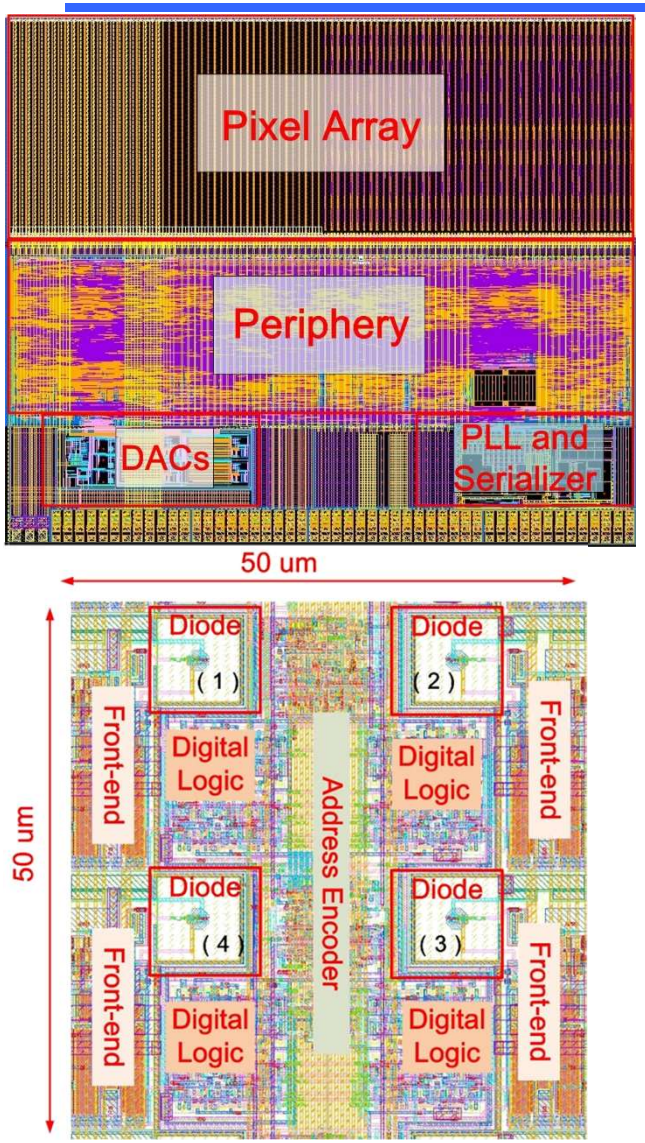


- **Main Functionality:**
  - **Trigger/Triggerless readout mode compatible**
    - **Data coincidence and trigger window logic**
  - **Two level FIFOs for hit derandomization**
  - **High speed serialization for data readout**
    - **4Gbps data rate capability**

From X.M. Wei for the CEPC Vertex MOST2 group meeting

- **Other necessary blocks**
  - **Slow control of the pixel array and full chip via SPI interface**
  - **Bias generation by current- and voltage- DACs**
  - **Clock management: Phase Lock Loop and serializer**
  - **Power management: LDOs for on-chip low ripple power supply**
  - **High speed interface: CML & LVDS Drivers**

Chip Status of TaichuPix1



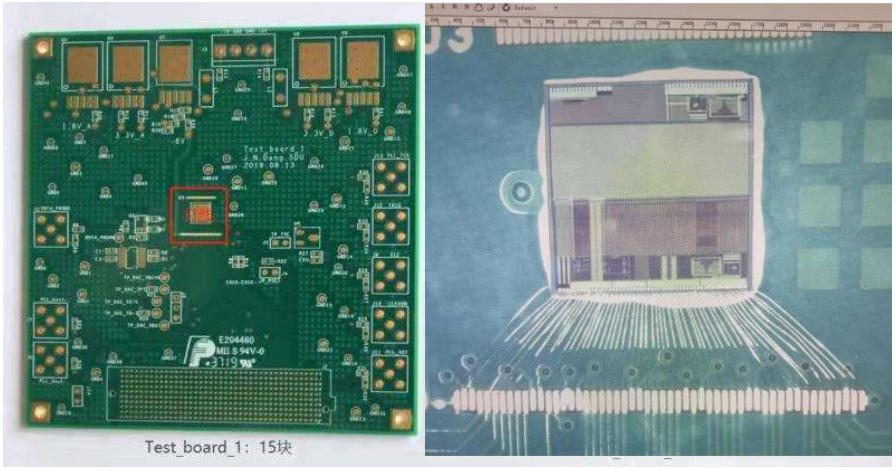
Chip size：5mm×5mm
Pixel size：25μm×25μm

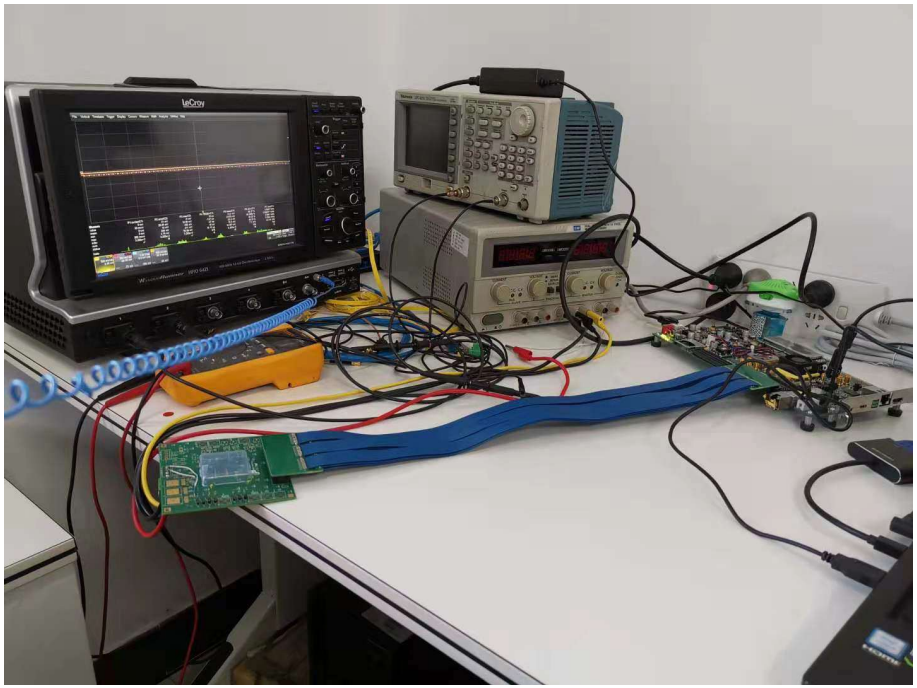
- First MPW tapeout was submitted in June,2019
  - Thanks IFAE for their tunnel for submission to TJ
- Chip received in Nov. 2019
  - With 60 chips, 40 chips delivered to China
- One block area of 5mm×5mm was fully occupied
  - A full functional pixel array (small scale)
    - 85% of the block area
    - A 64×192 Pixel array + Periphery + PLL + Serializer
    - Bias generation included
    - I/O arranged in one edge, as the final chip
  - other independent test blocks (less critical)
    - LDO + PLL

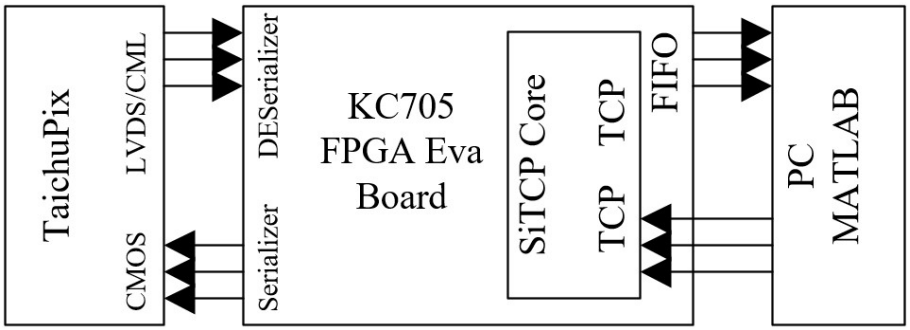
Outline

- TaichuPix1 chip design
- TaichuPix1 test status
- TaichuPix2 chip design
- Sensor TCAD simulation for TID

Test setup for chip evaluation





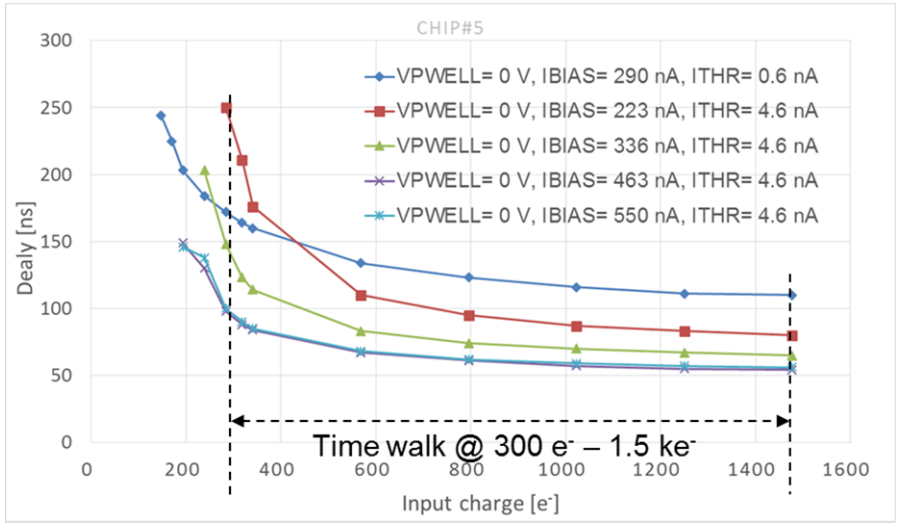


- **Test setup based on KC705 Xilinx FPGA Eva board**
- **General data stream**
  - **Downstream from PC to chip: TCPIP@MATLAB → SPI package@ FPGA → TaichuPix Periphery**
  - **Upstream from chip to PC: TaichuPix Serializer → FIFO@FPGA → TCPIP@MATLAB**
- **Test Firmware developed in IHEP (China side) by Jun HU and Wei WEI**
  - **Released version delivered to different collaborators, and functional worked**

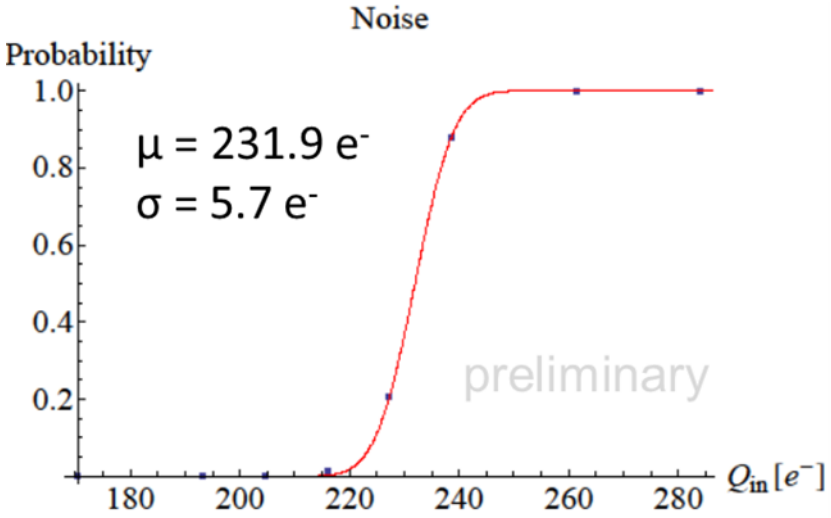
Test Status of TaichuPix1

- **Initiated in November, in parallel with Tcpx2 design**
- **Due to the limited time and some detected bugs, most tests were functional test before Tcpx2's submission**
- **Blocks test completed**
  - **Pixel Analog**
  - **Pixel Digital**
  - **Periphery Logic**
  - **Periphery Blocks**
    - **DAC**
    - **PLL & Serializer**
    - **LDO**
- **Test status summary**
  - **Major functionality proved**
  - **Weak substrate connection was found in the IO ring, tested by forcely power supply**
  - **Some bugs found & the problematic was located**
  - **Current performance test results meet with the requirement**

Pixel analog performance test

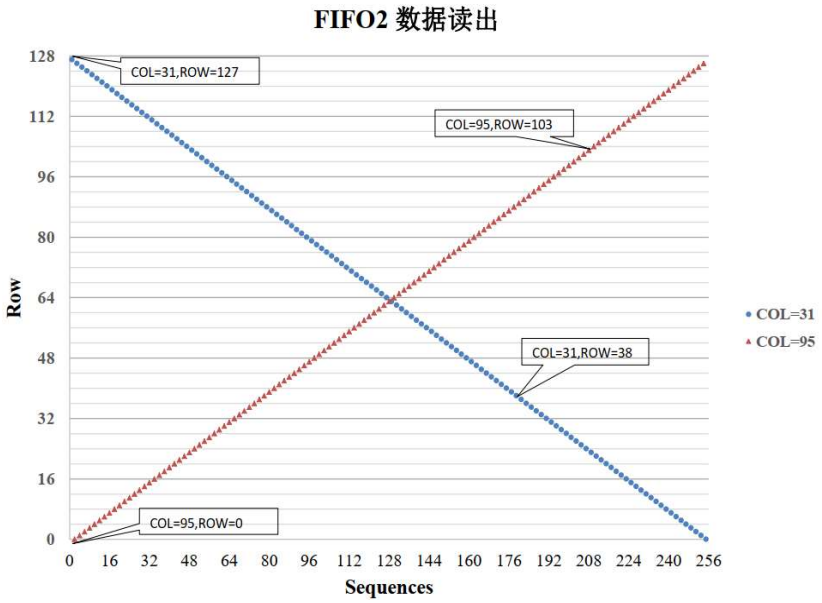


- **Pixel analog was tested by the probed output**
- **The tested performance was at the same level as in simulation, though the test condition is not perfect**
- **Tested noise 5.7e-**
- **Tested time walk 36ns(@300 e- – 1.5 ke-)**



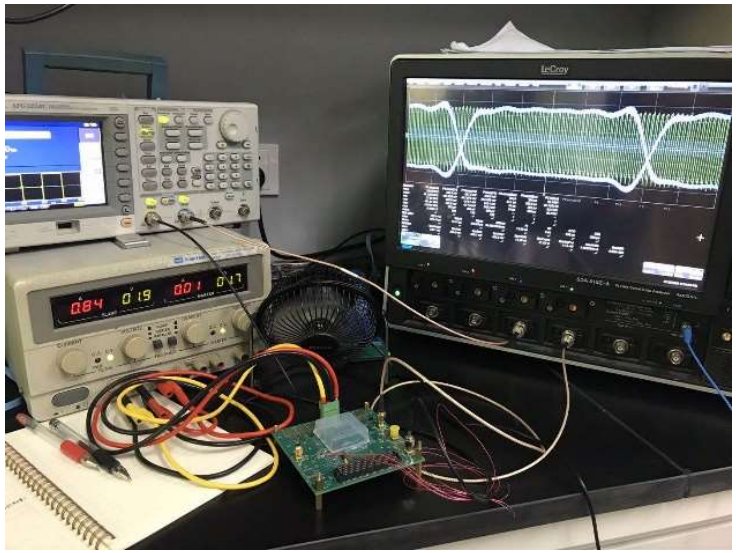
by Zhang Ying.

Pixel digital functionality

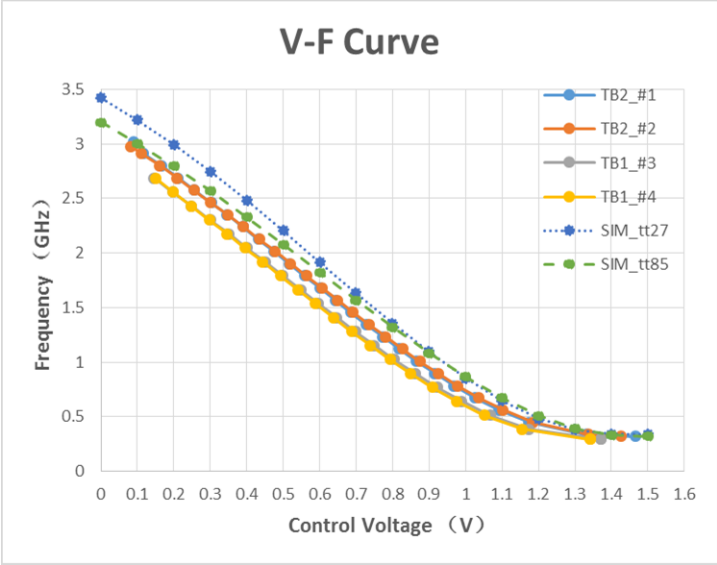


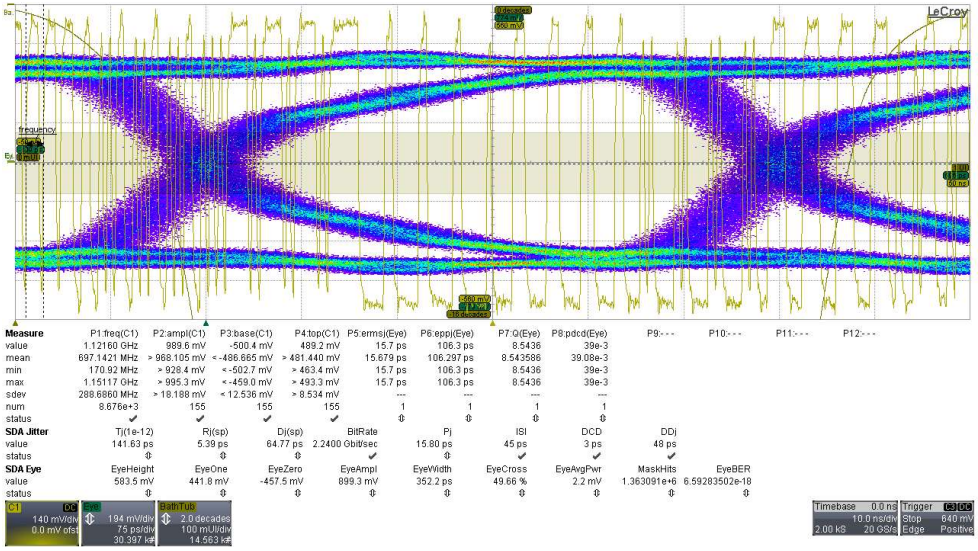
- Pixel digital's functionality was partially proved, some bugs were found
- Tested by the self-debug mode supported by the periphery logic
- The row addresses can be traversed, however, the column addresses was found unable to be correctly reset
- Bugs located in layout, modified in Tcpx2
- Periphery block ran reliably during the functional test

PLL and Serializer



- PLL and the serializer was thoroughly tested and proved
- PLL's tuning range 0.32~2.91GHz agrees with the simulation
- Good and robust eye-diagram observed at 2.24GHz, with the total jitter < 150ps (@ error rate < e^{-12})
- Serializer could run steadily @ 2.24GHz, meaning we will need two high speed ports for the triggerless (power, material budget, routing space)

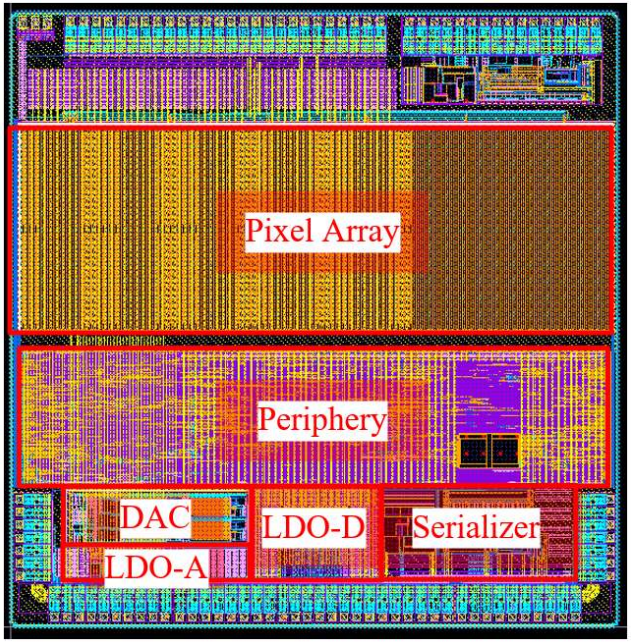




Outline

- TaichuPix1 chip design
- TaichuPix1 test status
- TaichuPix2 chip design
- Sensor TCAD simulation for TID

Status of TaichuPix2



- **Submitted on Feb 18, 5*5mm**
  - **Die received on July 23nd**
  - **Chips were under wire bonding**
- **All blocks fully integrated, as the final chip**
- **New features**
  - **A 64*192 pixel array with the same dimension as Tcpx1**
    - **32 + 32 double column modified FE-I3 readout, 32 dblcol modified ALPIDE readout**
    - **6 variations of pixel analog, each for 16 columns**
  - **Newly integrated blocks: Two LDOs for power supplies**
  - **8b10b encoder added for Triggerless output and balanced datastream**
  - **X-chip buses added for multiple chip interconnections**

Status of TaichuPix2

- **Major bugs (were tried to be) fixed**
  - **New IO rings were used, without DNW soft connect issues**
  - **DAC stability improved with higher phase margin**
- **Pixel readout optimized**
  - **To make larger headroom for the timing**
    - **Data latching @ 1clk -> 1.5clk**
  - **Address encoder pull-up added to avoid high-Z state**
- **Pixel analog new attempts**
  - **Smaller pixel area**
    - **Possible to be 24um*25um**
  - **One branch with enclosed gate for better TID**
- **X-chip interconnections attempts**
  - **SPI buses, PLL clock reference, reset signal, are possible to be propagated by chip-chip wire bonding**
  - **Save some routing space for the flex cable design**

Preliminary test status of Tcpx2

- **Functional verification status**
  - **IO rings works fine (problem solved)**
  - **Bandgap reference output proved (oscillation cancelled)**
  - **Periphery blocks tested**
  - **PLL lock function preliminarily proved**
  - **Pixel array digital communication with the periphery preliminarily proved**
- **More to be tested and understood**
  - **Pixel analog**
  - **Full data chain from pixel analog to PLL output**
  - **LDO for the power management**

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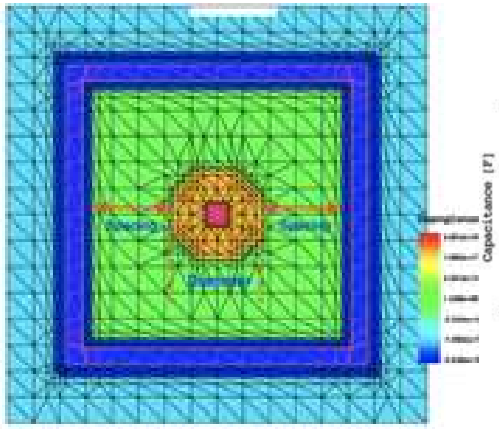
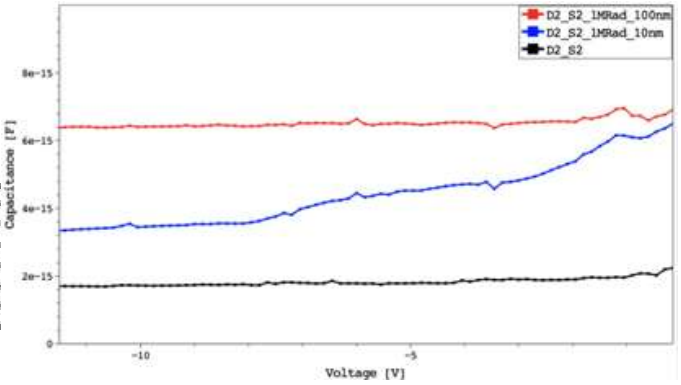
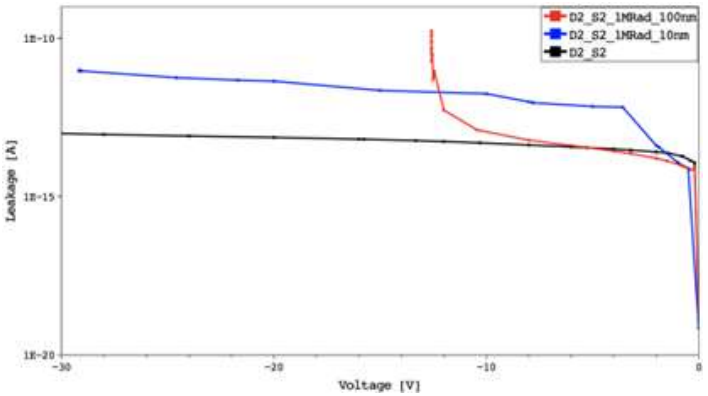
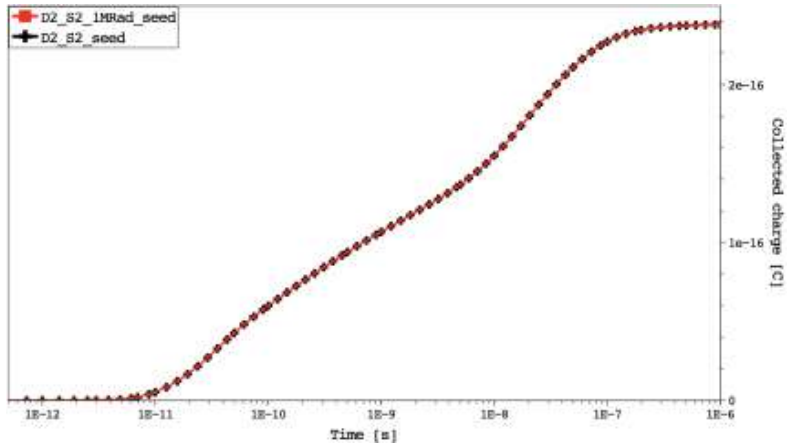
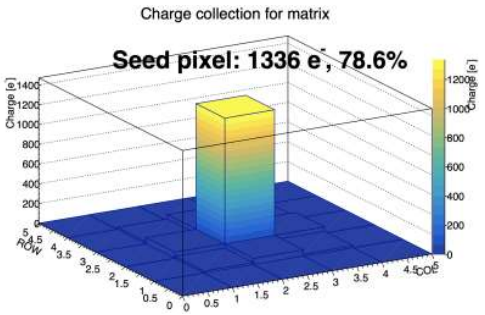
Sensor TCAD simulation for TID evaluation

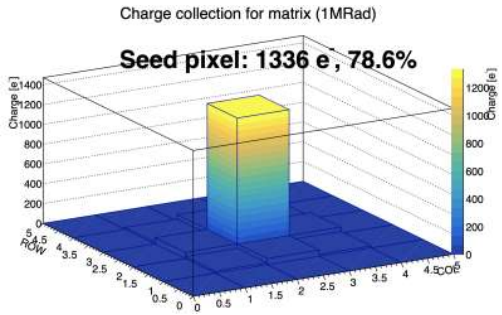










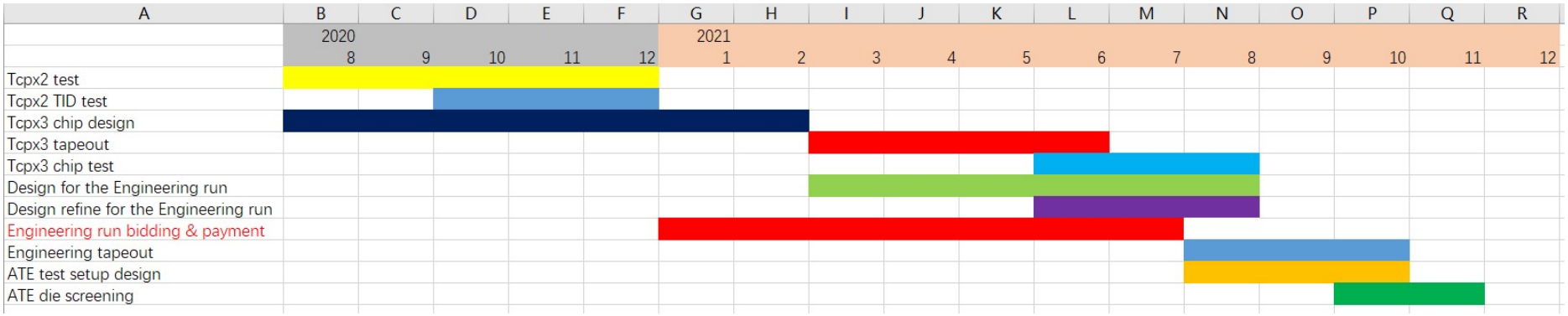


- **Sensing diode was simulated by TCAD to study its TID behavior**
- **The impact is negligible for the charge collection, and the leakage current after 1Mrad radiation**
- **However, we should give attention to the increasing capacitance**

Summary and Recent Schedule

- **Test of the Tcpx1 chip almost finished**
  - **All/most bugs were located/understood**
  - **Major functionality proved**
  - **(Testable) performance test agreed with the simulation**
    - **The test condition was not perfect, due to the IO ring issue and bias issues**
  - **Try to see if TID test is possible with Tcpx1**
- **Tcpx2 will soon be tested after wire-bonded**
  - **Functional debugging:~3weeks**
  - **Performance test**
  - **TID test**
- **Thinking about the following Tcpx3 MPW…**
  - **It is better to collect all the test results and bugs of Tcpx1 &2 before Tcpx3 submission**
  - **Expected to tapeout in the Spring of 2021**
  - **We have the chance to cancel Tcpx3 MPW, if Tcpx2's test showed good results**

Future plan



- **Key milestones:**
  - **Tcpx3 chip tapeout @2021.3**
  - **Tcpx Engineering run submission @2021.8**
  - **Tcpx ATE screening @ 2021.12**
    - **chip design accomplish**

Team organization

- **Design team:**
  - **IHEP, SDU, NWPU, IFAE & CCNU**
  - **Biweekly/weekly video design meeting on chip design (convened by IHEP)**

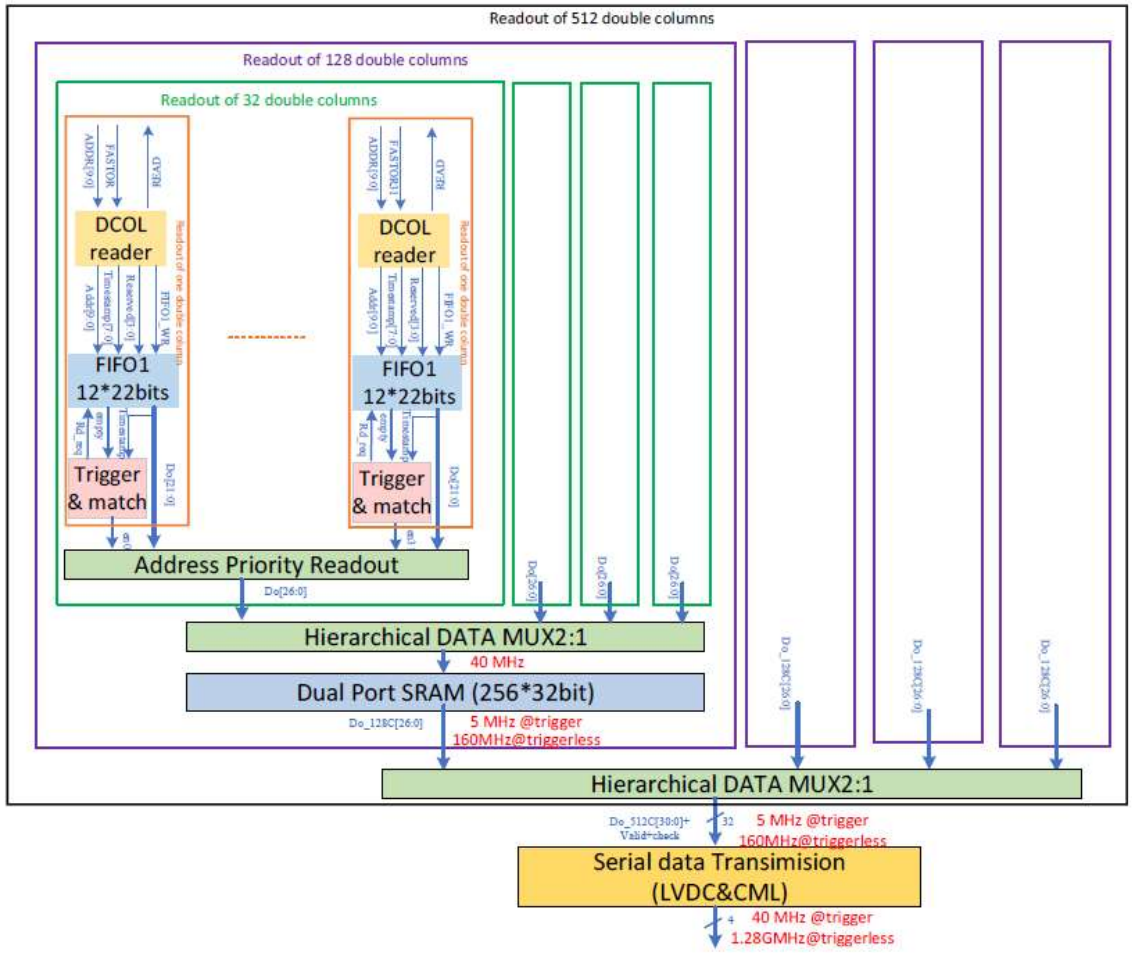
Institutes	Tasks	Designers
IHEP	Full chip modeling & simulation Pixel Analog, TCAD simulation High speed interface: PLL + Serializer	Wei Wei, Ying Zhang Xiaoting Li, Weiguo Lu, Mei Zhao
CCNU/IFAE	Pixel Digital	Tianya Wu, Raimon Casanova
NWPU	Periphery Logic, LDO	Xiaomin Wei, Jia Wang
SDU	Bias generation	Liang Zhang, Long Li

- **Chip characterization**
  - **Test system development: SDU (Jianing Dong) , IHEP & IFAE**
  - **Electrical test: all designers supposed to be involved in the related module + other interested parties**
  - **Irradiation test: X-ray irradiator + beam line**

Thank you !

外围电路逻辑

Readout architecture



列电路：

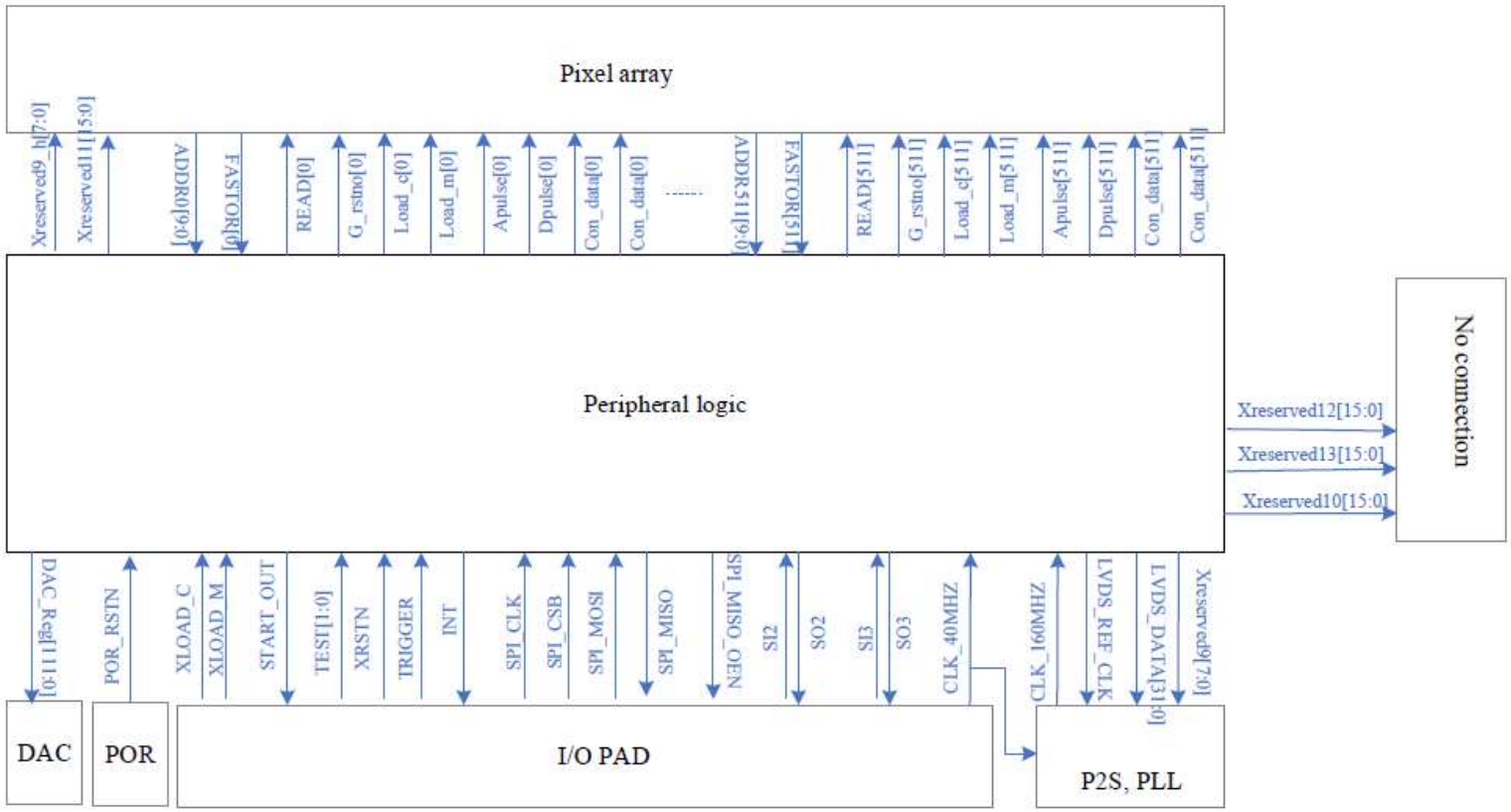
- 列端记录timestamp
- Trigger模式，在FIFO1输出时丢弃不匹配数据，FIFO2只存储时间戳匹配的数据

列并行读出方式：

- 512个双列并行读出以满足dead time 的要求，每列对应一个FIFO1
- 512分为4个128双列，每128对应一个FIFO2
- 128分为4个32双列，32双列内部采用数据驱动（分两级，8个一组），32双列之间轮询读出。轮询策略是每块读一个数就转读下一个块以避免数据拥塞。

外围电路逻辑

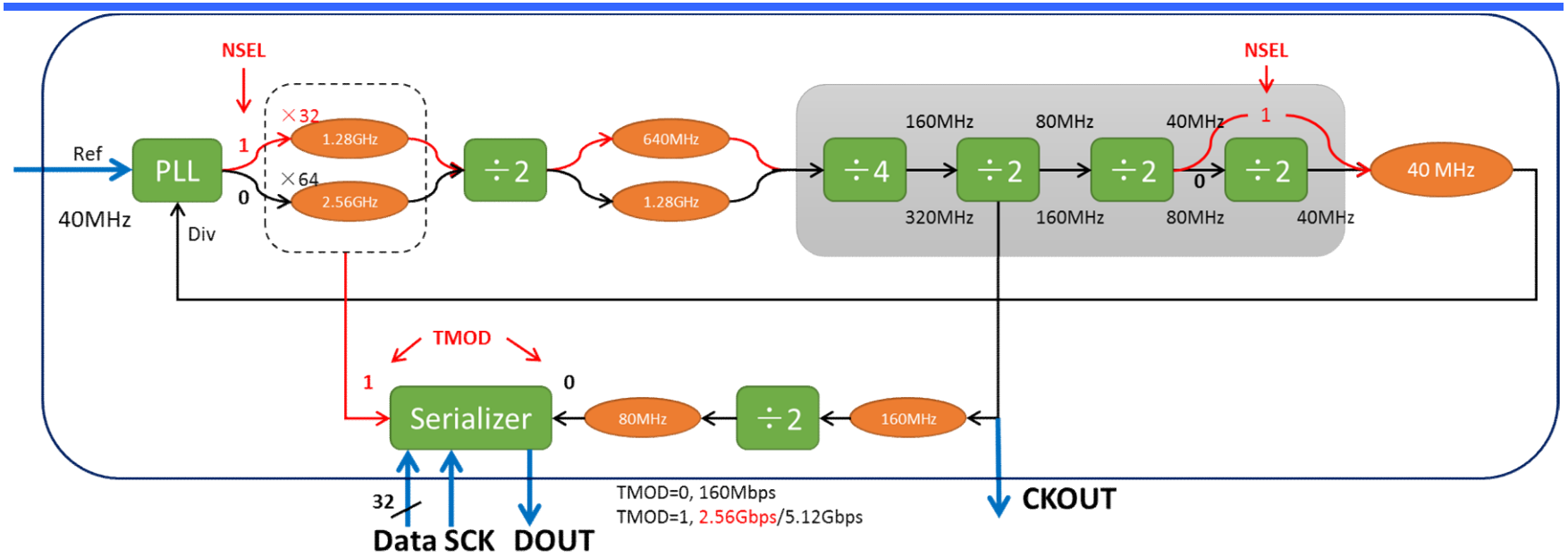
Interface & function



3个主要数据接口：像素阵列、SPI访问控制寄存器、数据输出至LVDS

3个功能设计：Trigger数据匹配、地址压缩、像素掩码

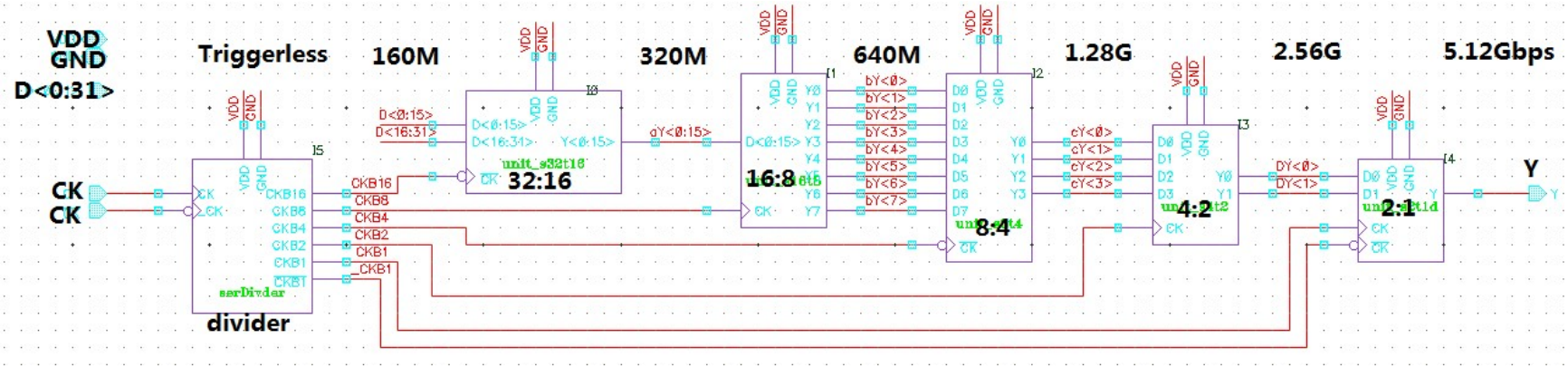
外围电路模块——高速数据接口

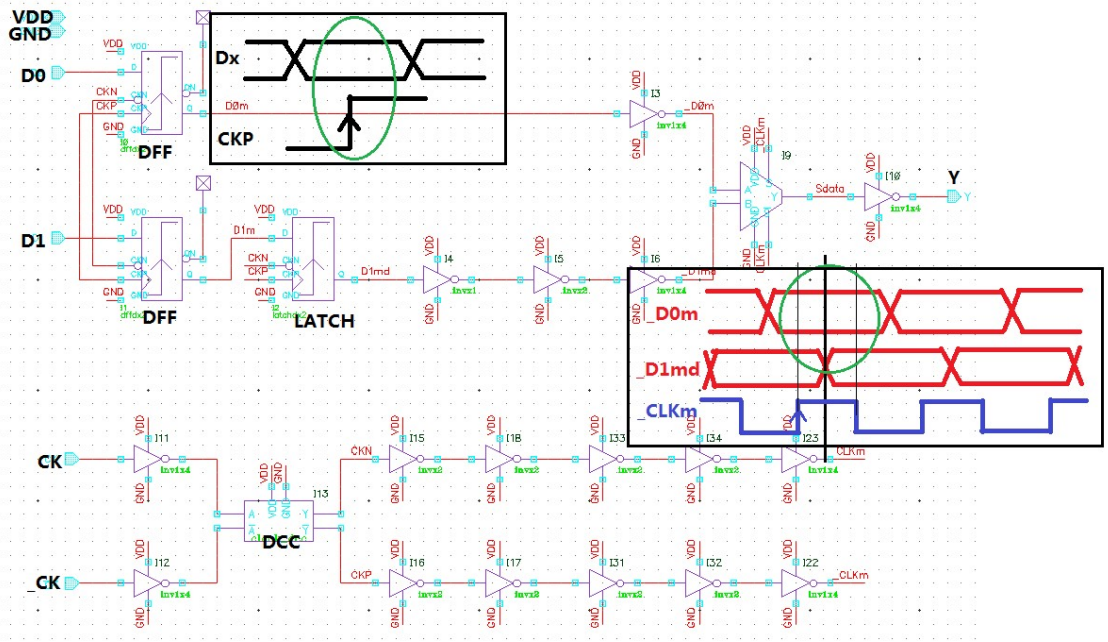


- **Tuning range @ SS 85**
  - 280MHz ~ 2.96GHz
- **Current range @ SS 85**
  - 3.57mA ~ 16.46mA
- **Phase noise**
  - ~ -100dBc/Hz@1MHz offset
- **Current @ 2.56GHz & FF -40**
  - 16.09mA
- **Current range @ FF -40**
  - 6.85mA ~ 26.26mA

- **NSEL: 0→2.56GHz, 1→1.28GHz**
- **ISEL1/ISEL0: 00/01/10/11 → 25/50/75/100μA**
- **BSEL： 0→3kΩ, 1→8kΩ**
- **TMOD: 0→Trigger, 1→Triggerless**

外围电路模块——高速数据接口

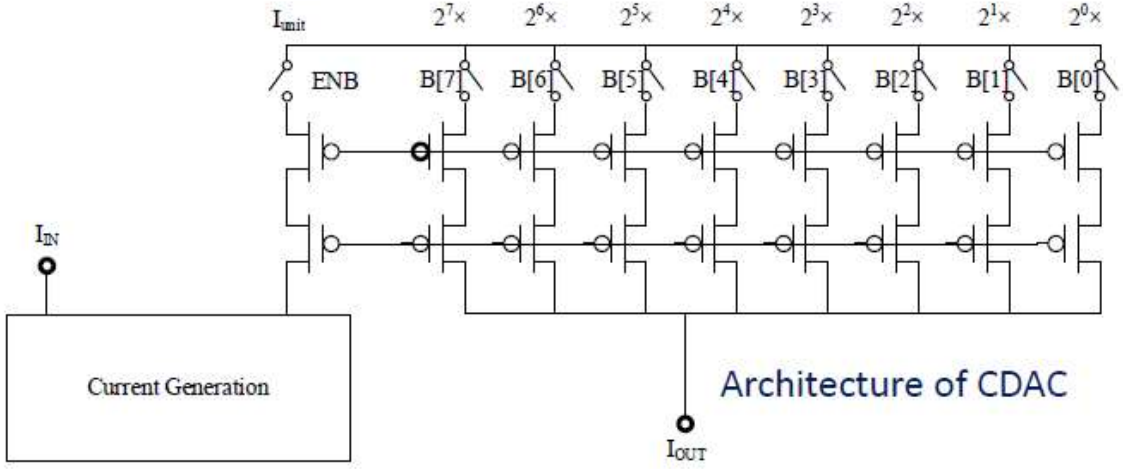




- **Timing**
  - Stage timing
    - Data sampling
  - Unit timing
    - Data sampling (Dx--CKP)
    - MUX (_Dxm--CLK)
  - 1UI = 500ps @ 2Gbps
    - Time margin is very small at high speed
    - Delay of data and clock
- **Big-small eye in eye diagram**
  - 50% DC of clock

偏置产生模块——多通道DAC

- **Characteristics**
  - Voltage DAC (VDAC)
    - 10 bit
    - LSB: 1.56 mV
    - Range: 0 – 1.6 V
  - Current DAC (CDAC)
    - 8 bit
    - LSB: 40 nA
    - Range: 0 nA ~ 10.2 μA

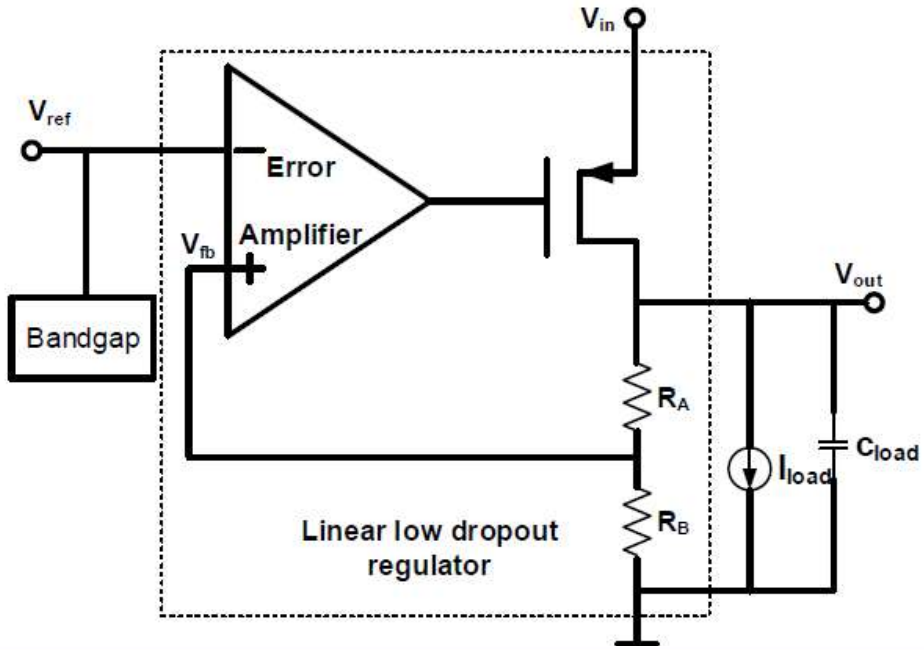


Architecture of CDAC

- **Current DAC**
  - Current mirror
  - Segmented architecture
    - 4 most significant bits (MSB)
      - ★ thermometer decode
    - 4 least significant bits (LSB)
      - ★ binary weighted
  - Output impedance
    - Min: 104KΩ
    - Max: 43 MΩ

- **Voltage DAC**
  - Current bias generation block
    - VBG: output of bandgap ~ 0.8 V
    - I_{unit} ~ 20 μA
  - Negative feedback to stabilize VBG @ 0.8 V
  - Current mirror with resistor load
  - Segmented architecture
    - 4 most significant bits (MSB): thermometer decode
    - 6 least significant bits (LSB): binary weighted

电源管理模块



Parameters	Value
Input voltage	<2 V
Output voltage	1.8 V
Maximum output current	200 mA
Load capacitance	~200 nF
TID	> 1 Mrad.
Maximum dropout voltage	0.2 V
Fully integrated on-chip	
Low noise, High PSR	