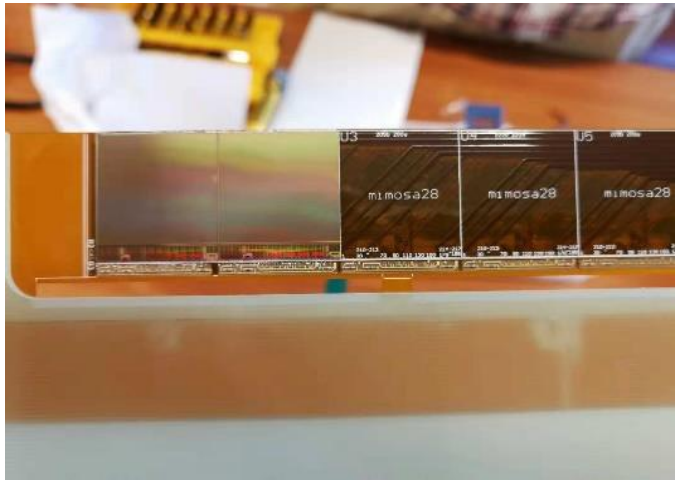
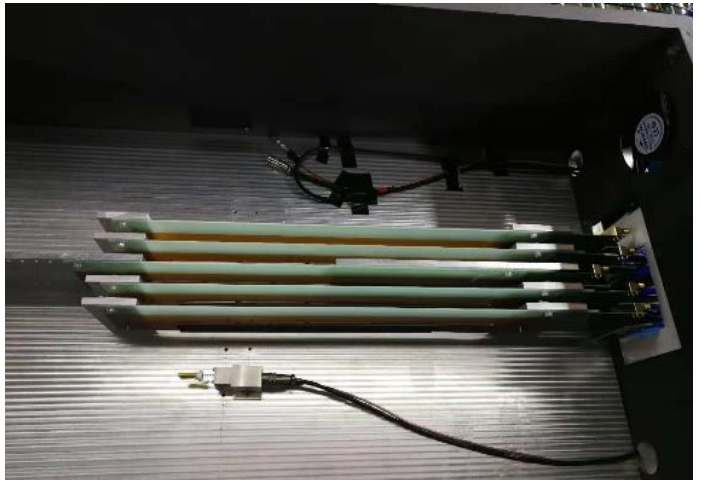
Most2 Silicon Detector DAQ

Zhang Hongyu

Current status – MAPS detector prototype

- MAPS prototype:
  - Silicon detector prototype based on Mimosa28 chips
    (Monolithic Active Pixel Sensor (MAPS) designed by Strasbourg IPHC)
  - consists of 5 pixel detector ladders
  - **DUT** – 1 ladder to be tested, equipped with 10 Mimasa28 sensors
  - **Telescope** - 4 ladders each has 2 Mimasa28 sensors, working as telescope when doing beam test.

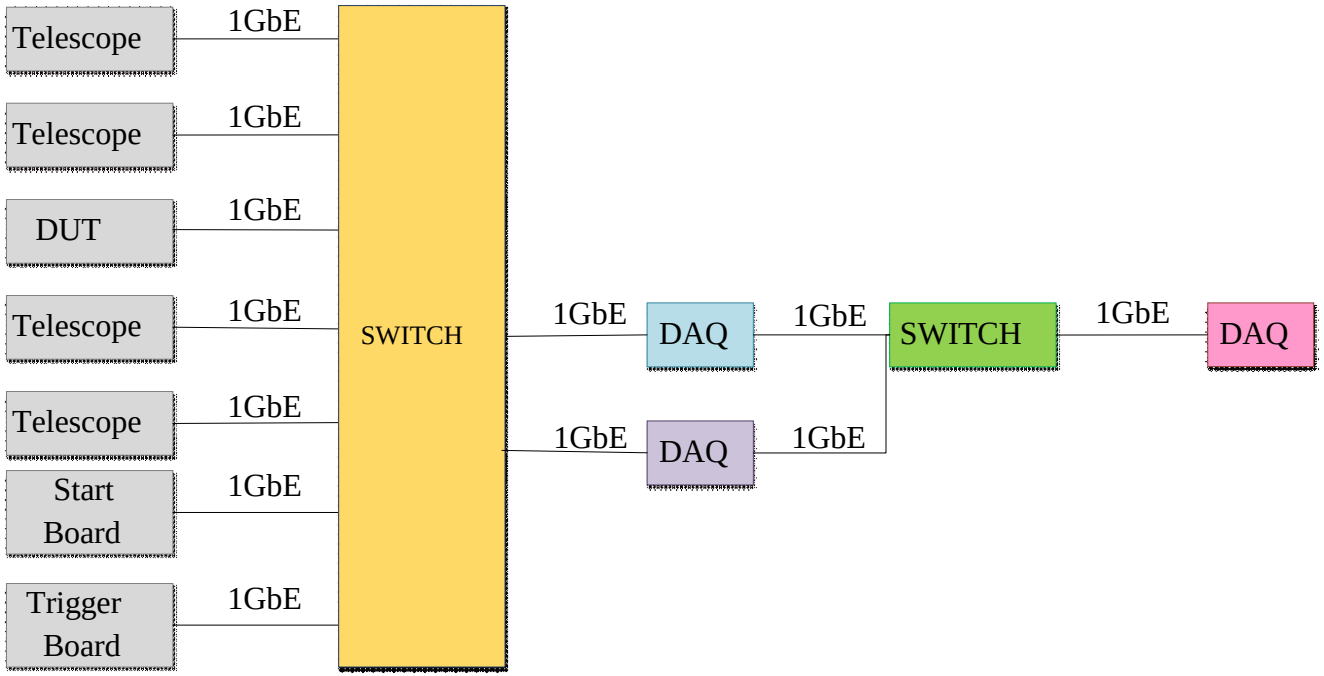




(Ladders developed by Dr. Dong Mingyi)

Current status – MAPS Readout Electronics

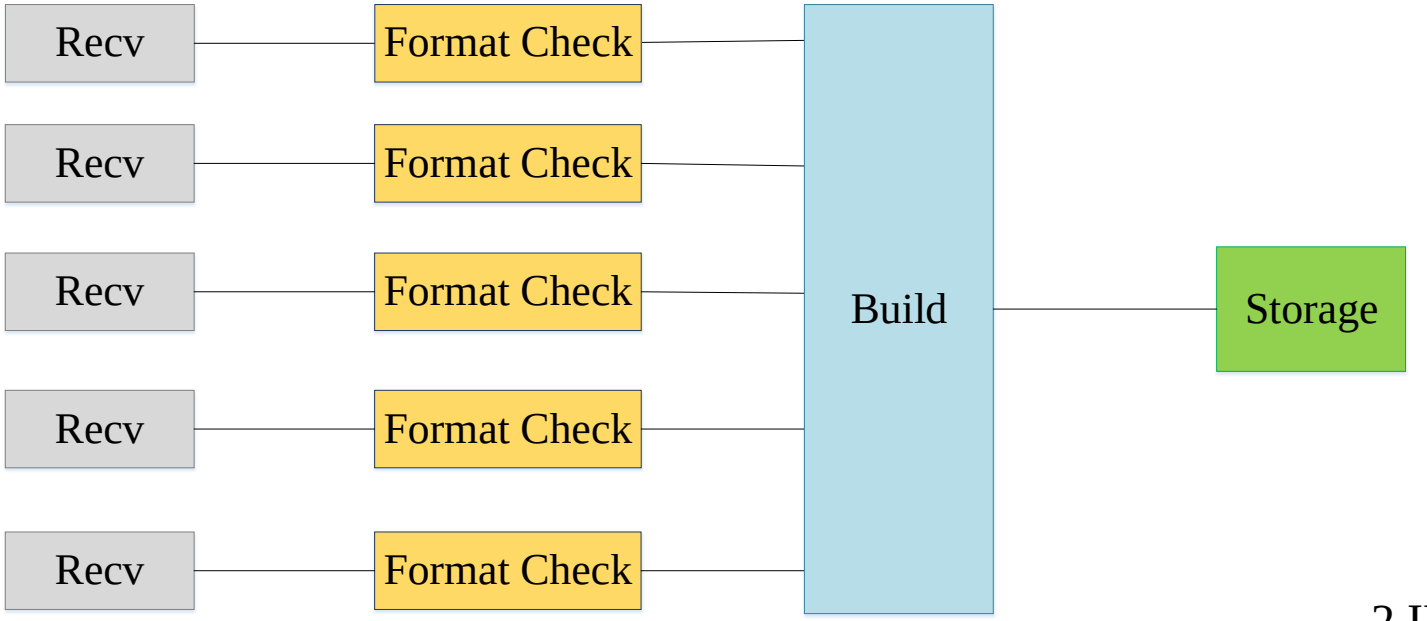
- Front-end Electronics boards:
  - Data Readout boards (x5) – collect sensor frame data and send to DAQ
  - External trigger signal fan-out (x1) - provide common trigger signal
  - Start signal Fan-out (0x1) – start Mimosa28 sensors to output frame data
- Readout port: SiTCP (1GbE)

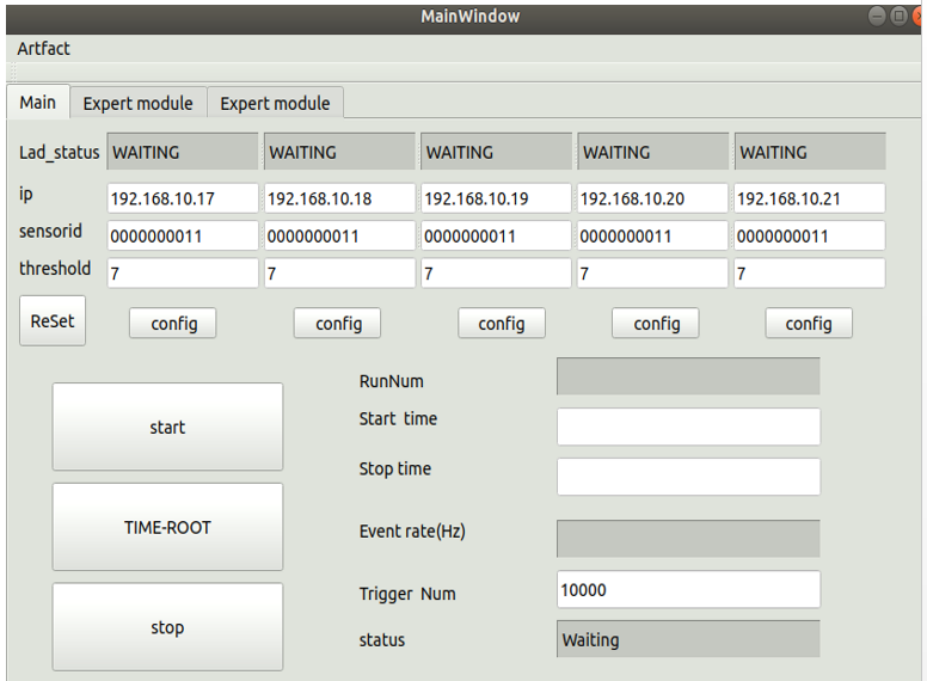


(FEE developed by Tian Xingcheng, Hu Jun)

Current status – MAPS DAQ

- Linux / C++
- FEE configuration
- Multi-thread Data Readout
- event building
- Data storage
- Sensor frame data process and hit map display





Radiation test

2 IPC (Industrial Personal Computer) for data acquisition

MAPS DAQ Data Format

- Raw data of sensors is eventually wrapped up with headers and trailers into DAQ data package for offline physics analysis

1 Chip Format = n * (Chip Head + Chip Data)

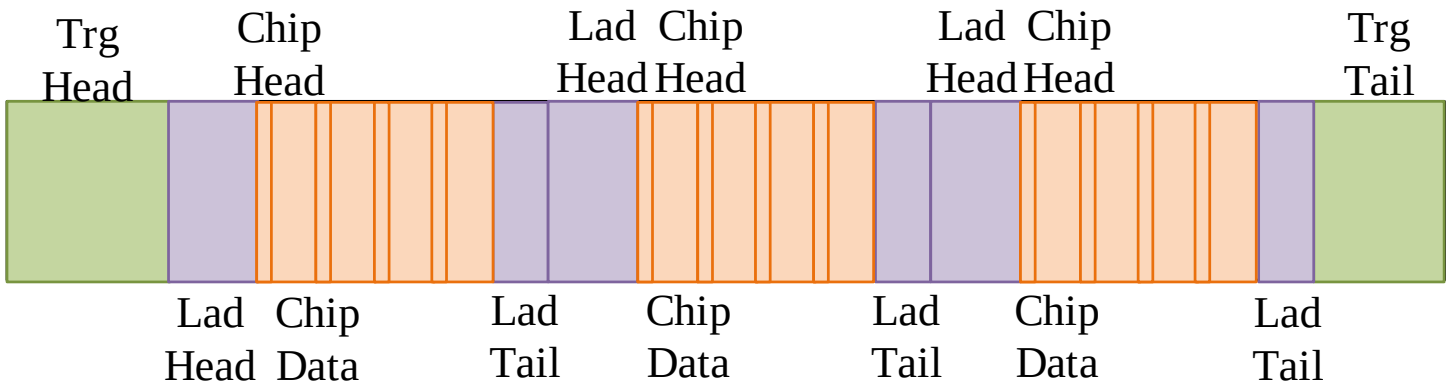
1 Ladder Format = 1 Ladder Head + n * Chip Format + 1 Ladder Tail

1 Trg Format = 1 Trg Head + n * Ladder Format + 1 Trg Tail

Chip Head	=	uint32_t Head Flag
Ladder Head	=	uint32_t Head Flag
	+	uint32_t Frame Count
	+	uint32_t Pack Length
	+	uint32_t Trigger ID

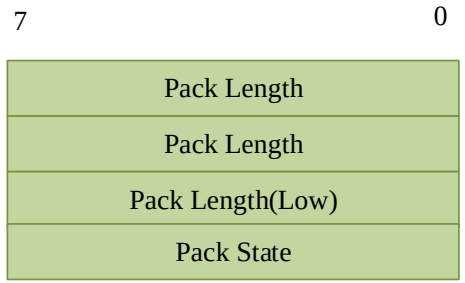
Ladder Tail	=	uint32_t Tail Flag
Trg Head	=	uint32_t Head Flag
	+	uint32_t Trigger ID
	+	uint32_t Pack Length
	+	uint8_t Pack State
Trg Tail	=	uint32_t Tail Flag

MAPS DAQ Data Format

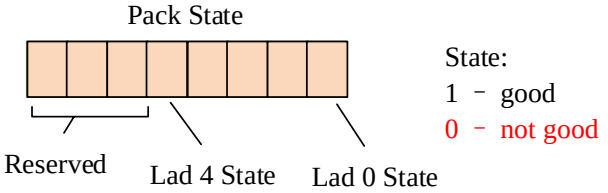


Trg Format

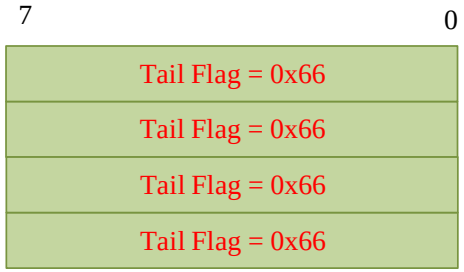
Trg Head(front)



Trg Head(end)

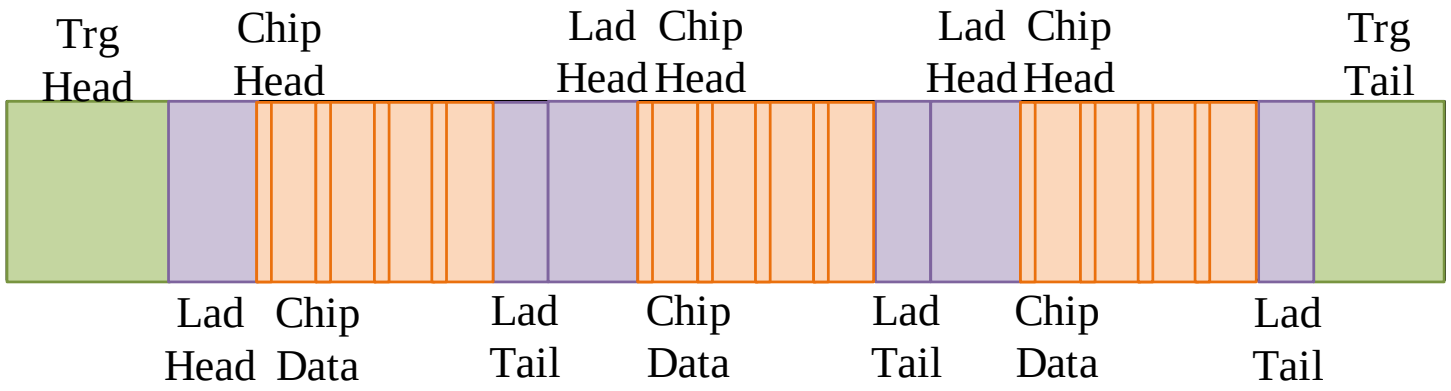


State:
1 – good
0 – not good

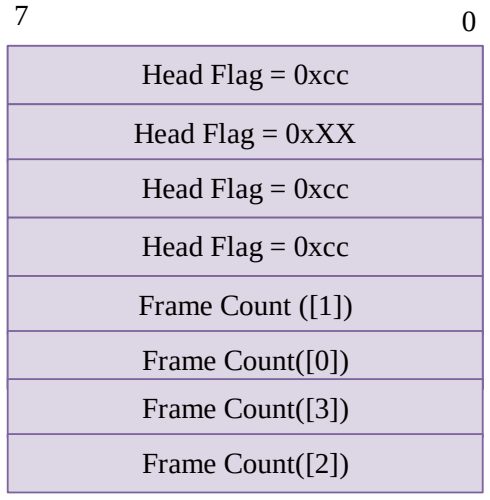


Trg Tail

MAPS DAQ Data Format

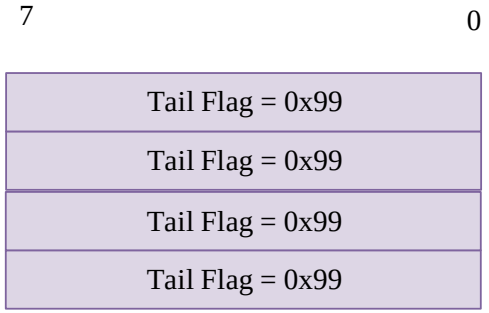


Trg Format



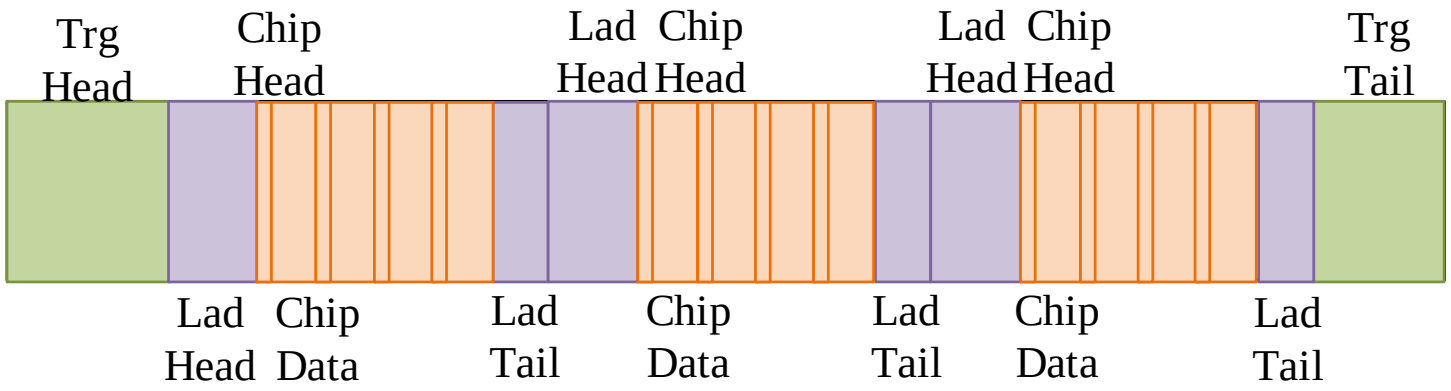
Lad Head(front)

Lad Head(end)

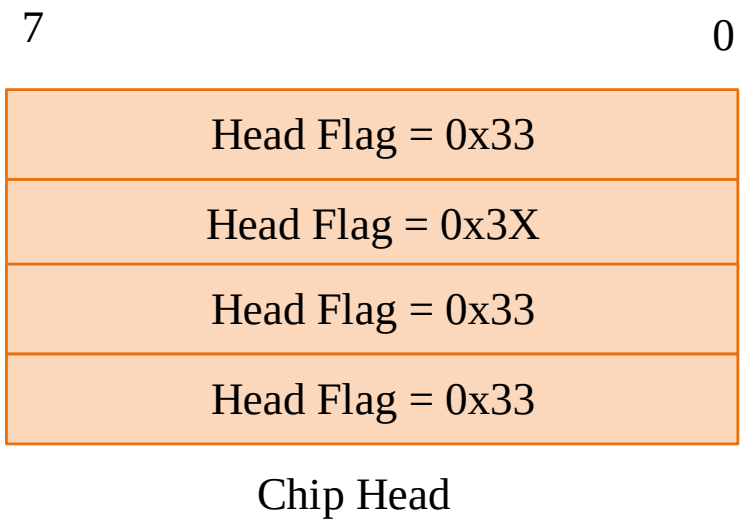


Lad Tail

MAPS DAQ Data Format

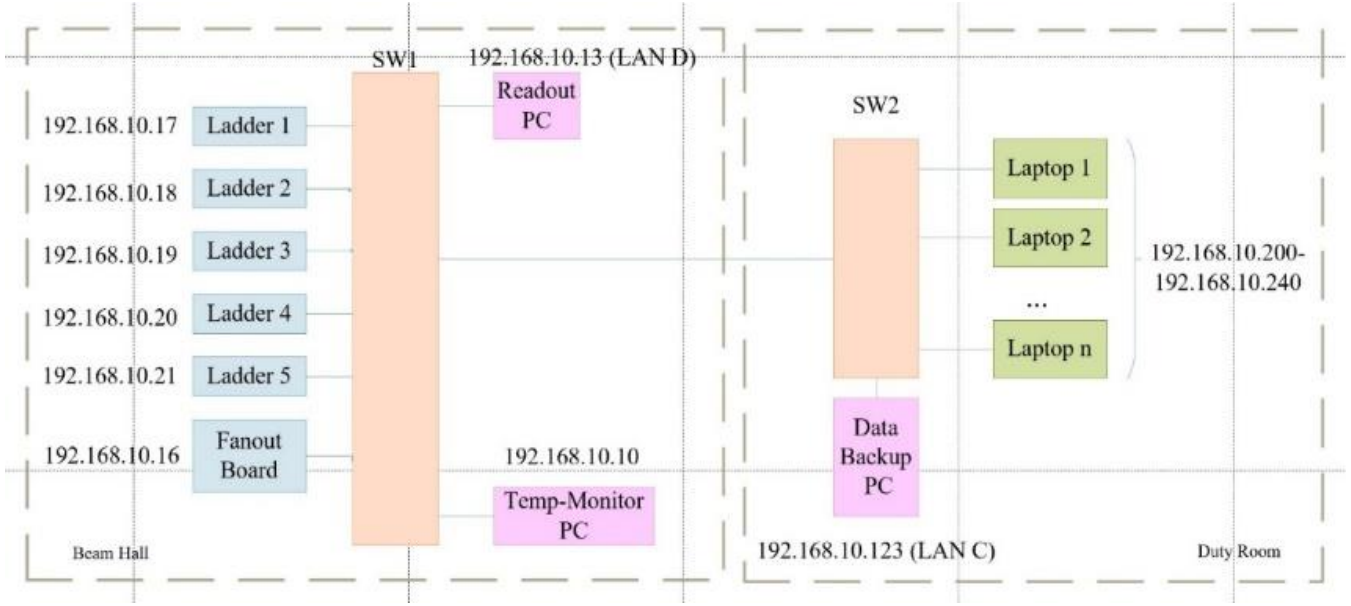


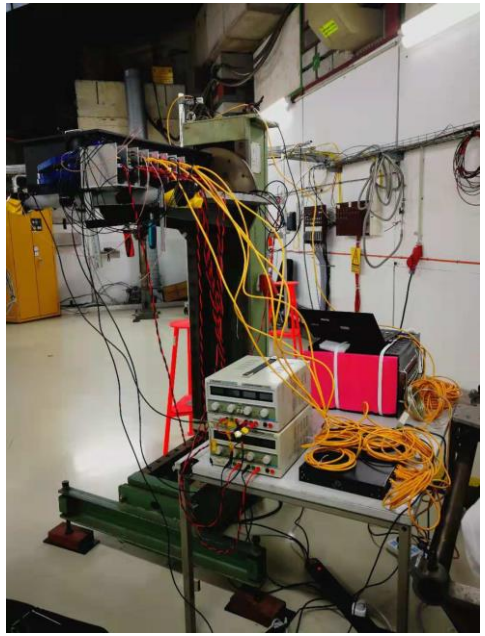
Trg Format

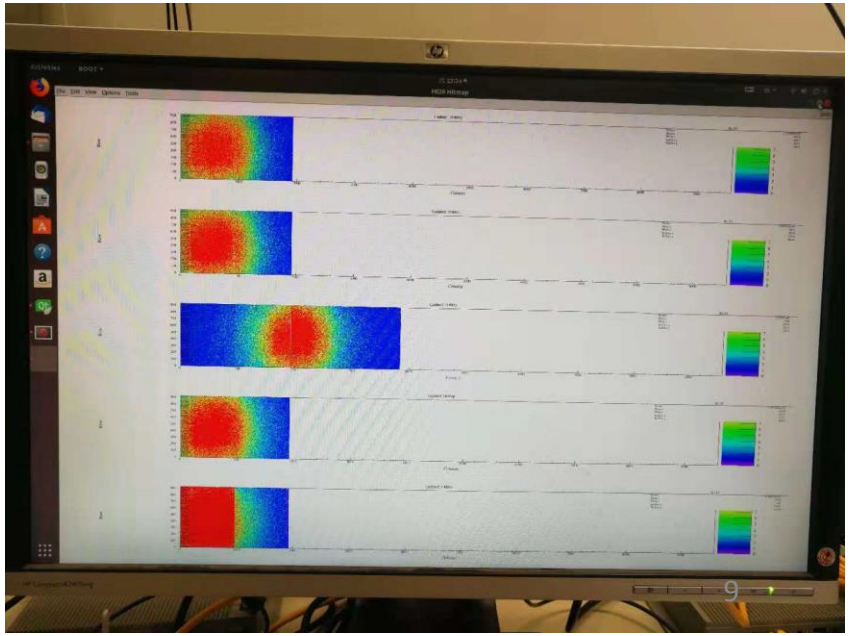


Chip Head

Beam Test at DESY





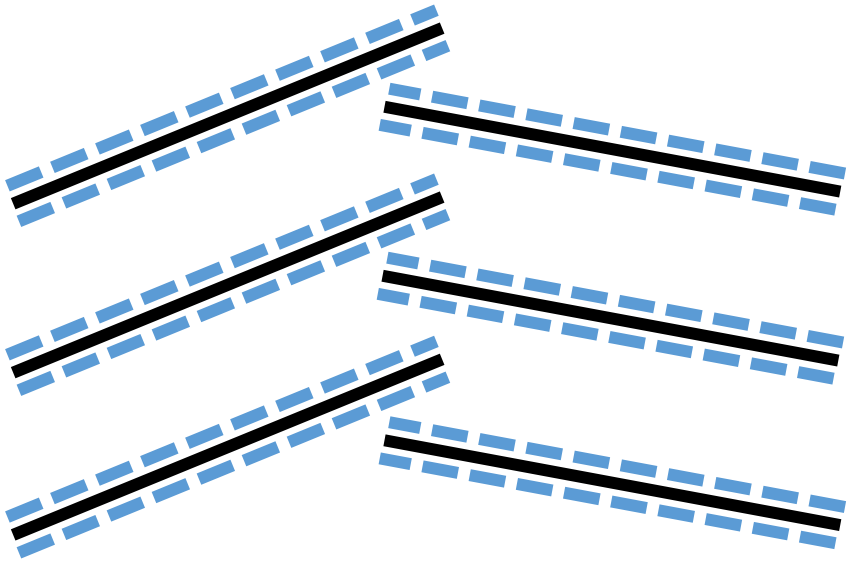


Most2 silicon detector DAQ

- **Requirements:**
  - Up to 6 double-sided ladders (10 sensors on each ladder)
  - Sensor work modes: trigger / triggerless
  - Readout electronics: 1GbE / 10 GbE Ethernet port
  - Run Control / configuration/ data taking / data storage
  - Online event building or data processing (?)

3 double-sided ladders

- **Important aspects for prototype DAQ development:**
  - Interface with FEE:
    - 1GbE/10GbE/?
    - TCP/UDP
  - Sensor/FEE configuration parameters
  - Data format:
    - Sensor Frame data: is there zero suppression or not?
    - Data package data format:
      - Trigger mode: Trigger Number
      - Triggerless mode: Time Stamp
  - Data rate



6 double-sided ladders

Data rate estimation

- **Trigger mode**
  - **1GbE port for each ladder**
    - 110Mbps/sensor * 10 sensors = 1100Mbps > 933Mbps ✗
    - 110Mbps/sensor * 5 sensors = 550Mbps < 933Mbps ✓
  - **10GbE port for each ladder**
    - 110Mbps/sensor * 10 sensors = 1100Mbps > 9330Mbps ✓
- **Triggerless mode**
  - **1GbE port for each ladder**
    - 3.84Gbps /sensor * 1 sensor > 933Mbps ✗
  - **10GbE port for each ladder**
    - 3.84Gbps /sensor * 2 sensor < 9330Mbps ✓

◆**Option 1: 1GbE port**
trigger mode: 5 sensors / FEE board
No triggerless mode

◆**Option 2: 10GbE port**
trigger mode: 10 sensors / FEE board
Triggerless mode: 2 sensors enabled, 8 sensors disabled

Future Plan

1.3	数据获取系统	Data acquisition system	2018/5/1	2021/7/26
1.3.1	为初次MPW的芯片研制前端电路板	Developed the front end circuit board for the initial MPW chip	2018/5/1	2019/3/18
1.3.2	研制**单个传感器芯片**的数据获取系统	A data acquisition system for a **single sensor chip** is developed	2019/3/19	2020/3/23
1.3.3	研制**单个探测器模块**的数据获取系统	A data acquisition system for a **single detector module** is developed	2020/3/24	**2021/2/1**
1.3.4	研制**探测器原型机**的数据获取系统	A data acquisition system for the **prototype detector** is developed	**2021/2/2**	**2021/7/26**
1.5.4	对工程批芯片做测试	Test engineering chip	**2021/11/8**	2022/3/25
1.6	束流测试与数据分析	Beam testing and data analysis	**2022/5/11**	2023/2/7
1.6.1	束流测试实验	Beam test experiment	2022/5/11	2022/8/2

- 2020.08 – 2021.05
  - develop DAQ software for prototype detector
  - use simulated FEE and data
  - better to know sensor & FEE data format and configuration information earlier
- 2021.06 – 2021.10
  - test with FEE boards
  - test with Ladders & FEE boards
- 2021.11 – 2022.02
  - Beam test experiment

Hope FEE boards could be available before 2021.05