CEPC Vertex Detector

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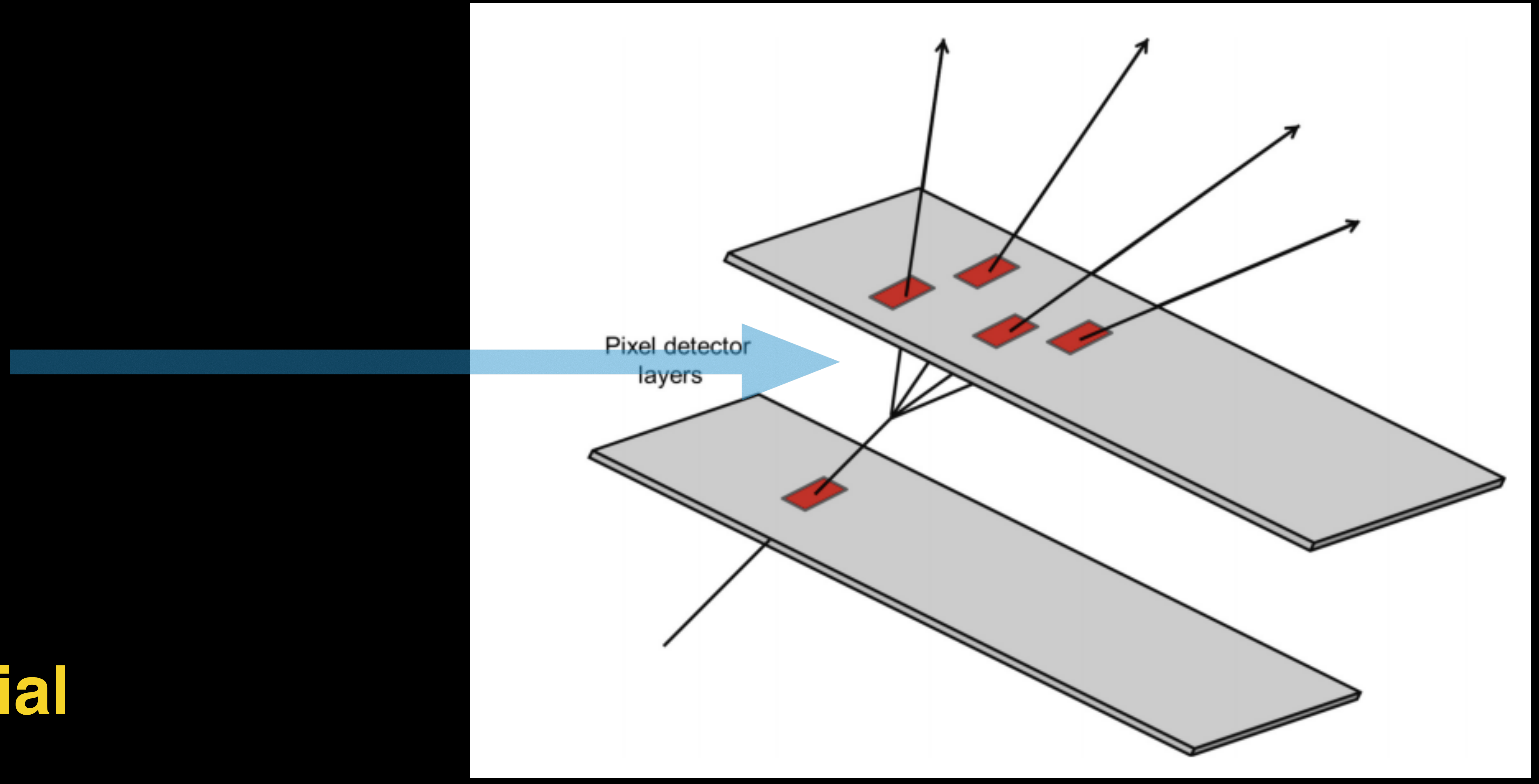
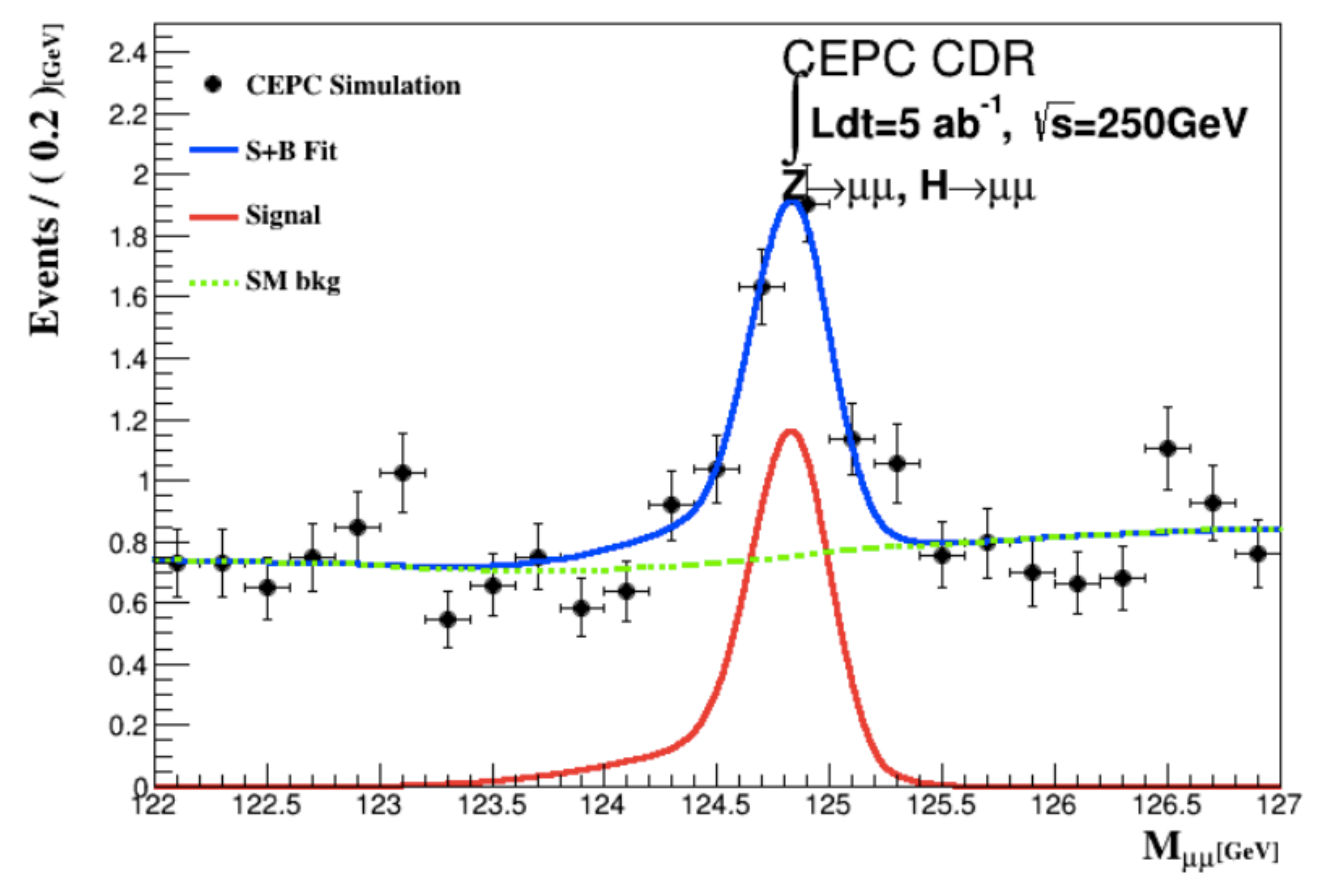
Vertex detector: Physics goal

- Higgs precision measurement
  - H → bb precise vertex reconstruction
  - H → μμ (precise momentum measurement)



**Need tracking detector with
high spatial resolution, low material**

- Main technology
  - High spatial resolution technology → pixel detector
  - Low-mass detector technology
  - Radiation resistance technology

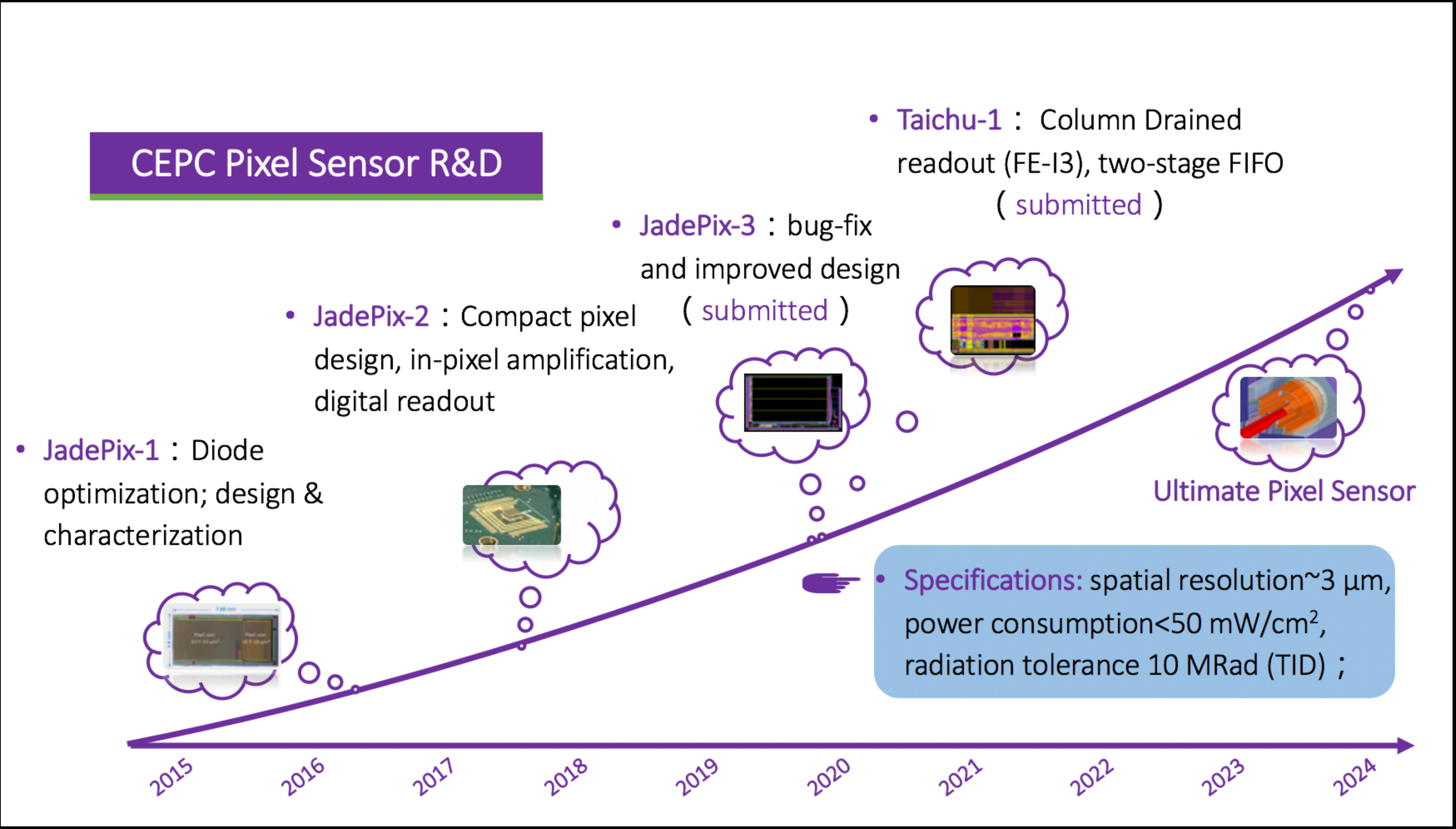


CEPC vertex detector R & D

- Three on-going R & D programs on vertex detector
  - Previous update in CEPC day (June 15th) https://indico.ihep.ac.cn/event/11875/
- This talk focuses on MOST2 project
  - MOST2 aims to build full-size vertex detector prototype

Funding agency	Process	International collaborators	Objectives of the project	schedule
MOST1	CMOS	Strasburg IPHC	Small pixel size design with in-pixel digitization and low power frontend	2016.6-2021.5
MOST2	CMOS	IFAE/Oxford/ Livepool …	full-size vertex detector prototyping （Full-size sensor support structure, module …)	2018.5-2023.4
NSFC	SOI	KEK/SOIPIX collaboration	Verification of SOI process with small pixel size and low noise design	2016-

CEPC vertex detector R & D



CEPC Pixel Sensor R&D

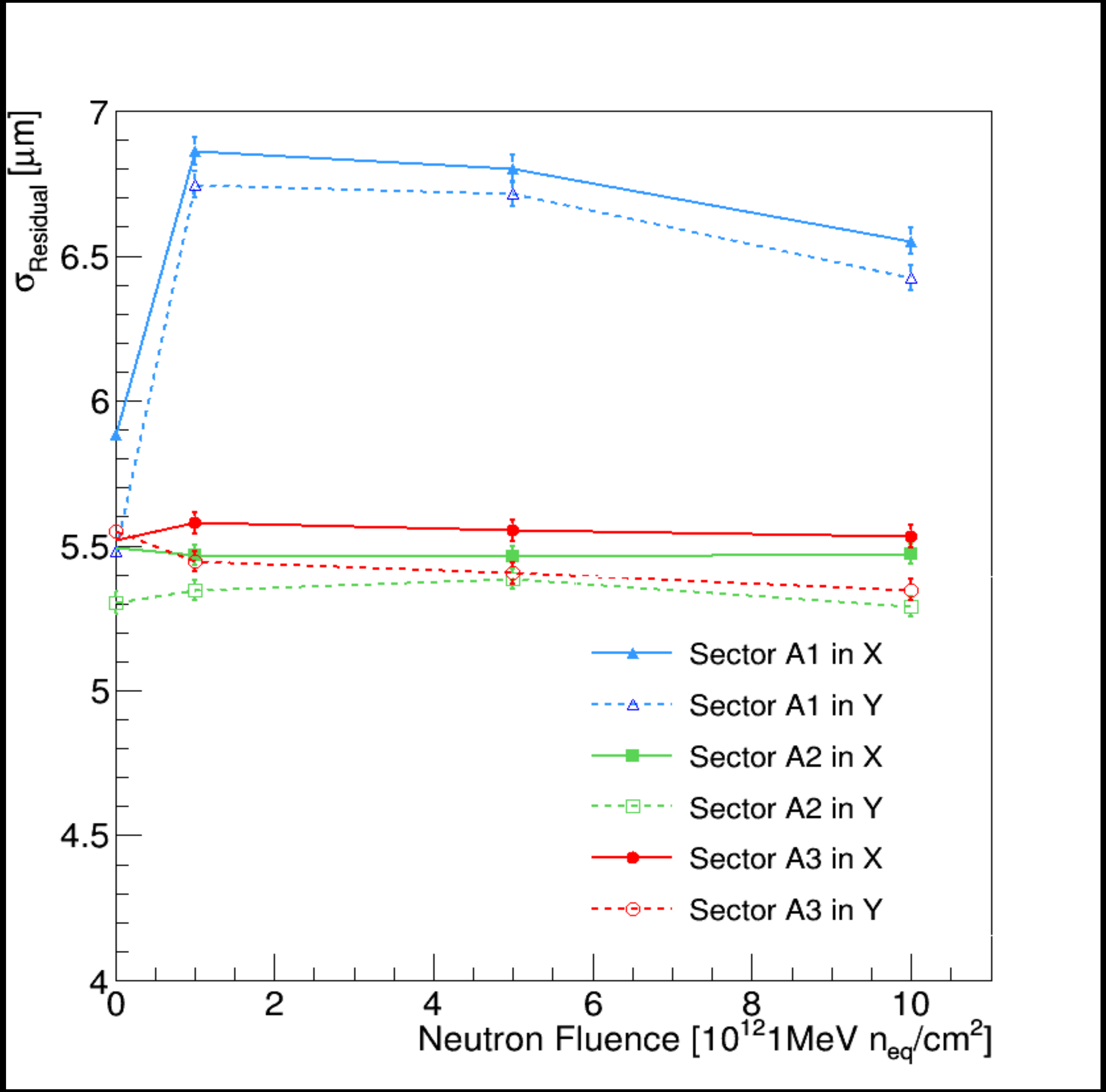
- **JadePix-1**：Diode optimization; design & characterization
- **JadePix-2**：Compact pixel design, in-pixel amplification, digital readout
- **JadePix-3**：bug-fix and improved design （submitted）
- **Taichu-1**： Column Drained readout (FE-I3), two-stage FIFO （submitted）

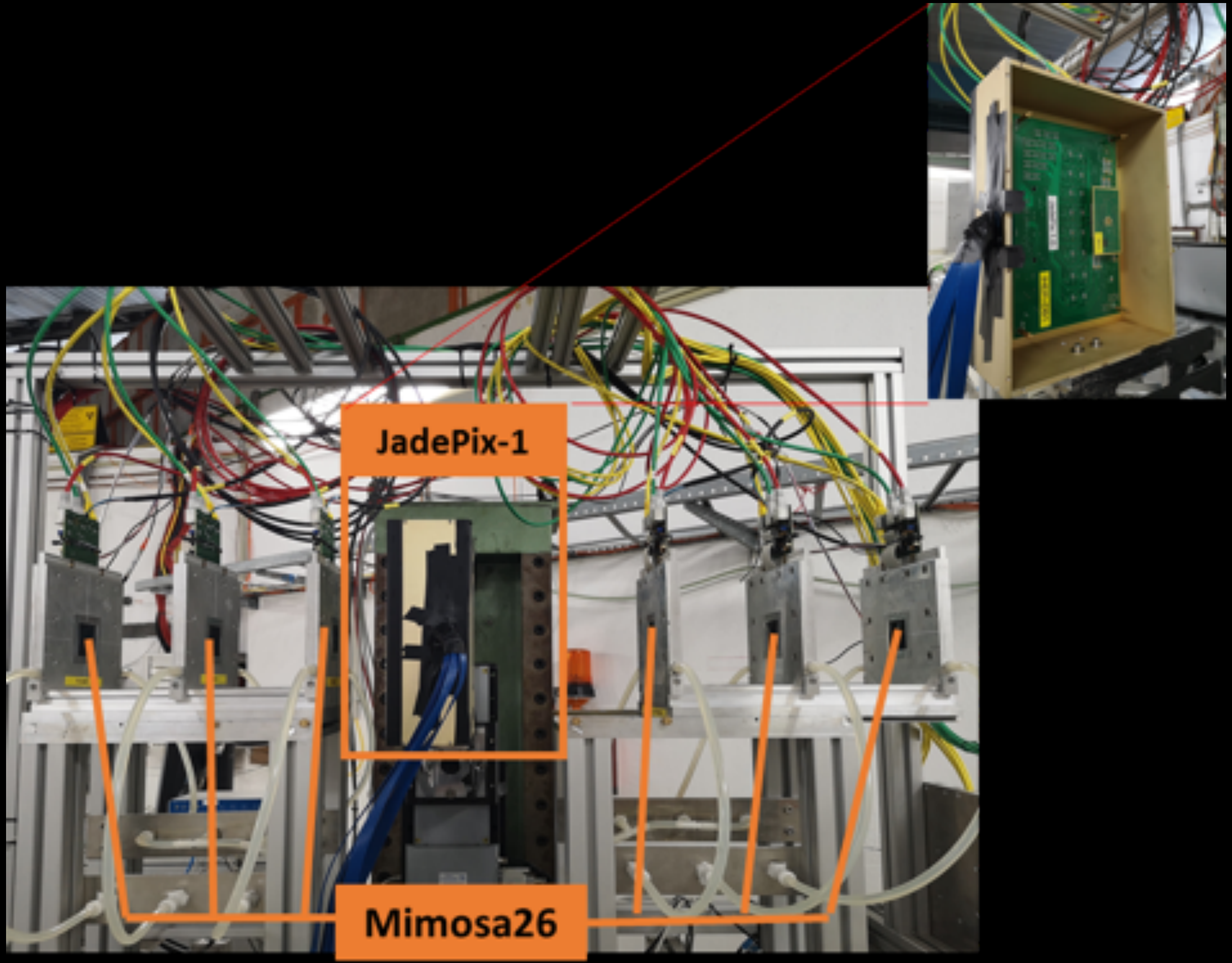
Ultimate Pixel Sensor

- **Specifications:** spatial resolution~3 μm, power consumption<50 mW/cm^2, radiation tolerance 10 MRad (TID)；

JADEPIX-1 RESOLUTIONS

- 5~7 μm spatial resolution achieved in DESY electron beam test

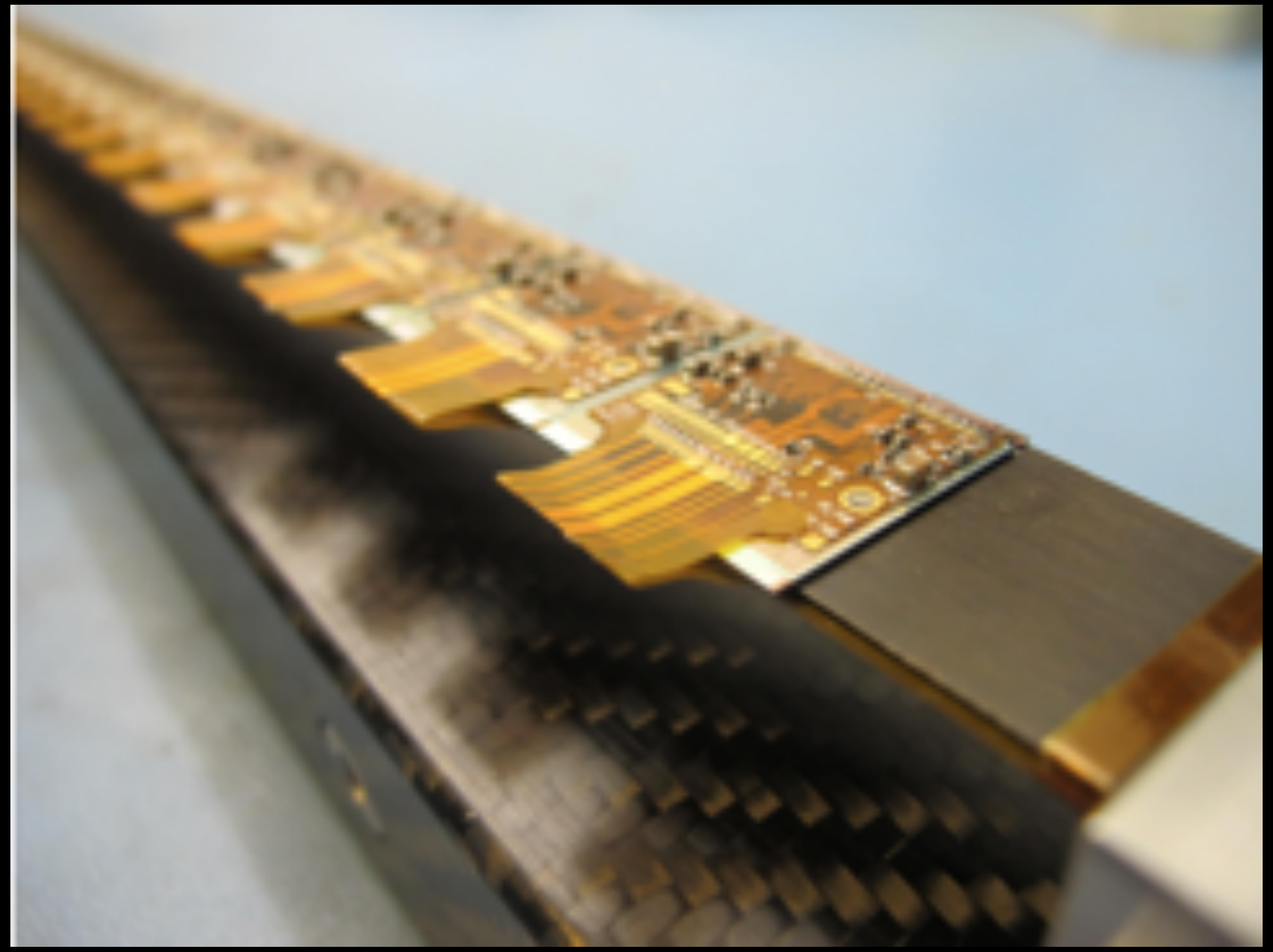




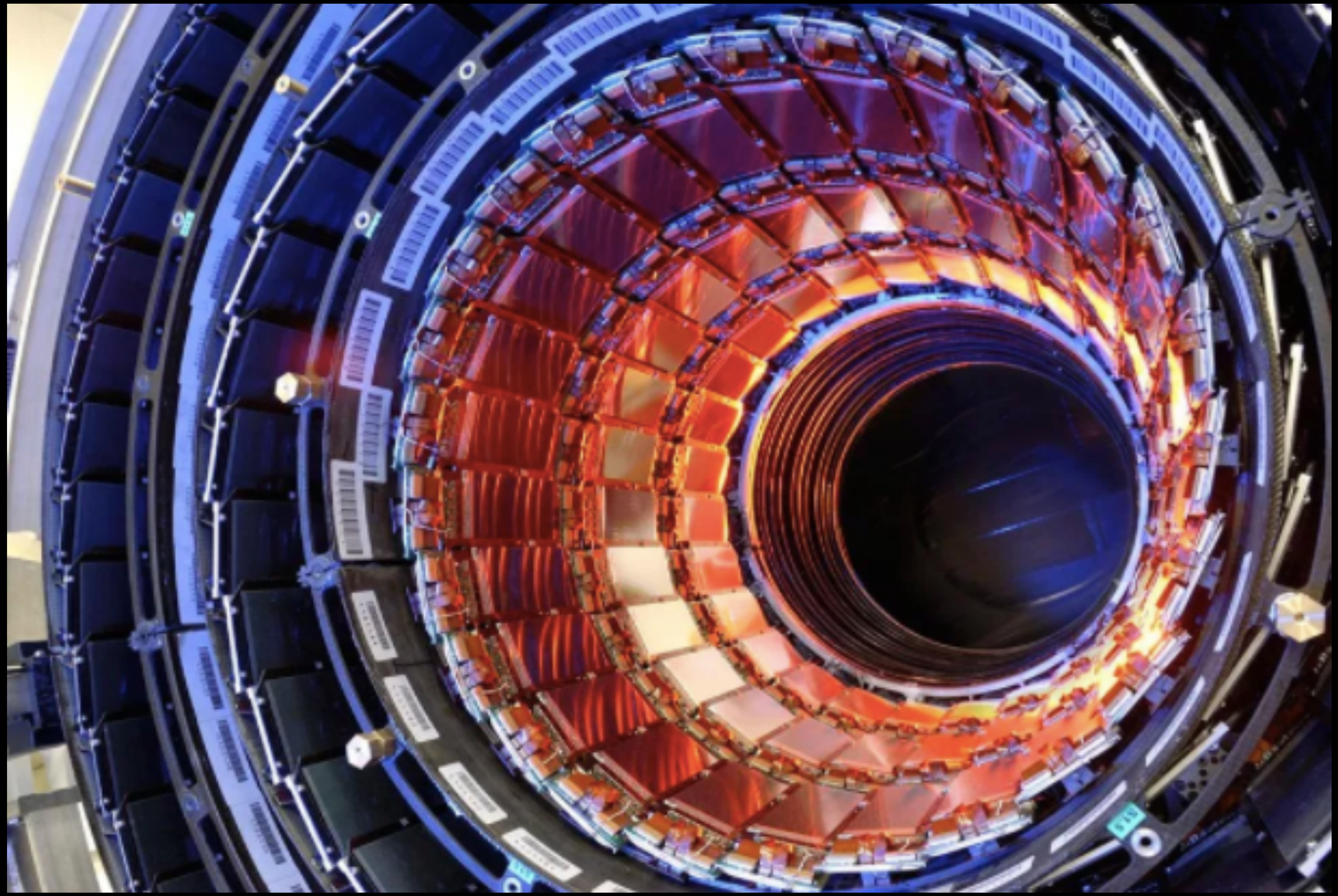
MOST2 vertex detector R & D: Research Goal

- Produce a world class vertex detector prototype
  - Spatial resolution 3~5 μm (pixel detector)
  - Radiation hard (>1 MRad)
  - Material budget 0.15%X_0 per layer
- Preliminary design of prototype
  - Three layer, module ~1 cm × 12 cm^2

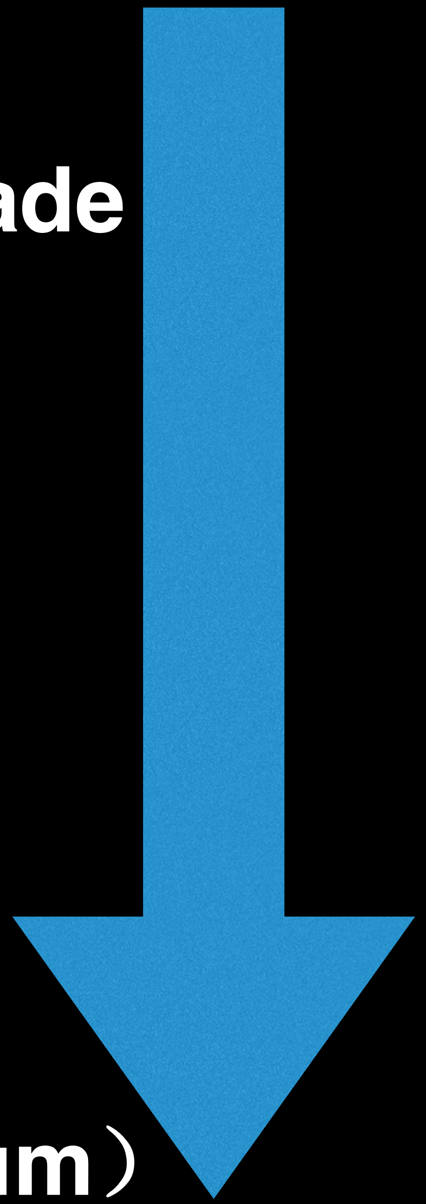
Typical module



Typical tracker



Resolution



ATLAS/CMS upgrade
（~15 μm）

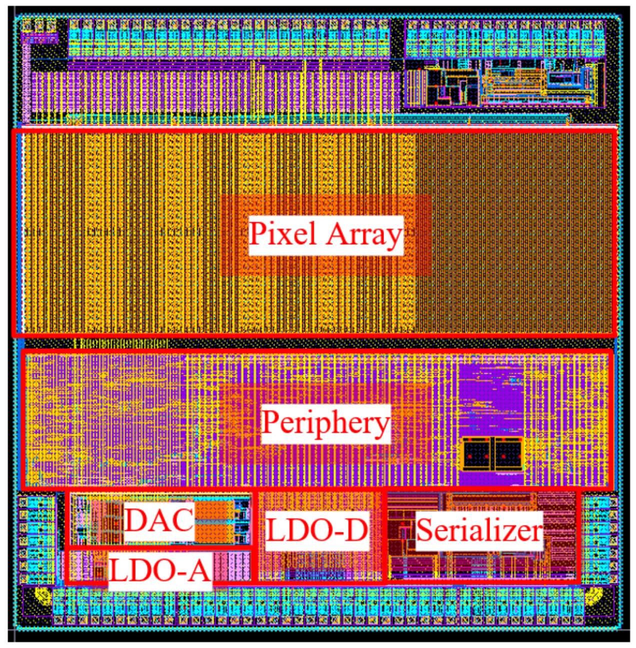
Alice upgrade
（5~10 μm）

World leading This project（3~5 μm）

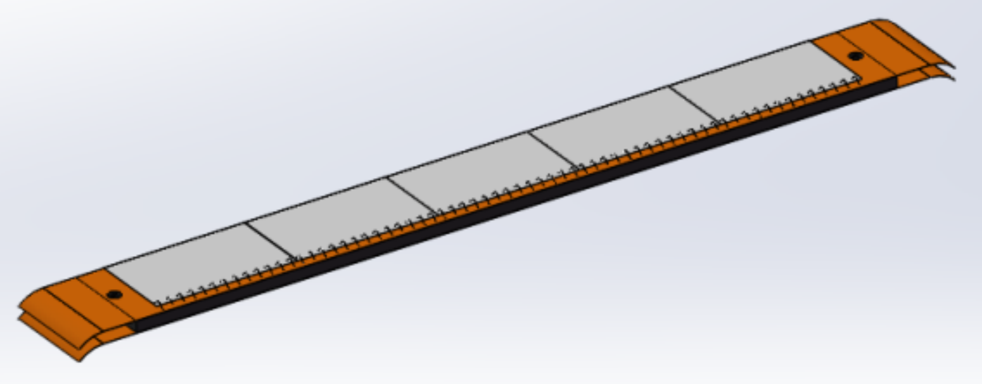
Overview of MOST2 vertex detector R & D

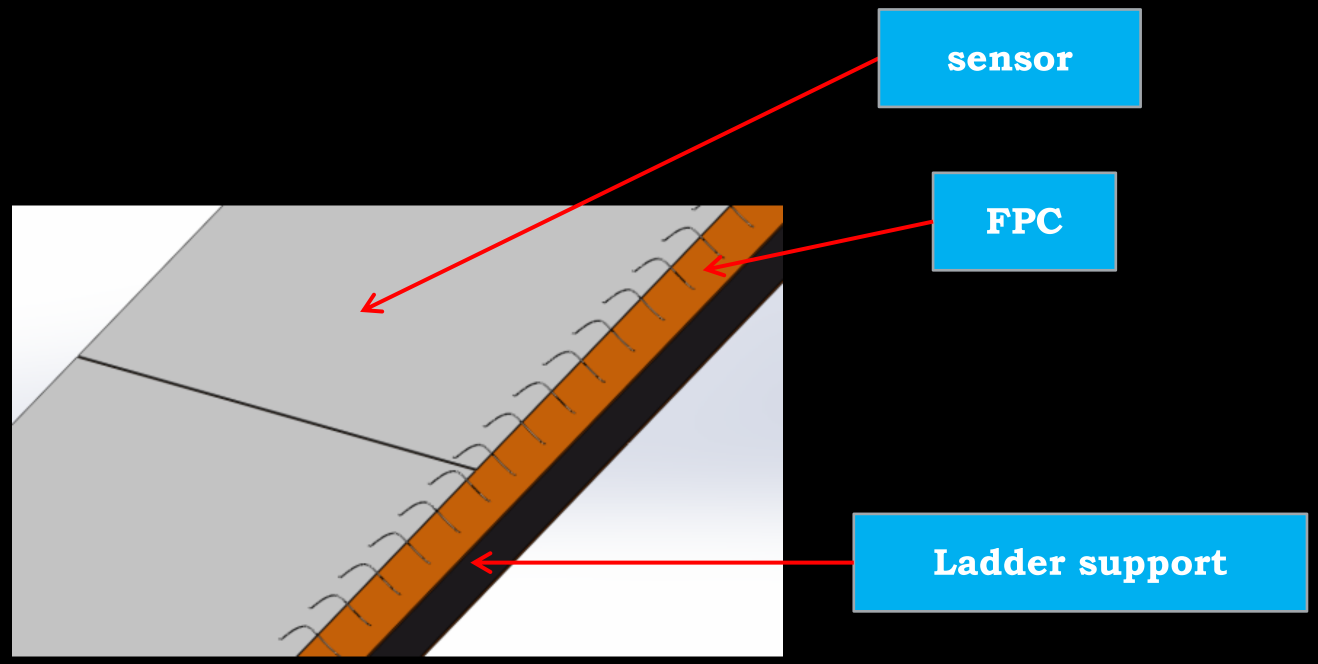
- Can break down into sub-tasks:
  - CMOS imaging sensor chip R & D
  - Detector layout optimization, Ladder and vertex detector support structure R & D
  - Detector assembly
  - Data acquisition system R & D

CMOS imaging sensor prototyping

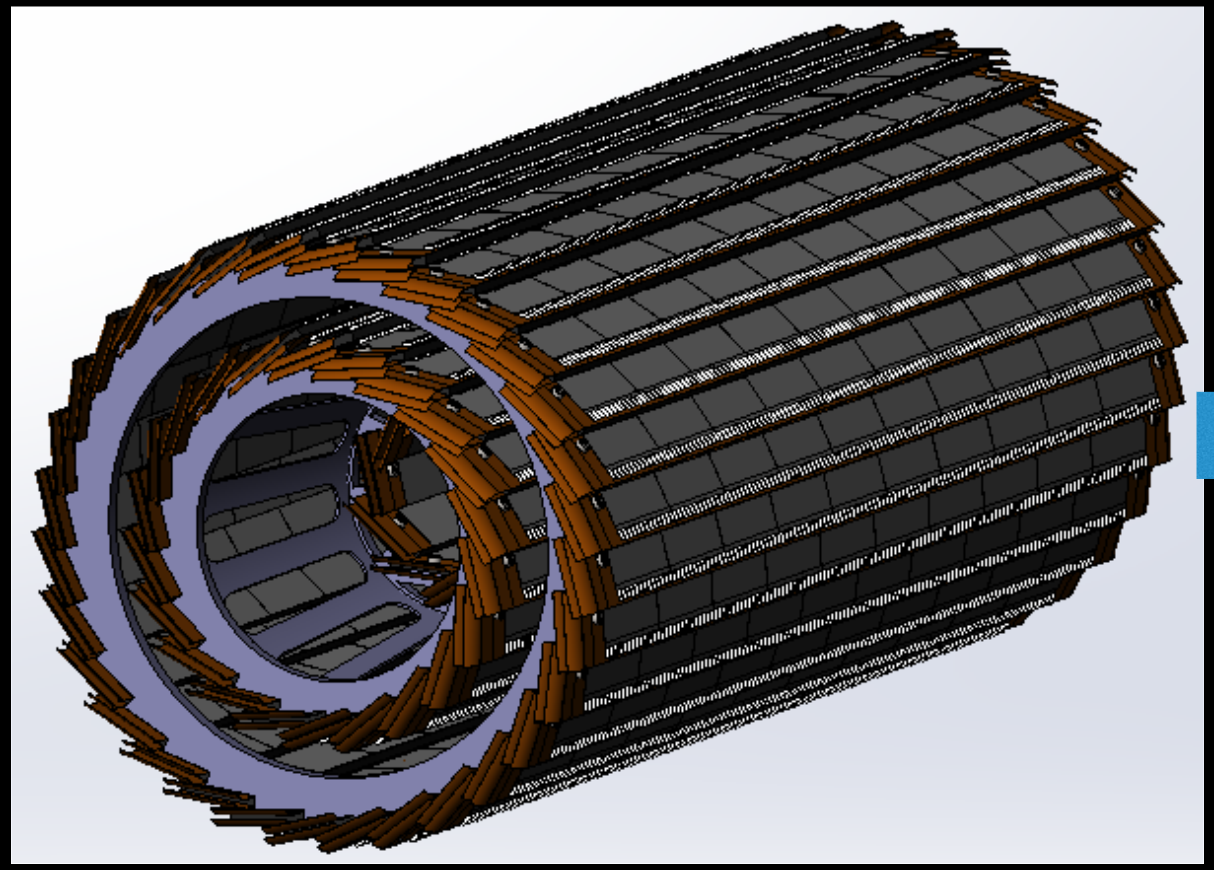


Detector module (ladder) Prototyping

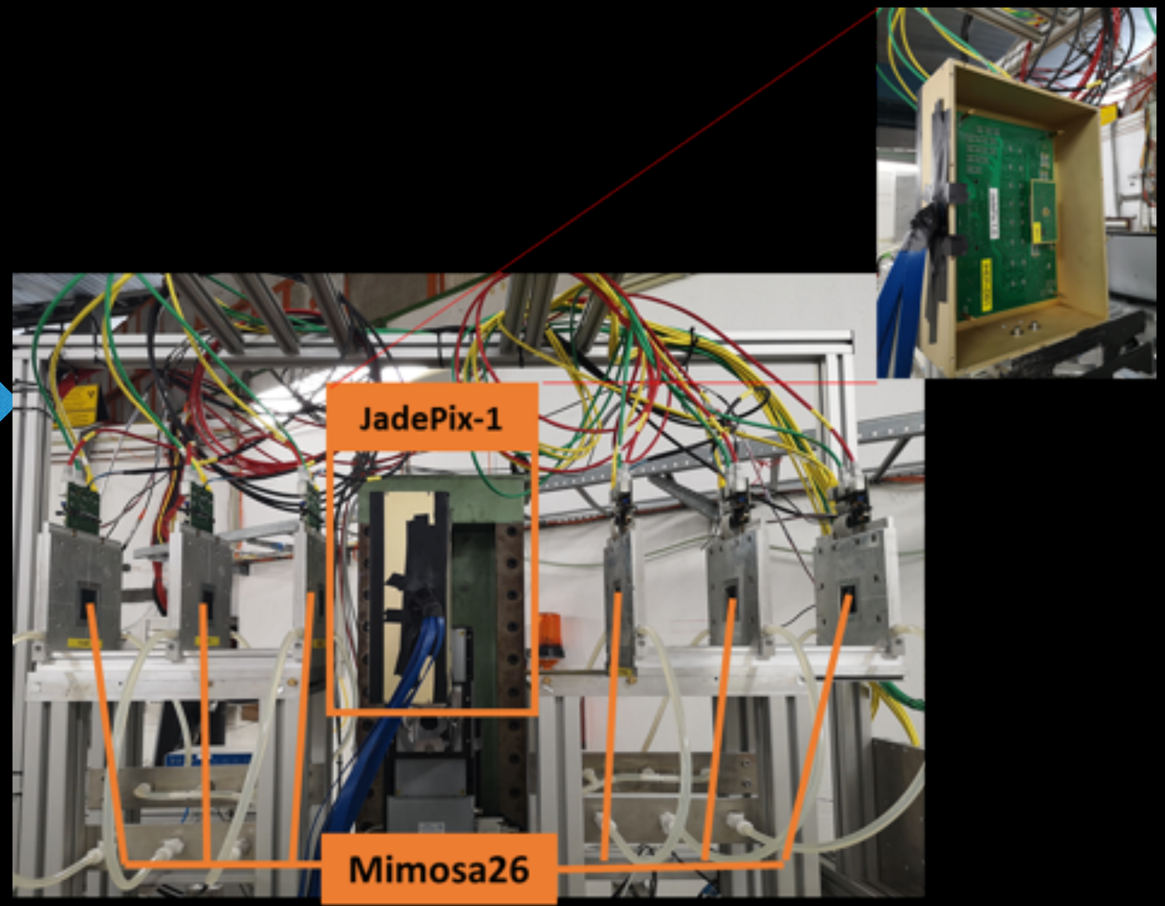




Full size vertex detector Prototype

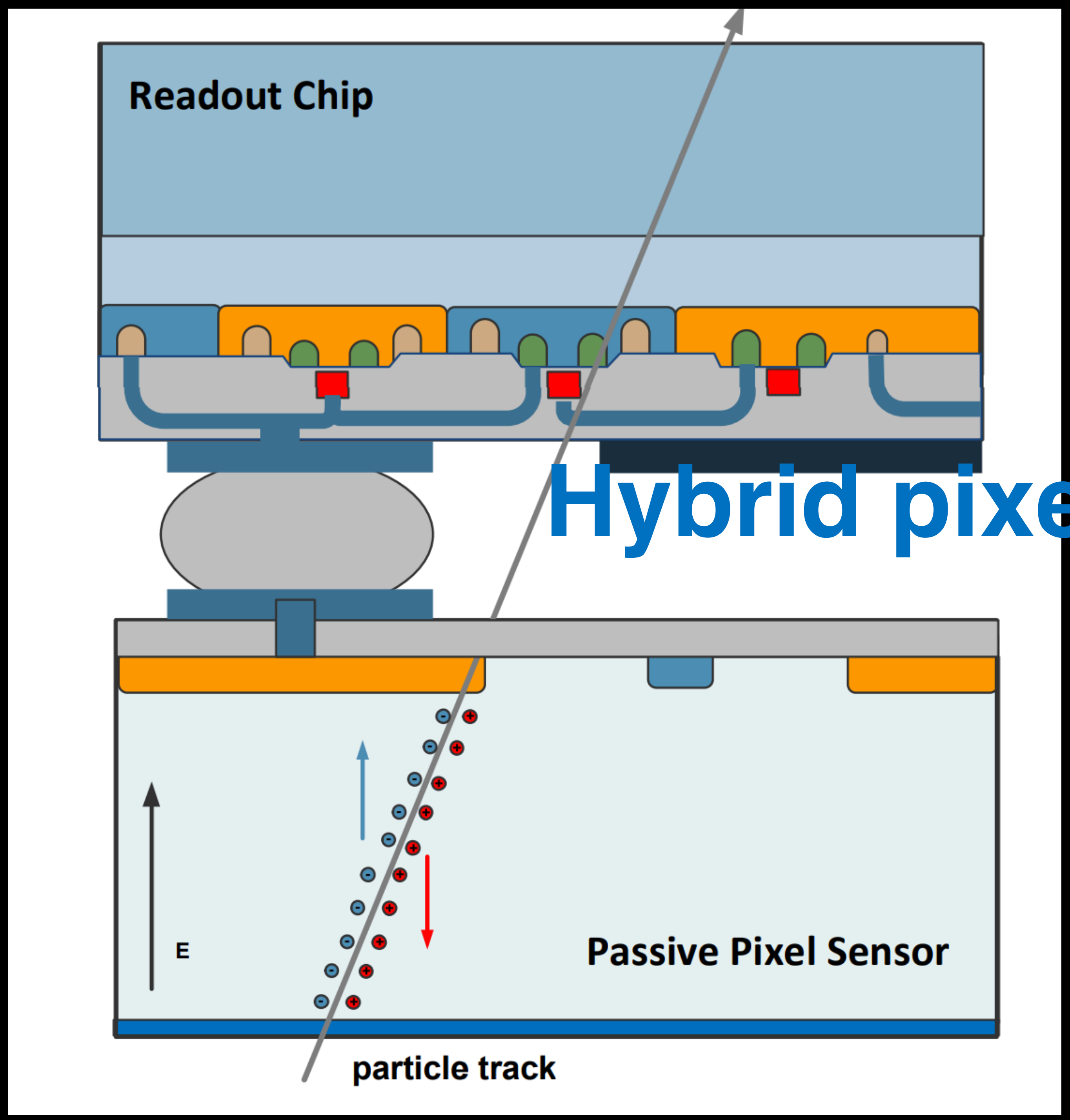


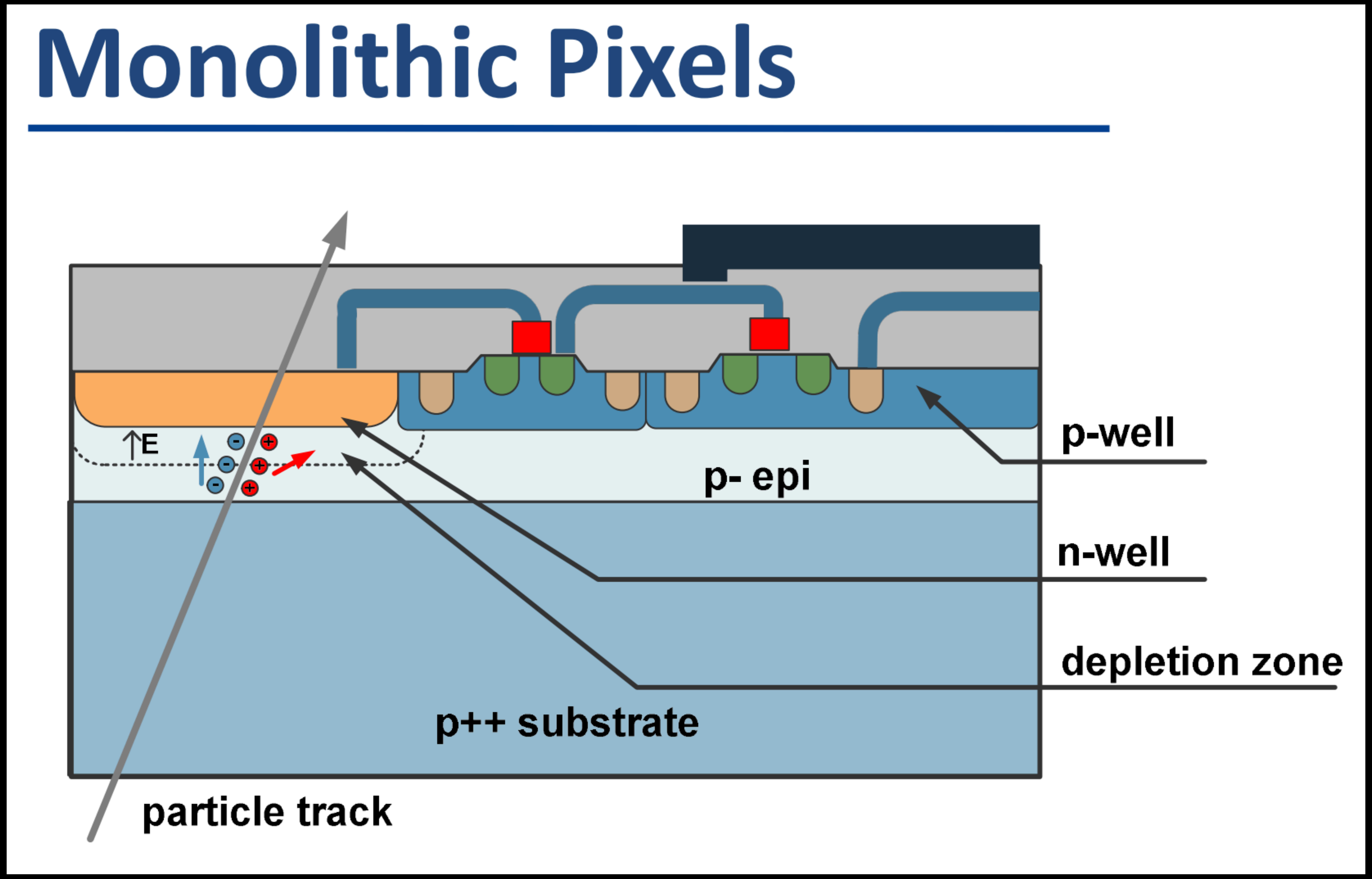
Beam test to verify its spatial resolution



CMOS MONOLITHIC PIXEL SENSOR

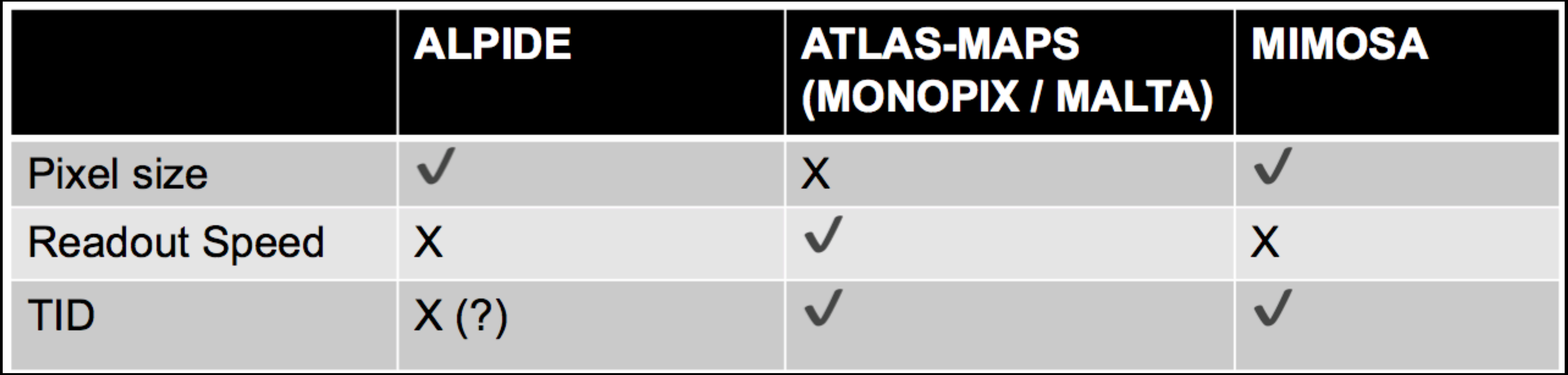
- CMOS Monolithic pixel (CIS process) is ideal for CEPC application
  - low material budget (can be thin down to 50µm)
  - This project use TowerJazz CIS 180nm technology
- Hybrid pixel technology developed by ATLAS and CMS
  - Thickness of sensor is about 200~300 µm
  - Need to bump bonding with readout ASIC (ASIC thickness is about 300µm)
  - Material budget about silicon sensor is about 10 times larger than CIS process





CMOS Sensor chip R & D

- The existing CMOS monolithic pixel sensors can’t fully satisfy the requirement
- Major Challenges for the CMOS sensor
  - Small pixel size -> high resolution (3-5 μm)
  - High readout speed (<500ns deadtime @40MHz at Z pole) -> for CEPC Z pole high lumi
  - Radiation tolerance **(per year):** 1 MRad



	ALPIDE	ATLAS-MAPS (MONOPIX / MALTA)	MIMOSA
Pixel size	✓	X	✓
Readout Speed	X	✓	X
TID	X (?)	✓	✓

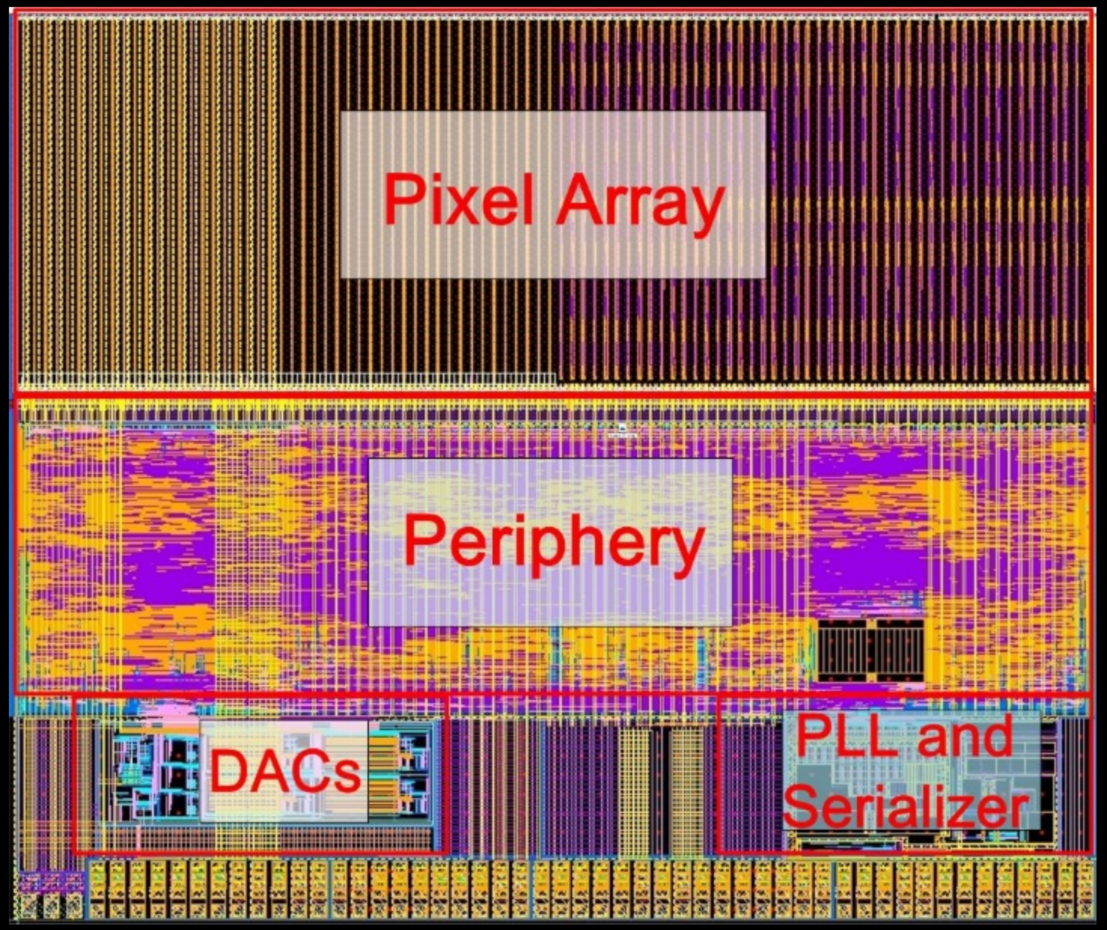
Sensor prototyping

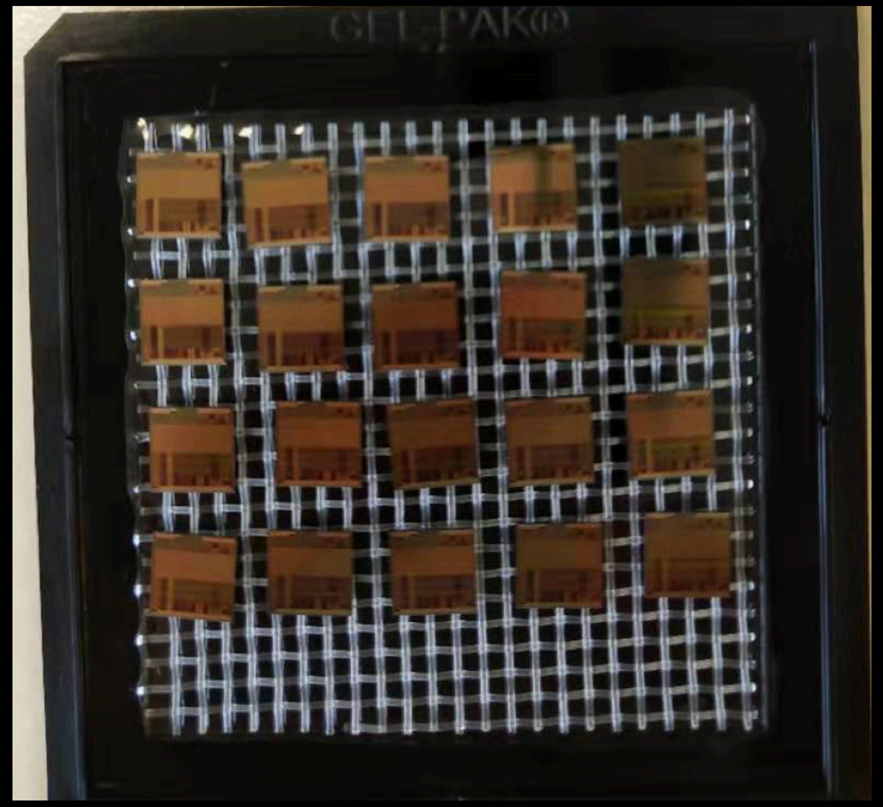
- Completed two round of sensor prototyping
  - 1st Multi-wafer project chip (Taichupix1)
    - Submitted in June 2019, received in November 2019
    - Test functional blocks
      - pixel array (in-pixel amplifier and digital logic)
      - Periphery block: digital readout architecture
      - Periphery block: PLL and Serializer
      - Periphery block: LDO and power supply
  - 2nd Multi-wafer project chip(Taichupix2)
    - Submitted in Feb 2020, received in July 2020
    - Major bugs fixed in Taichupix1
    - Radiation hard design (enclosed gate) in pixel analog

Taichupix1

Chip size：5mm×5mm

Pixel size：25μm×25μm

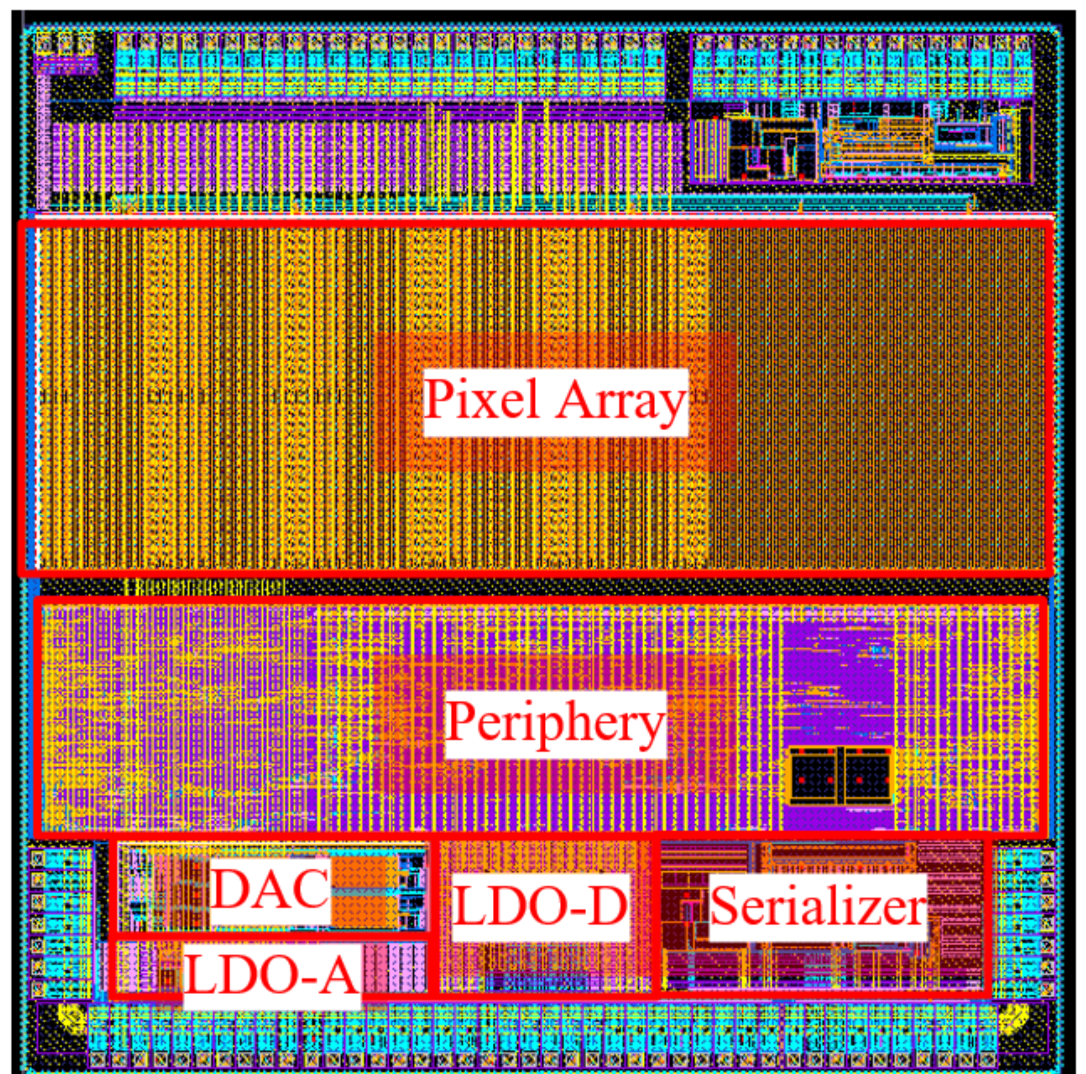




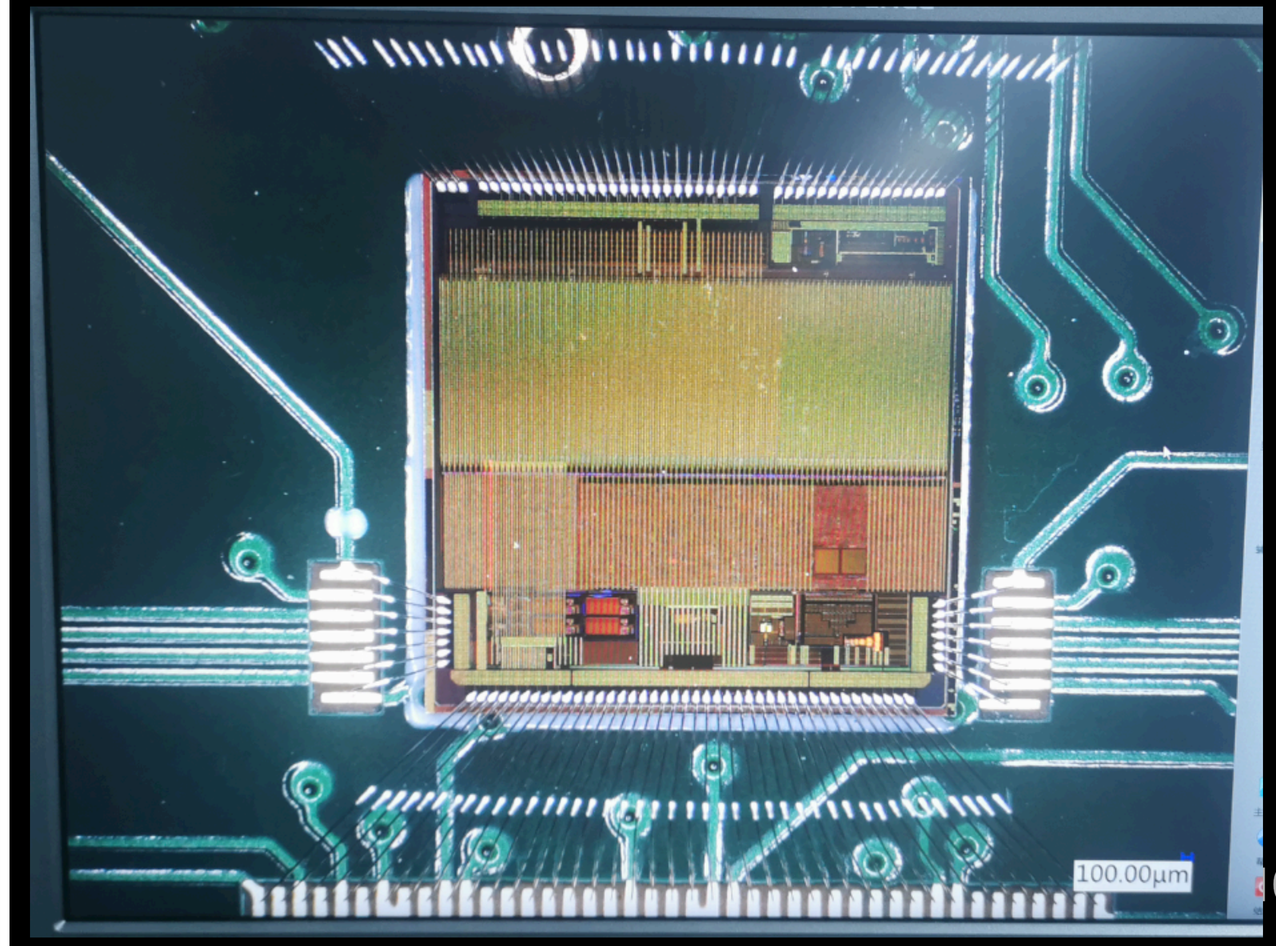
Taichupix2

Chip size：5mm×5mm

Pixel size：25μm×25μm



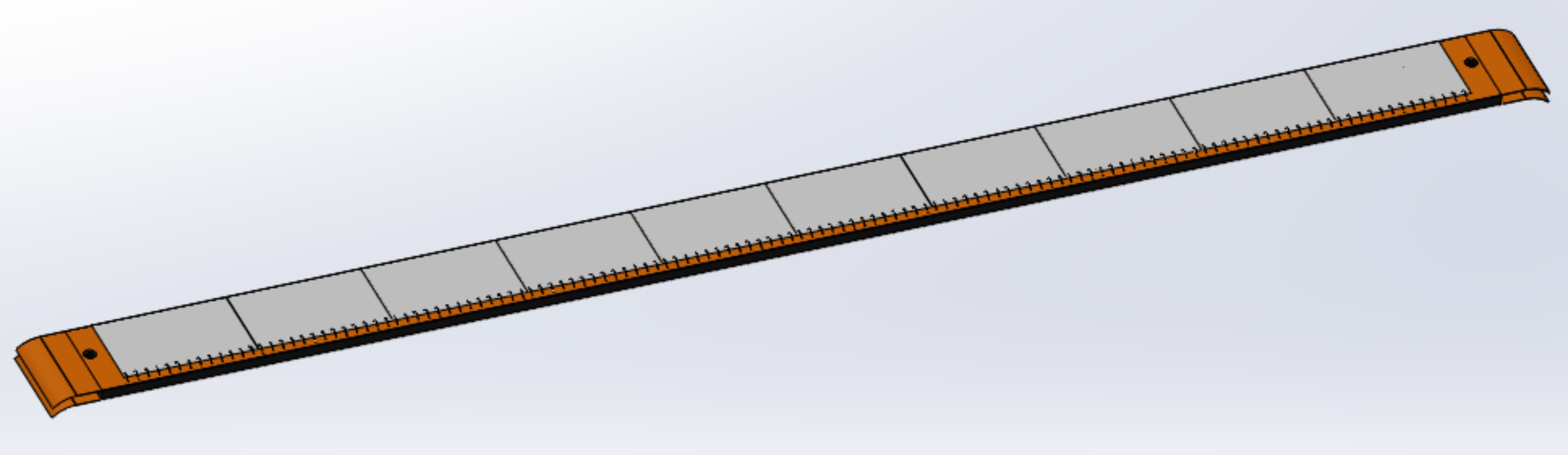
Taichupix2 on test board



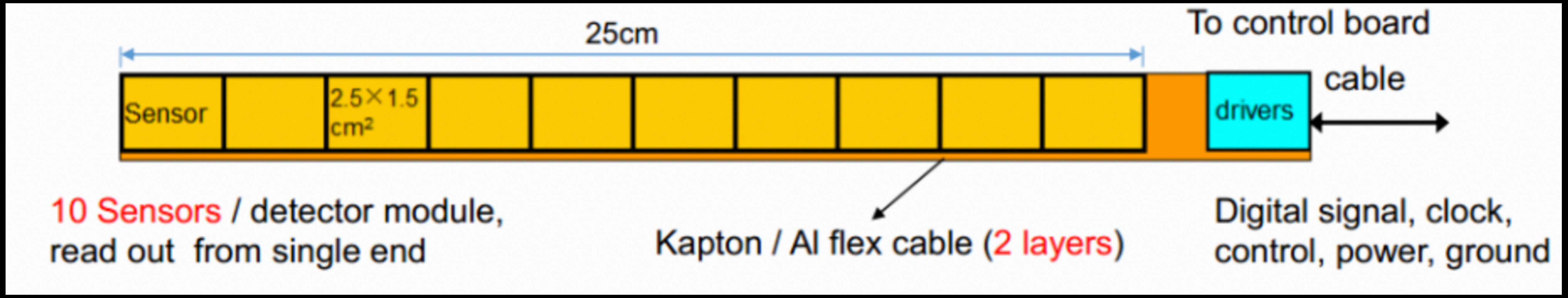
Detector module (ladder) R & D

- Completed preliminary version of detector module (ladder) design
  - Detector module (ladder)= 10 sensors + support structure+ flexible PCB+ control board
  - Sensors will be glued and wire bonded to the flexible PCB
  - Flexible PCB will be supported by carbon fiber support structure
  - Signal, clock, control , power, ground will be handled by control board through flexible PCB

3D model of the ladder



Schematic of ladder electronics



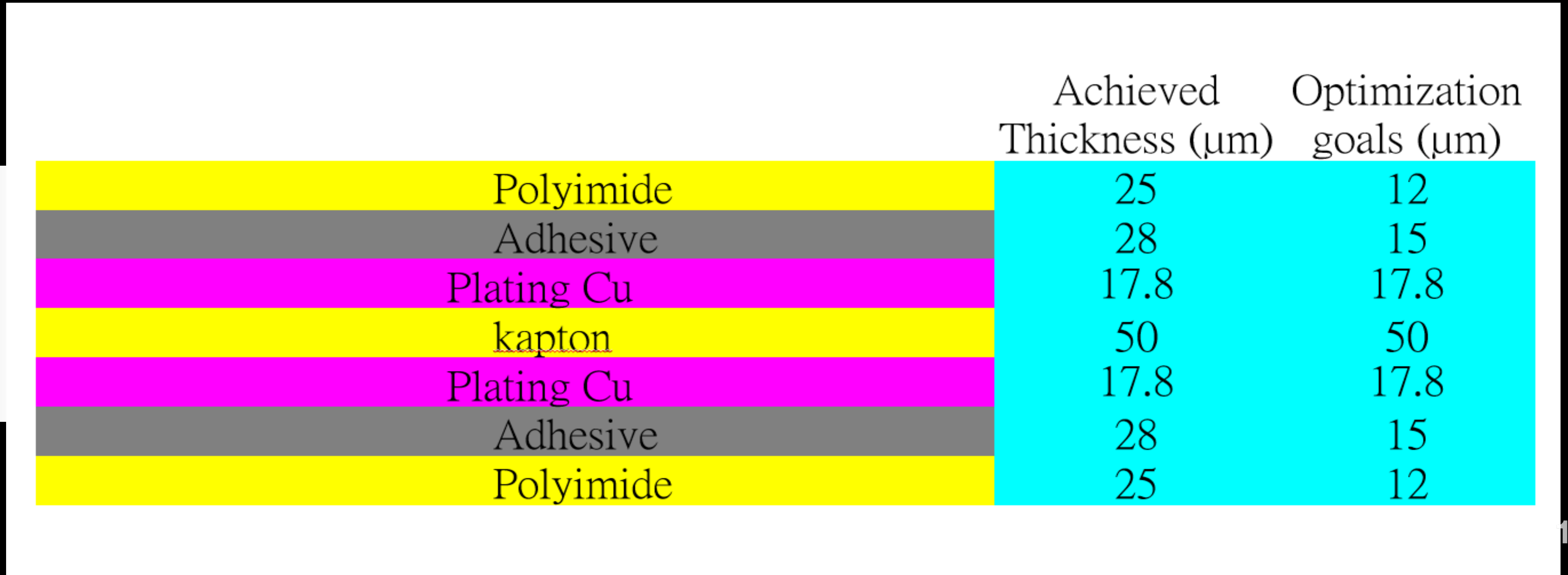
10 Sensors / detector module, read out from single end

Kapton / Al flex cable (2 layers)

Digital signal, clock, control, power, ground

Flexible PCB prototype

Profile of flexible PCB

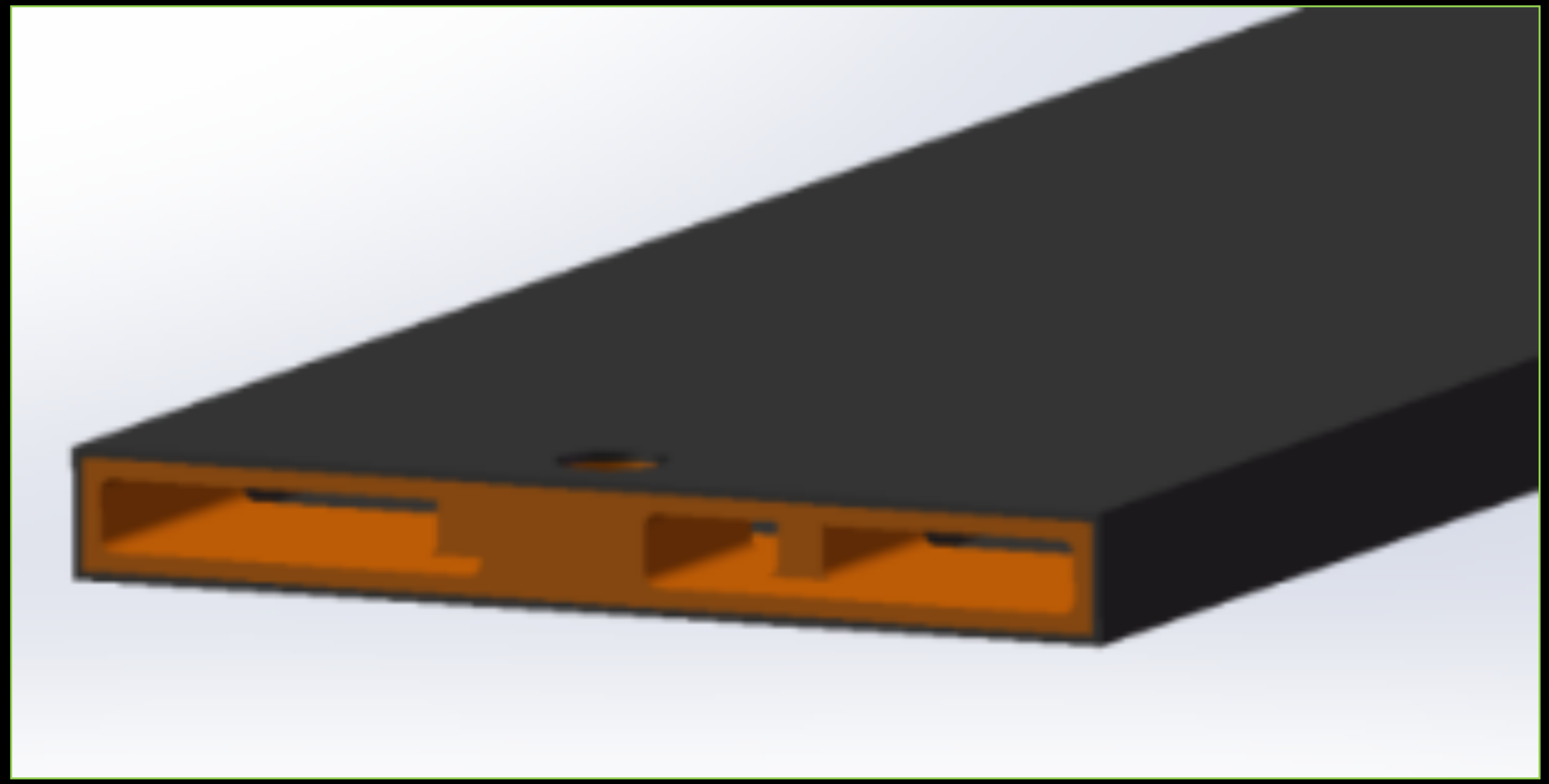


	Achieved Thickness (μm)	Optimization goals (μm)
Polyimide	25	12
Adhesive	28	15
Plating Cu	17.8	17.8
kapton	50	50
Plating Cu	17.8	17.8
Adhesive	28	15
Polyimide	25	12

Support structure of the ladder

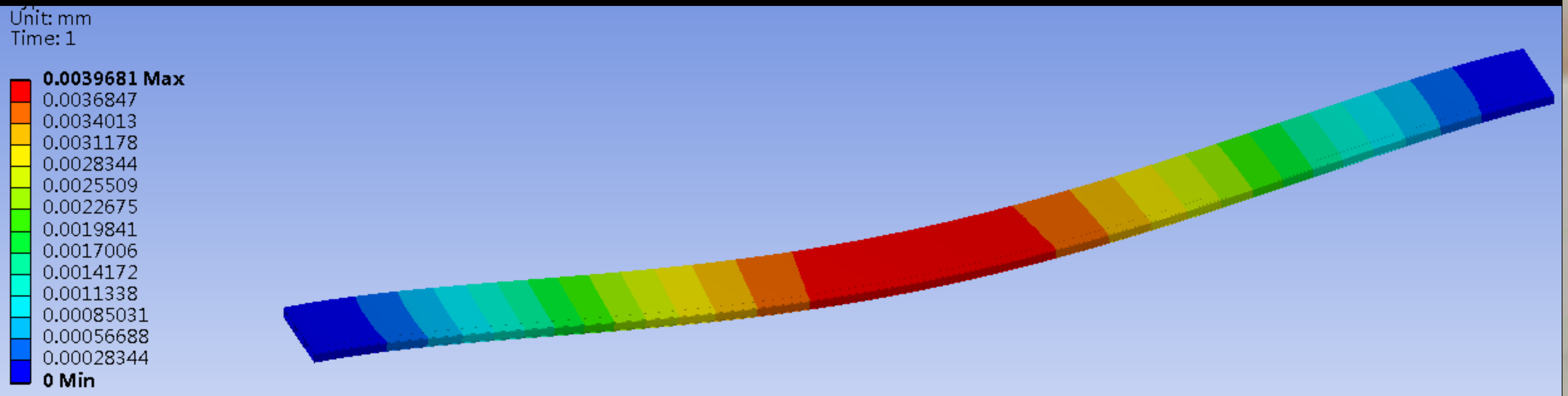
- Support structure of the ladder: 3 layer of carbon fiber, 0.15mm thick
  - 3 time thinner than conventional carbon fiber
  - A few times more rigid than conventional carbon fiber
  - for tracks with small cosθ, radiation length ~0.015 X0 (reduce multi-scattering)

Ladder support structure 3D model



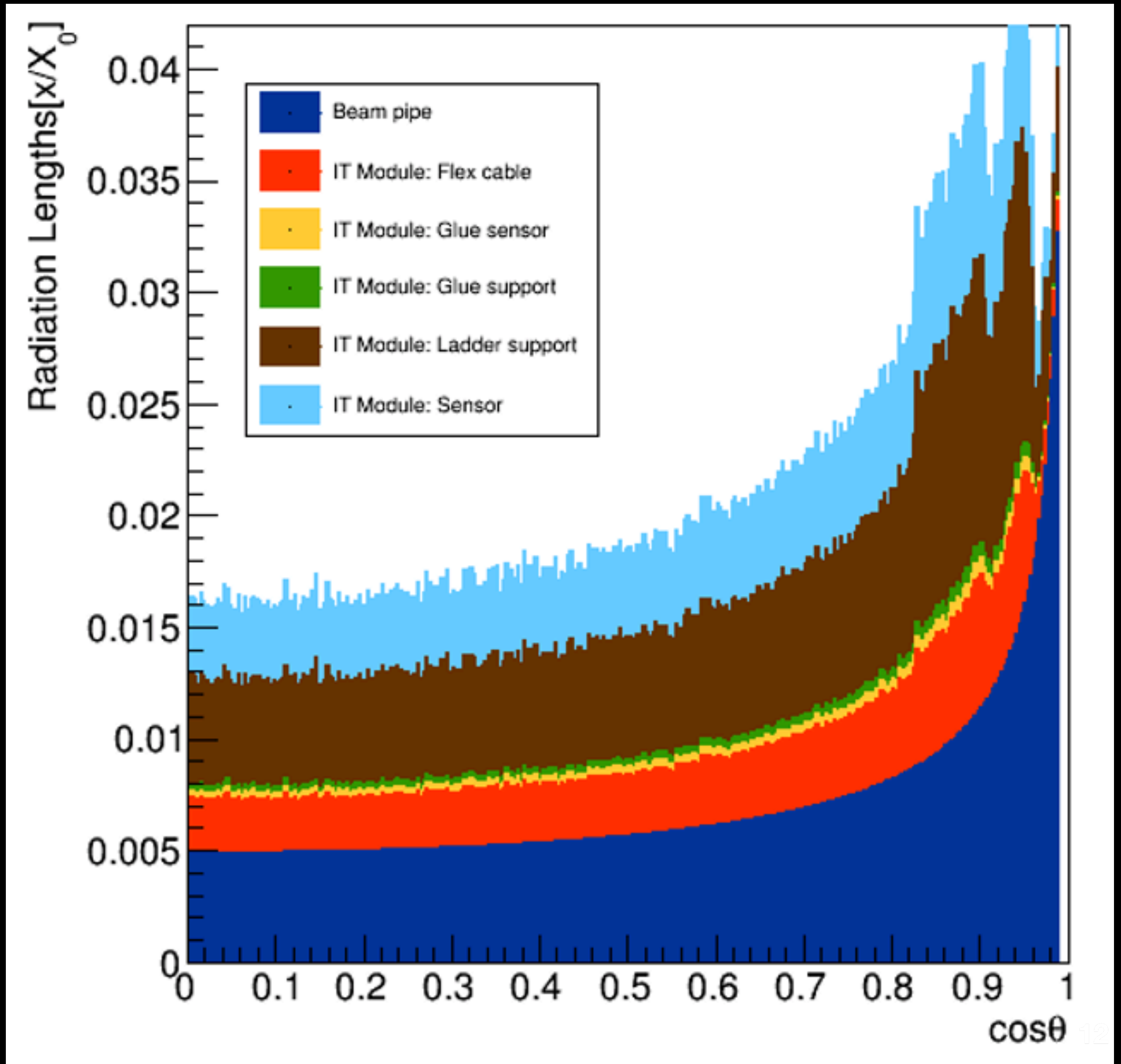
Finite elements analysis

Max def. under full load: 5.3 um



Conventional carbon fiber 0.15mm (1 layer)

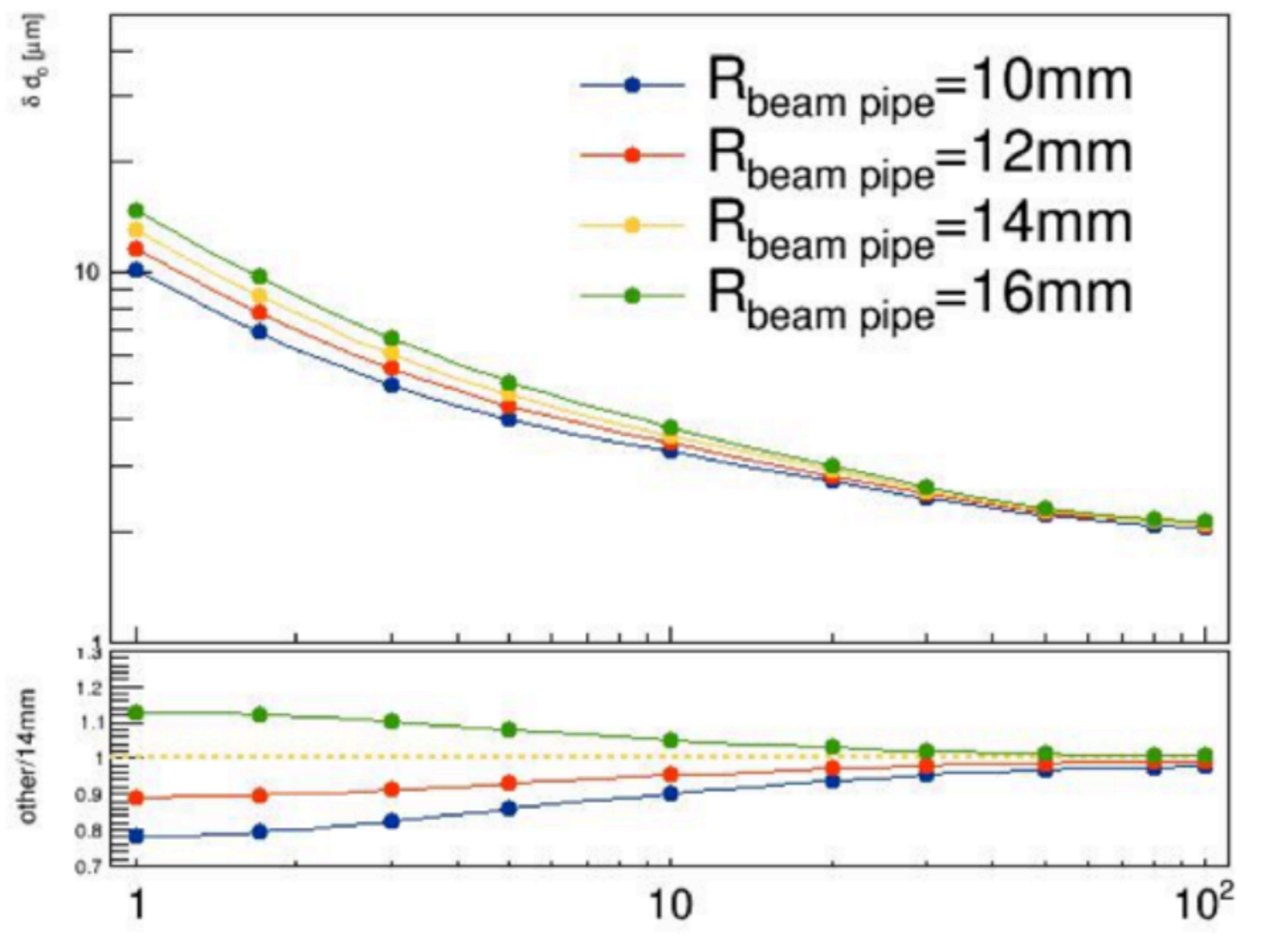
Flexible PCB prototype



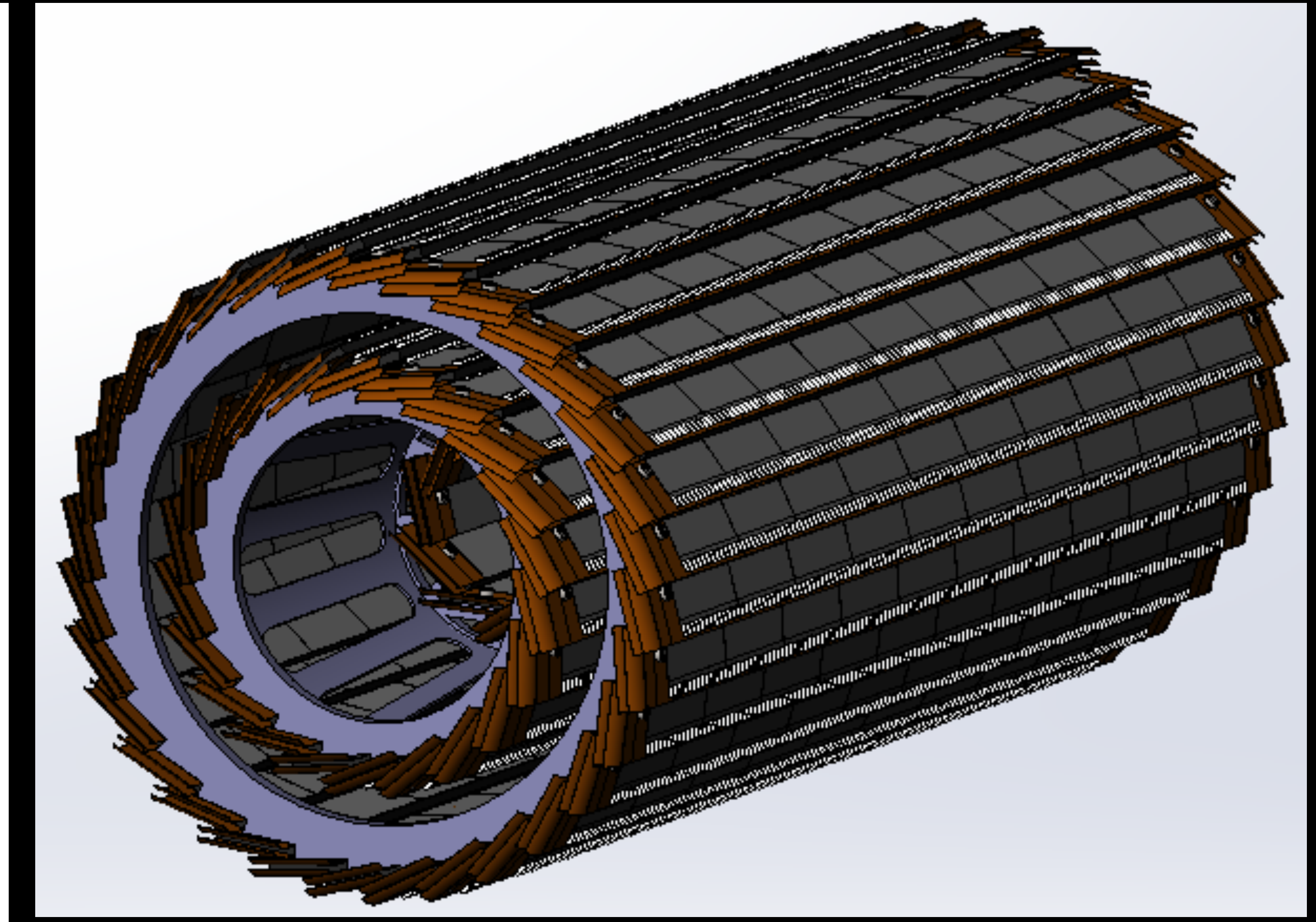
Vertex Detector Prototype R & D

- Completed preliminary version of detector engineering design
  - 3 double layer barrel design
  - 10 modules in inner layer, 22 modules in 2nd layer, 32 modules in outer layer
  - Start thermal design (air cooling)
- Physics simulation to optimize vertex detector layout design.
  - The length of inner layer pixel should be the same as other two layers
  - Inner pixel radius should be as close to beam pipe as possible

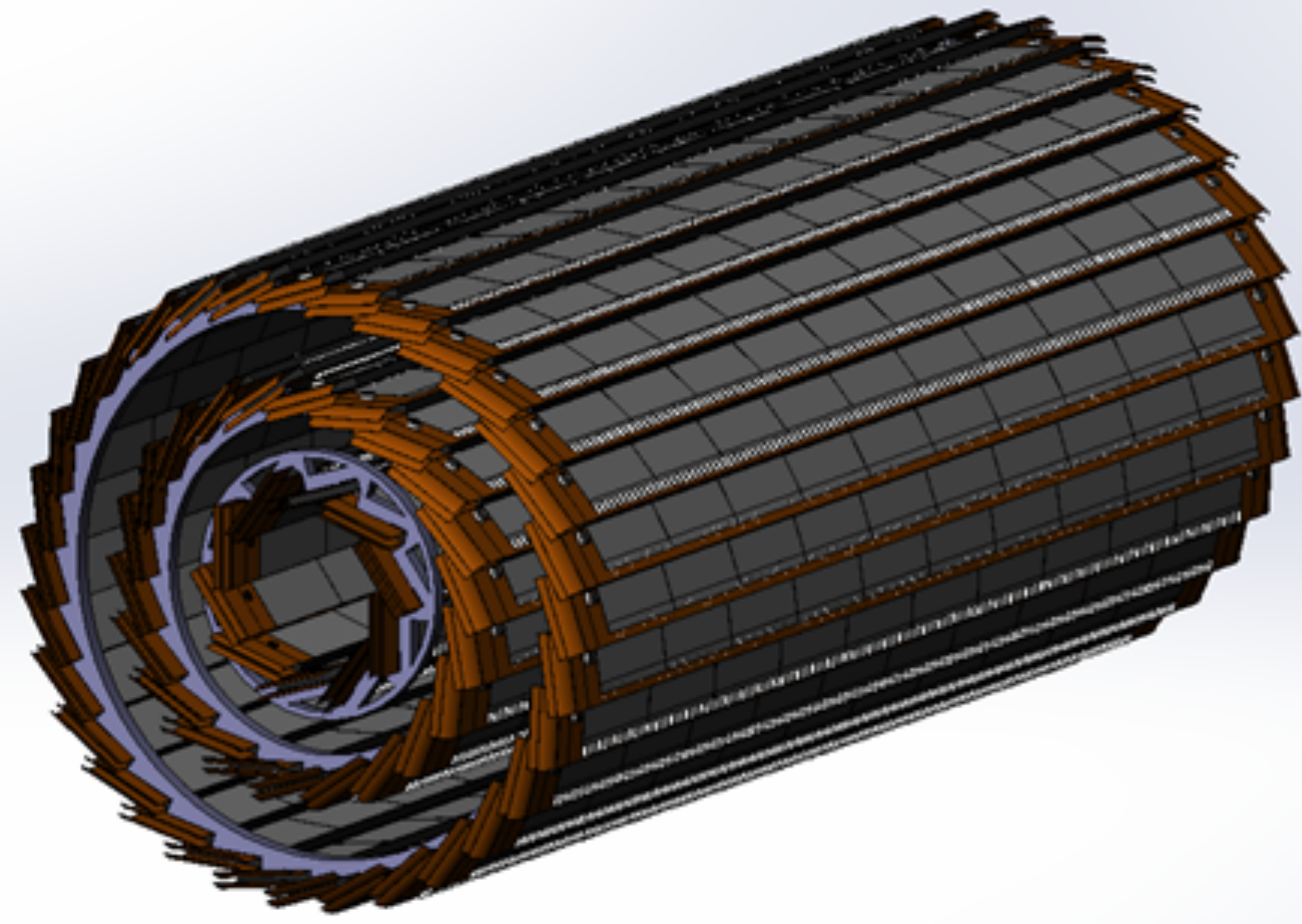
Impact parameter resolution Vs beam pipe radius



Old design



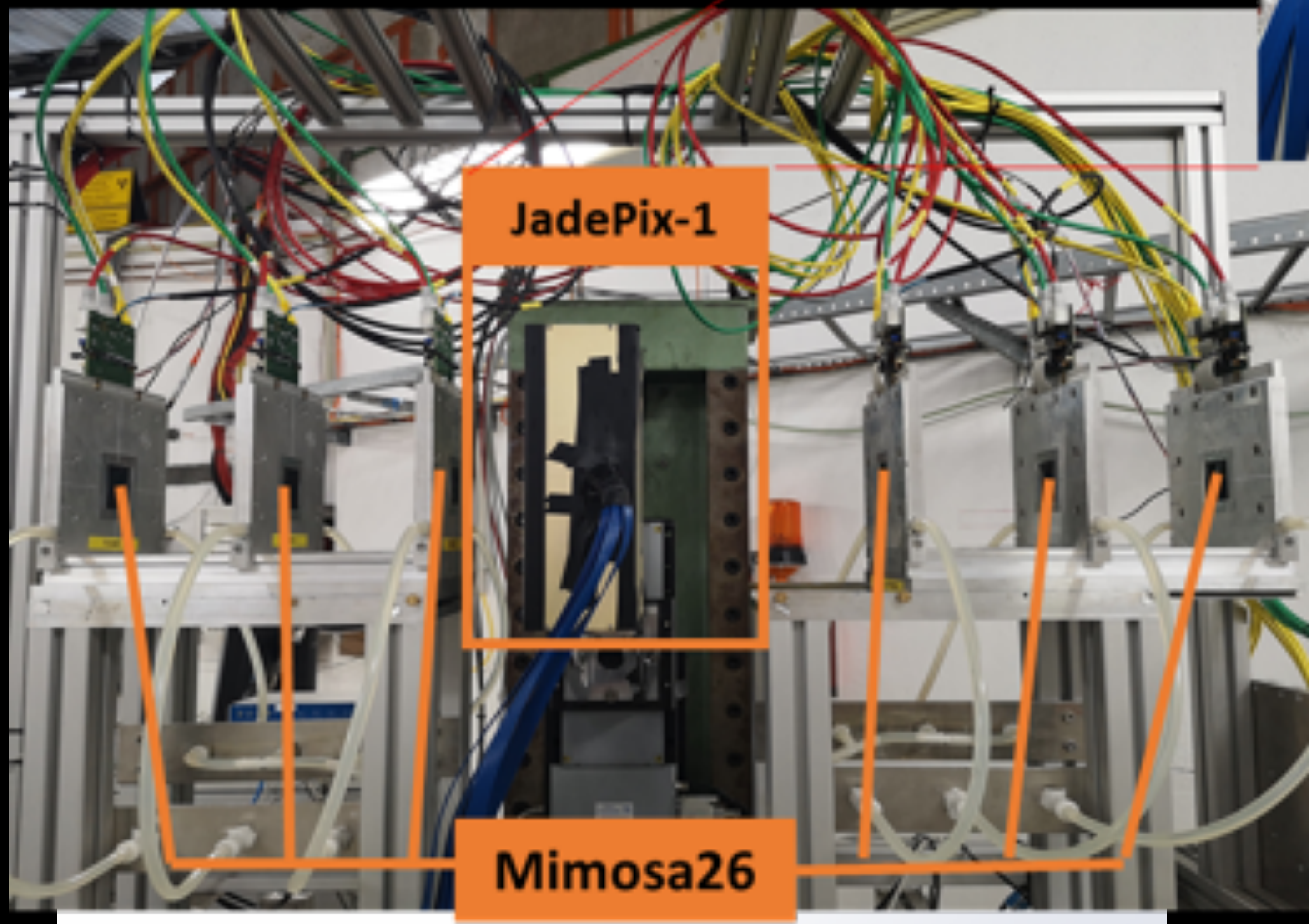
After optimization

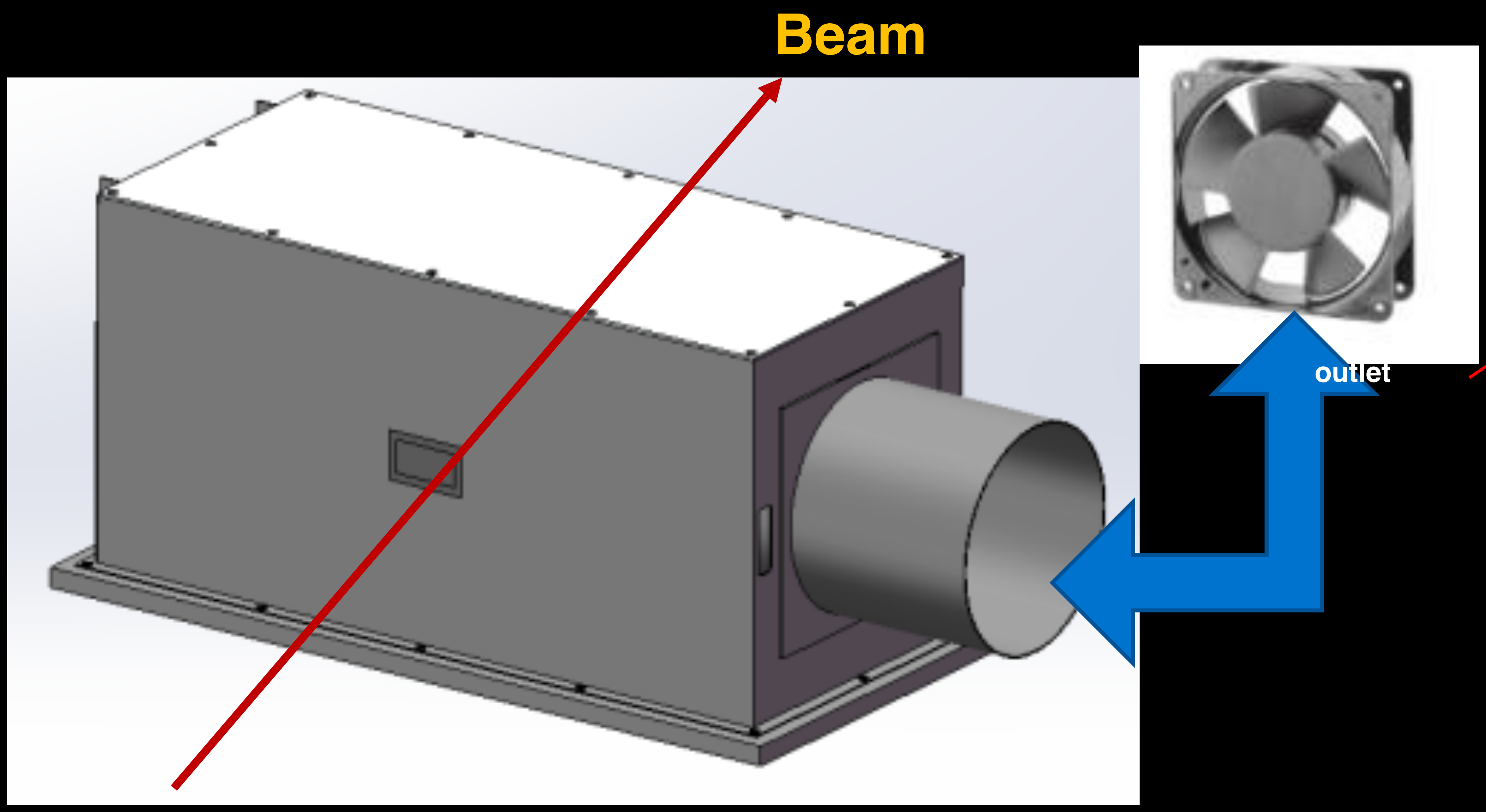


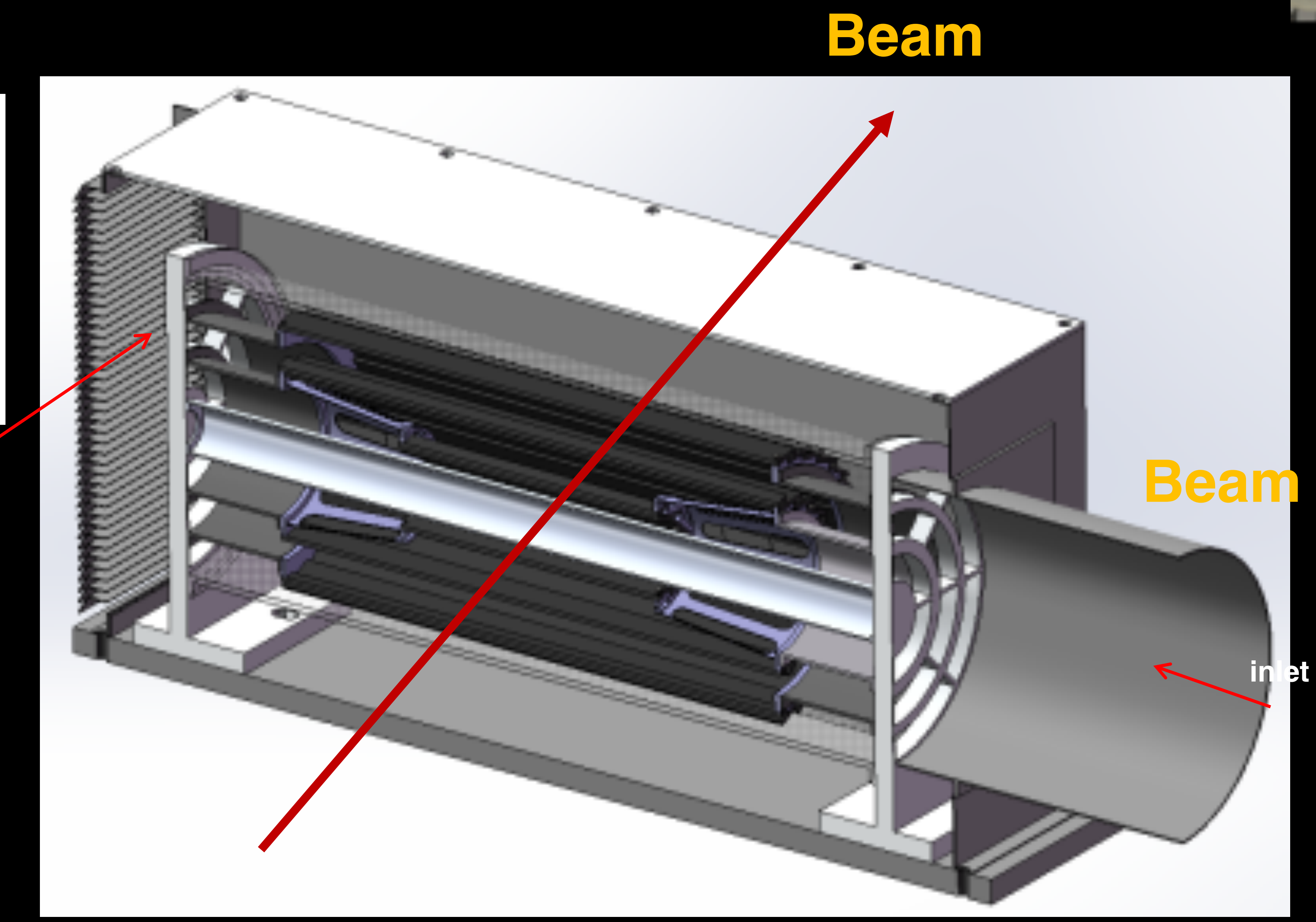
Plan for test beam

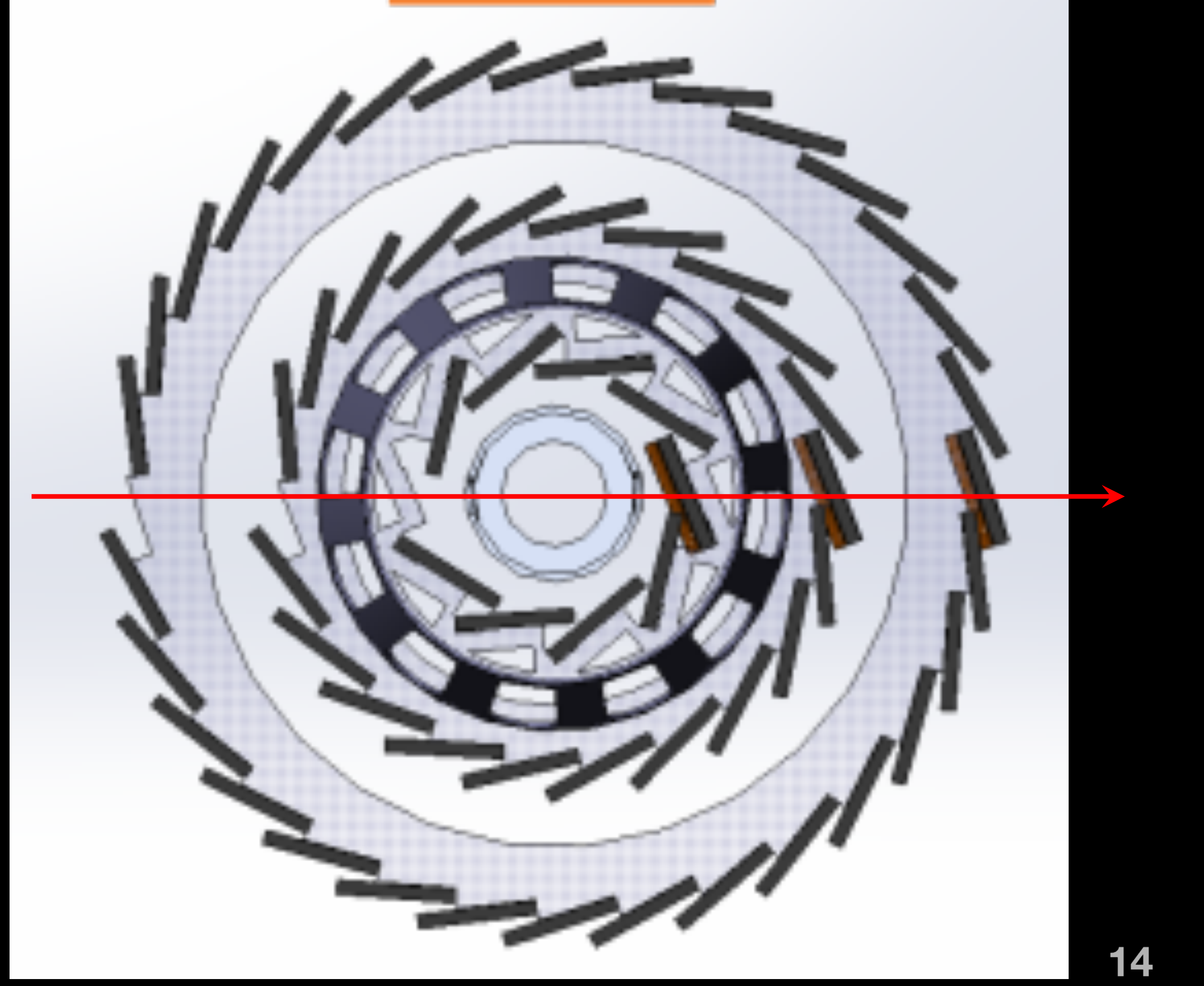
- Expect to perform beam test in DESY(3 - 7GeV electron beams)
  - IHEP test beam facility as backup plan (a few hundreds MeV electrons)
- Enclosure for detector with air cooling is developed for beam test
  - Beam is shooting at one sectors of vertex detectors

DESY test beam



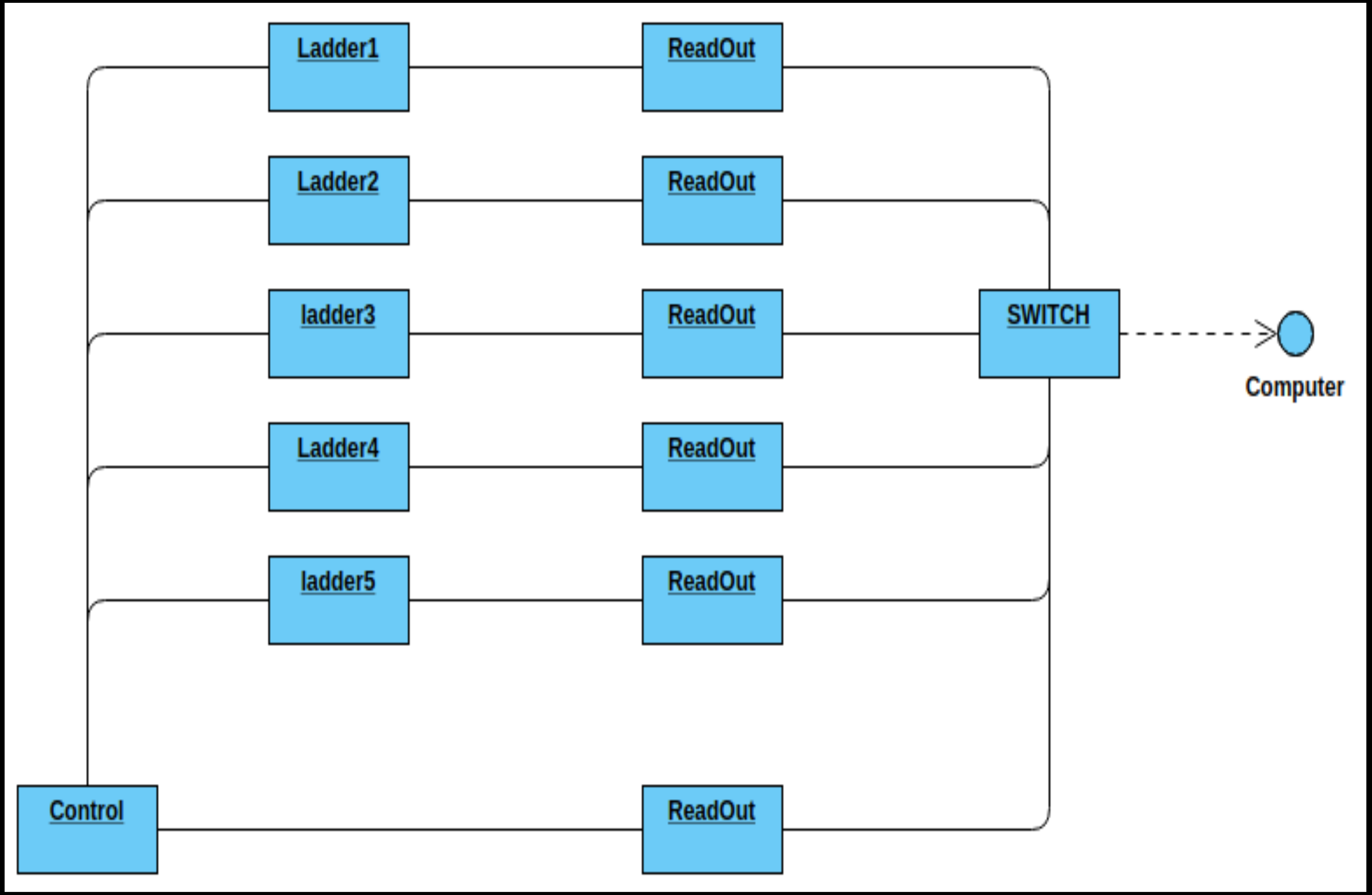






Data acquisition system

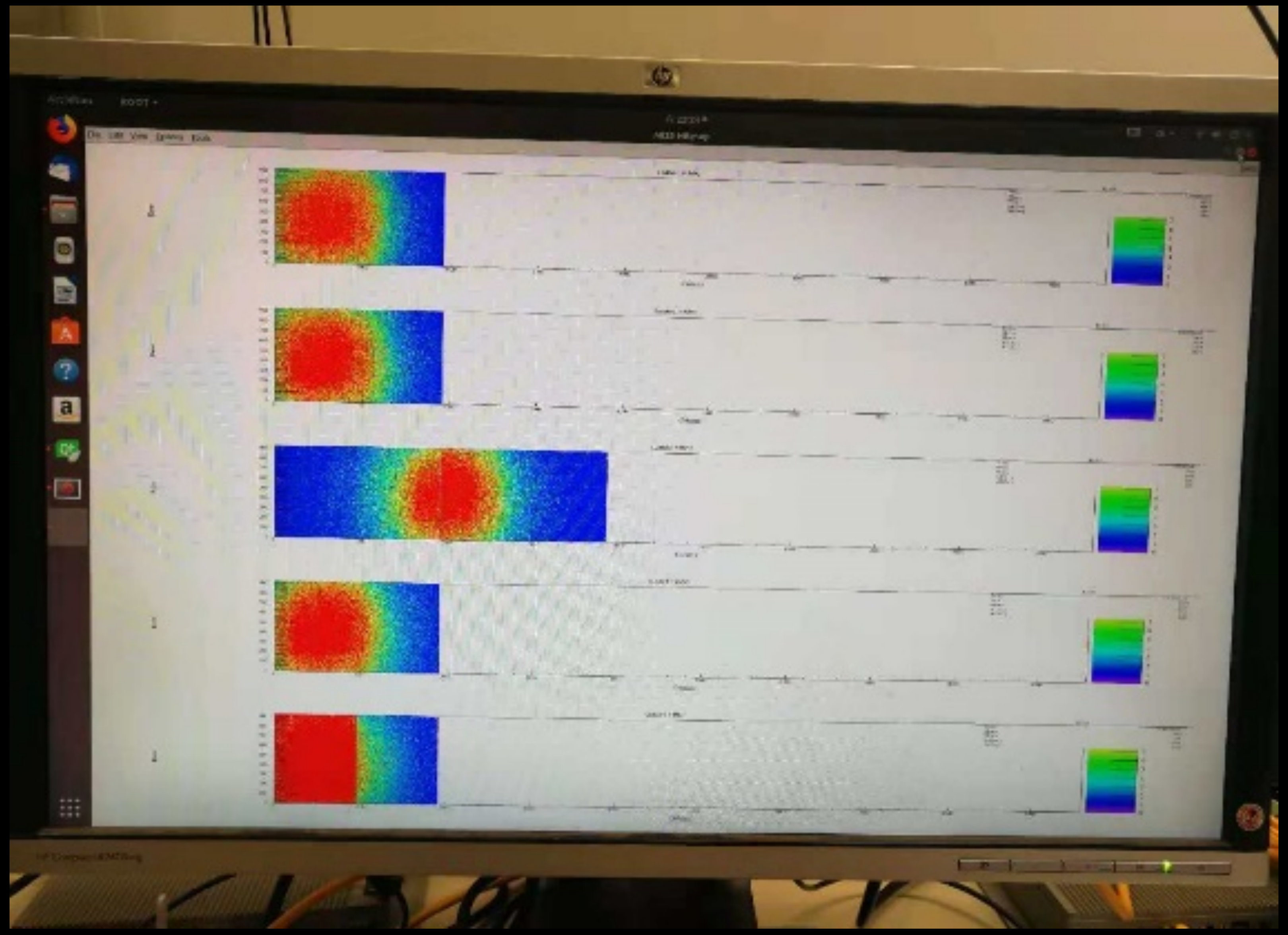
- Preliminary design of data acquisition system(DAQ)
  - Ladders are reader by readout boards
  - All readout boards connected to computer through a switch
  - User interface developed
  - DAQ tested in five modules equipped with MIMOSA sensors



Ladder1
ReadOut
Ladder2
ReadOut
ladder3
ReadOut
SWITCH
Computer
Ladder4
ReadOut
ladder5
ReadOut
Control
ReadOut

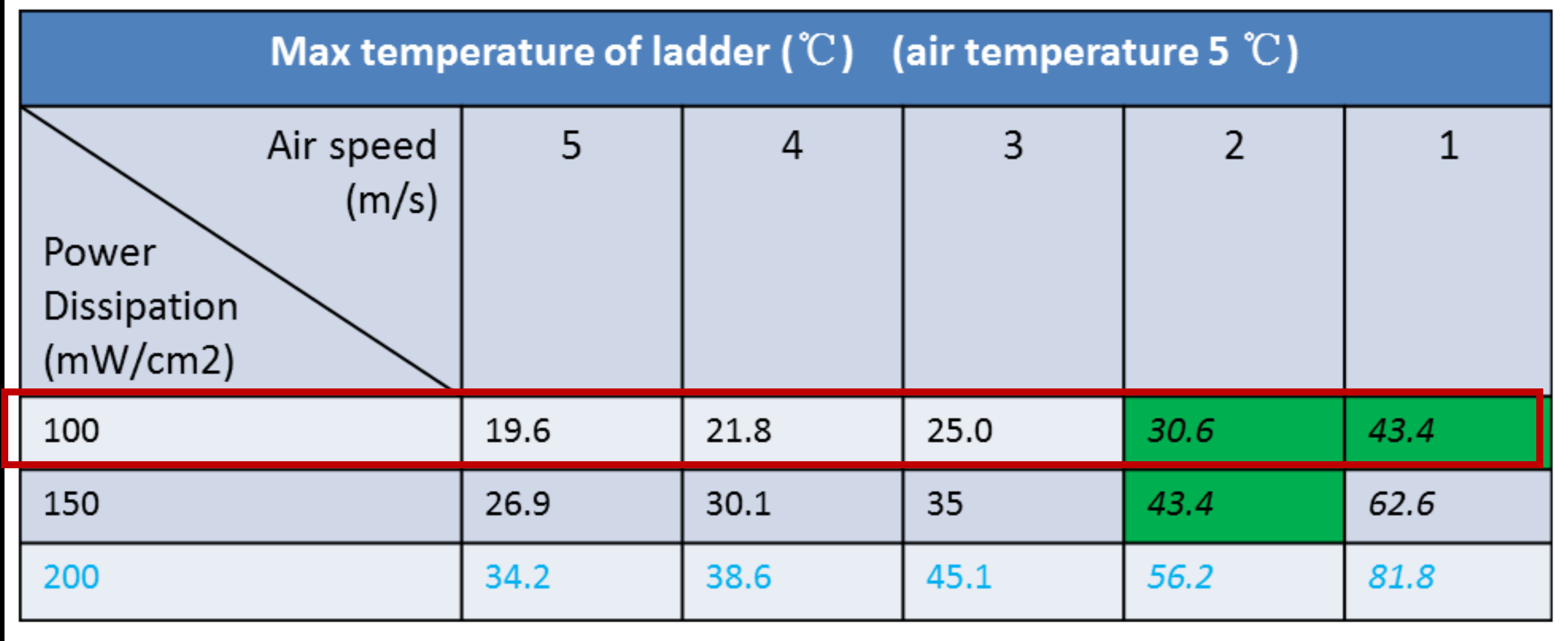
DAQ Tests with 5 MIMOSA chips

DAQ system data display
Tested with MIMOSA modules



Cooling design

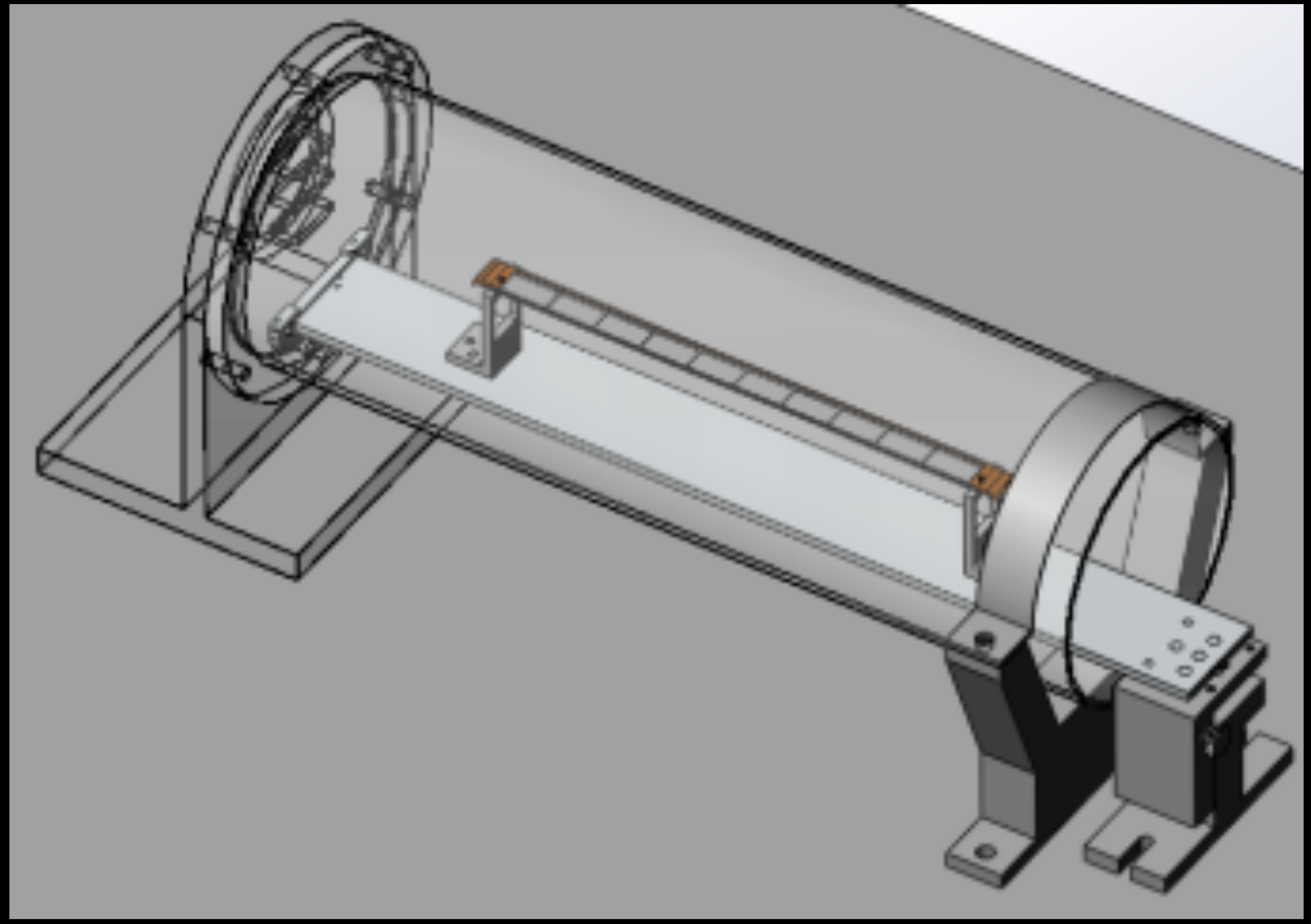
- **Air cooling is baseline design for CEPC vertex detector**
- **Sensor Power dissipation:**
  - Taichupix : $\leq 100\ \mathrm{mW/cm^2}$. (trigger mode)
  - CEPC final goal : $\leq 50\ \mathrm{mW/cm^2}$
- Cooling simulations of a single complete ladder with detailed FPC were done.
  - Need 2 m/s air flow to cool down the ladder to 30 °C
  - Testbench setup has been designed for air cooling , vibration …



Max temperature of ladder (℃) (air temperature 5 ℃)

Air speed (m/s) / Power Dissipation (mW/cm2)	5	4	3	2	1
100	19.6	21.8	25.0	*30.6*	*43.4*
150	26.9	30.1	35	*43.4*	*62.6*
200	34.2	38.6	45.1	*56.2*	*81.8*

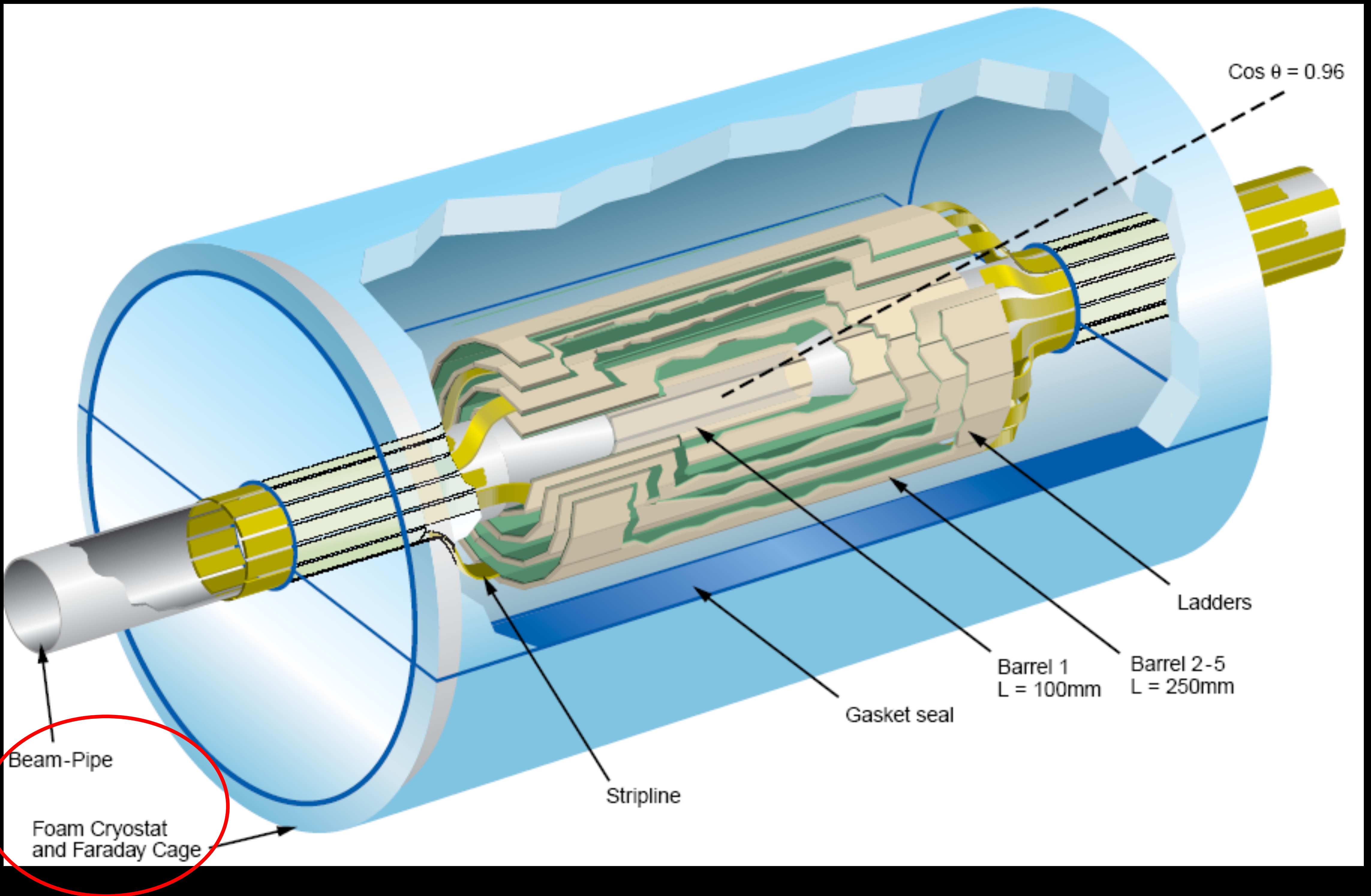
Test setup for ladder cooling
Use compressed air for cooling



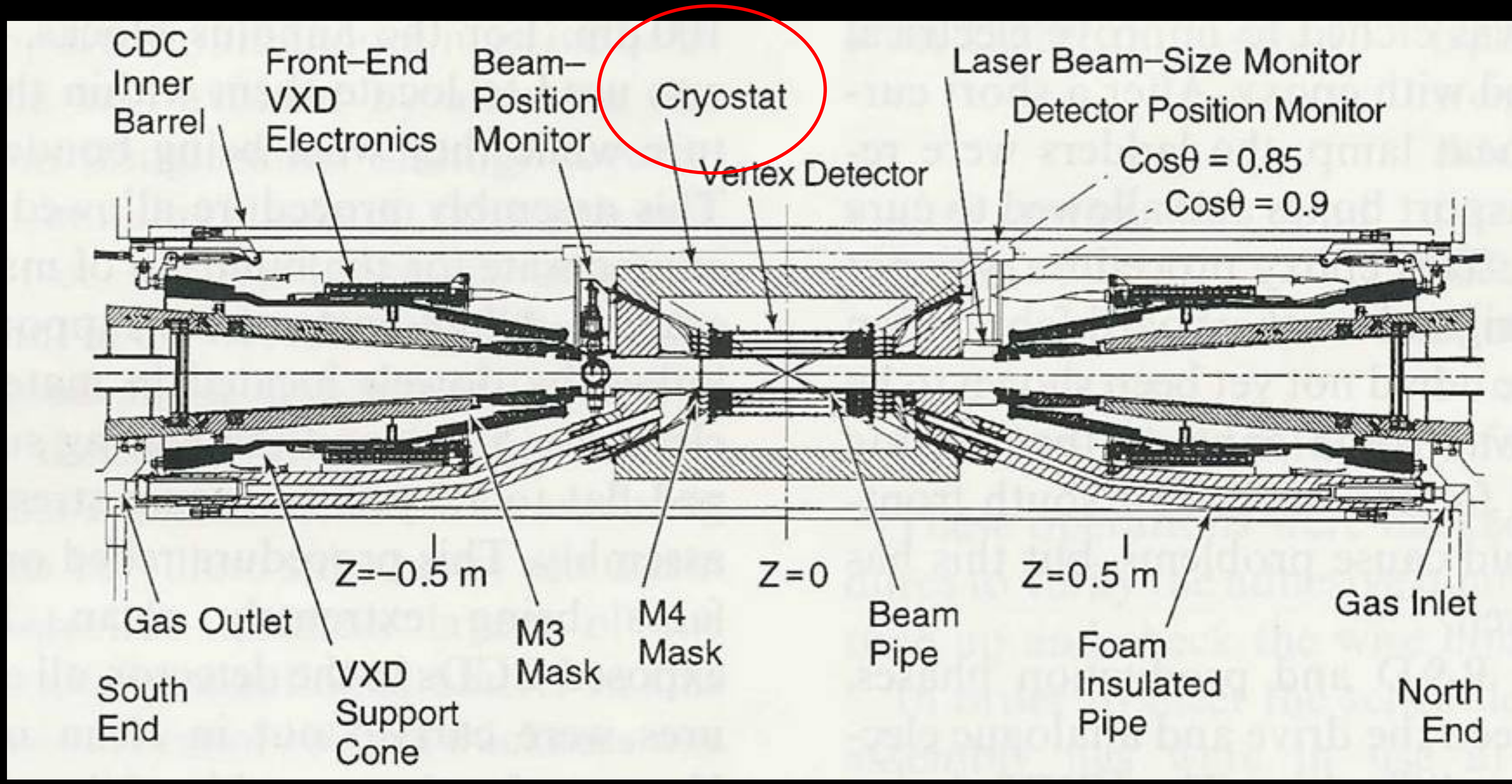
Cooling design

- Liquid nitrogen cooling design will needed to be considered.

SID vertex detector

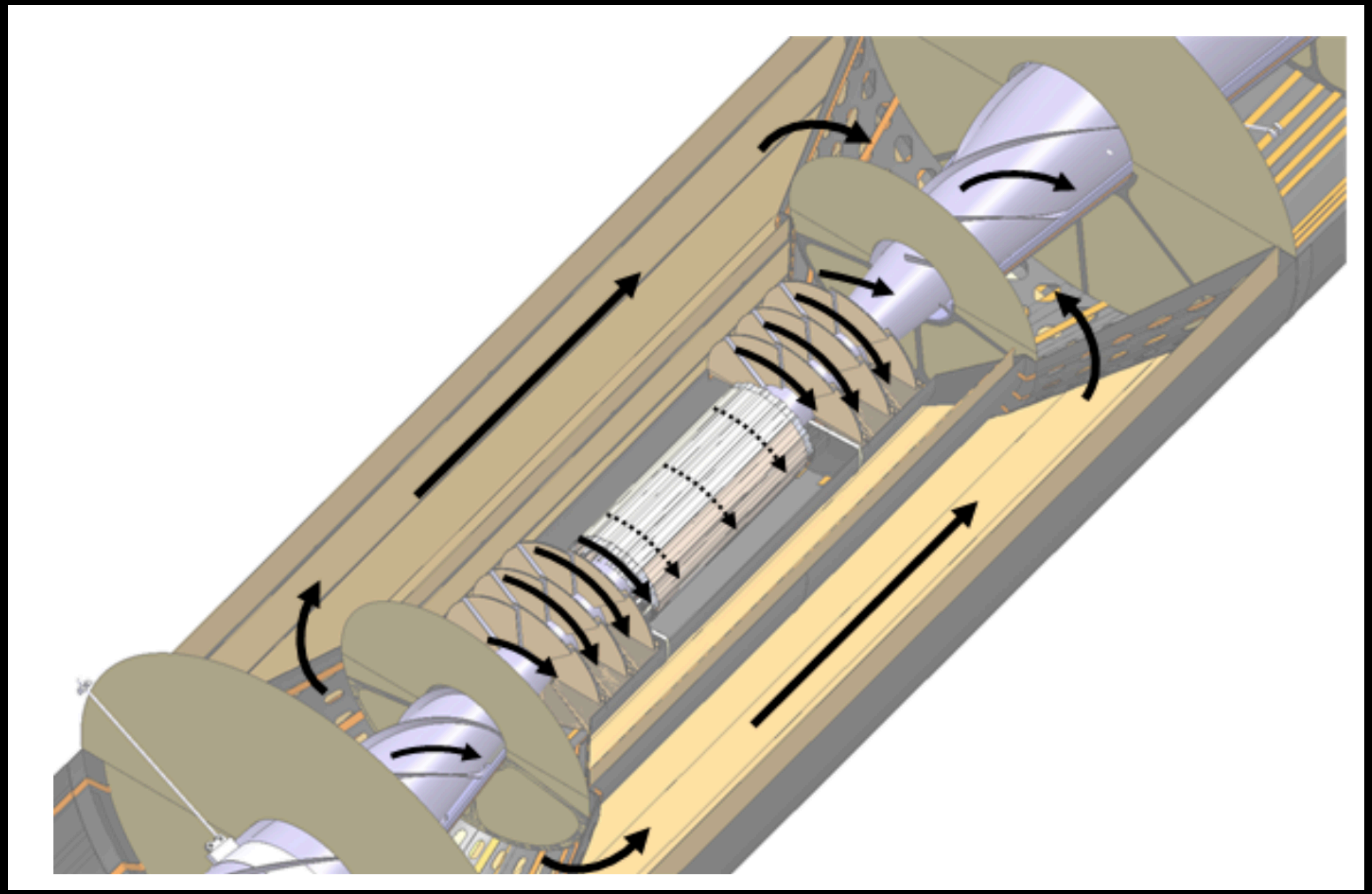


SLAC SLD vertex detector in MDI

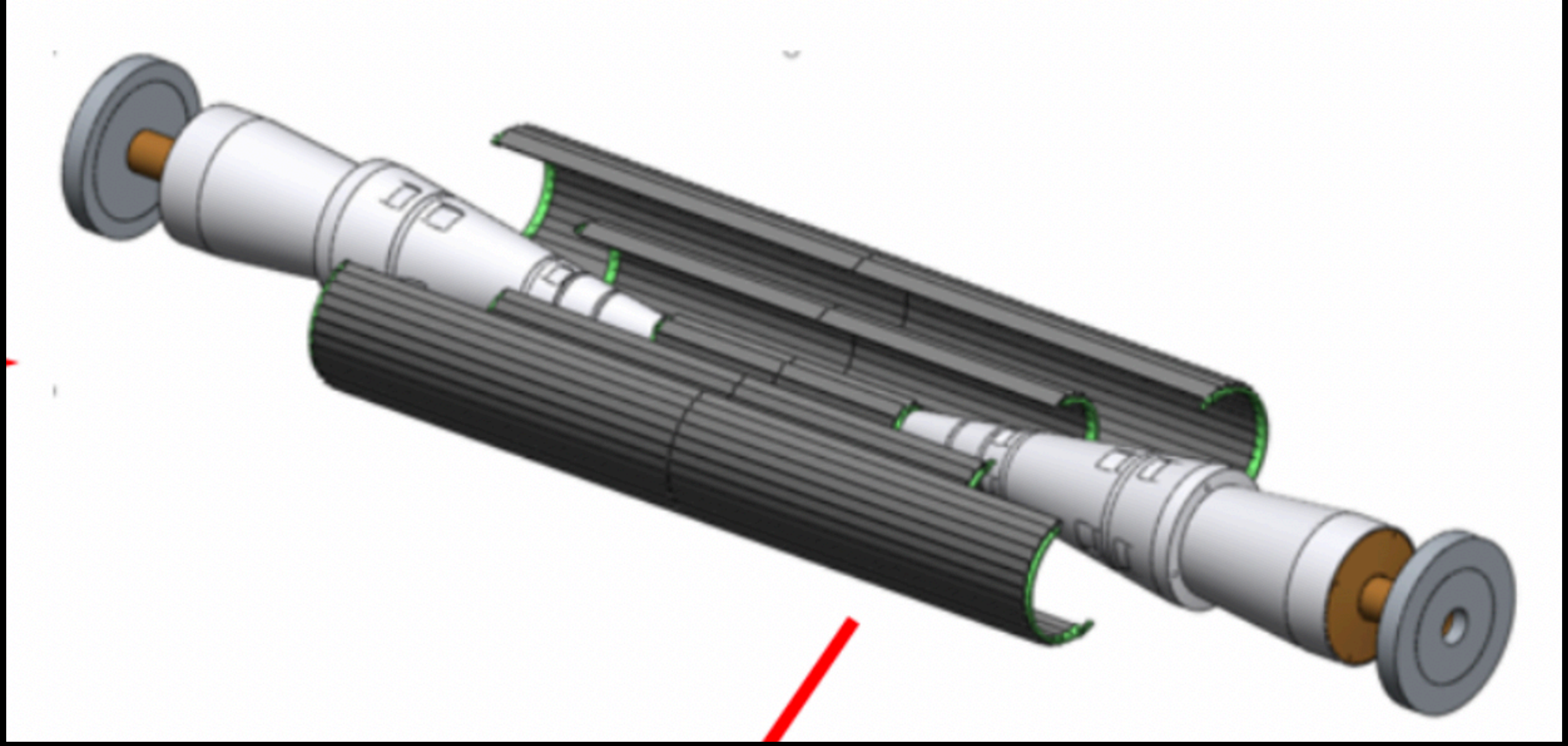


Layout design

- Long barrel design vs Short Barrel +disk
-



Long Barrel 3D model by Quan



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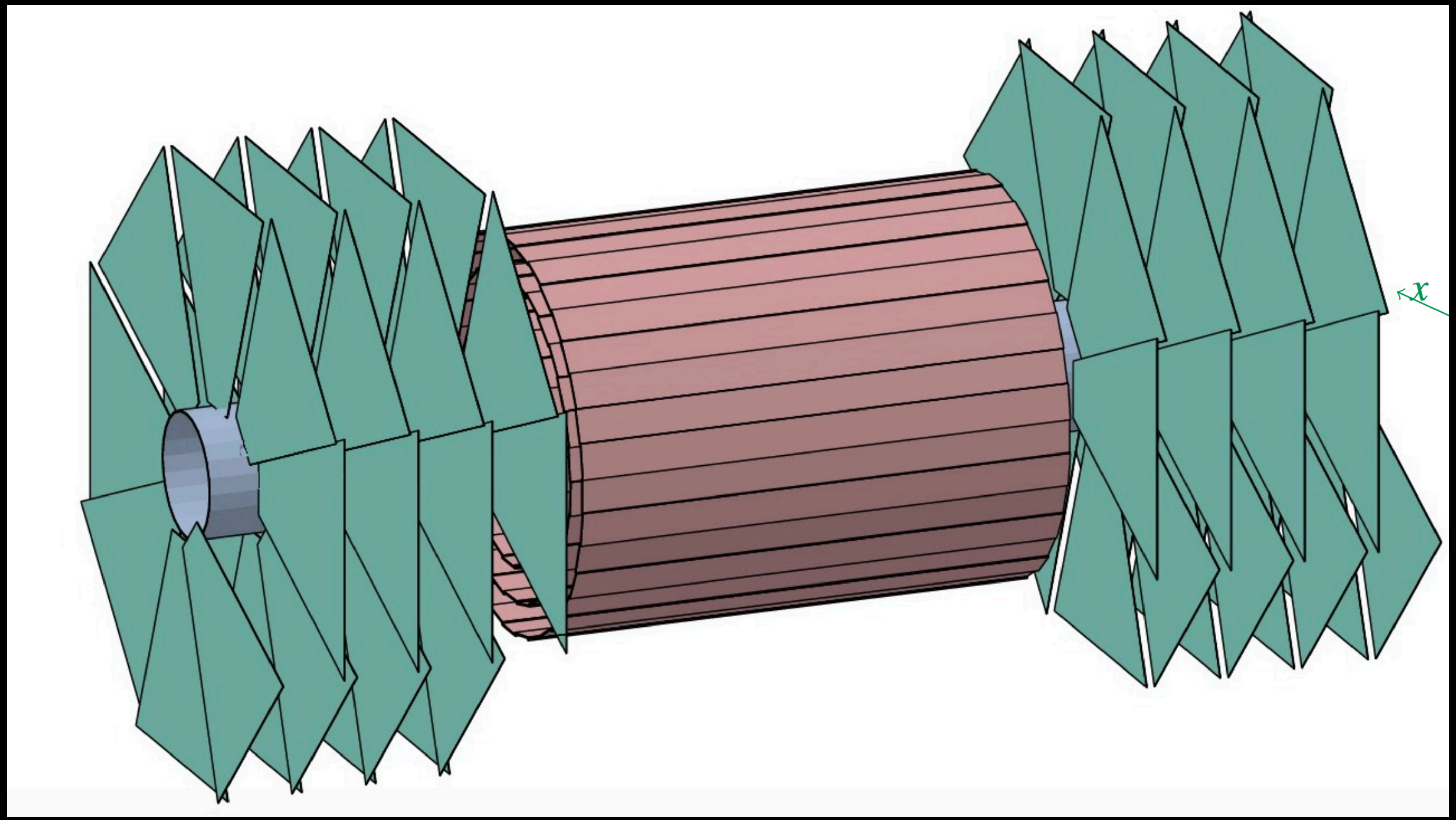
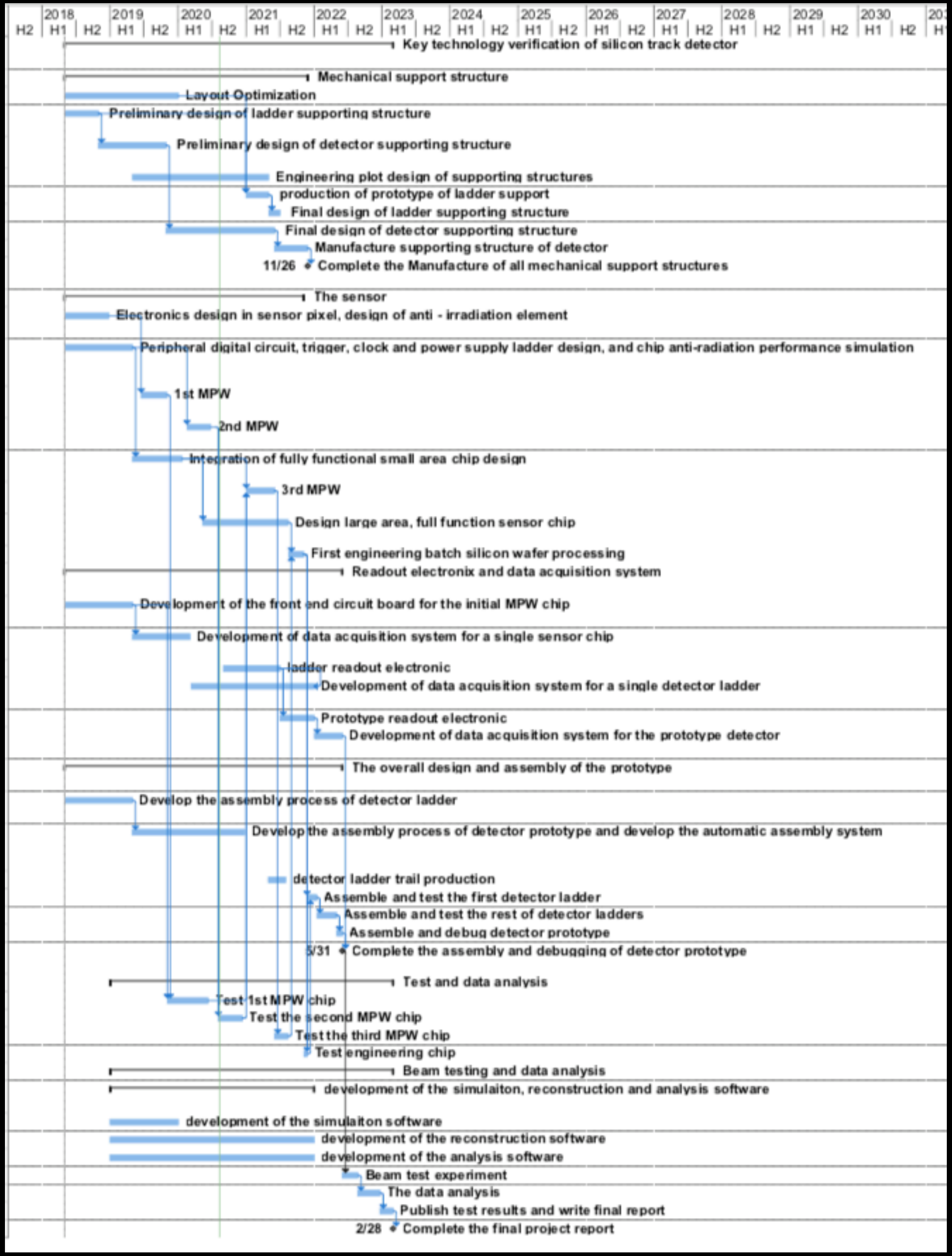


Future plan

- 3rd Year:
  - 3rd CMOS sensor fabricated and tested

    → may be skipped if 2nd MPW chip is fully working
  - Final support structure engineering design completed
  - Fabricated support structure for ladders
- 4th Year:
  - Competed R & D large area sensor
  - Manufactured the support structure for whole detector
  - Assembling and installing the detector prototype
  - Completed DAQ system for whole detector
- 5th Year:
  - Completed detector assembly and commissioning
  - Test beam and data analysis
  - Finish assembling of prototype



International collaboration

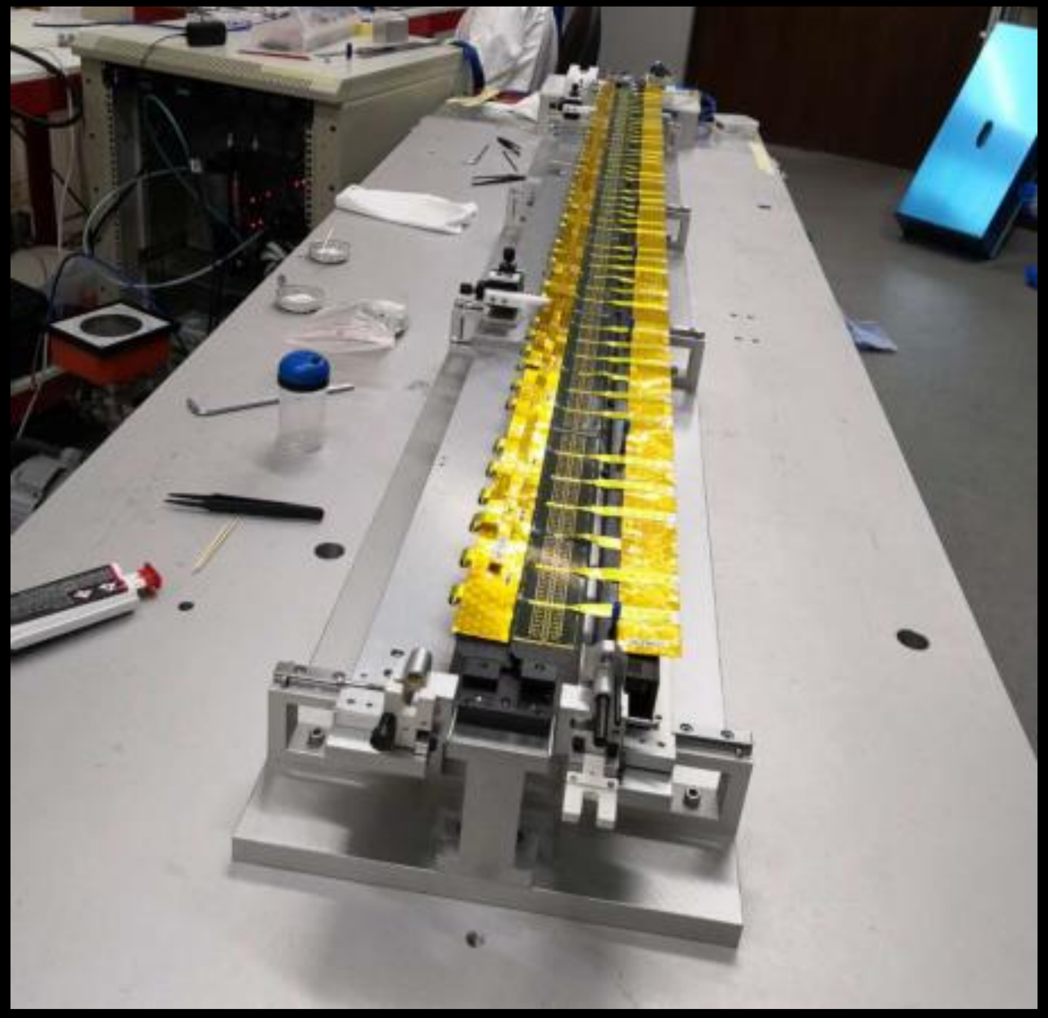
- **IFAE(Spain): very active in CMOS Sensor design and testing**
- Liverpool (UK): Tracker mechanical design,
- Oxford(UK): CMOS sensor design validation, thermal design
- RAL(UK): Pixel module design
- Queen Mary(UK): module mechanical design (Zero mass concept)
- Strasbourg (FR): CMOS sensor design, Tracker mechanical design
- University of Massachusetts (US): Tracker mechanical design, thermal design

In 2019, we have one engineer visited Oxford and Liverpool for 4 weeks, learned a lots about silicon.

Lab visit in Oxford

Mu3e ladder, Atlas barrel strip stave prototype.

Labs visit in Liverpool



Module of Alice's OB tracker, Advance material Lab

Summary

- Complete preliminary design for the followings
  - Detector module (ladder)
  - Vertex detector overall support structure
  - Data acquisition system
- Strong international connection, large impact to the community if the project success.
- Next major milestones
  - Competed full size full functionality sensors design (3rd year)
  - Manufactured support structure for vertex detector (4th year)
  - Finished detector assembly and commissioning and beam test (5th year)

backup

Mid-term review of MOST2 project

- Midterm review meeting (Aug 20-21)

国家重点研发计划“高能环形正负电子对撞机关键技术研发与验证”项目

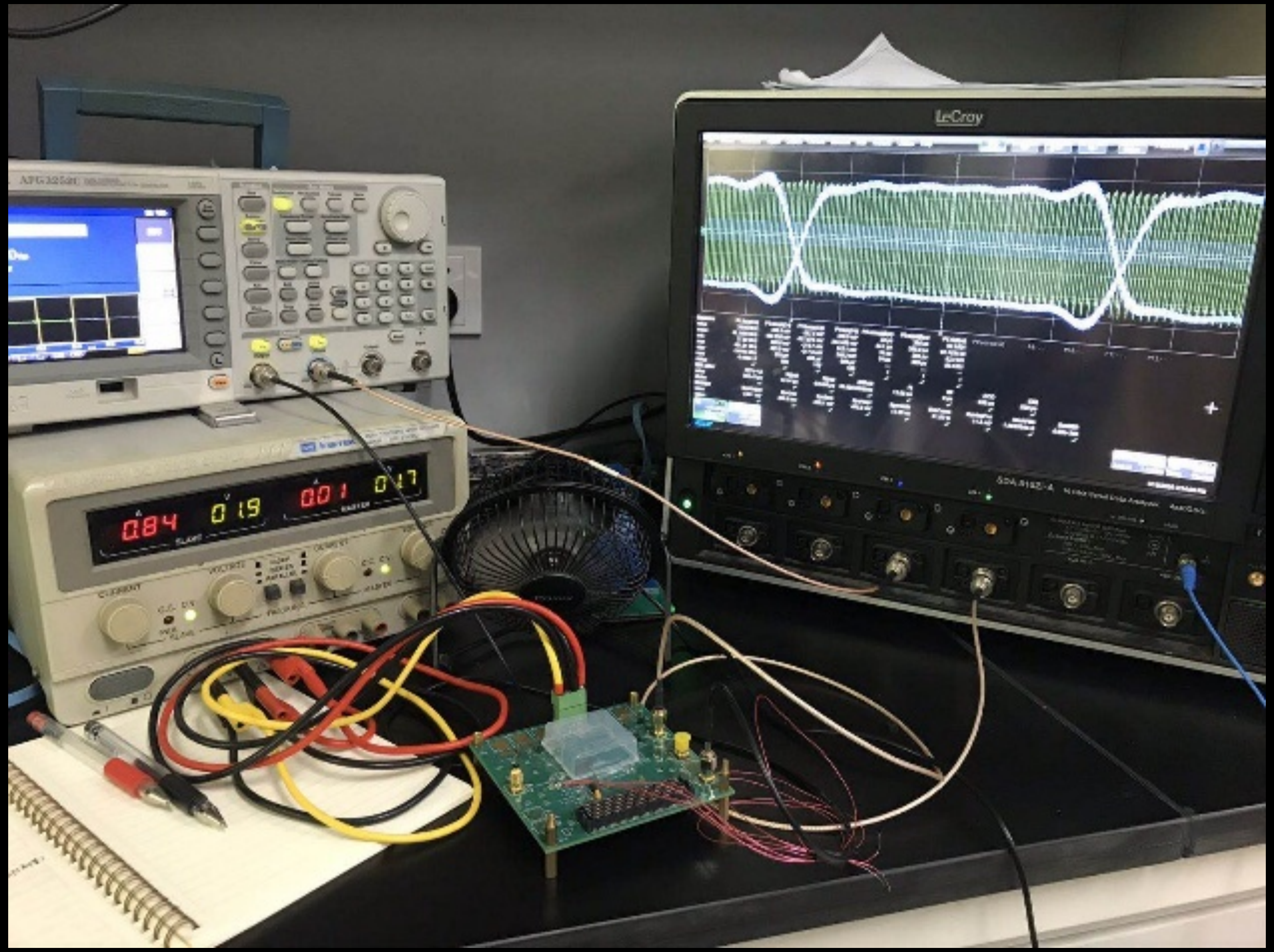
中期自查会议

2020.08.20-21, IHEP

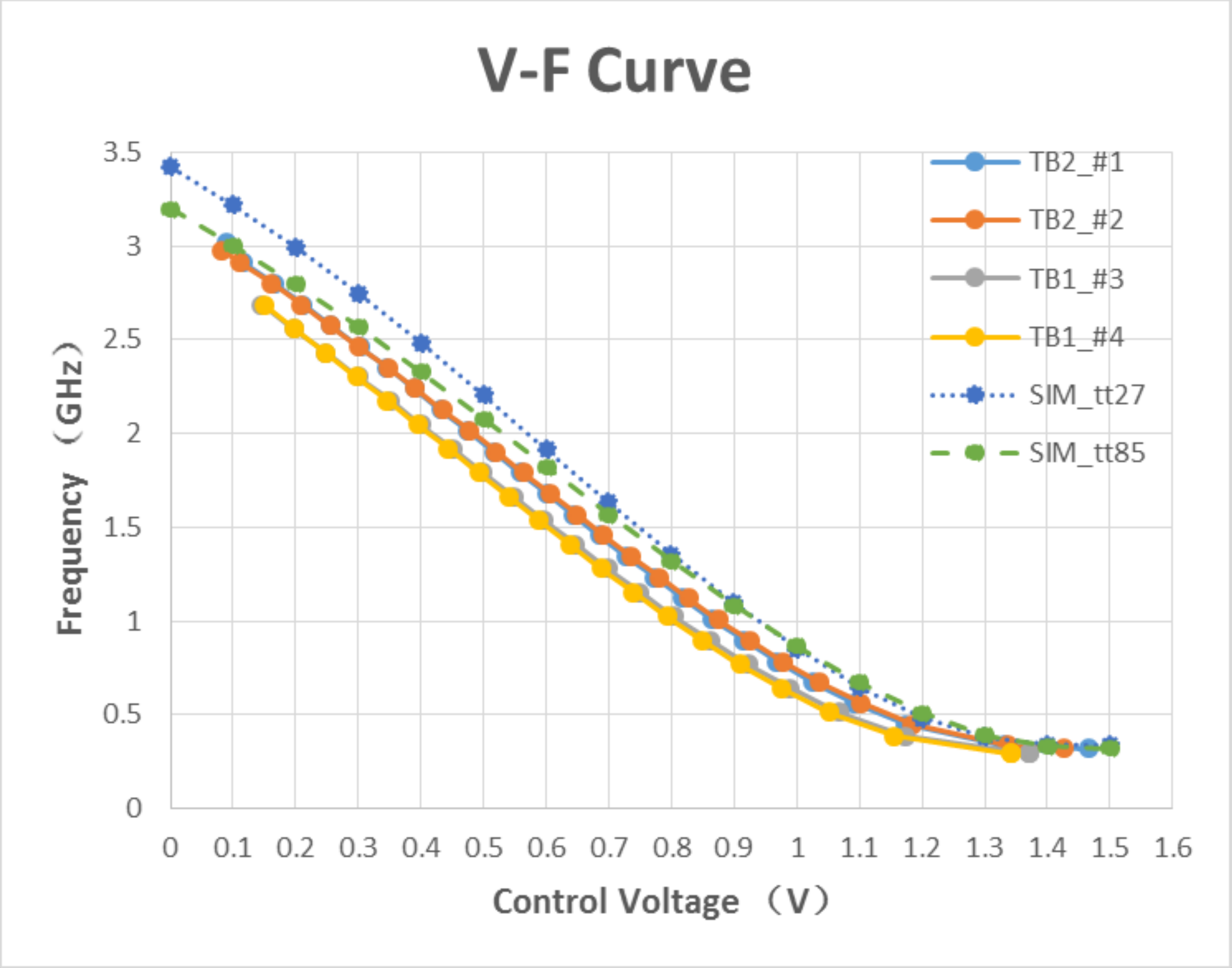
Mid-term review of MOST2 project

- Comments from review:
  - This topic is a cutting-edge technology of high-energy particle detection,
  - Good progress of the project
  - Suggestion:
    - Check uniformity of the sensors
    - Should try to further reduce the power consumption
    - Should start testing radiation hardness of the sensor chip
    - Should pay more attention to mechanical support, air cooling , power consumption
    - → related to spatial resolution of vertex detector prototype
    - This project may be short of funding at the end, suggest to give more support

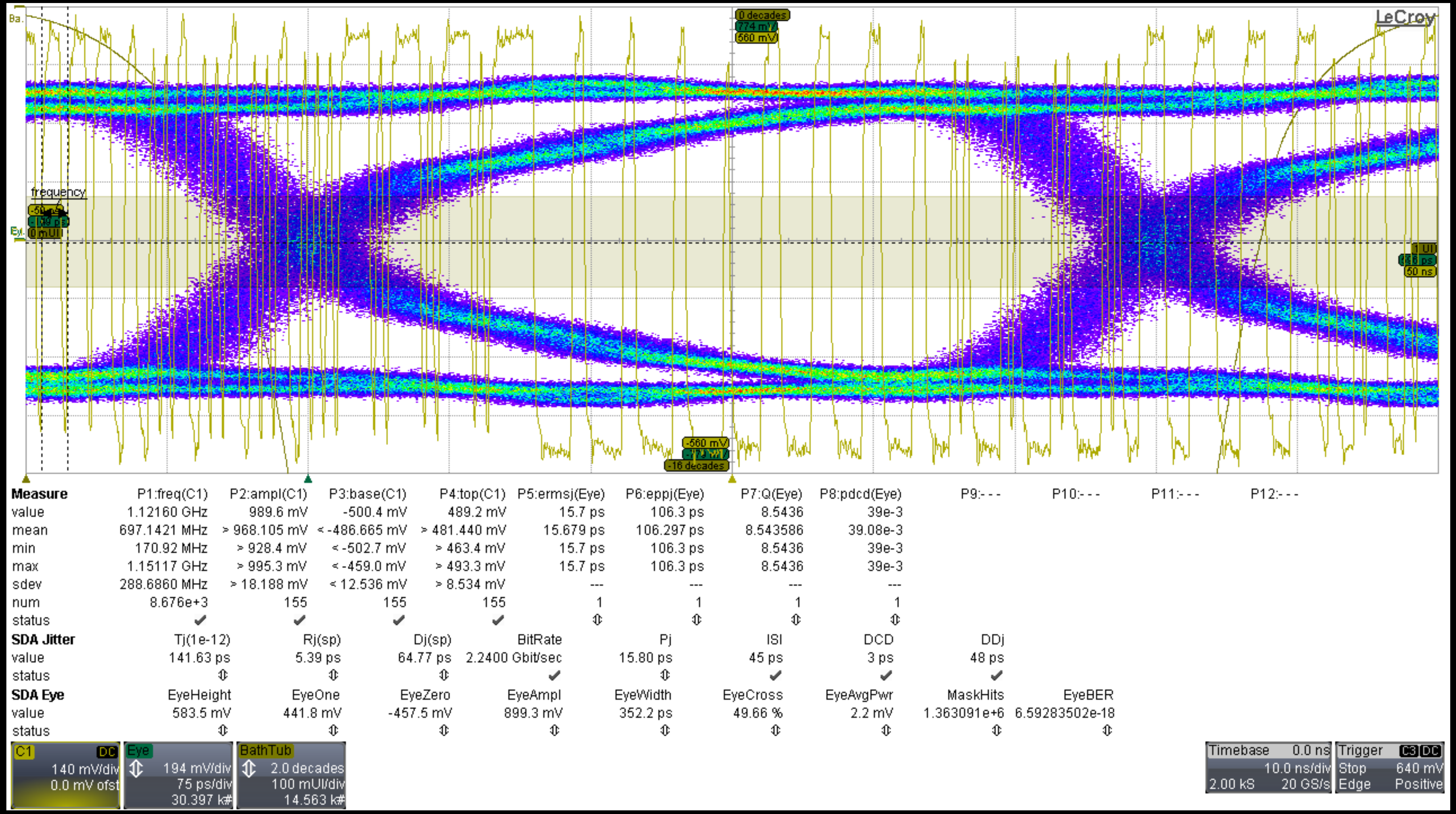
PLL and Serializer Testing



- PLL and the serializer was thoroughly tested and proved
- PLL's tuning range 0.32~2.91GHz agrees with the simulation
- Good and robust eye-diagram observed at 2.24GHz, with the total jitter < 150ps (@ error rate < e^{-12})
- Serializer could run steadily @ 2.24GHz for trigger less mode



Eye-diagram



Measure	P1:freq(C1)	P2:ampl(C1)	P3:base(C1)	P4:top(C1)	P5:ermsj(Eye)	P6:eppj(Eye)	P7:Q(Eye)	P8:pdcd(Eye)	P9:- - -	P10:- - -	P11:- - -	P12:- - -
value	1.12160 GHz	989.6 mV	-500.4 mV	489.2 mV	15.7 ps	106.3 ps	8.5436	39e-3				
mean	697.1421 MHz	> 968.105 mV	< -486.665 mV	> 481.440 mV	15.679 ps	106.297 ps	8.543586	39.08e-3				
min	170.92 MHz	> 928.4 mV	< -502.7 mV	> 463.4 mV	15.7 ps	106.3 ps	8.5436	39e-3				
max	1.15117 GHz	> 995.3 mV	< -459.0 mV	> 493.3 mV	15.7 ps	106.3 ps	8.5436	39e-3				
sdev	288.6860 MHz	> 18.188 mV	< 12.536 mV	> 8.534 mV	---	---	---	---				
num	8.676e+3	155	155	155	1	1	1	1				
status	✓	✓	✓	✓	⇕	⇕	⇕	⇕				

SDA Jitter	Tj(1e-12)	Rj(sp)	Dj(sp)	BitRate	Pj	ISI	DCD	DDj
value	141.63 ps	5.39 ps	64.77 ps	2.2400 Gbit/sec	15.80 ps	45 ps	3 ps	48 ps
status	⇕	⇕	⇕	✓	⇕	✓	✓	✓

SDA Eye	EyeHeight	EyeOne	EyeZero	EyeAmpl	EyeWidth	EyeCross	EyeAvgPwr	MaskHits	EyeBER
value	583.5 mV	441.8 mV	-457.5 mV	899.3 mV	352.2 ps	49.66 %	2.2 mV	1.363091e+6	6.59283502e-18
status	⇕	⇕	⇕	⇕	⇕	⇕	⇕	⇕	⇕

C1 DC 140 mV/div 0.0 mV ofst

Eye 194 mV/div 75 ps/div 30.397 k#

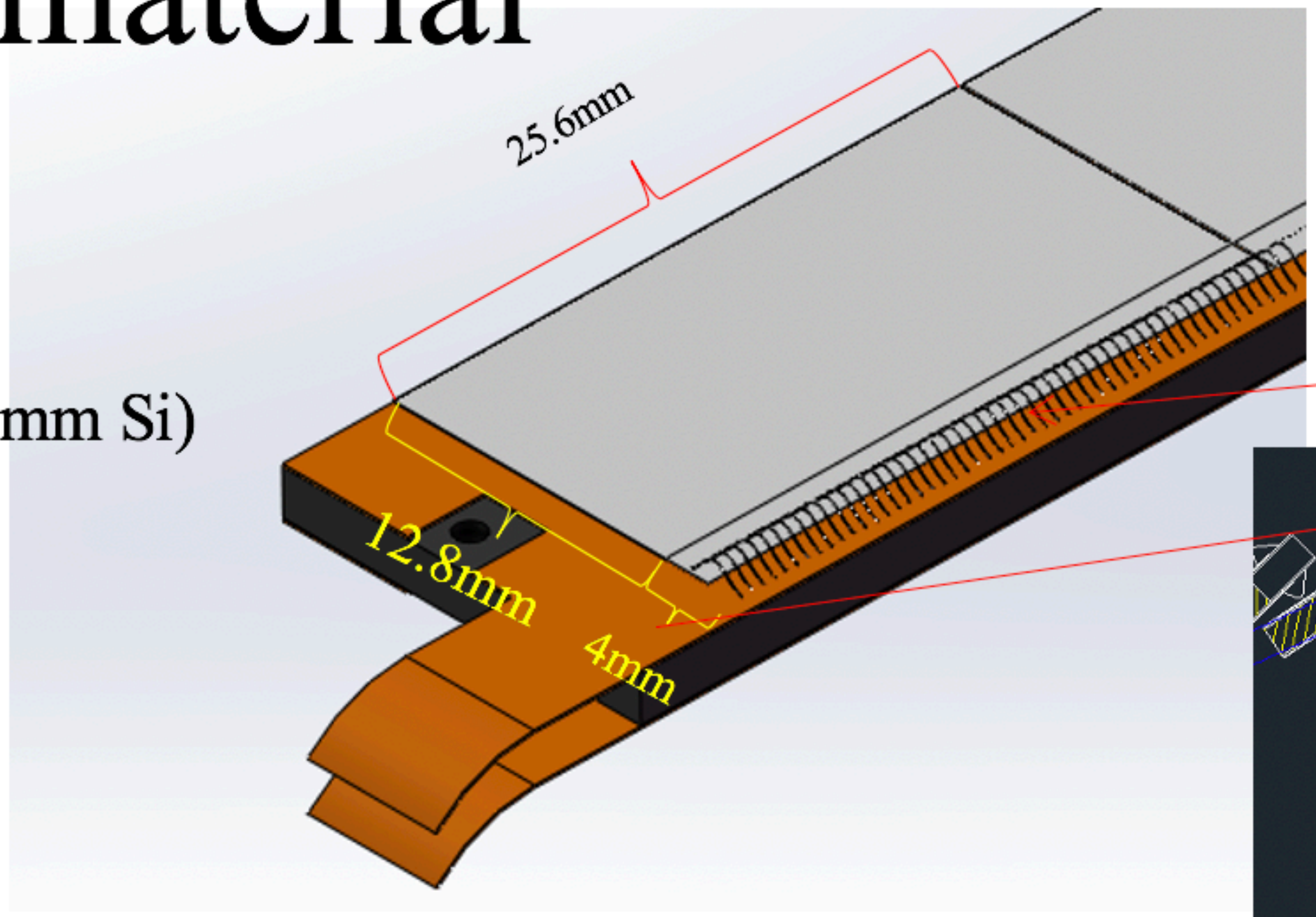
BathTub 2.0 decades 100 mUI/div 14.563 k#

Timebase 0.0 ns 10.0 ns/div 2.00 kS 20 GS/s

Trigger C3 DC Stop 640 mV Edge Positive

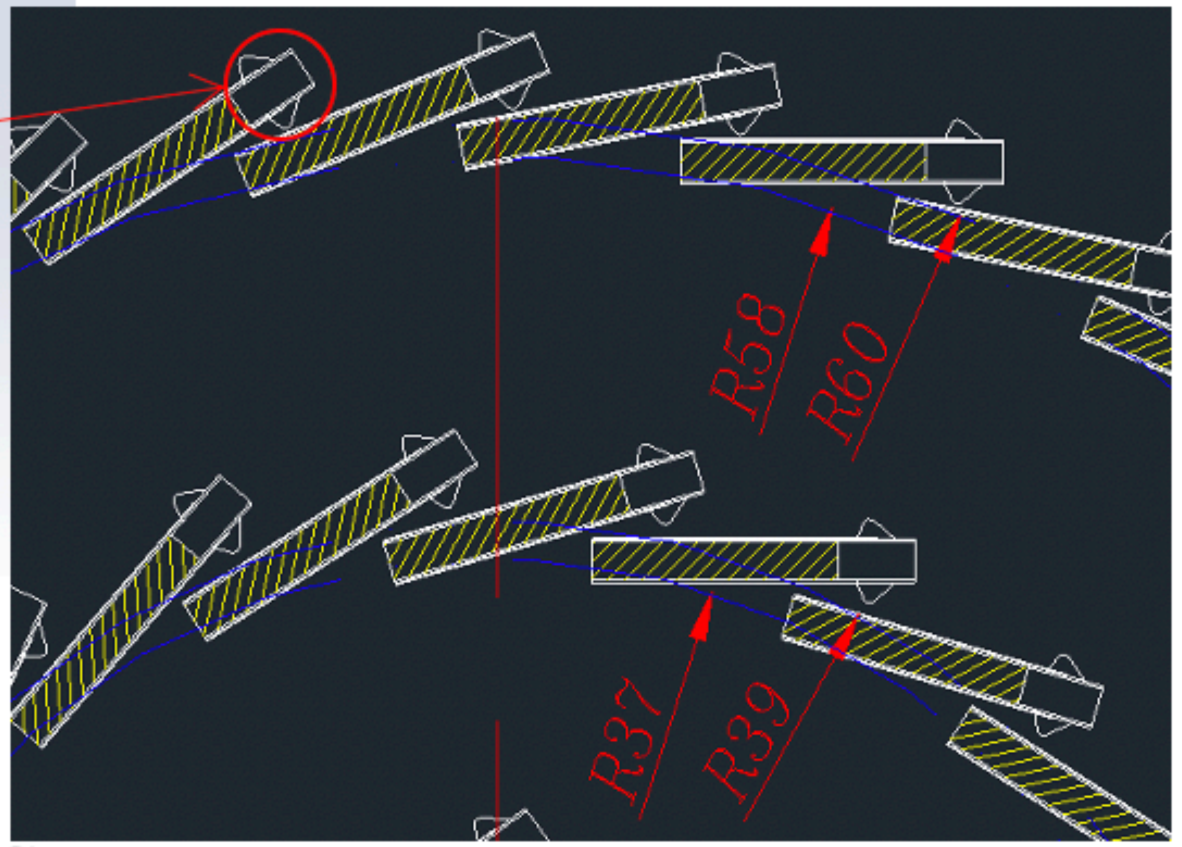
Pixel module material

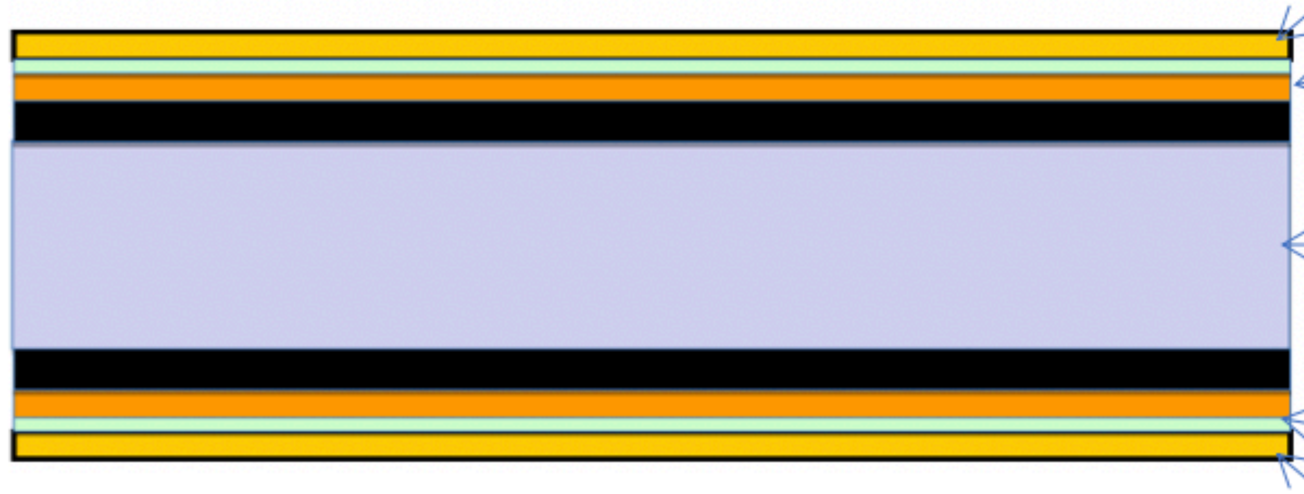
Top view:
active area: 12.8mm × 25.6mm
dead area: 4mm × 25.6mm (only 2mm Si)
Side view:
5 symmetric layer, gluing together.



One half dead area:

Sensor(Si, 25um)
Al wire
glue(Epoxy, 7.5um)
Al(17.8um)
Kapton(50um)
Glue(Epoxy, 15um)
Ladder support(carbon fiber,175um)

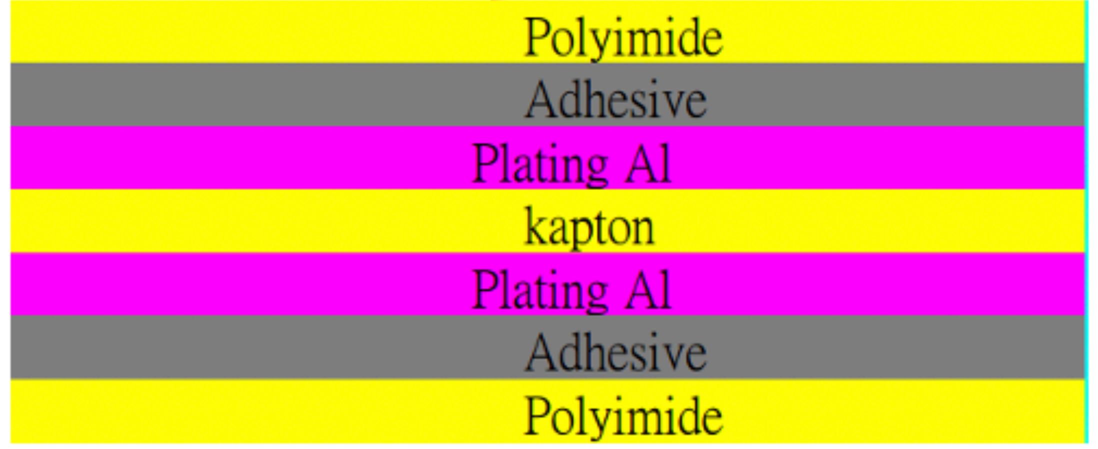




Sensor(Si, 50um)
glue(Epoxy, 15um)
Al(17.8um)
Kapton(50um)
Glue(Epoxy, 15um)
Ladder support(carbon fiber,350um)
Glue(Epoxy,15um)
Kapton(50um)
Al(17.8um)
Glue(Epoxy, 15um)
Sensor(Si, 50um)

(1) Sensor
(2) Flex cable
(3) Ladder support
(4) Flex cable
(5) sensor

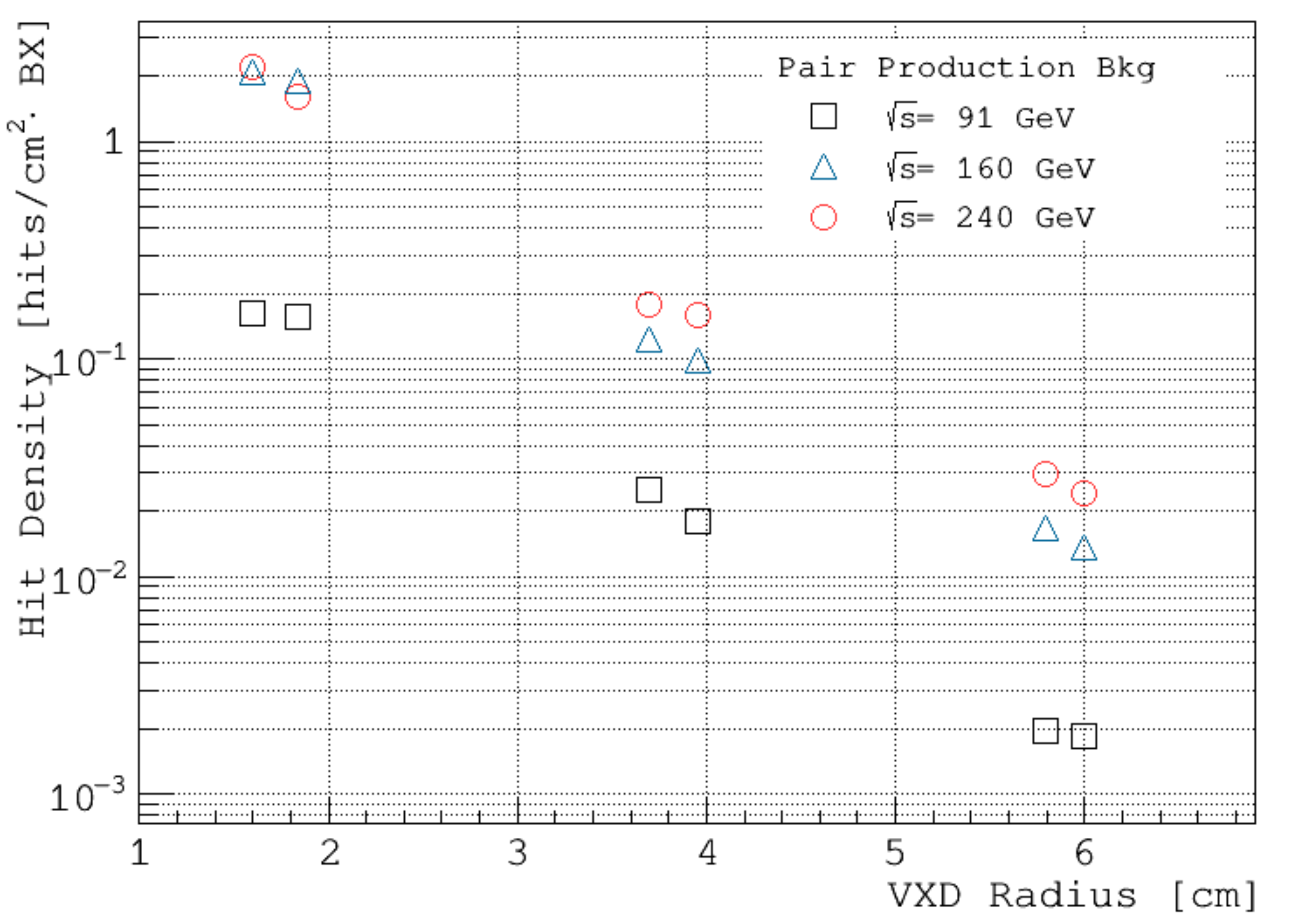
recent discussion shows that we need add more material into flex cable



Polyimide
Adhesive
Plating Al
kapton
Plating Al
Adhesive
Polyimide

Main specs of the full size chip for high rate vertex detector

- Bunch spacing
  - CEPC Z+Higgs (240GeV): 680ns;
  - WW threshold scan (160GeV): 210ns;
  - CEPC Z pole runing (90GeV) Z: 25ns
- High Hit density
  - 2.5hits/bunch/cm^2 for Higgs/WW runs
  - 0.2hits/bunch/cm^2 for Z pole running



For Vertex	**Specs**	**For High rate Vertex**	**Specs**	**For Ladder Prototype**	**Specs**
Pixel pitch	<25μm	Hit rate	120MHz/chip	Pixel array	512row×1024col
TID	>1Mrad	Date rate	3.84Gbps --triggerless ~110Mbps --trigger	Power Density	< 200mW/cm^2 (air cooling)
		Dead time	<500ns --for 98% efficiency	Chip size	~1.4cm×2.56cm