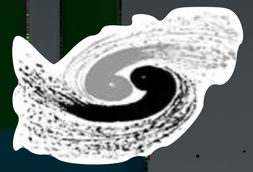
Status of Pixel Vertex Detector

Zhijun Liang
(IHEP, Chinese Academy of Sciences)

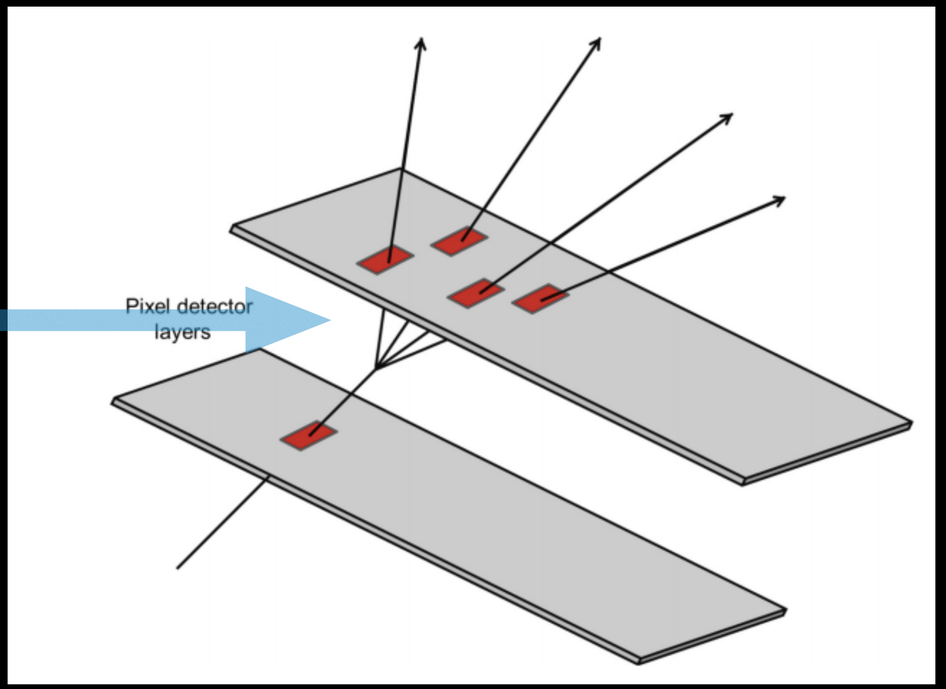


中國科學院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

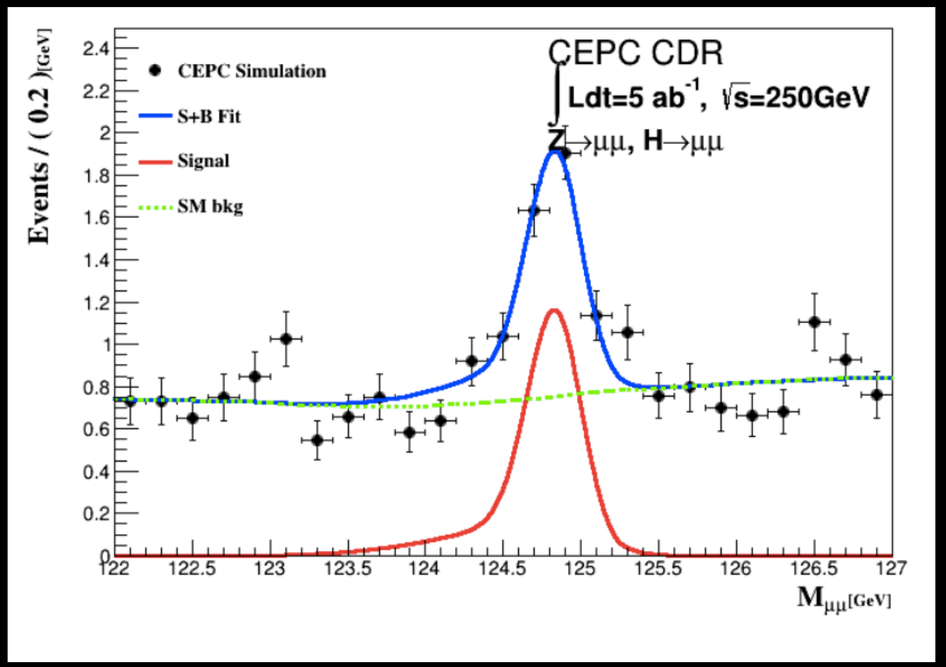
Vertex detector: Physics goal

- Higgs precision measurement
  - H → bb precise vertex reconstruction
  - H → μμ (precise momentum measurement)

Need tracking detector with high spatial resolution, low material



- Main technology
  - High spatial resolution technology → pixel detector
  - Low-mass detector technology
  - Radiation resistance technology



CEPC vertex detector R & D

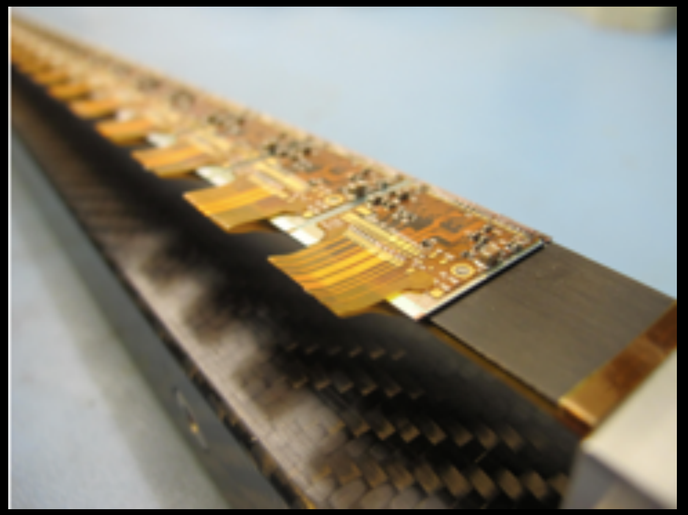
- Three on-going R & D programs on vertex detector
  - Previous update in CEPC day (June 15th) https://indico.ihep.ac.cn/event/11875/
- This talk focuses on MOST2 project
  - MOST2 aims to build full-size vertex detector prototype

Funding agency	Process	International collaborators	Objectives of the project	schedule
MOST1	CMOS	Strasburg IPHC	Small pixel size design with in-pixel digitization and low power frontend	2016.6-2021.5
MOST2	CMOS	IFAE/Oxford/ Livepool …	full-size vertex detector prototyping (Full-size sensor support structure, module …)	2018.5-2023.4
NSFC	SOI	KEK/SOIPIX collaboration	Verification of SOI process with small pixel size and low noise design	2016-

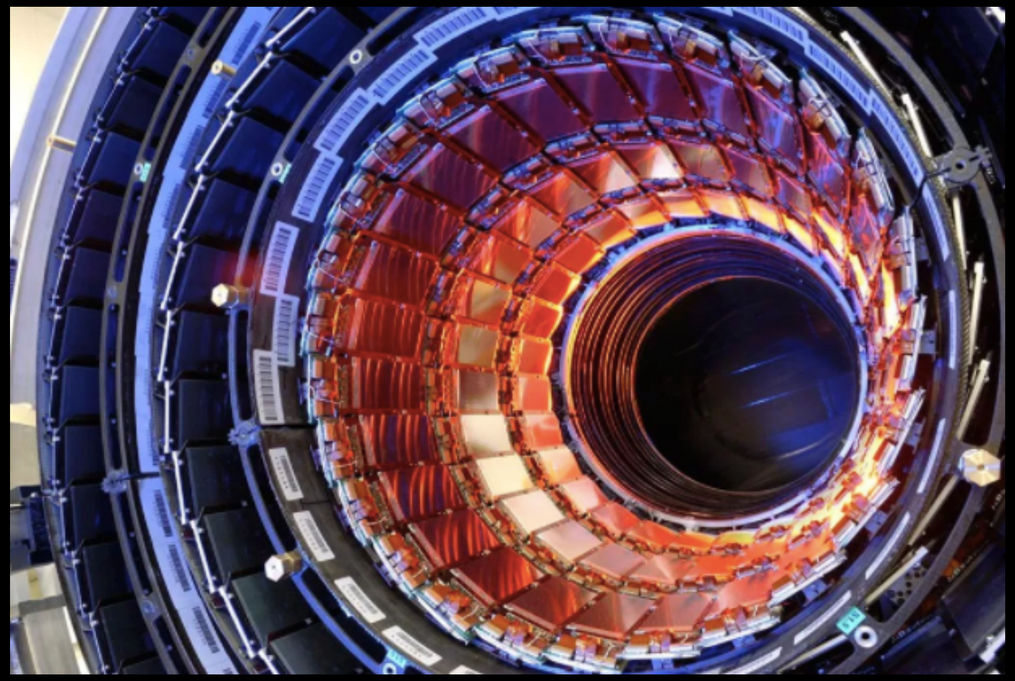
MOST2 vertex detector R & D: Research Goal

- Produce a world class vertex detector prototype
  - Spatial resolution 3~5 μm (pixel detector)
  - Radiation hard (>1 MRad)
- Preliminary design of prototype
  - Three layer, module ~1 cm × 12 cm^2

Typical module



Typical tracker



Resolution

ATLAS/CMS upgrade
（~15 μm）

Alice upgrade
（5~10 μm）

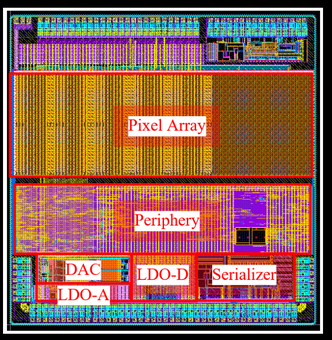
World leading

This project（3~5 μm）

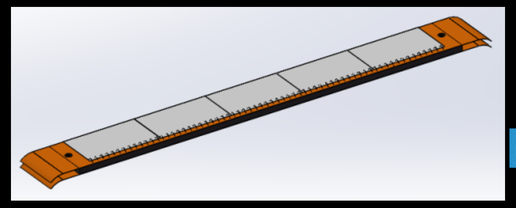
Overview of MOST2 vertex detector R & D

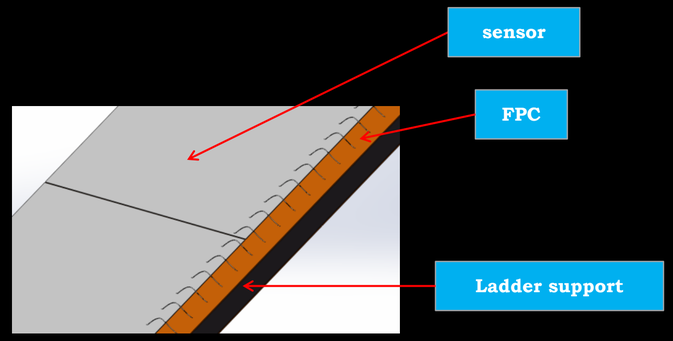
- Can break down into sub-tasks:
  - CMOS imaging sensor chip R & D
  - Detector layout optimization, Ladder and vertex detector support structure R & D
  - Detector assembly
  - Data acquisition system R & D

CMOS imaging sensor prototyping

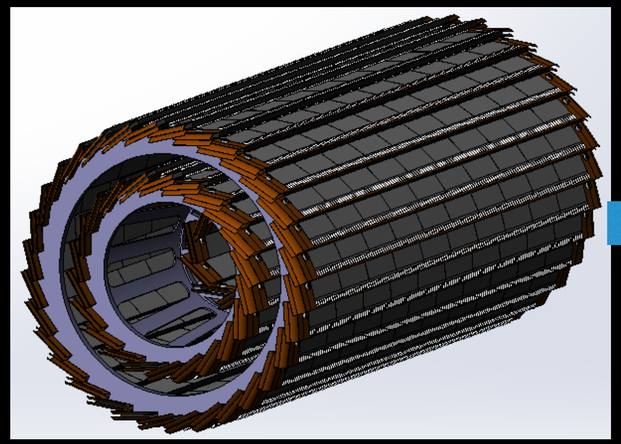


Detector module (ladder) Prototyping

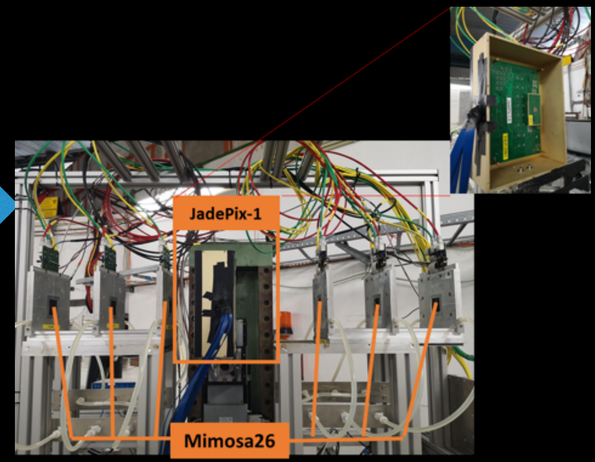




Full size vertex detector Prototype



Beam test to verify its spatial resolution



Research Team in MOST2 silicon project

4 institutes

课题2：**IHEP - 中国科学院高能物理研究所**
SDU - 山东大学
NJU - 南京大学
NWU - 西北工业大学

Institutes	Tasks
IHEP	Full CMOS chip modeling, Pixel Analog, PLL block Detector module (ladder) prototyping Data acquisition system R & D Vertex detector assembly and commissioning
CCNU/IFAE	CMOS sensor chip: Pixel Digital
NWPU	CMOS sensor chip: Periphery Logic, LDO
SDU	CMOS sensor chip: Bias generation, TCAD simulation Sensor test board design
NJU	Irradiation, test beam organization

Achievement Presentation and Assessment Methods

Silicon Detector

考核指标[2]				考核方式(方法)及评价手段[4]
指标名称	立项时已有指标值/状态	中期指标值/状态[3]	完成时指标值/状态	
硅径迹探测器原型机的空间分辨率	无	研制出小型传感器芯片，像素单元尺寸小于或等于25微米 ×25微米。	3-5微米	同行专家评审。(通过束流实验，离线分析数据获得空间分辨率。该测试结果写入原型机设计与测试报告，以供同行专家评审)
所设计的抗辐照硅传感器能承受的总剂量	无	完成传感器的初步设计，通过仿真初步验证其抗辐照性能	1 MRad	同行专家评审 (提供传感器的设计与测试报告供专家评审)

Assessment index

Spatial resolution

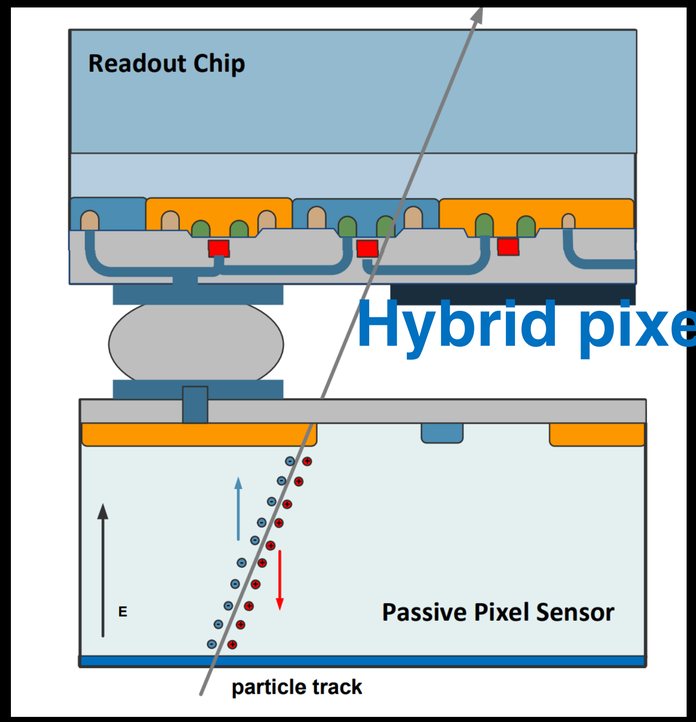
- Mid-term: produce **25*25 μm** pixel size chip
- Final : **3-5 μm** resolution in **Beam test**

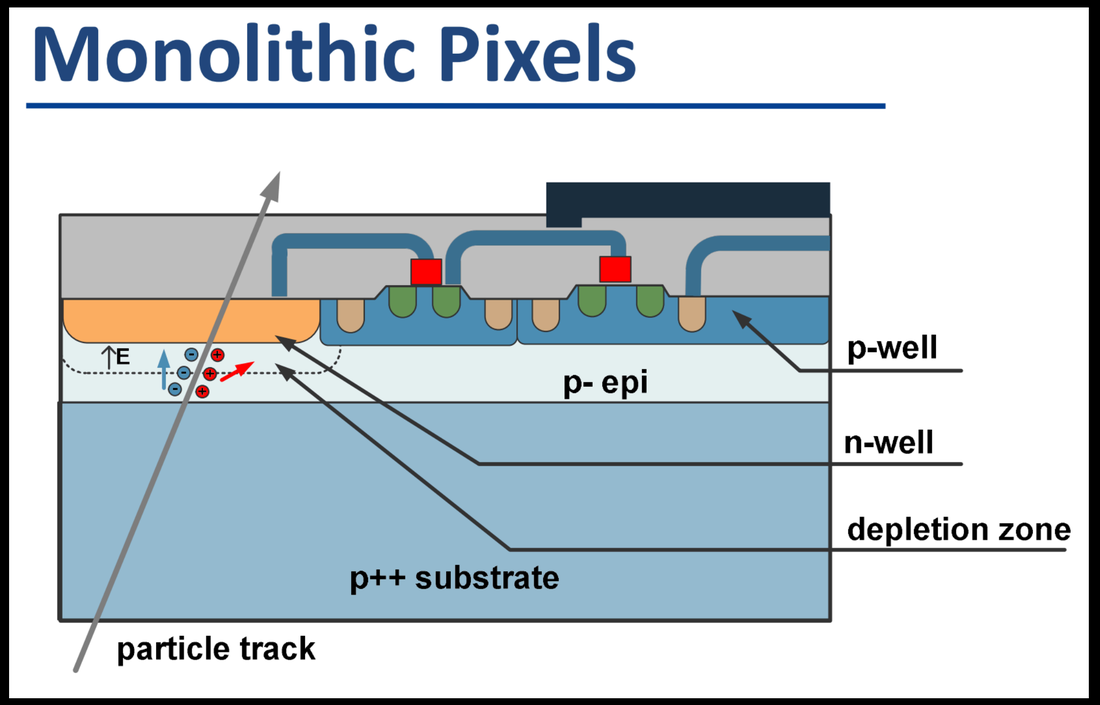
Radiation hardness

- mid-term: verified by TCAD simulation
- Final : Total ionization dose **>1 Mrad**

CMOS Monolithic pixel sensor

- CMOS Monolithic pixel (CIS process) is ideal for CEPC application
  - low material budget (can be thin down to 50μm)
  - This project use TowerJazz CIS 180nm technology
- Hybrid pixel technology developed by ATLAS and CMS
  - Thickness of sensor is about 200~300 μm
  - Need to bump bonding with readout ASIC (ASIC thickness is about 300μm)
  - Material budget about silicon sensor is about 10 times larger than CIS process





CMOS Sensor chip R & D

- The existing CMOS monolithic pixel sensors can’t fully satisfy the requirement
- Major Challenges for the CMOS sensor
  - Small pixel size -> high resolution (3-5 μm)
  - High readout speed (<500ns deadtime @40MHz at Z pole) -> for CEPC Z pole high lumi
  - Radiation tolerance **(per year):** 1 MRad

	ALPIDE	ATLAS-MAPS (MONOPIX / MALTA)	MIMOSA
Pixel size	✓	X	✓
Readout Speed	X	✓	X
TID	X (?)	✓	✓

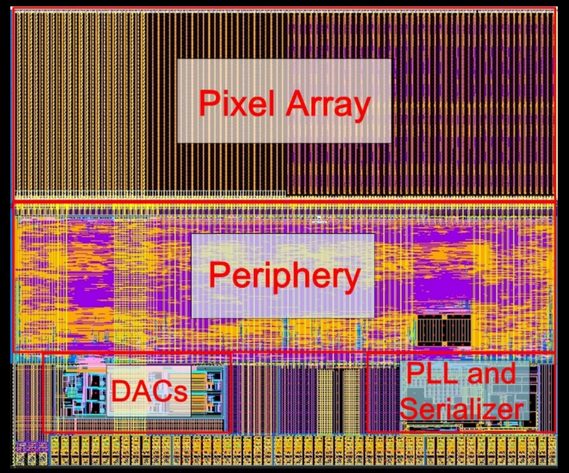
Sensor prototyping

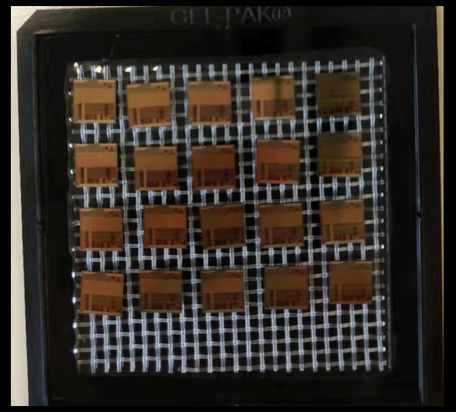
- Completed two round of sensor prototyping
  - 1st Multi-wafer project chip (Taichupix1)
    - Submitted in June 2019, received in November 2019
    - Test functional blocks
      - pixel array (in-pixel amplifier and digital logic)
      - Periphery block: digital readout architecture
      - Periphery block： PLL and Serializer
      - Periphery block： LDO and power supply
  - 2nd Multi-wafer project chip(Taichupix2)
    - Submitted in Feb 2020, received in July 2020
    - Major bugs fixed in Taichupix1
    - Radiation hard design (enclosed gate) in pixel analog

Taichupix1

Chip size： 5mm×5mm

Pixel size： 25μm×25μm

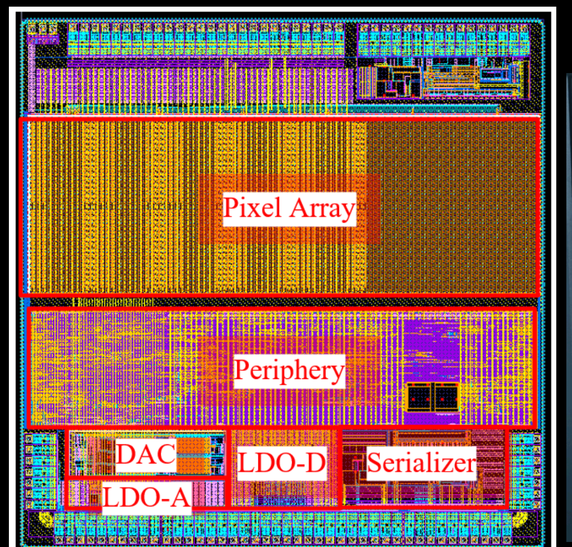




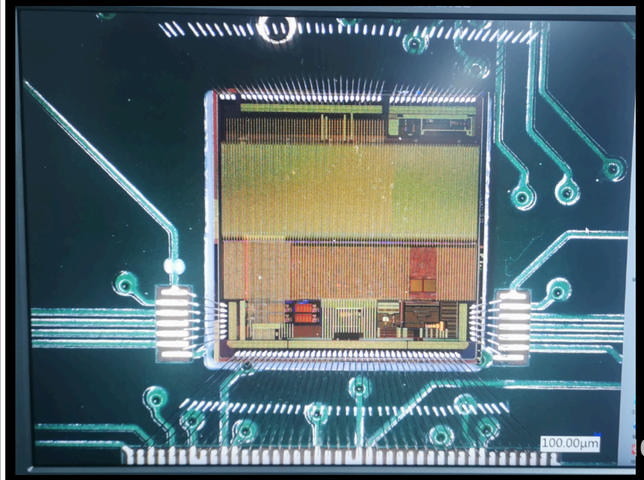
Taichupix2

Chip size： 5mm×5mm

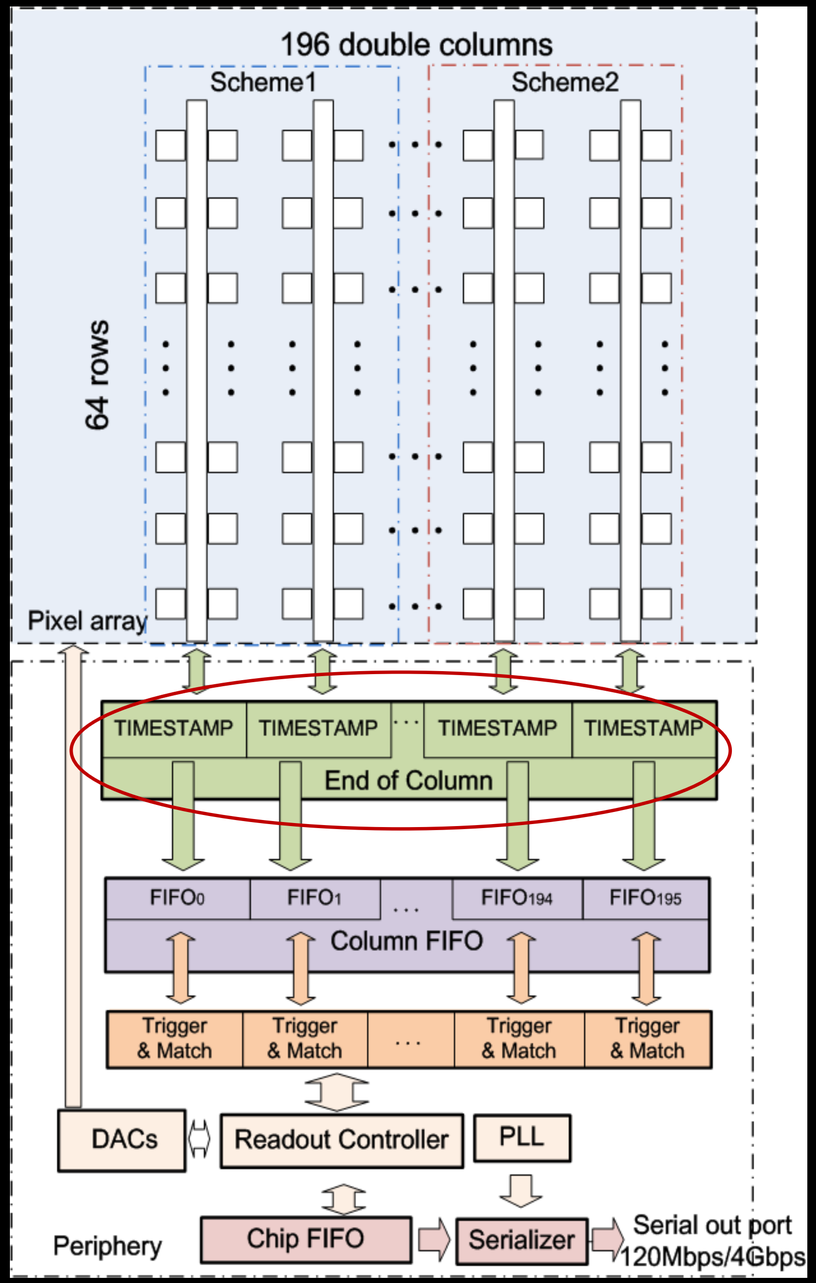
Pixel size： 25μm×25μm



Taichupix2 on test board



New proposed readout architecture in TaichuPix

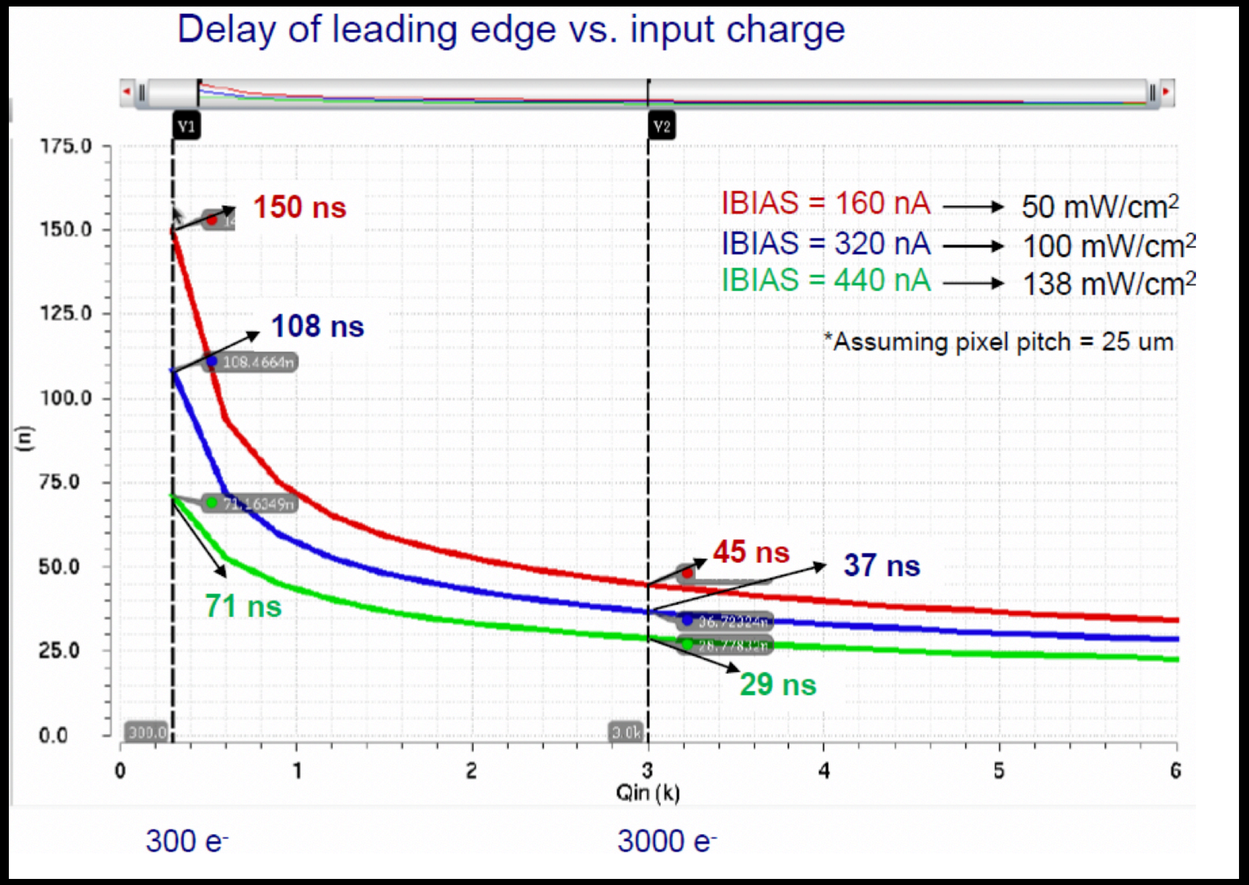


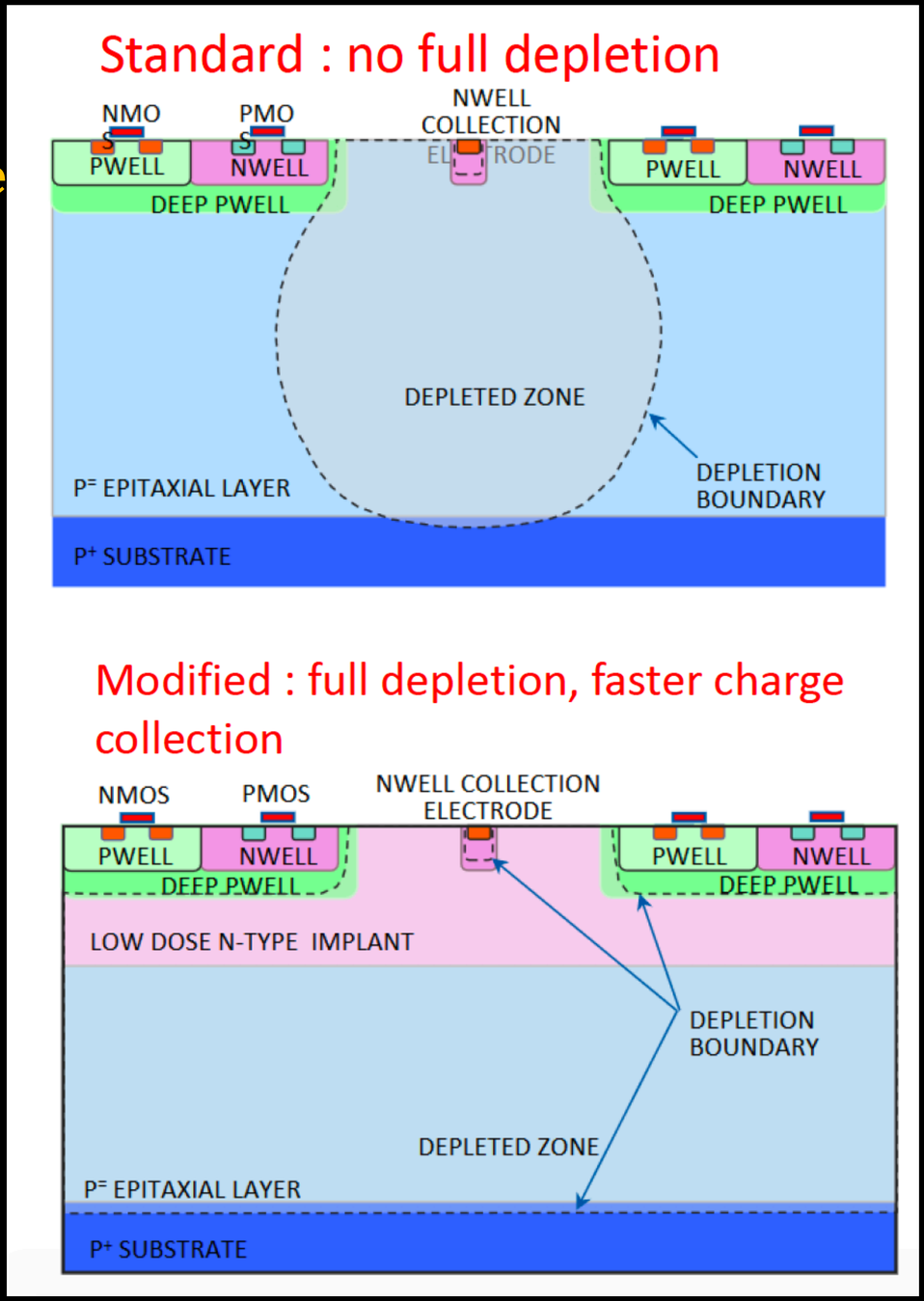
- New readout architecture
- → reduce power consumption and reduce pixel size
- CEPC readout time requirement:
  - <500ns deadtime @40MHZ(Z pole)

- Taichu-1 Column-drain readout
  - Priority based data driven readout; time stamp at EOC
  - Dead time: 2 CLK for each pixel (50ns @40MHz CLK)
  - Two digital pixel designs: FEI3-like and ALPIDE-like design
- 2-level FIFO architecture
  - L1: column level, to de-randomize injecting charge
  - L2: chip level, to match in/out data rate between core and interface
- Trigger readout:
  - Coincidence by time stamp, matched event read out

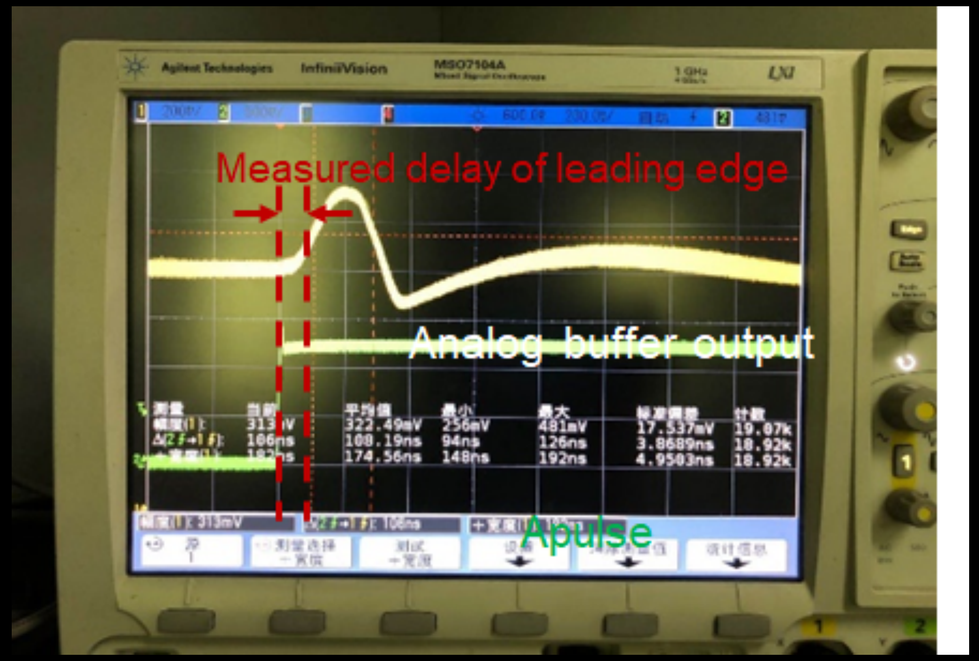
Pixel Analog design

- CEPC time stamping precision requirement:
  - 25-100ns, better to time stamping each collision at Z pole
- Taichu-1 pixel analog design:
  - 50ns~150ns (based one standard CMOS MAPS tech.)
  - Consider to use depleted CMOS MAPS



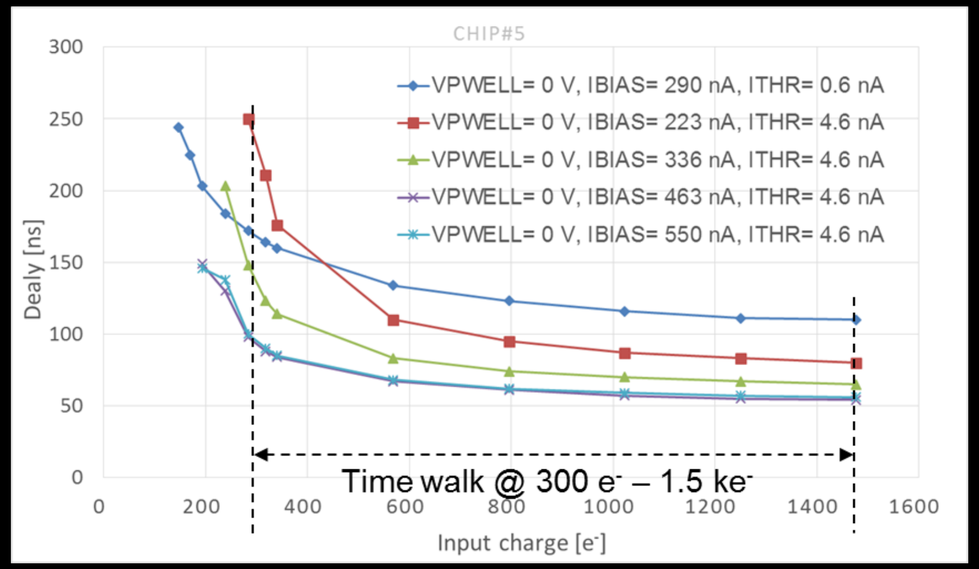


Pixel Analog Testing

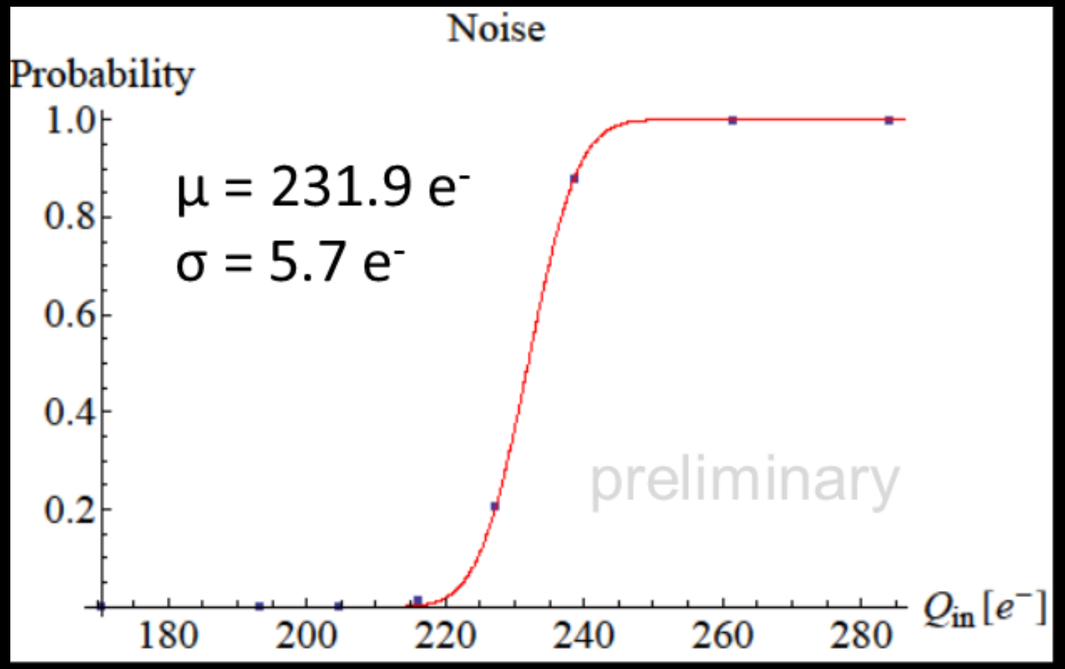


- Pixel analog was tested by the probed output
- The tested performance was at the same level as in simulation, though the test condition is not perfect
- Tested noise 5.7e-
- Tested time walk 36ns(@300 e^-–1.5 ke^-)

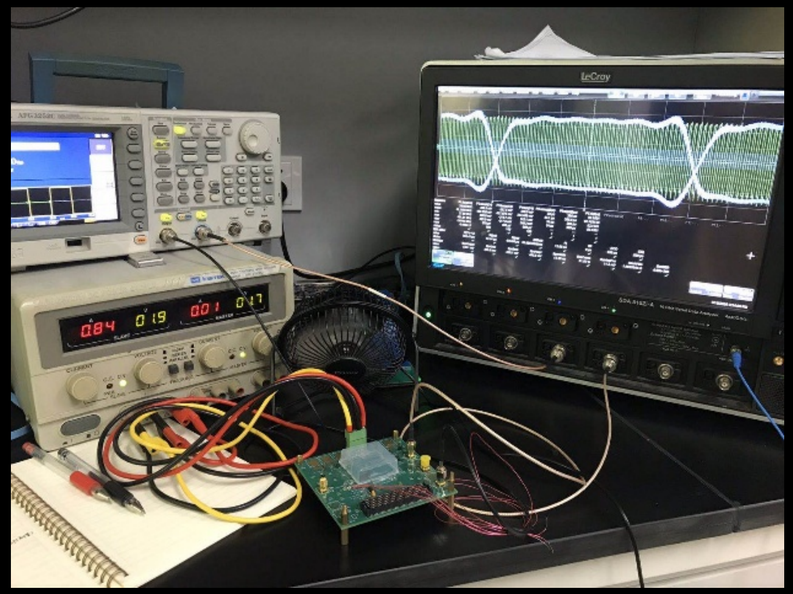
Tested time walk measurements



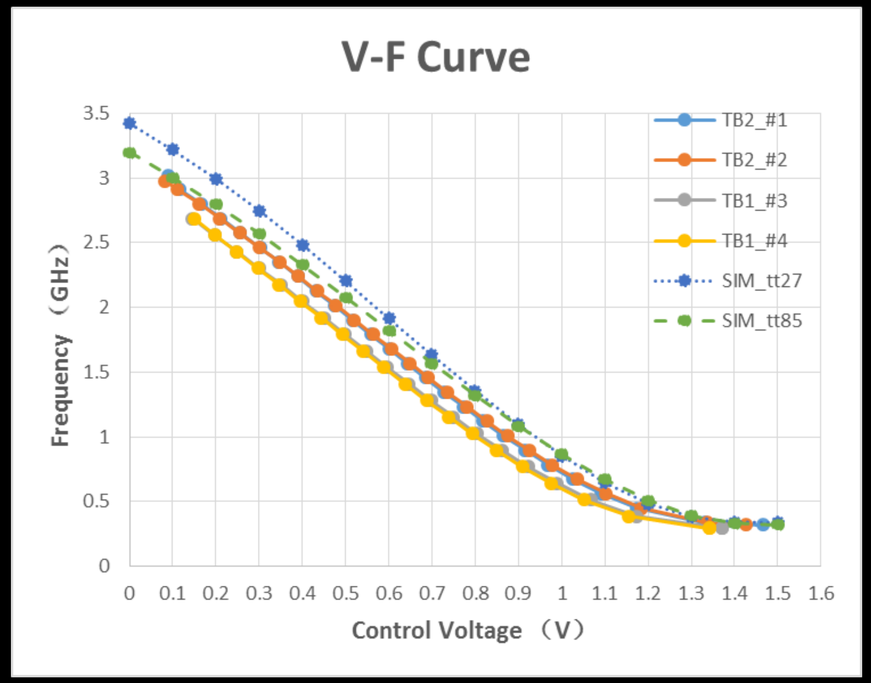
Noise measurements



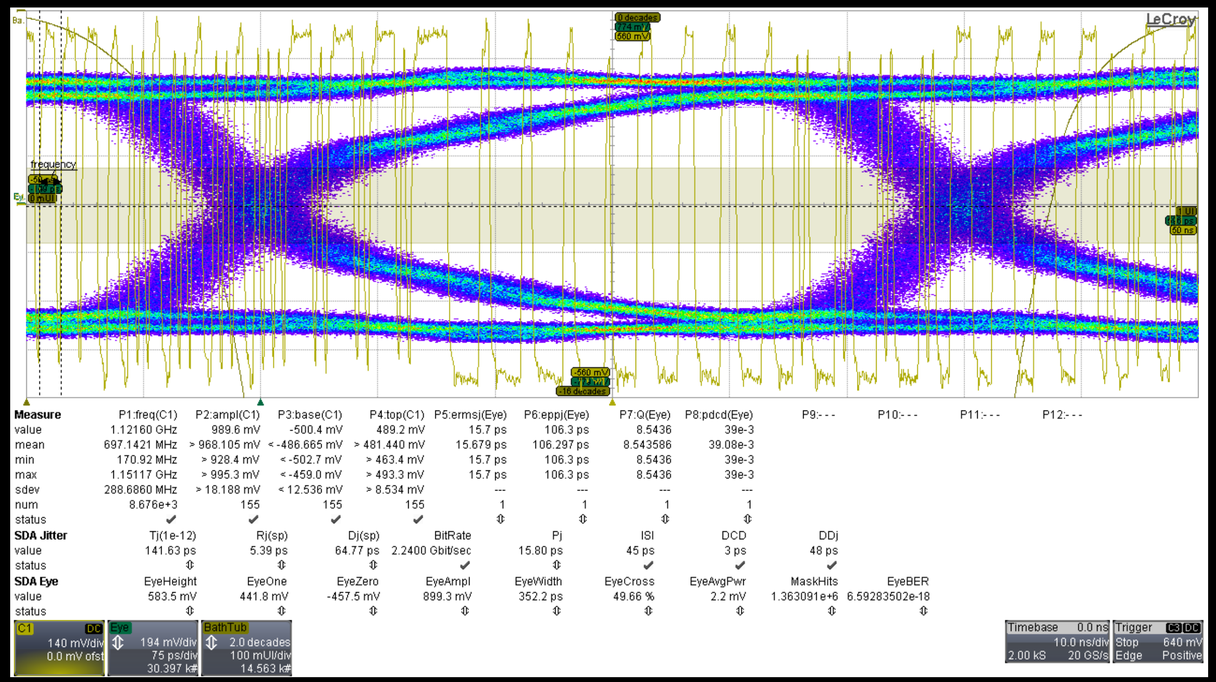
PLL and Serializer Testing



- PLL and the serializer was thoroughly tested and proved
- PLL's tuning range 0.32~2.91GHz agrees with the simulation
- Good and robust eye-diagram observed at 2.24GHz, with the total jitter < 150ps (@ error rate < e^{-12})
- Serializer could run steadily @ 2.24GHz for trigger less mode

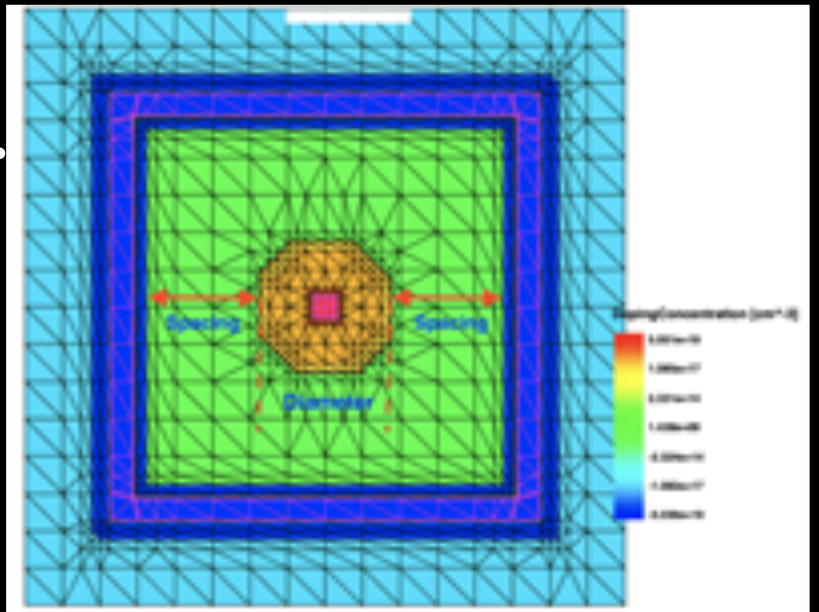


Eye-diagram



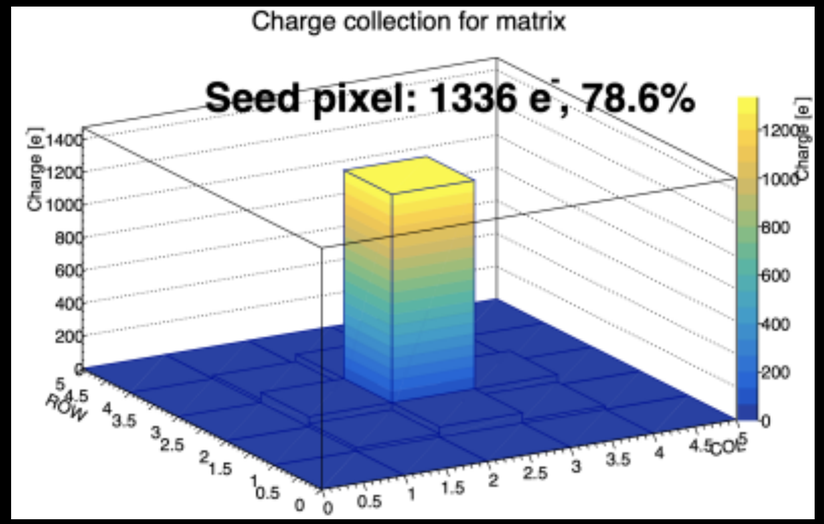
Radiation hardness

TCAD simulation model

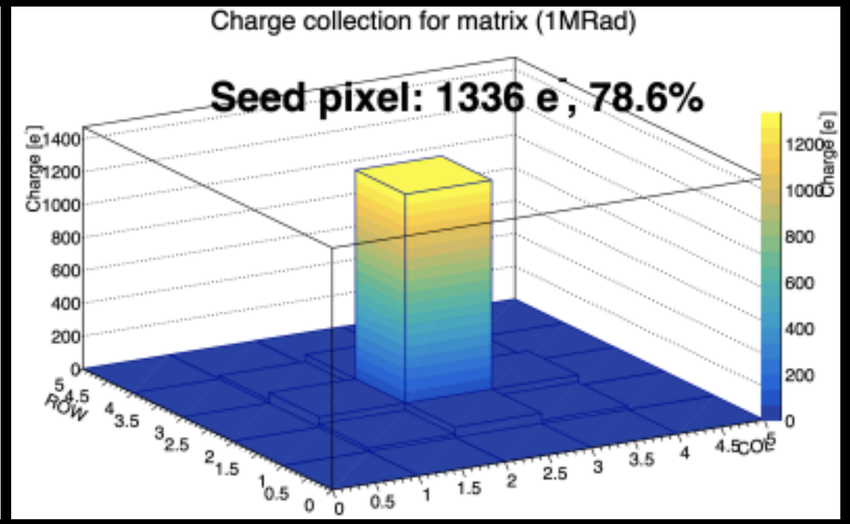


- Sensing diode was simulated by TCAD to study its TID behavior
- The impact is negligible for the charge collection, and the leakage current after 1Mrad radiation
- X ray irradiator in IHEP has been setup for irradiation tests

Collected charge
Before irradiation



Collected charge
After 1 Mad total ionization dose



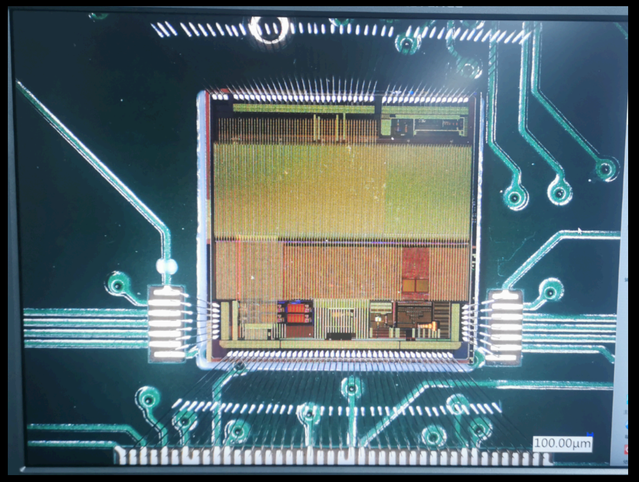
X ray irradiator

Status of TaichuPix2

- New features
  - A 64*192 pixel array with the same dimension as Tcpx1
  - 32 + 32 double column modified FE-I3 readout
  - 32 double column modified ALPIDE readout
  - Newly integrated blocks: Two LDOs for power supplies
  - 8b10b encoder added for Triggerless output
  - X-chip buses added for multiple chip interconnections
- Functional verification status
  - IO rings works fine (problem solved)
  - Bandgap reference output proved (oscillation cancelled)
  - Periphery blocks tested
  - PLL lock function preliminarily proved
  - Pixel array digital communication with the periphery

received chips in July 23rd , 2020

Taichupix2 on test board



Oscillation issue reported in last update
Fixed in TaichuPix2

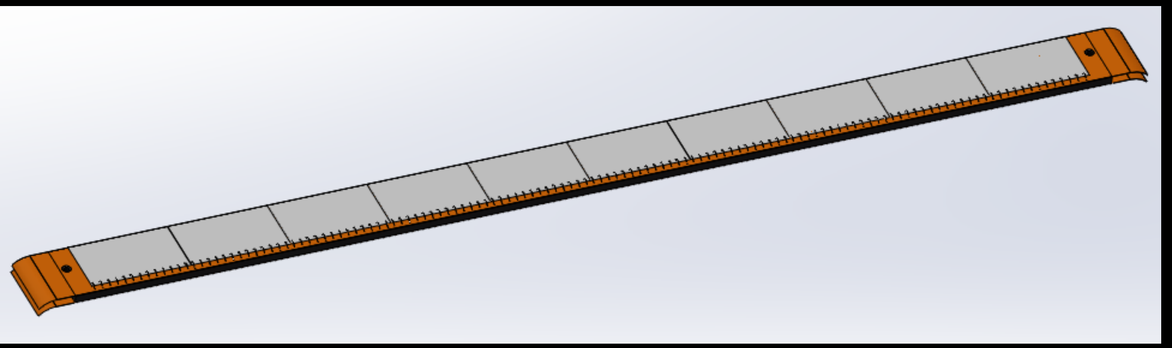
Summary of CMOS Sensor chip R & D

- Major achievement in two round of prototyping
  - High Spatial resolution
    - Pixel size reduced to 24×25 μm → reach midterm Assessment index (实现中期指标）
  - Radiation hard
    - According to TCAD simulation, the impact is negligible for the charge collection, and leakage current after 1Mrad total ionization dose radiation→ reach midterm Assessment index (实现中期指标）
- Next steps
  - 3rd Multi-wafer project (to be submit early 2021)
    - Goal: All functional blocks work together
    - Maybe skipped if 2nd MPW chip is working
  - Full size sensor engineering run (in August 2021)
    - Goal: full-size, full functionality

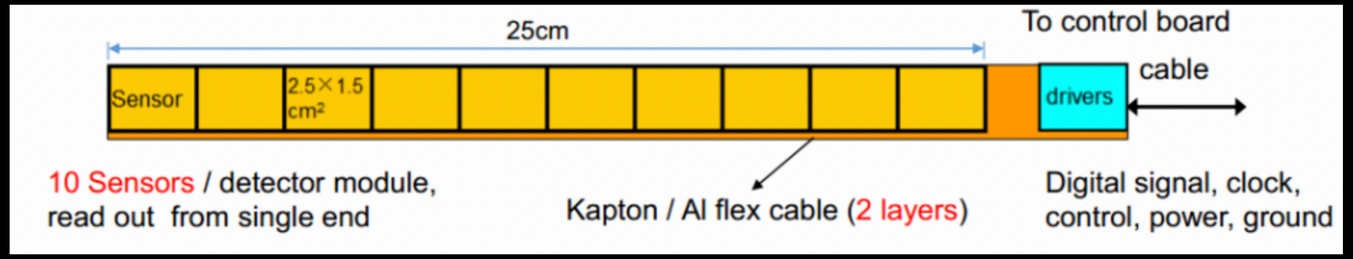
Detector module (ladder) R & D

- Completed preliminary version of detector module (ladder) design
  - Detector module (ladder)= 10 sensors + support structure+ flexible PCB+ control board
  - Sensors will be glued and wire bonded to the flexible PCB
  - Flexible PCB will be supported by carbon fiber support structure
  - Signal, clock, control , power, ground will be handled by control board through flexible PCB

3D model of the ladder



Schematic of ladder electronics



Flexible PCB prototype

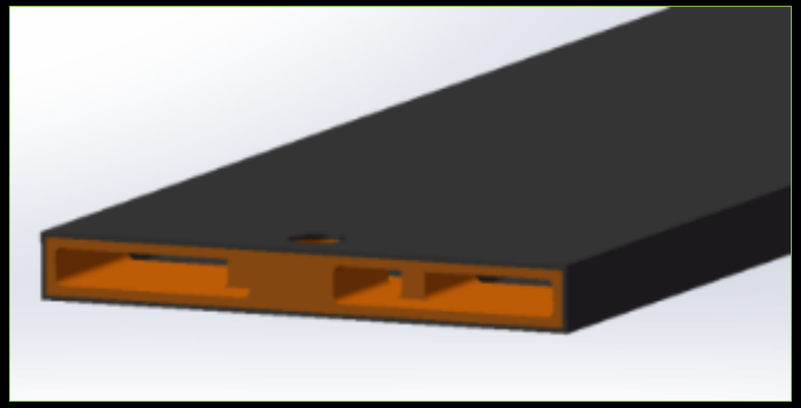
Profile of flexible PCB

	Achieved Thickness (μm)	Optimization goals (μm)
Polyimide	25	12
Adhesive	28	15
Plating Cu	17.8	17.8
kapton	50	50
Plating Cu	17.8	17.8
Adhesive	28	15
Polyimide	25	12

Support structure of the ladder

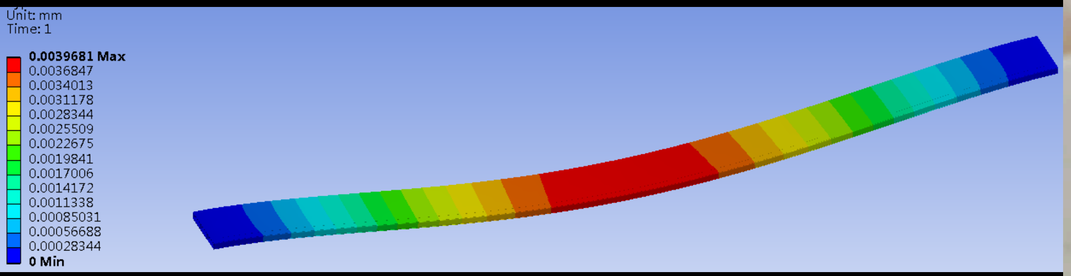
- Support structure of the ladder: 3 layer of carbon fiber, 0.15mm thick
  - 3 time thinner than conventional carbon fiber
  - A few times more rigid than conventional carbon fiber
  - for tracks with small cosθ, radiation length ~0.015 X0 (reduce multi-scattering)

Ladder support structure 3D model



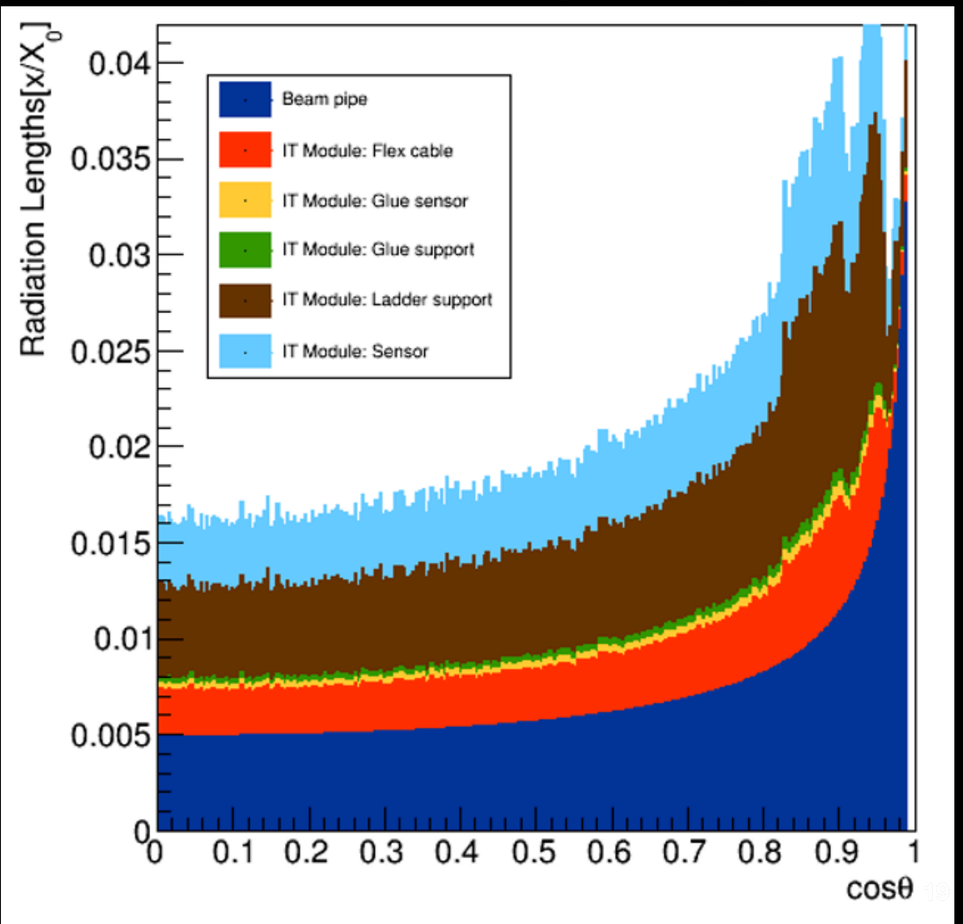
Finite elements analysis

Max def. under full load: 5.3 um



Conventional carbon fiber 0.15mm (1 layer)

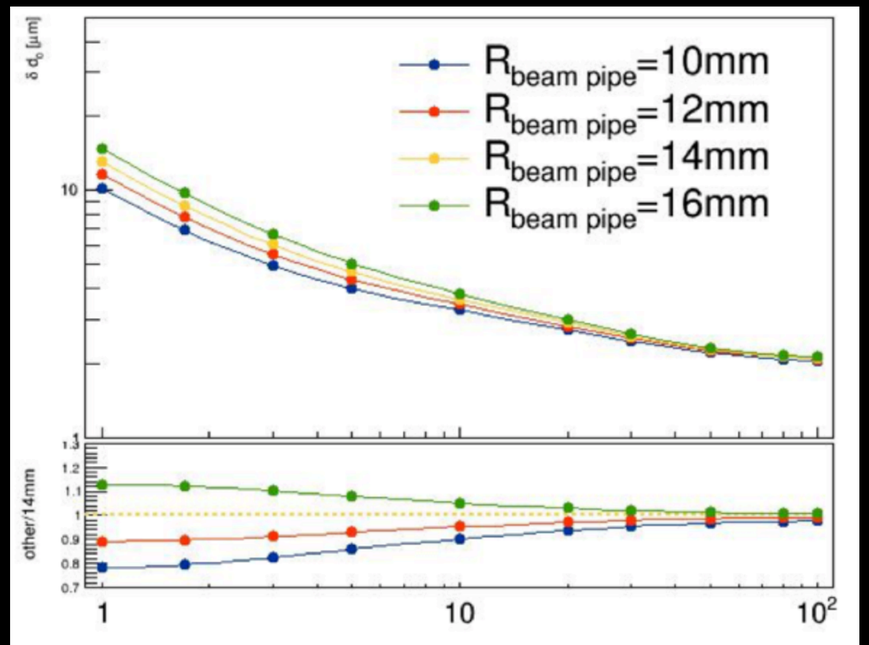
Flexible PCB prototype



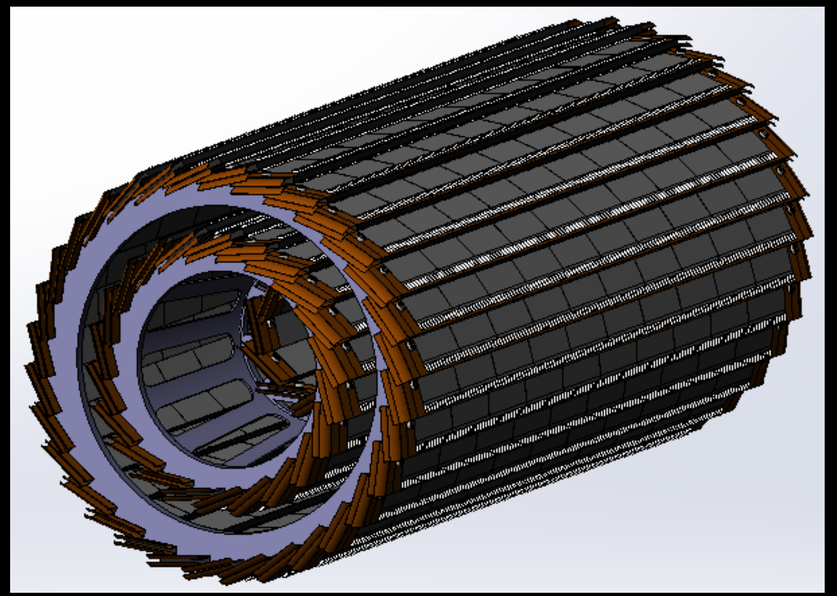
Vertex Detector Prototype R & D

- Completed preliminary version of detector engineering design
  - 3 double layer barrel design
  - 10 modules in inner layer, 22 modules in 2nd layer, 32 modules in outer layer
  - Start thermal design (air cooling)
- Physics simulation to optimize vertex detector layout design.
  - The length of inner layer pixel should be the same as other two layers
  - Inner pixel radium should be as close to beam pipe as possible

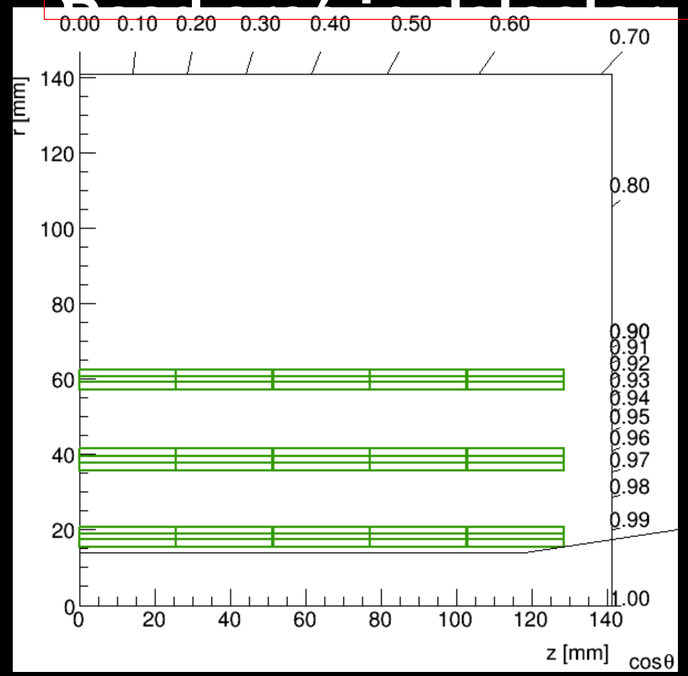
Impact parameter resolution Vs beam pipe radius



3D Model of vertex detector



Vertex detector layout (R-Z view)

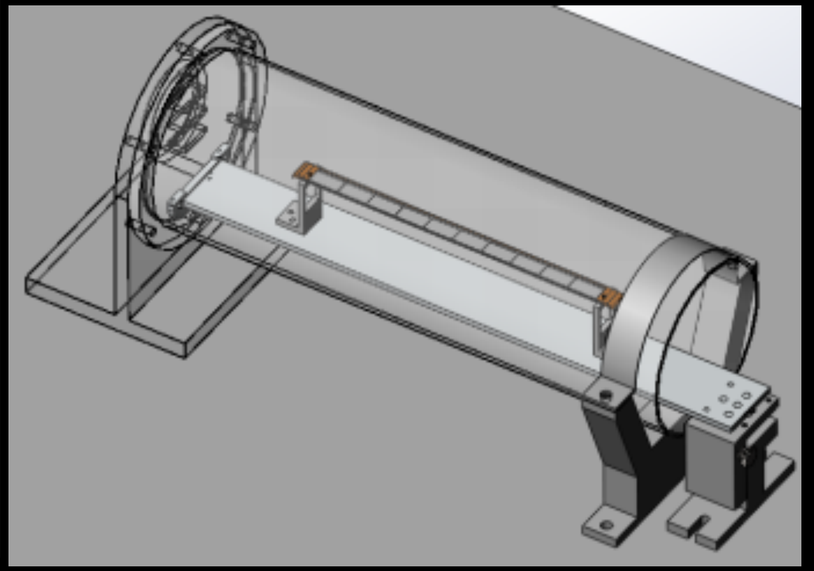


Cooling design

- **Air cooling is baseline design for CEPC vertex detector**
- **Sensor Power dissipation:**
  - Taichupix : $\leq 100\ mW/cm^2$. (trigger mode)
  - CEPC final goal : $\leq 50\ mW/cm^2$
- Cooling simulations of a single complete ladder with detailed FPC were done.
  - Need 2 m/s air flow to cool down the ladder to 30 ℃
  - Testbench setup has been designed for air cooling , vibration …

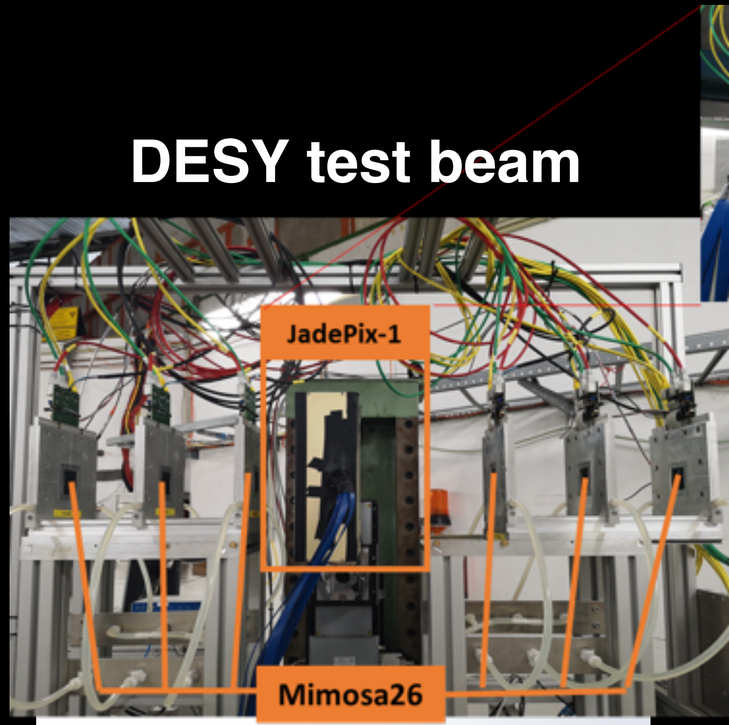
Max temperature of ladder (℃) (air temperature 5 ℃)					
Power Dissipation (mW/cm2) \ Air speed (m/s)	5	4	3	2	1
100	19.6	21.8	25.0	*30.6*	*43.4*
150	26.9	30.1	35	*43.4*	*62.6*
200	34.2	38.6	45.1	*56.2*	*81.8*

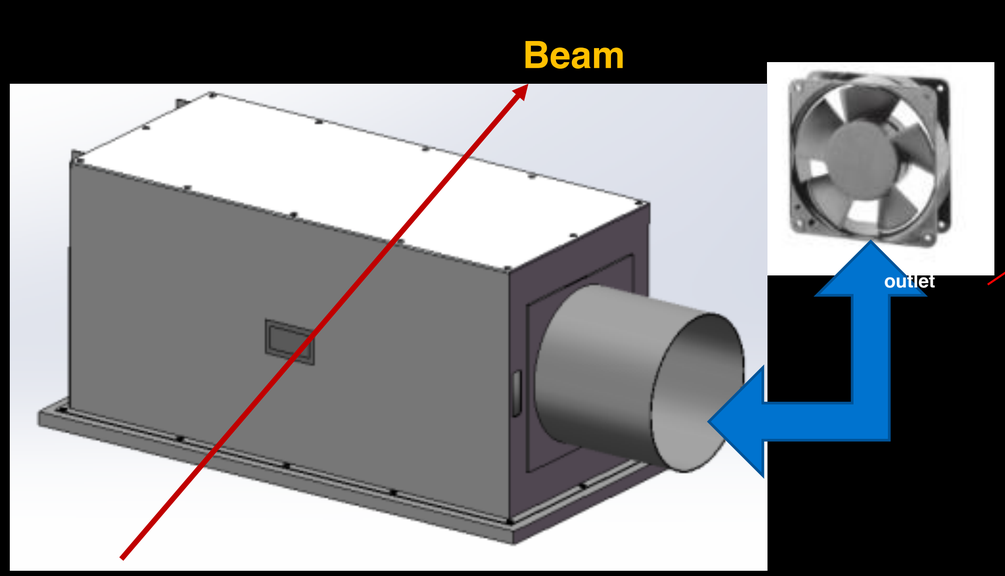
Test setup for ladder cooling
Use compressed air for cooling

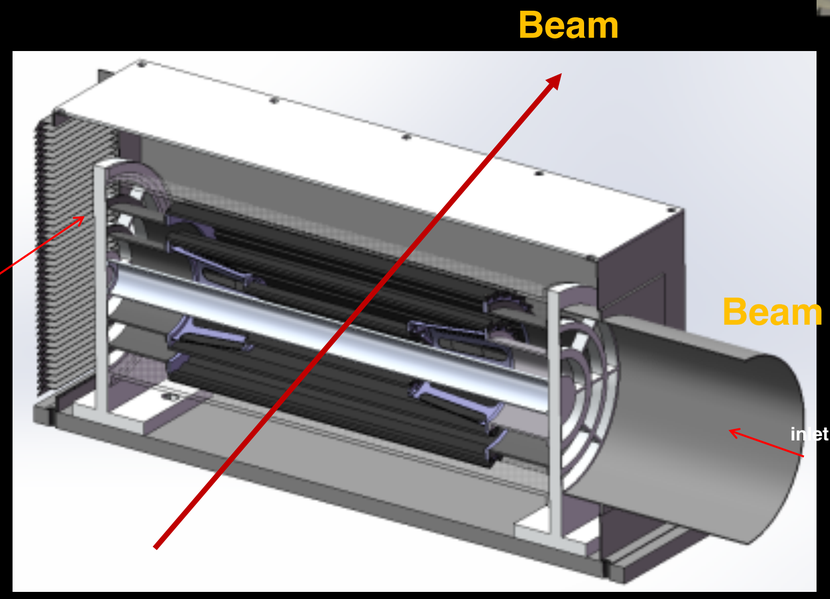


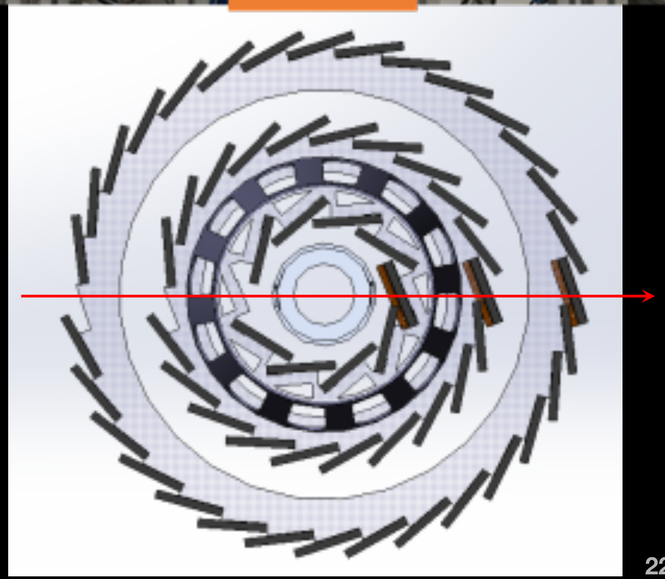
Plan for test beam

- Expect to perform beam test in DESY(3 - 7GeV electron beams)
  - IHEP test beam facility as backup plan (a few hundreds MeV electrons)
- Enclosure for detector with air cooling is developed for beam test
  - Beam is shooting at one sectors of vertex detectors



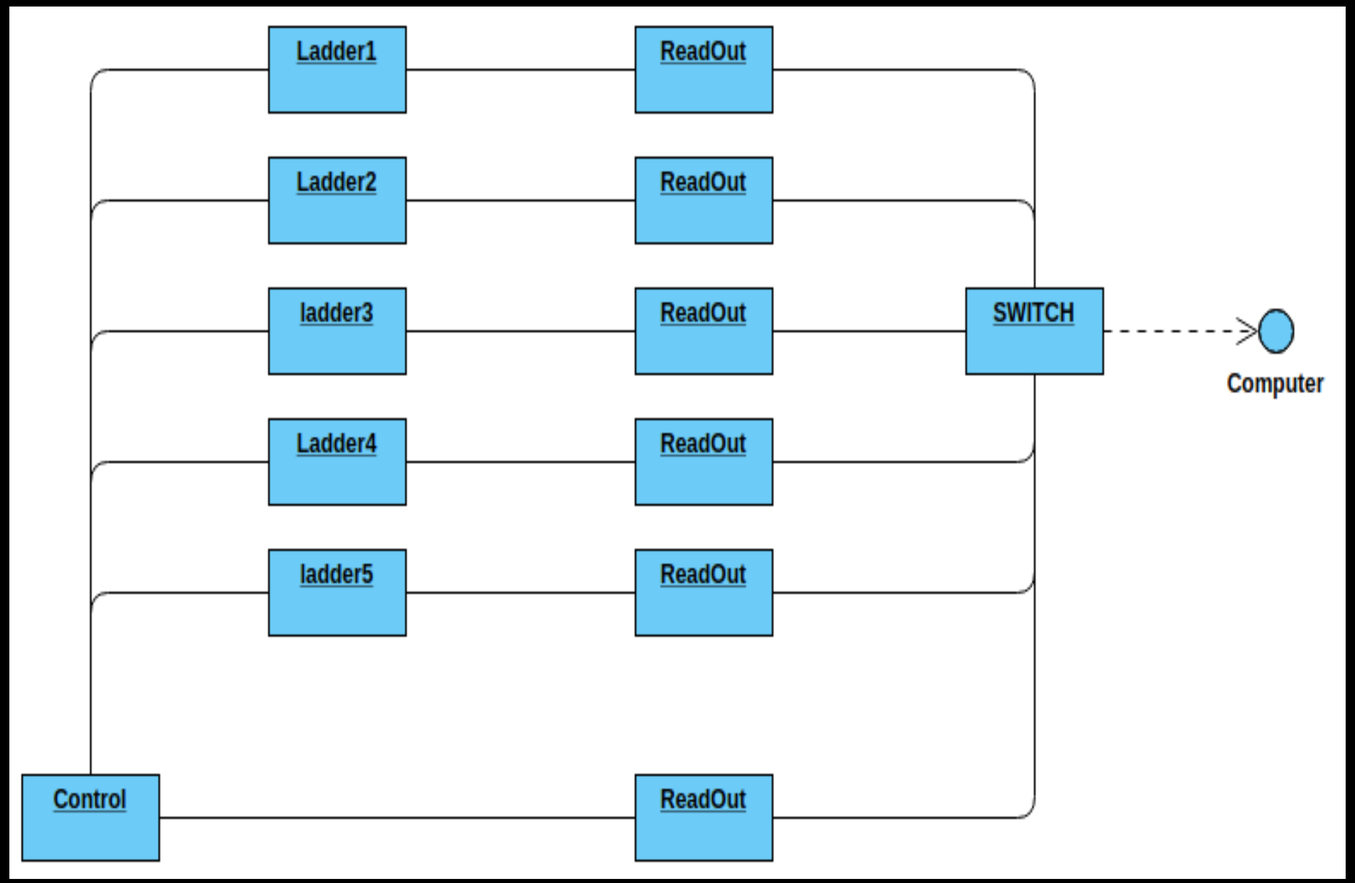






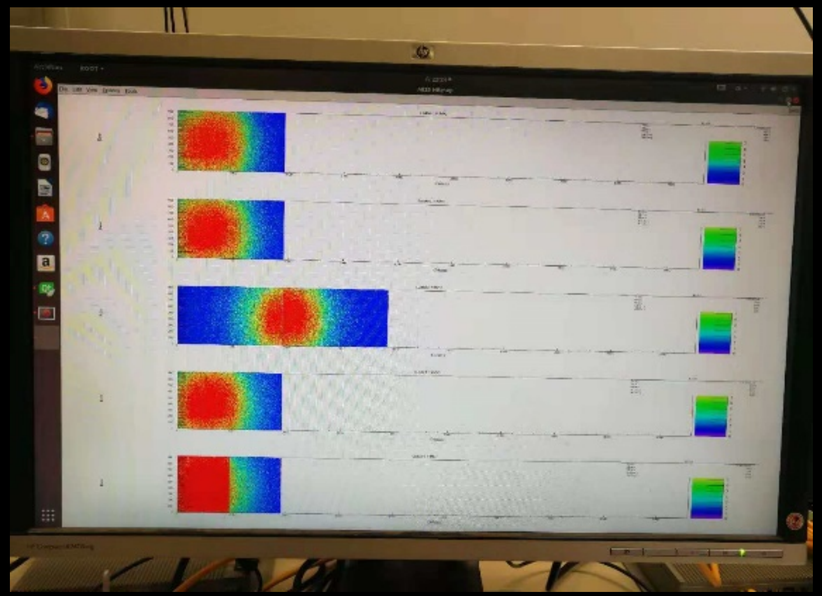
Data acquisition system

- Preliminary design of data acquisition system(DAQ)
  - Ladders are reader by readout boards
  - All readout boards connected to computer through a switch
  - User interface developed
  - DAQ tested in five modules equipped with MIMOSA sensors



DAQ Tests with 5 MIMOSA chips

DAQ system data display
Tested with MIMOSA modules



Publications and International talks

Publication:

High data-rate readout logic design of a 512 × 1024 pixel array dedicated for CEPC vertex detector

X. Wei,[a,1] W. Wei,[b] T. Wu,[c,d] Y. Zhang,[b] X. Li,[b] L. Zhang,[e] W. Lu,[b] Z. Liang,[b] J. Dong,[e] L. Li,[e] J. Wang,[a] R. Zheng,[a] R. Casanova,[d] S. Grinstein,[d] Y. Hu[f] and J. Guimaraes da Costa[b]

JINST 14 (2019) C12012

A full functional Monolithic Active Pixel Sensor prototype for the CEPC vertex detector

Tianya Wu[1,2], Raimon Casanova[2], Wei Wei[3], Xiaomin Wei[4], Ying Zhang[3], Liang Zhang[5], Xiaoting Li[3], Zhijun Liang[3], Joao Guimaraes da Costa[3], Weiguo Lu[3], Jianing Dong[5], Long Li[5], Wang Jia[4], Ran Zheng[4], Ping Yang[1], Guangming Huang[1] and Sebastian Grinstein[2]

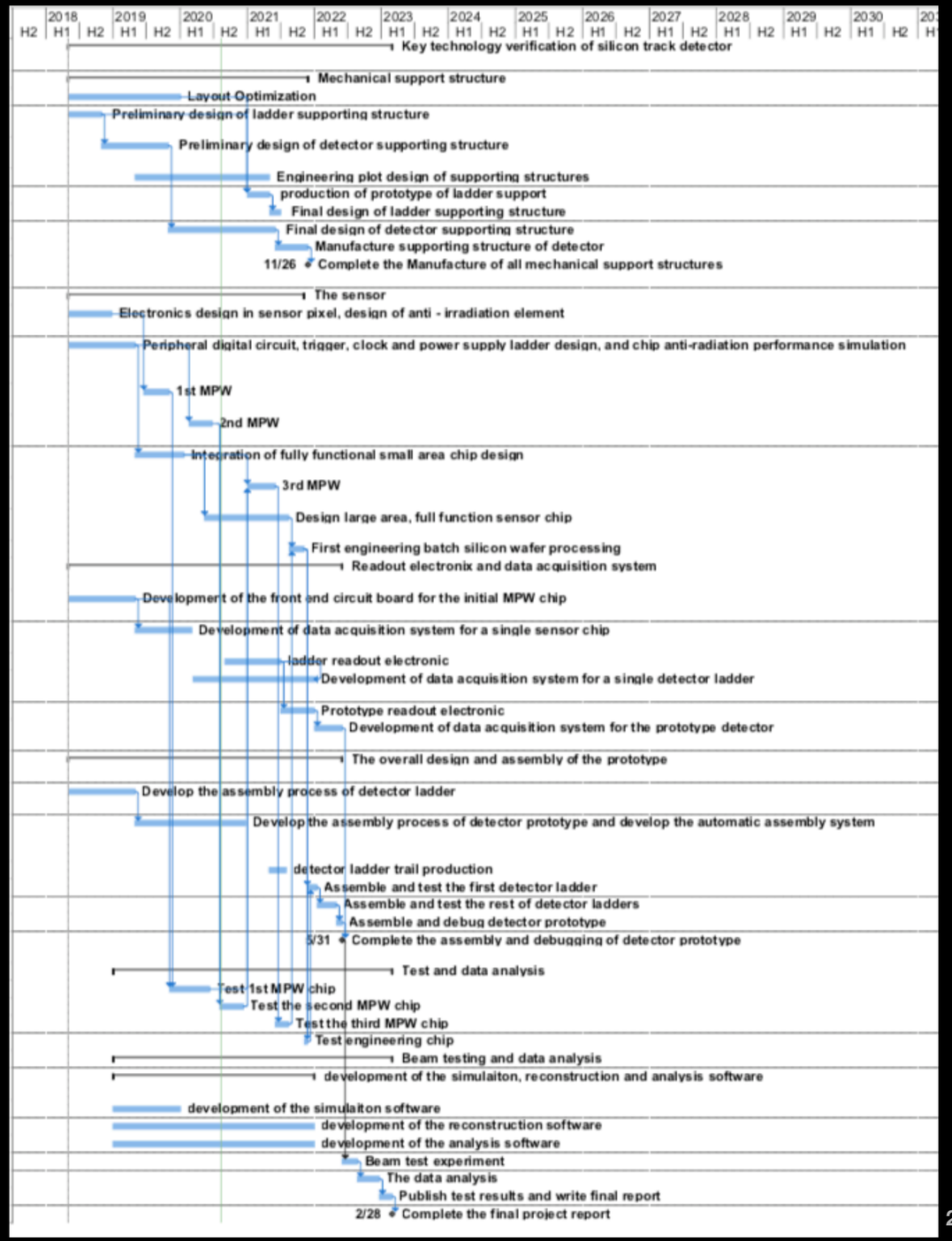
- International conference talks:

IEEE ICECS (doi: 10.1109/ICECS46596.2019.8965105.)

- Joao Guimaraes Da Costa, CepC phys/detectors, Workshop on the Circular Electron-Positron Collider,EU Edition, April 15 - 17, 2019, Oxford, UK
- T. Wu , A full functional Monolithic Active Pixel Sensor prototype for the CEPC vertex detector, in proceeding of International Conference on Electronics Circuits and Systems, Nov. 27-29, 2019, Genova, Italy.
- Xiaomin Wei, High data-rate readout logic design for 1024*512 CMOS pixel array dedicated for CEPC experiment, International workshop on radiation imaging detectors, International workshop on radiation imaging detectors, July 2019, Crete, Greece
- Ying Zhang, Overview of the chip design for the MOST2 CEPC vertex project, Workshop on the Circular Electron-Positron Collider,EU Edition, April 15 - 17, 2019, Oxford, UK
- Wei Wei, Full size pixel chip for high-rate CEPC Vertex Detector， Workshop on the Circular Electron-Positron Collider,EU Edition, April 15 - 17, 2019, Oxford, UK

Future plan

- 3rd Year:
  - 3rd CMOS sensor fabricated and tested
    → may be skipped if 2nd MPW chip is fully working
  - Final support structure engineering design completed
  - Fabricated support structure for ladders
- 4th Year:
  - Competed R & D large area sensor
  - Manufactured the support structure for whole detector
  - Assembling and installing the detector prototype
  - Completed DAQ system for whole detector
- 5th Year:
  - Completed detector assembly and commissioning
  - Test beam and data analysis
  - Finish assembling of prototype



International collaboration

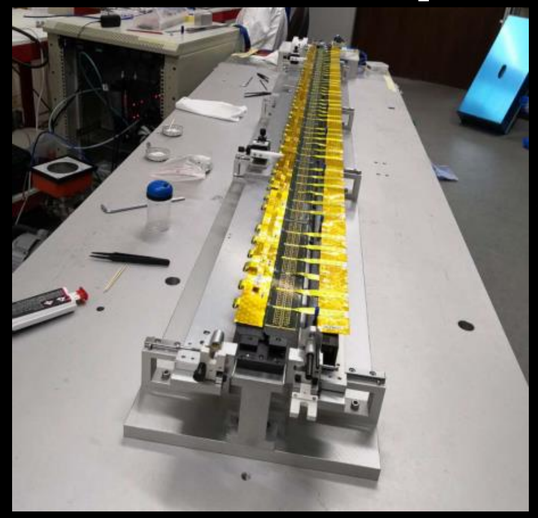
- **IFAE(Spain): very active in CMOS Sensor design and testing**
- Liverpool (UK): Tracker mechanical design,
- Oxford(UK): CMOS sensor design validation, thermal design
- RAL(UK): Pixel module design
- Queen Mary(UK): module mechanical design (Zero mass concept)
- Strasbourg (FR): CMOS sensor design, Tracker mechanical design
- University of Massachusetts (US): Tracker mechanical design, thermal design

In 2019, we have one engineer visited Oxford and Liverpool for 4 weeks, learned a lots about silicon.

Mu3e ladder, Atlas barrel strip stave prototype.

Lab visit in Oxford

Labs visit in Liverpool



Module of Alice's OB tracker, Advance material Lab

Risk and Opportunity

- Risk: Schedule for sensor chip is very tight

  → Opportunity to skip 3rd Multi-project runs, if 2nd MPW chip is fully working

  - May submit full-size sensor engineering run in early 2021 (7 months earlier than schedule)
  - Save 0.4M RMB in funding

- Risk: 1st full-size sensor engineering runs doesn't work completed
- →If this happens, we need 2nd full-size sensor engineering runs
- → risk of not having enough fund for 2nd engineering runs (~2M RMB)

Mid-term review of MOST2 project

- Midterm review meeting (Aug 20-21)

Mid-term review of MOST2 project

- Comments from review:
  - This topic is a cutting-edge technology of high-energy particle detection,
  - Good progress of the project
  - Suggestion:
    - Check uniformity of the sensors
    - Should try to further reduce the power consumption
    - Should start testing radiation hardness of the sensor chip
    - Should pay more attention to mechanical support, air cooling , power consumption
    - → related to spatial resolution of vertex detector prototype
    - This project may be short of funding at the end, suggest to give more support

Summary

- Completed two round of CMOS sensor prototyping
  - New readout architecture to reduce pixel size to 25μm*24μm
    → Reach midterm Assessment index (实现中期指标）
  - According to TCAD simulation Radiation hardness >1Mrad total ionization dose radiation
  - → Reach midterm Assessment index (实现中期指标）
- Complete preliminary design for the followings
  - Detector module (ladder)
  - Vertex detector overall support structure
  - Data acquisition system
- Strong international connection, large impact to the community if the project success.
- Next major milestones
  - Competed full size full functionality sensors design (3rd year)
  - Manufactured support structure for vertex detector (4^{th} year)
  - Finished detector assembly and commissioning and beam test (5^{th} year)

backup

Mid-term review of MOST2 project

中期执行情况评述：（包括：1. 对课题中期进展的总体评价，是否完成预定任务、达到预期目标；2. 取得的阶段性成果和人才培养情况；3. 经费管理使用情况；4. 课题组织管理情况等；5. 检查等级建议）

该课题的工作属高能粒子探测的前沿技术，具有研究探索性质，虽然有疫情影响，但工作进展比较顺利，基本按照原进度进行，研制出 25 微米*25 微米的小型传感器芯片，做了功能测量，模拟研究给出了传感器的抗辐照性能。

主要问题及建议：（包括课题执行中存在的重大问题，对项目更好达到预期目标的具体建议等。）

除芯片的电性能外， 更需要注重一致性，信号的阈值等粒子探测方面的研究。功耗方面还需进一步降低。建议对芯片的抗辐射性能进行测量。重视达到位置分辨率指标的机械、气流、功耗等的影响。

经费可能紧张，需要给以更多支持

专家组长（签字）：

2020 年 8 月 20 日

Budget status

- Implementation rate（执行率） is about 60% for first two years
  - Cost profile is not linear, expect to spend more in 3rd and 4th year for detector fabrication
  - Testing fee(测试加工费）is mainly allocated for sensor chip engineering runs (to be done in 2021)
  - Device fee: will purchase gantry system for automatic assembly in next 1~2 months

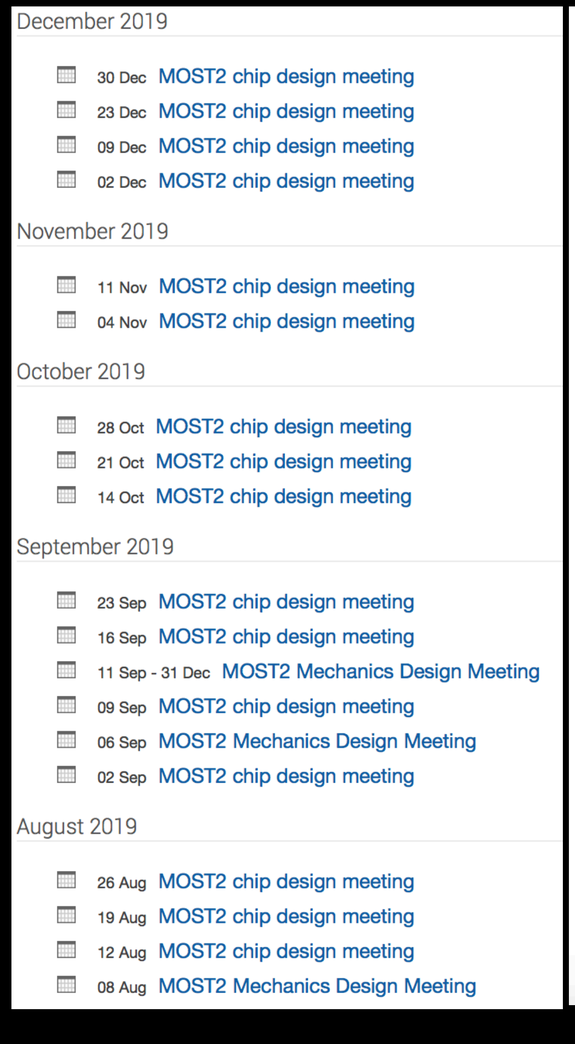
序号	预算科目名称	total	Budget until Midterm	Implementation until 2020/6/30	Rate of expense/total budget	Rate of expense/midterm budget
2	（一）direct fee	1047.700	402.583	234.84	22.41%	58.33%
3	1、device fee	196.300	176.2	53.11	27.06%	30.14%
4	（1）purchase device	196.300	176.2	53.11	27.06%	30.14%
7	2、material fee	235.66	112.49	52.01	22.07%	46.24%
8	3、testing fee	299.8	9.45	2.20	0.73%	23.28%
9	4、power fee	20.64	8.26	0.00	0.00%	0.00%
10	5、travel/conference/international communication	123.81	39.9	44.80	36.18%	112.28%
11	6、publication	8.5	3.4	1.90	22.35%	55.88%
12	7、labor	157	50.5	81.27	51.76%	160.93%
13	8、consult	6	2.4	1.56	26.00%	65.00%

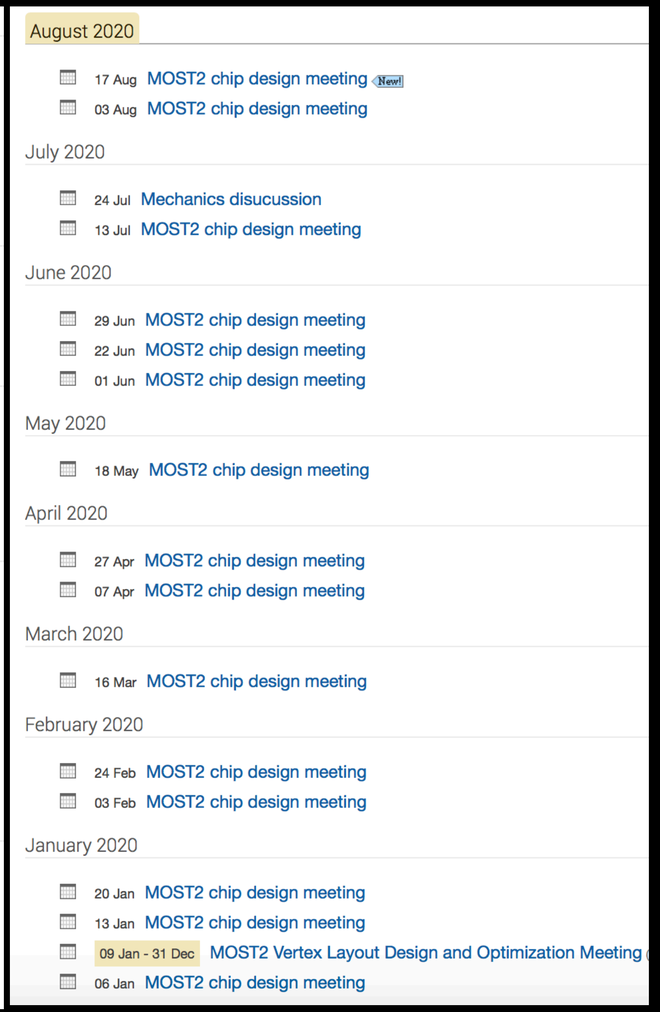
Internal organization

Task 2 meetings

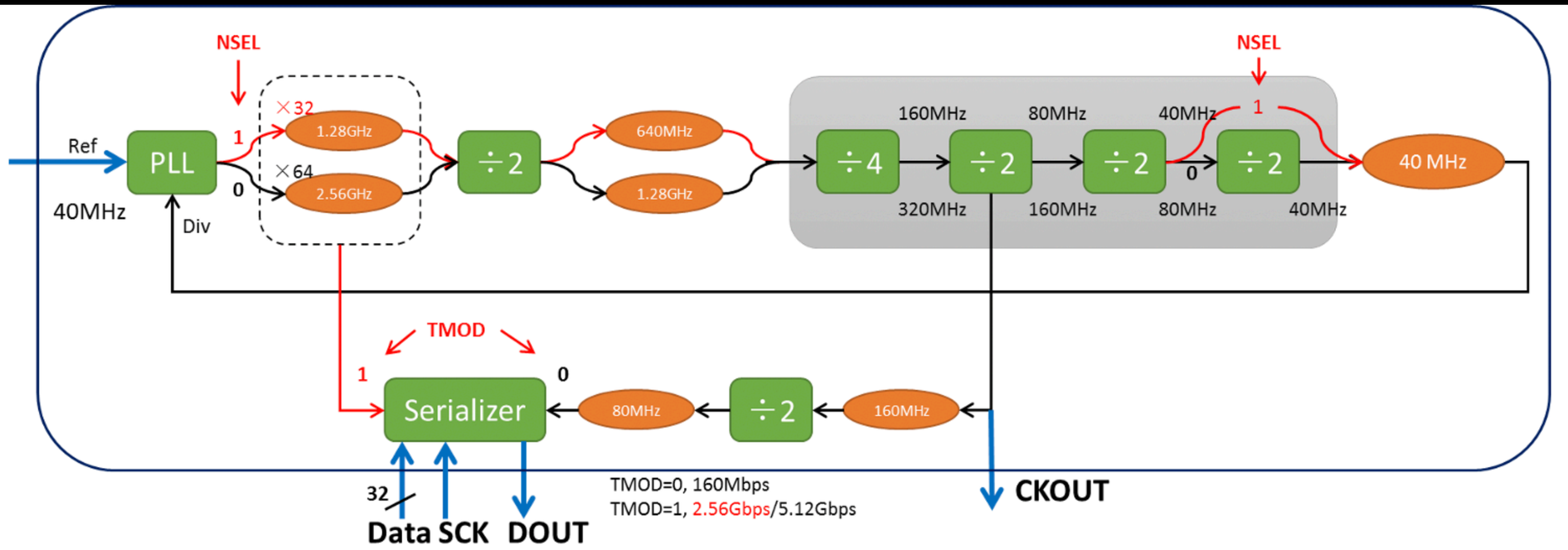
- CMOS sensors chip design meeting (weekly)
- Vertex detector overall design meeting (weekly)
- Full-day internal review meeting (every 3 months)
- Institutes worked closely
- Project leader followed closely the progress

Task 2 meetings





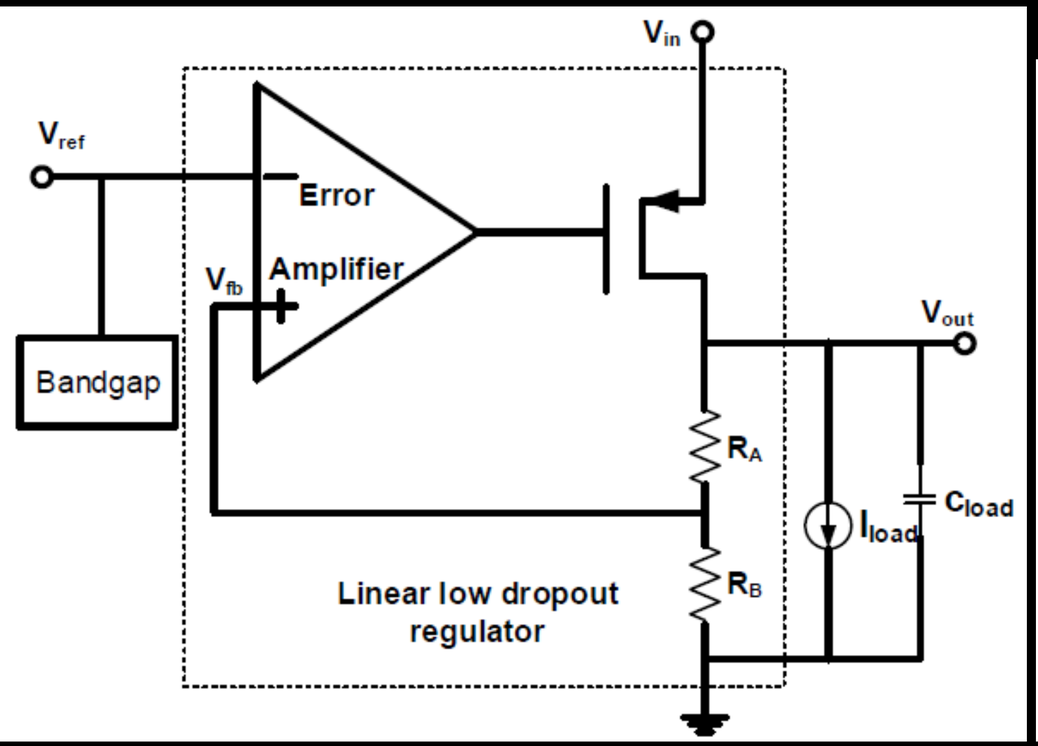
Backup:外围电路模块——高速数据接口



- **Tuning range @ SS 85**
  - 280MHz ~ 2.96GHz
- **Current range @ SS 85**
  - 3.57mA ~ 16.46mA
- **Phase noise**
  - ~ -100dBc/Hz@1MHz offset
- **Current @ 2.56GHz & FF -40**
  - 16.09mA
- **Current range @ FF -40**
  - 6.85mA ~ 26.26mA

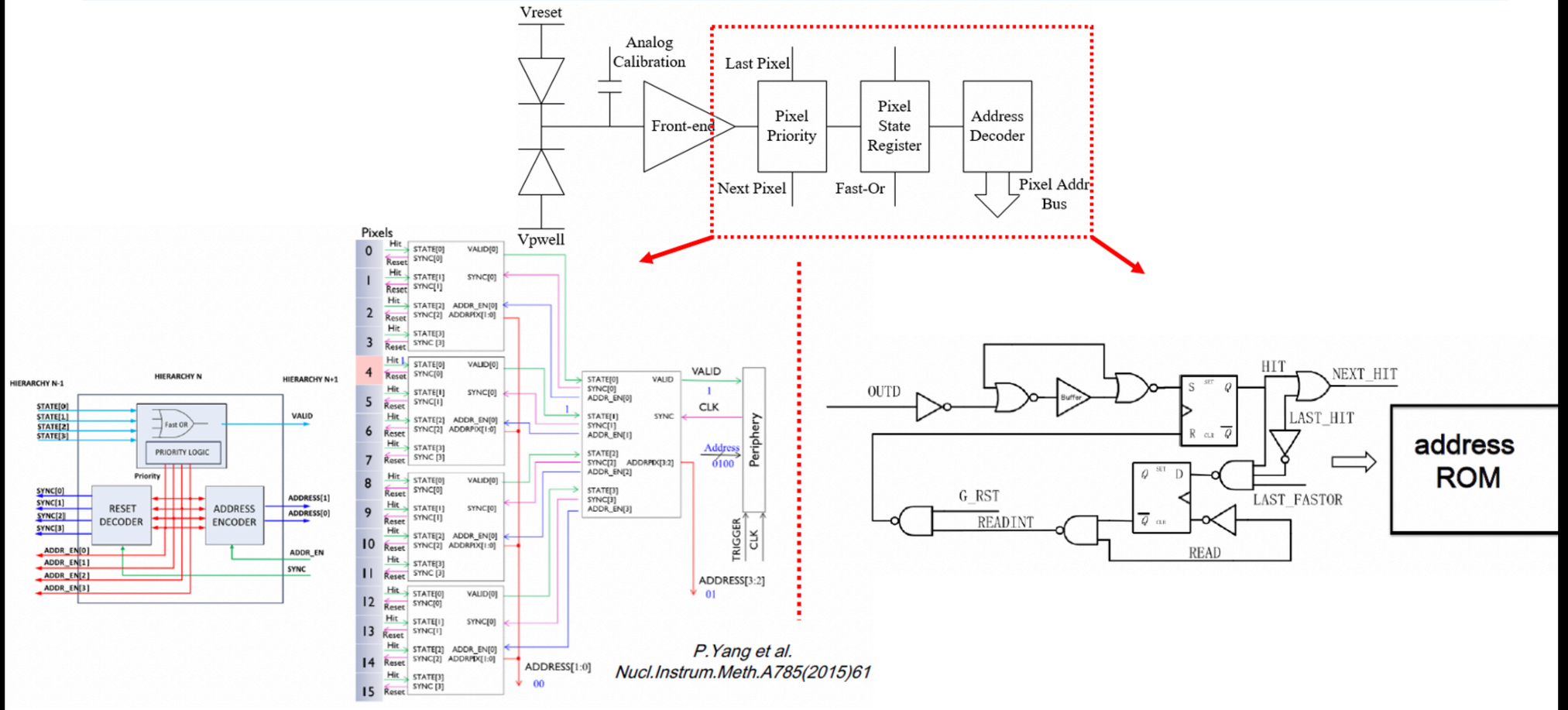
- **NSEL: 0→2.56GHz, 1→1.28GHz**
- **ISEL1/ISEL0: 00/01/10/11 → 25/50/75/100μA**
- **BSEL： 0→3kΩ, 1→8kΩ**
- **TMOD: 0→Trigger, 1→Triggerless**

Power managements in TaichuPix chip



Parameters	Value
Input voltage	<2 V
Output voltage	1.8 V
Maximum output current	200 mA
Load capacitance	~200 nF
TID	> 1 Mrad.
Maximum dropout voltage	0.2 V
Fully integrated on-chip	
Low noise, High PSR	

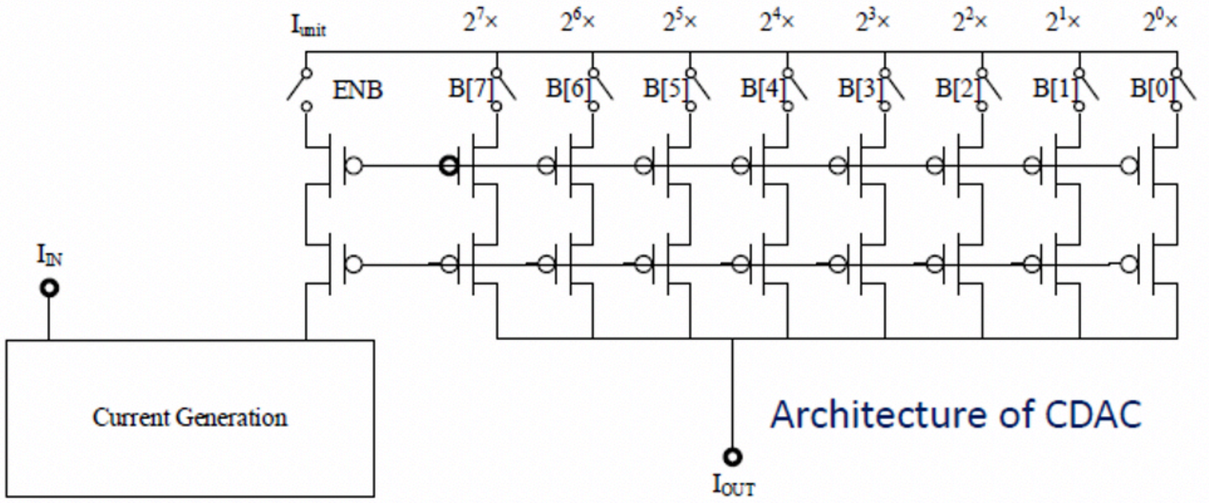
Pixel architecture – parallel digital schemes



- **Two parallel digital readout architectures were designed:**
  - **Scheme 1： ALPIDE-like: benefit from the proved digital readout in small pixel size**
  - **Scheme 2： FE-I3-like: benefit from the proved fast readout @40MHz BX (ATLAS)**

偏置产生模块——多通道DAC

- **Characteristics**
  - Voltage DAC (VDAC)
    - 10 bit
    - LSB: 1.56 mV
    - Range: 0 – 1.6 V
  - Current DAC (CDAC)
    - 8 bit
    - LSB: 40 nA
    - Range: 0 nA ~ 10.2 μA

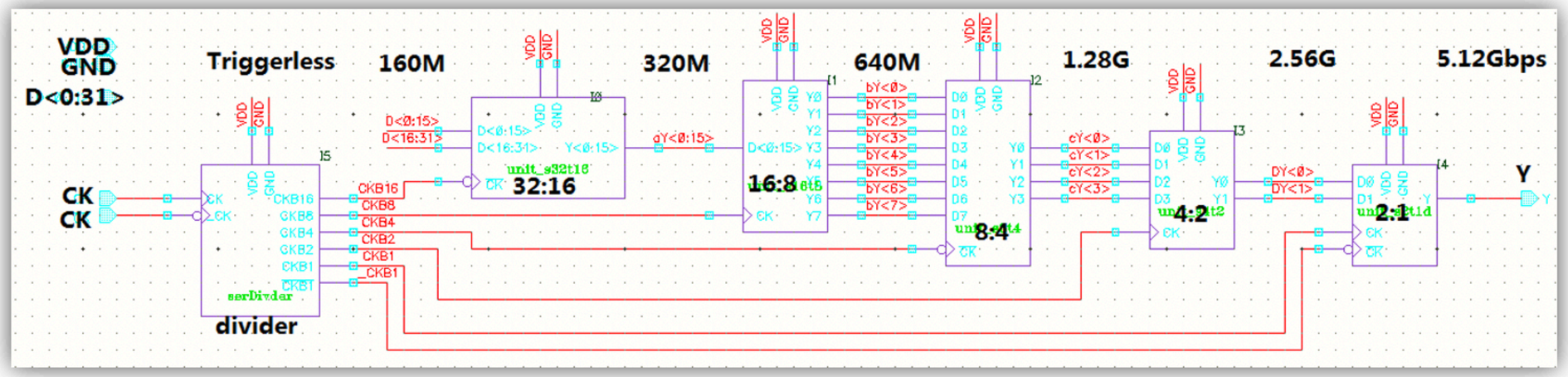


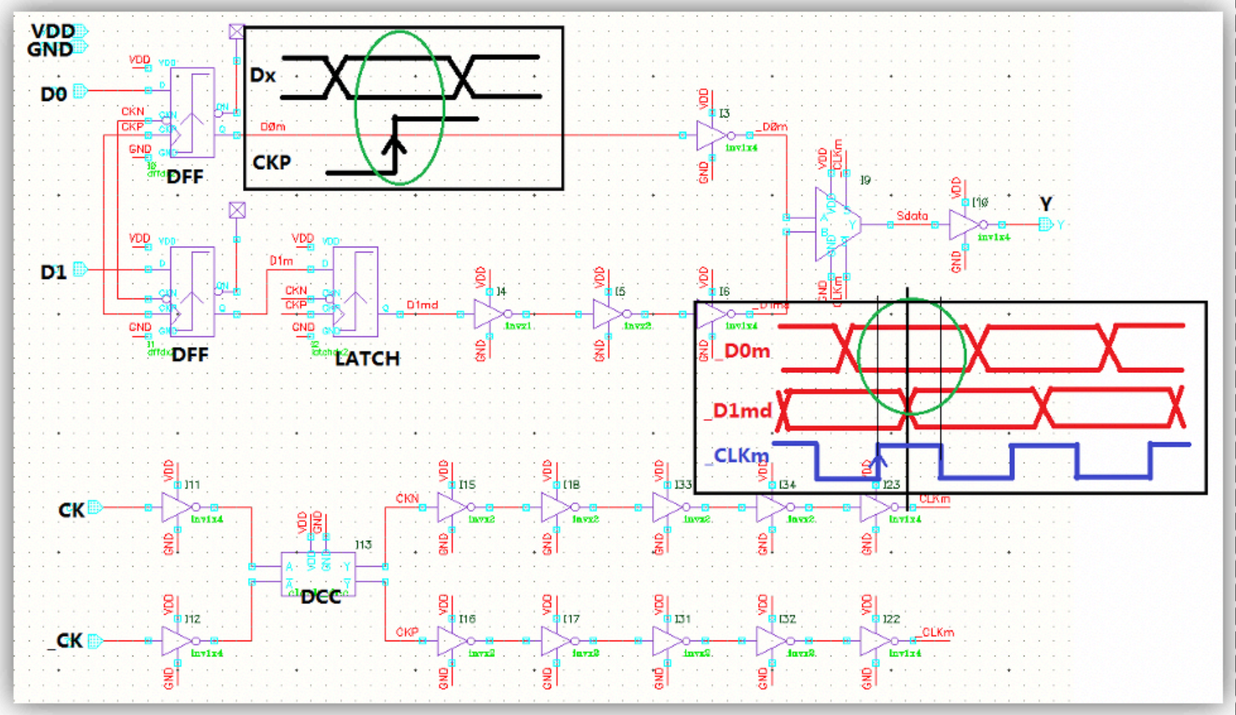
Architecture of CDAC

- **Current DAC**
  - Current mirror
  - Segmented architecture
    - 4 most significant bits (MSB)
      - ★ thermometer decode
    - 4 least significant bits (LSB)
      - ★ binary weighted
  - Output impedance
    - Min: 104KΩ
    - Max: 43 MΩ

- **Voltage DAC**
  - Current bias generation block
    - VBG: output of bandgap ~ 0.8 V
    - I_{unit} ~ 20 μA
  - Negative feedback to stabilize VBG @ 0.8 V
  - Current mirror with resistor load
  - Segmented architecture
    - 4 most significant bits (MSB): thermometer decode
    - 6 least significant bits (LSB): binary weighted

外围电路模块——高速数据接口





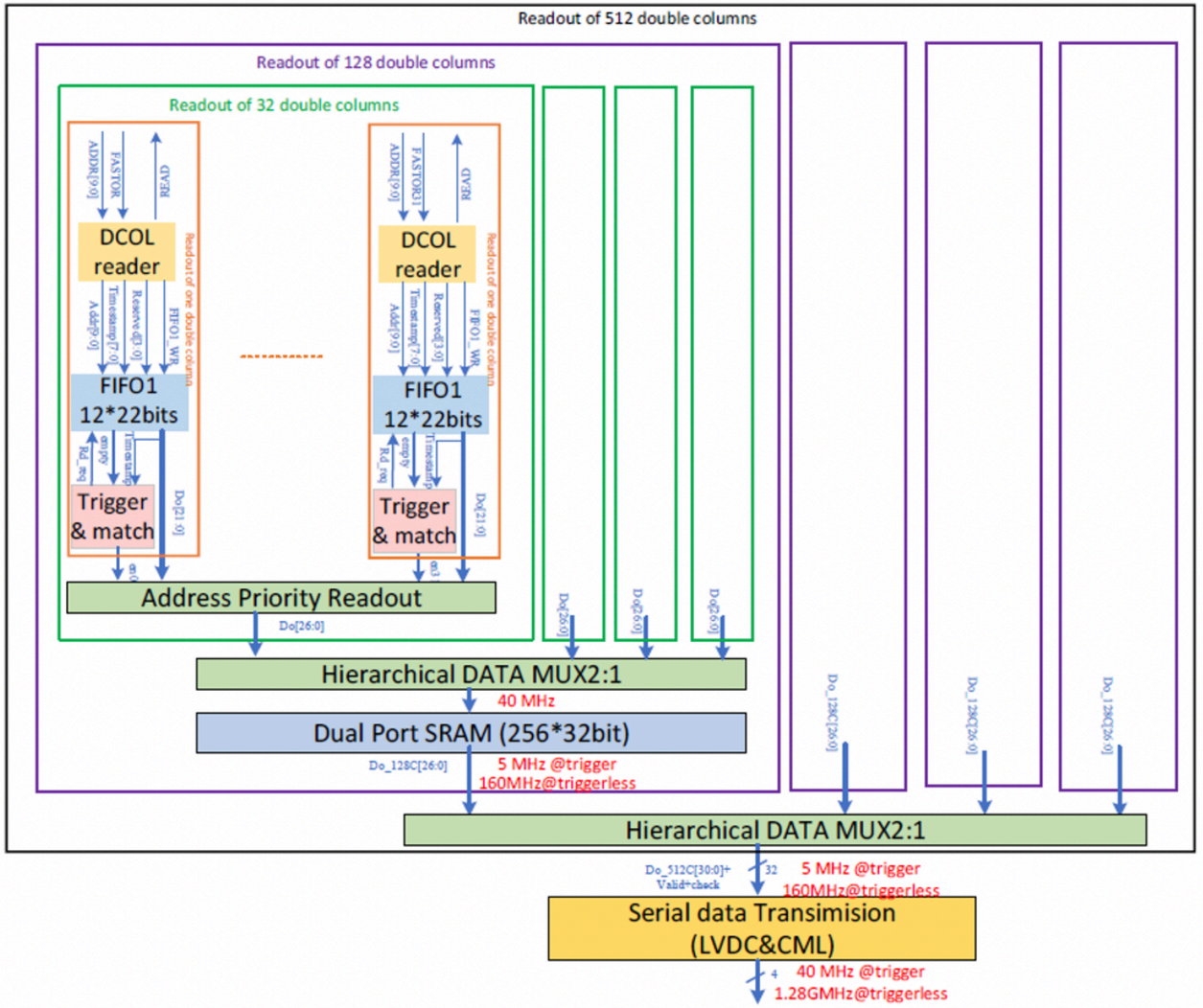
- **Timing**
  - Stage timing
    - Data sampling
  - Unit timing
    - Data sampling (Dx--CKP)
    - MUX (_Dxm--CLK)
  - 1UI = 500ps @ 2Gbps
    - Time margin is very small at high speed
    - Delay of data and clock
- **Big-small eye in eye diagram**
  - 50% DC of clock

Status of TaichuPix2

- **Major bugs (were tried to be) fixed**
  - **New IO rings were used, without DNW soft connect issues**
  - **DAC stability improved with higher phase margin**
- **Pixel readout optimized**
  - **To make larger headroom for the timing**
    - **Data latching @ 1clk -> 1.5clk**
  - **Address encoder pull-up added to avoid high-Z state**
- **Pixel analog new attempts**
  - **Smaller pixel area**
    - **Possible to be 24um*25um**
  - **One branch with enclosed gate for better TID**
- **X-chip interconnections attempts**
  - **SPI buses, PLL clock reference, reset signal, are possible to be propagated by chip-chip wire bonding**
  - **Save some routing space for the flex cable design**

外围电路逻辑

Readout architecture



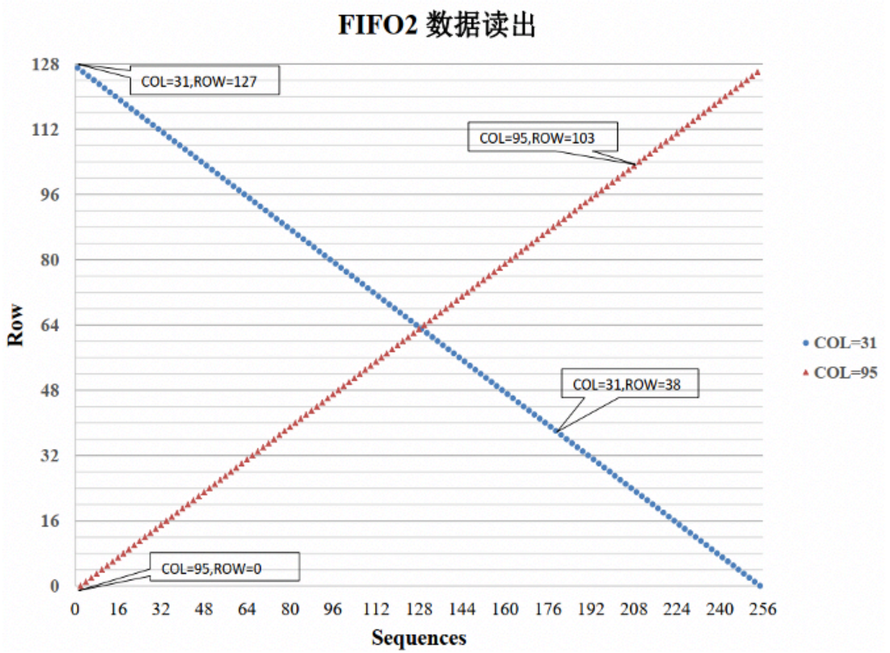
列电路：

- 列端记录timestamp
- Trigger模式，在FIFO1输出时丢弃不匹配数据，FIFO2只存储时间戳匹配的数据

列并行读出方式：

- 512个双列并行读出以满足dead time 的要求，每列对应一个FIFO1
- 512分为4个128双列，每128对应一个FIFO2
- 128分为4个32双列，32双列内部采用数据驱动（分两级，8个一组），32双列之间轮询读出。轮询策略是每块读一个数就转读下一个块以避免数据拥塞。

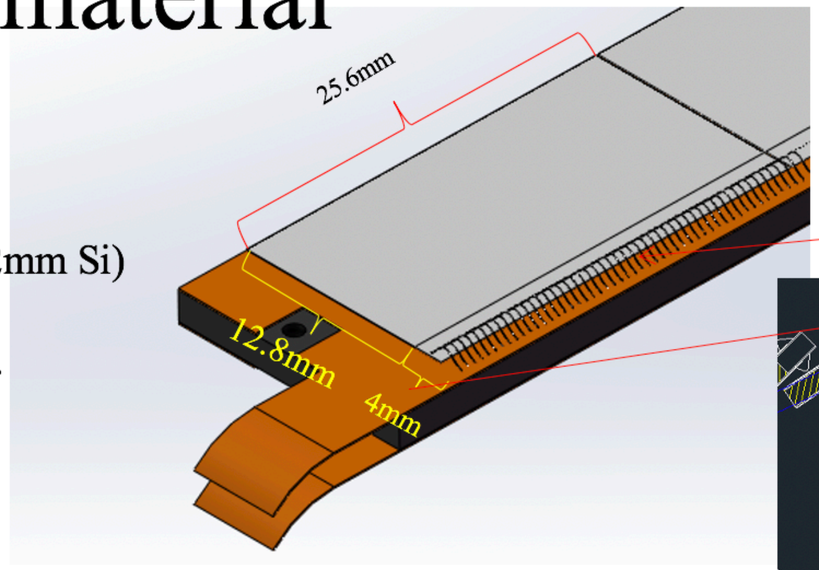
Pixel digital functionality



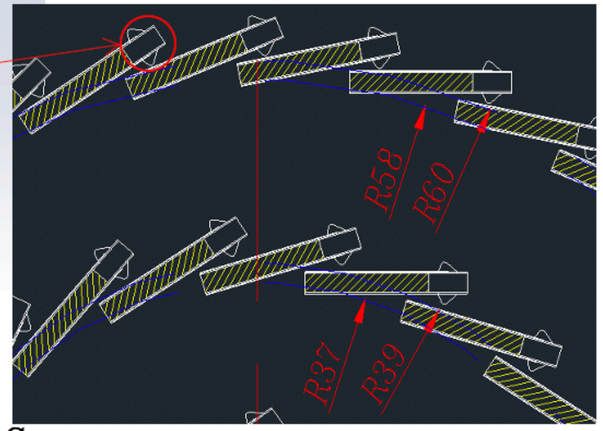
- Pixel digital's functionality was partially proved, some bugs were found
- Tested by the self-debug mode supported by the periphery logic
- The row addresses can be traversed, however, the column addresses was found unable to be correctly reset
- Bugs located in layout, modified in Tcpx2
- Periphery block ran reliably during the functional test

Pixel module material

Top view:
active area: 12.8mm × 25.6mm
dead area: 4mm × 25.6mm (only 2mm Si)
Side view:
5 symmetric layer, gluing together.

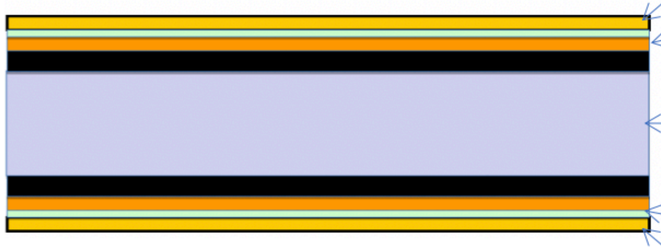


Al wire



One half dead area:

Sensor(Si, 25um)
Al wire
glue(Epoxy, 7.5um)
Al(17.8um)
Kapton(50um)
Glue(Epoxy, 15um)
Ladder support(carbon fiber,175um)



Sensor(Si, 50um)
glue(Epoxy, 15um)
Al(17.8um)
Kapton(50um)
Glue(Epoxy, 15um)
Ladder support(carbon fiber,350um)
Glue(Epoxy,15um)
Kapton(50um)
Al(17.8um)
Glue(Epoxy, 15um)
Sensor(Si, 50um)

(1) Sensor
(2) Flex cable
(3) Ladder support
(4) Flex cable
(5) sensor

Polyimide
Adhesive
Plating Al
kapton
Plating Al
Adhesive
Polyimide

recent discussion shows that we need add more material into flex cable

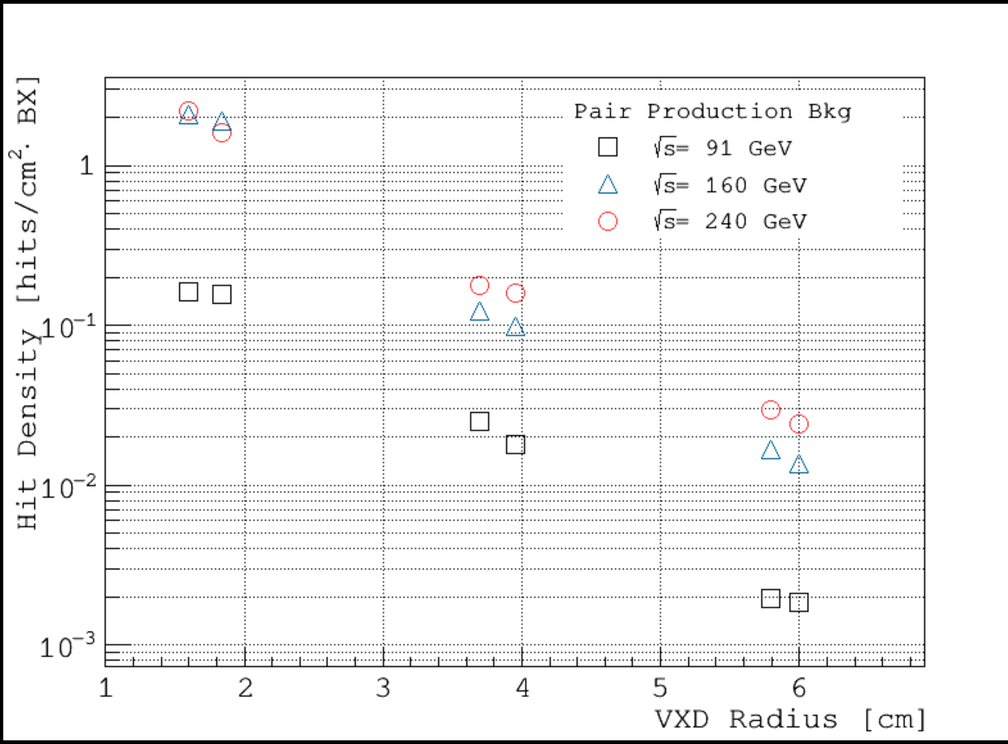
Goal for the second year

- Achieve the target in task book for the 1st and 2nd years
  - Completed preliminary engineering designs of support structure for vertex detector prototype
  - Completed second sensor CMOS chip prototyping
  - Completed data acquisition system for sensor testing

年度	任务	考核指标
2019 年 5 月 | 2020 年 4 月	细化探测器整体支撑结构设计，绘制该结构的工程图，开始加工模块的结构；对第一次 MPW 的芯片做测试以验证其功能，其中包括初步小剂量的辐照测试；完成芯片的像素阵列与外围读出电路等功能模块之间的集成，并进行第二次多项目晶圆（MPW）流片加工；开始设计探测器单元模块的读出电子学与数据获取系统。	1. 完成传感器芯片上所有功能模块的初步设计，并把各功能模块的设计集成，完成第二次传感器流片的设计，传感器像素单元尺寸小于或等于 25 微米 × 25 微米，通过仿真初步验证其抗辐照性能。 2. 研制出单个传感器芯片的读出电子学、数据获取系统，对第一次 MPW 流片传感器芯片进行初步测试。

Main specs of the full size chip for high rate vertex detector

- Bunch spacing
  - CEPC Z+Higgs (240GeV): 680ns;
  - WW threshold scan (160GeV): 210ns;
  - CEPC Z pole runing (90GeV) Z: 25ns
- High Hit density
  - 2.5hits/bunch/cm^2 for Higgs/WW runs
  - 0.2hits/bunch/cm^2 for Z pole running



For Vertex	Specs	For High rate Vertex	Specs	For Ladder Prototype	Specs
Pixel pitch	<25μm	Hit rate	120MHz/chip	Pixel array	512row×1024col
TID	>1Mrad	Date rate	3.84Gbps --triggerless ~110Mbps --trigger	Power Density	< 200mW/cm^2 (air cooling)
		Dead time	<500ns --for 98% efficiency	Chip size	~1.4cm×2.56cm