Update progress on TPC R&D

Huirong Qi and Zhi Deng

Zhiyang Yuan, Yiming Cai, Yue Chang, Hongyu Zhang, Ye Wu, Jian Zhang, Wei Liu, Yulan Li, Hui Gong

IHEP and Tsinghua

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Outline

- Status of TPC detector
- Status of ASIC R&D
- Status of the collaboration

Preliminary results

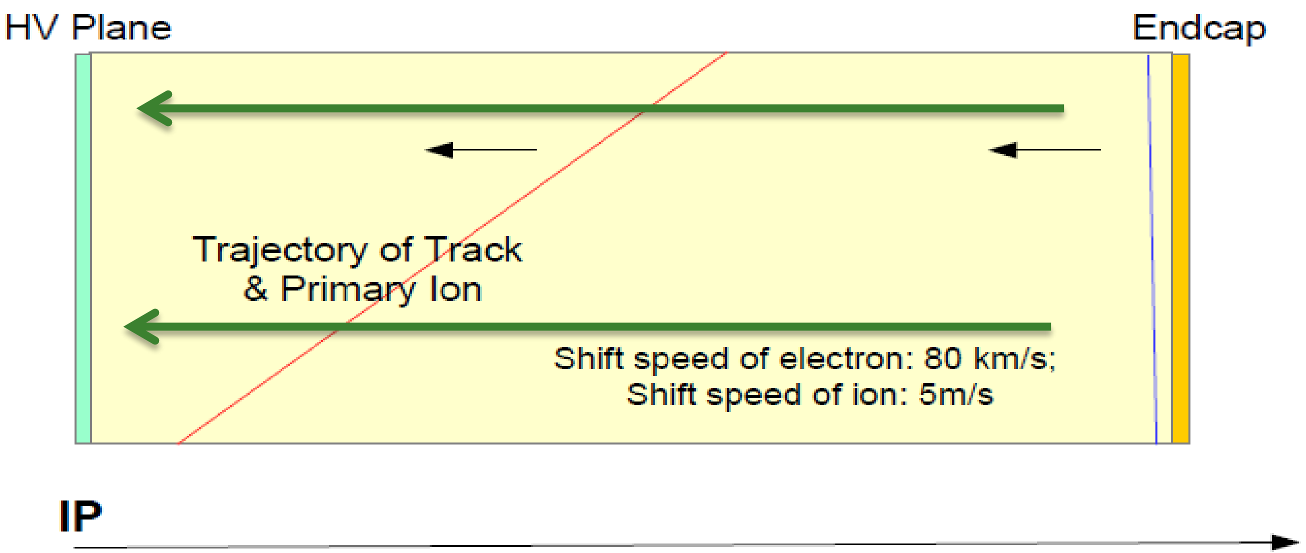
- Status of the prototype

Motivation

TPC limitations for Z

- Ions back flow in chamber MOST1
- Calibration and alignment NSFC
- Low power consumption FEE ASIC chip MOST1

	International collaboration	Leading institutions
MOST1 2016.6-2021.6	LCTPC	IHEP, Tsinghua
NSFC 2016.1-2020.12		IHEP, Tsinghua

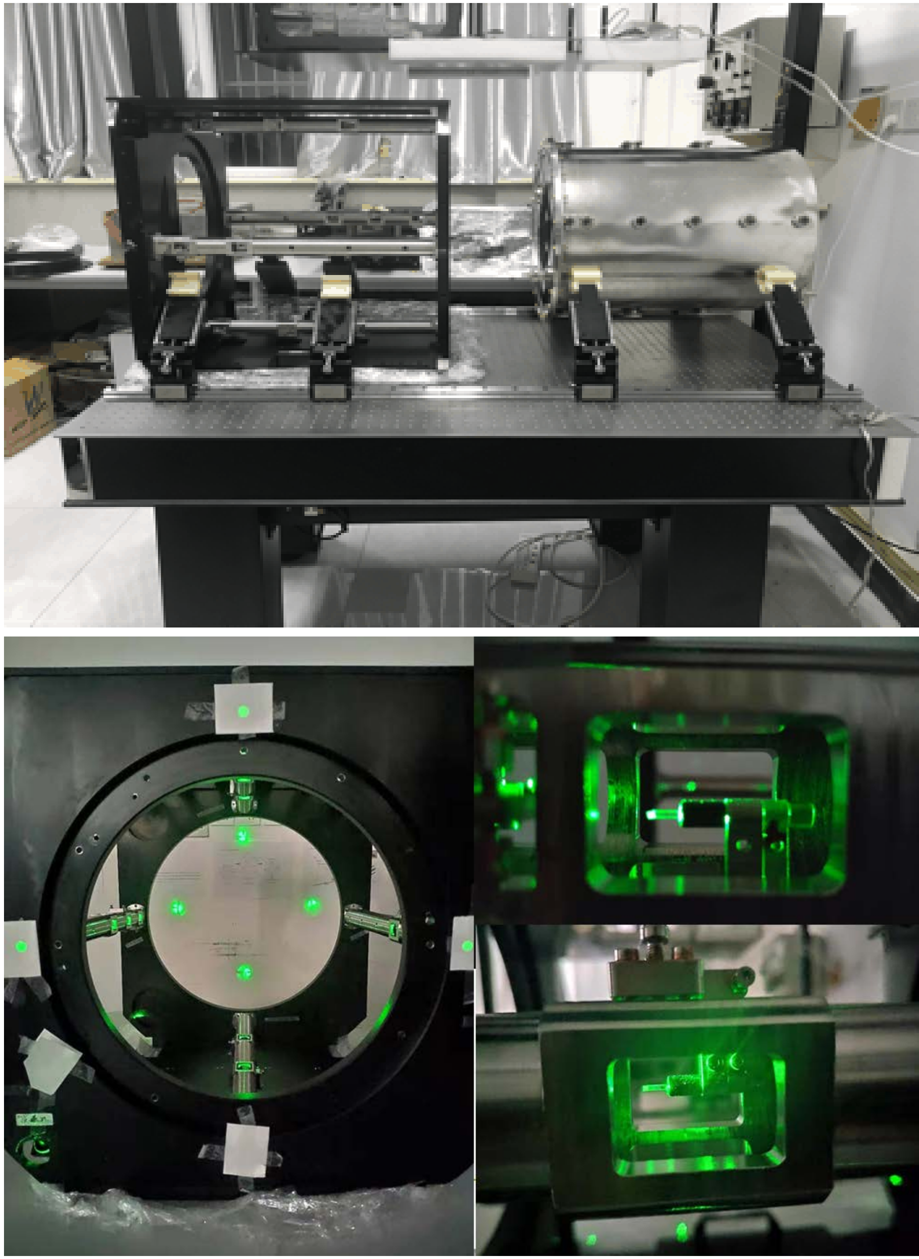


Compare with ALICE TPC and CEPC TPC

Study of TPC prototype

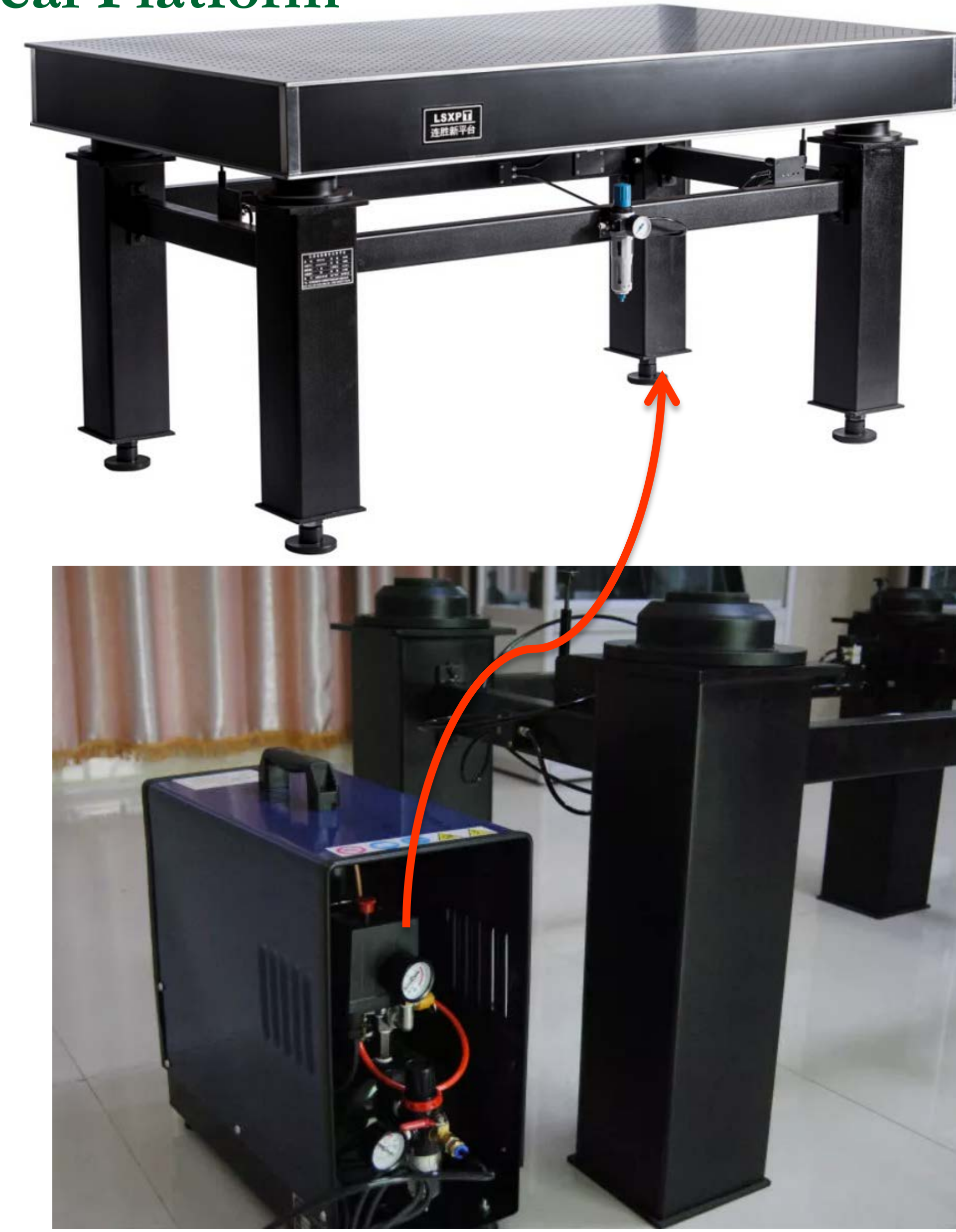
TPC prototype features:

- Anti-vibration Pneumatic optical Platform
  - 1.2m×0.8m
- 266 nm UV laser beam split installation
  - 42 UV laser beams
  - 0.75mm diameter of laser beam
  - 9 layer along the drift length
- TPC detector
  - TPC chamber
  - High voltage crate
  - 1280 channels readouts
- Q-smart laser device
  - Repeat frequency: 1Hz-20Hz
  - Initial power: 20mJ/pulse
  - Duration of the pulse: 5ns



Photos of the prototype

Anti-vibration Pneumatic optical Platform



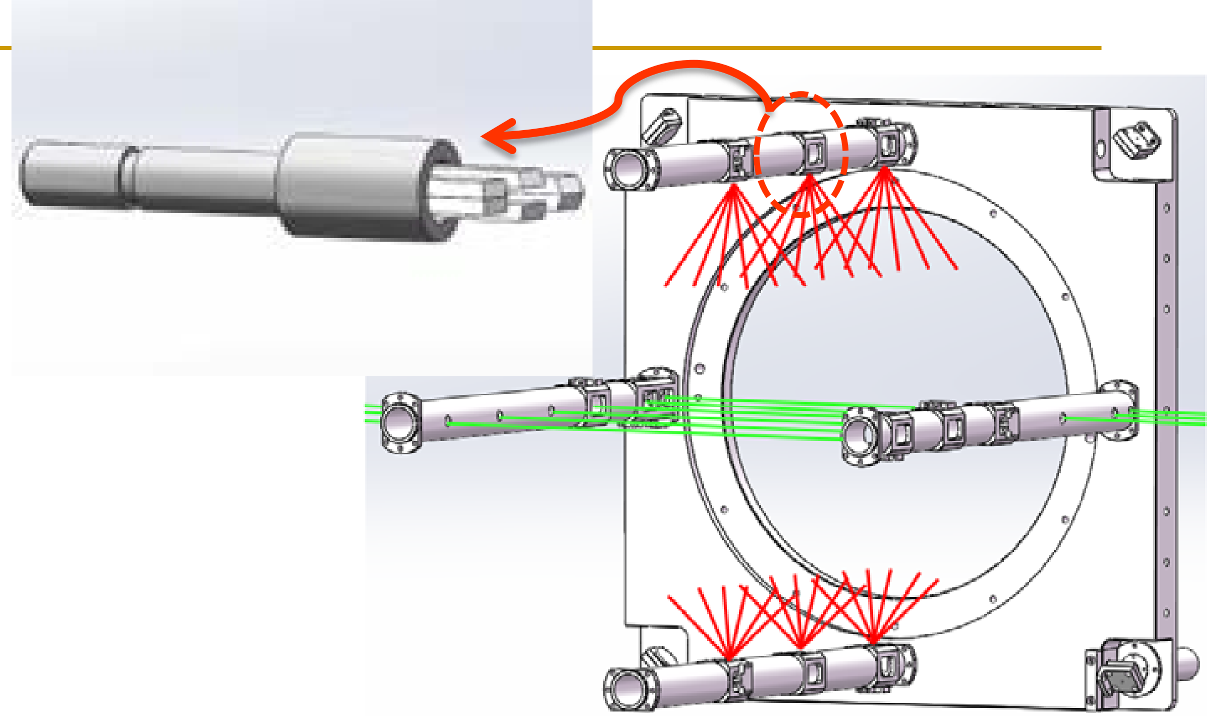
Technical Parameters：

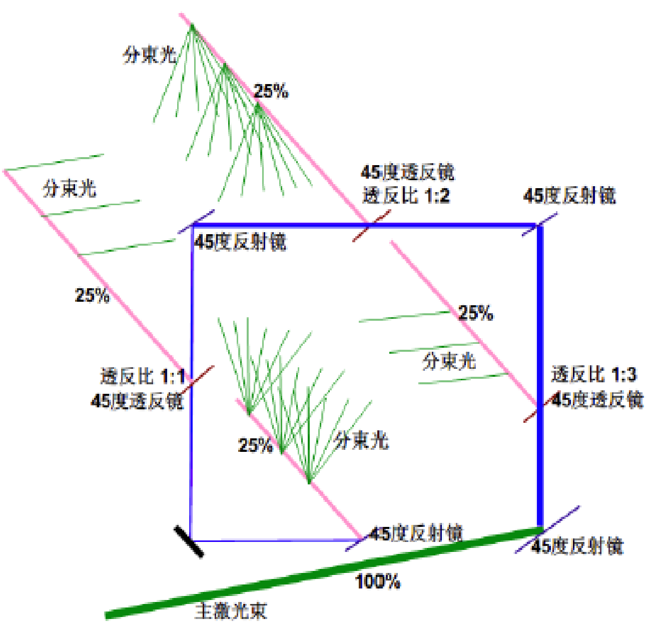
- Self balancing and centering with air spring as well as pendulum bar
- Provide excellent vibration isolation performance in both vertical and horizontal direction
- Auto inflation system
- High density honey comb core breadboard
- Surface Roughness: 0.5-0.6μm
- Flatness/Unevenness: 20μm
- Inherent Frequency: 1.5-2Hz
- Amplitude: <1μm

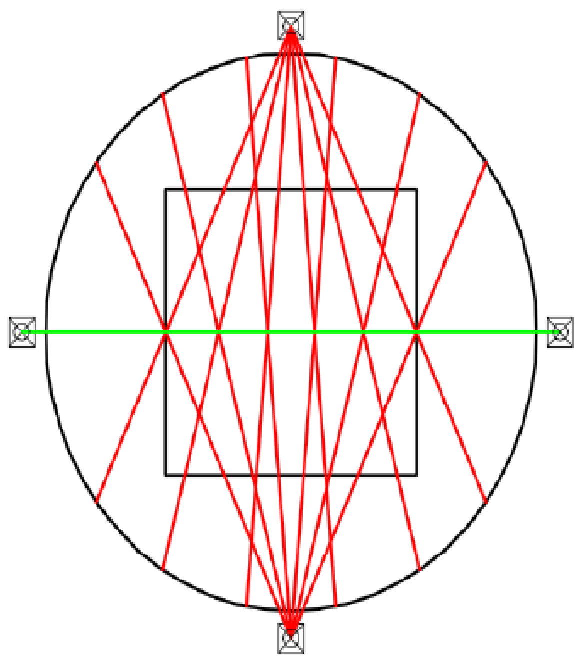
Laser map

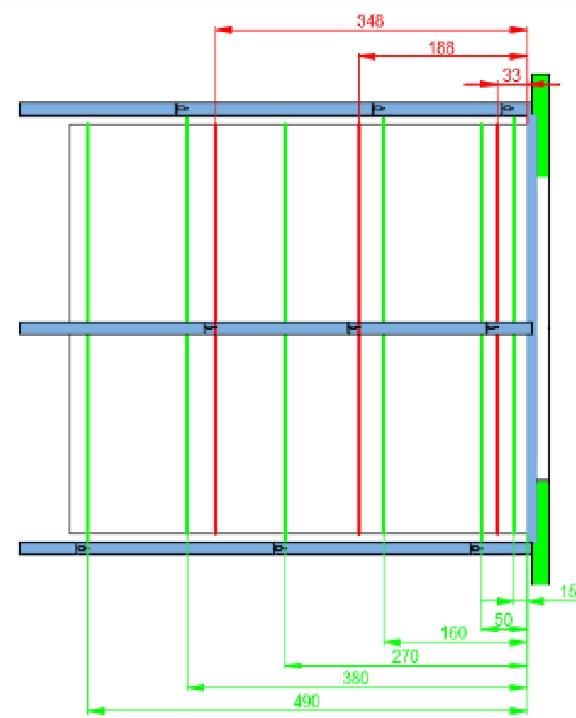
Laser map parameters：

- 266 nm UV laser beam
    - 42 UV laser beams
    - Along drift length
    - Reflection mirror array(±5°，±15°，±25°)





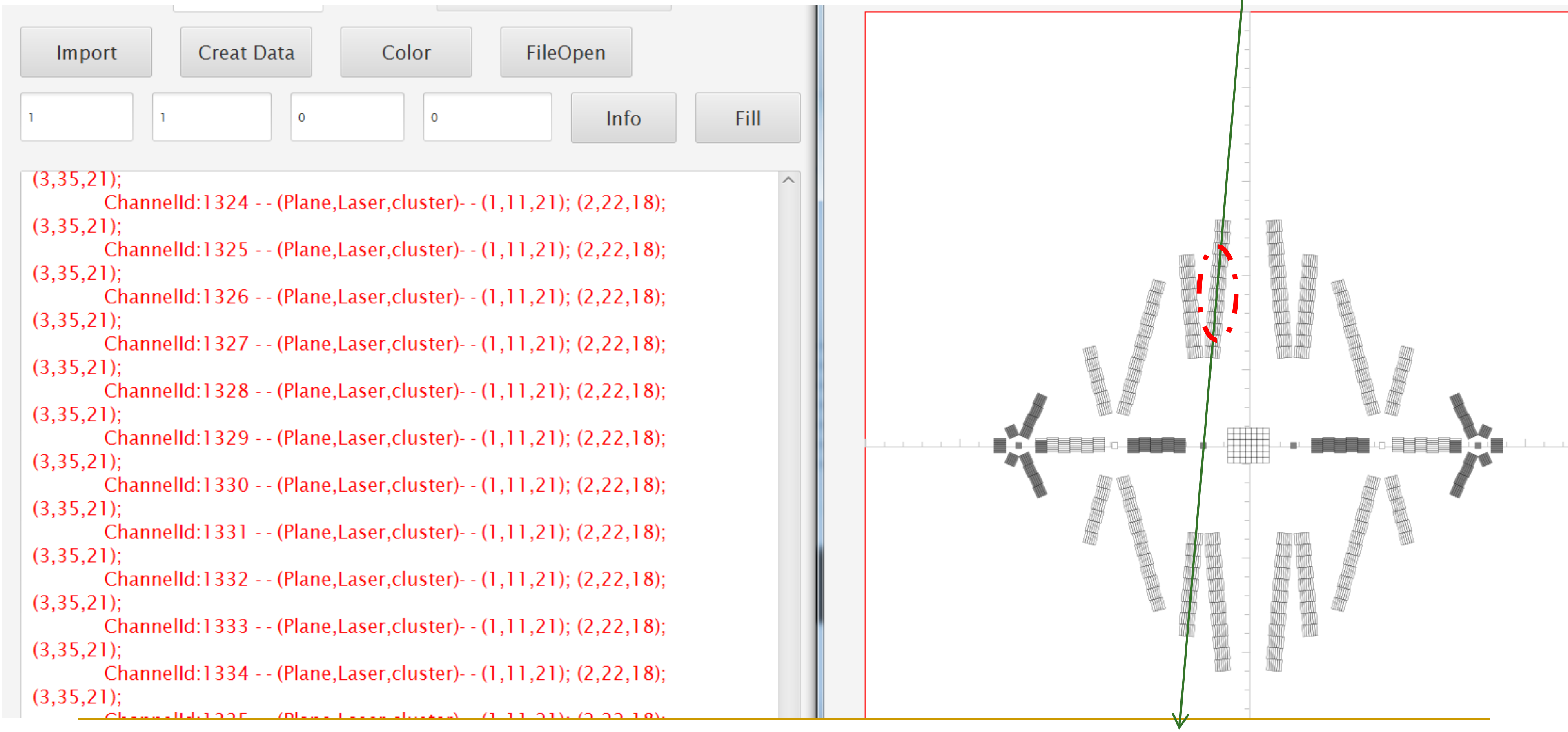




Event display interface @V2.1

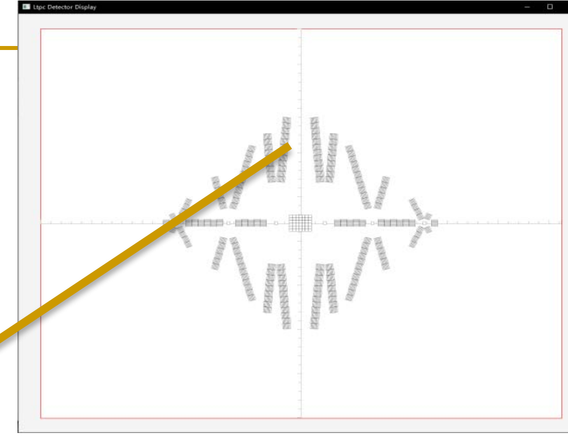
- Event display software
  - Integrated with DAQ software packages
  - Event and some information display interface developed
  - Energy spectrum

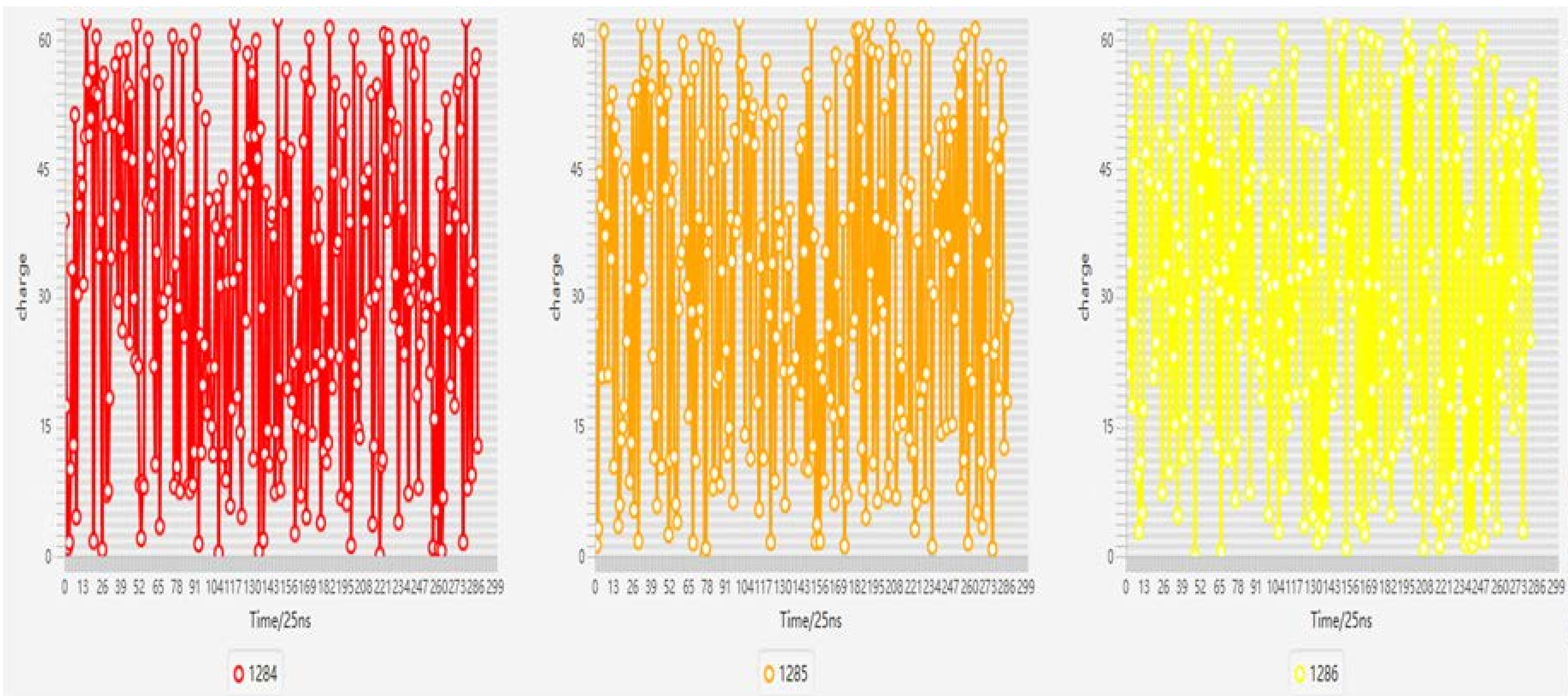
UV Laser



Noise of adjacent pads

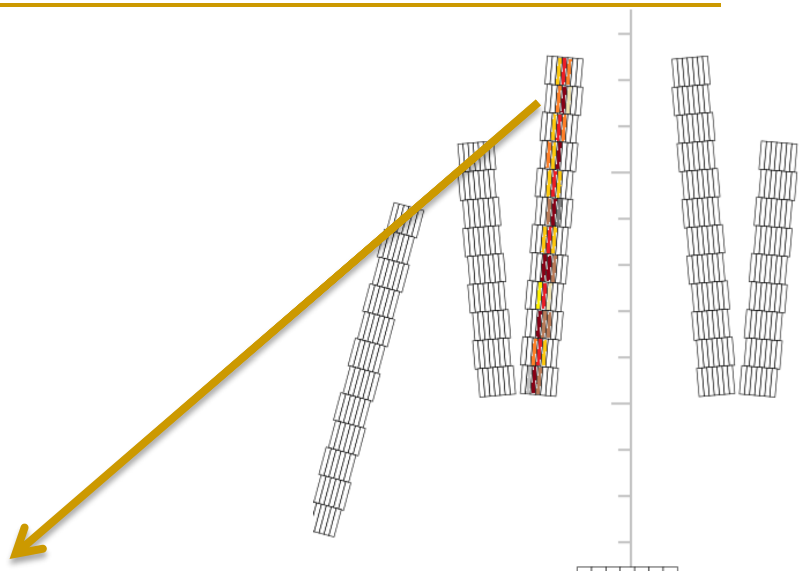
- Noise of the adjacent pads
  - Click and three figures display
  - HV of the detector and field cage: ON
  - Waveform sampling results: 25ns
  - Laser power: ON
  - Baseline uniformity to zero

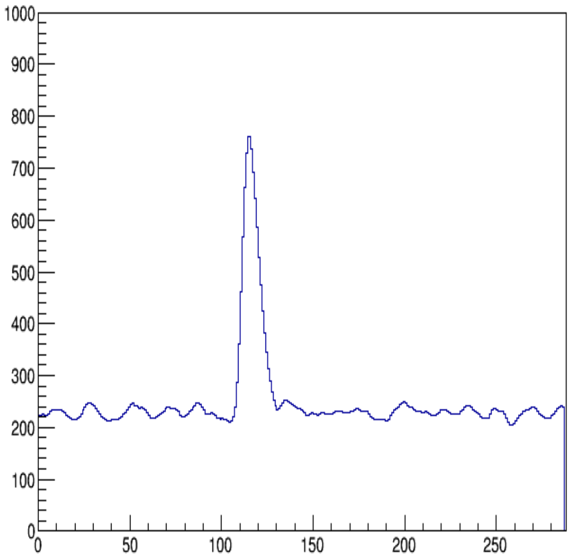


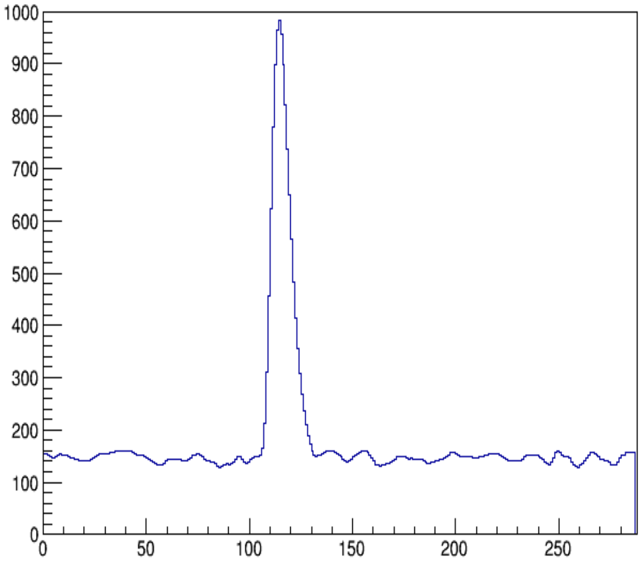


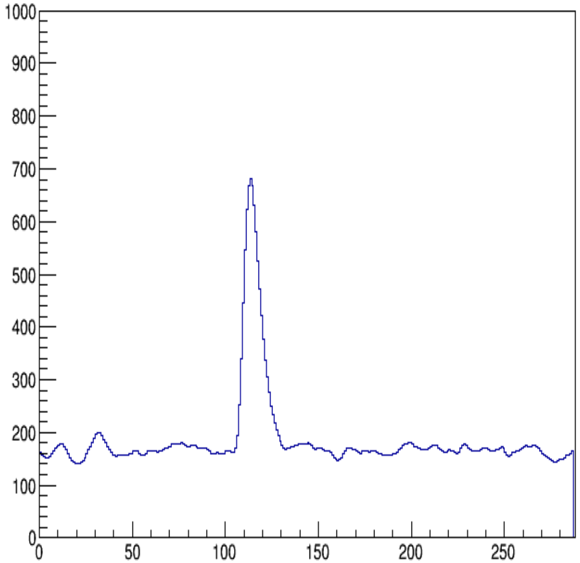
Signals of adjacent pads

- FEE Signal of the adjacent pads
  - HV of the detector and field cage: ON
  - Waveform sampling results: 25ns
  - Laser power: ON
  - Keep the original baseline
  - FEE gain:20mV/fC
  - Detector gain: 4500-5000



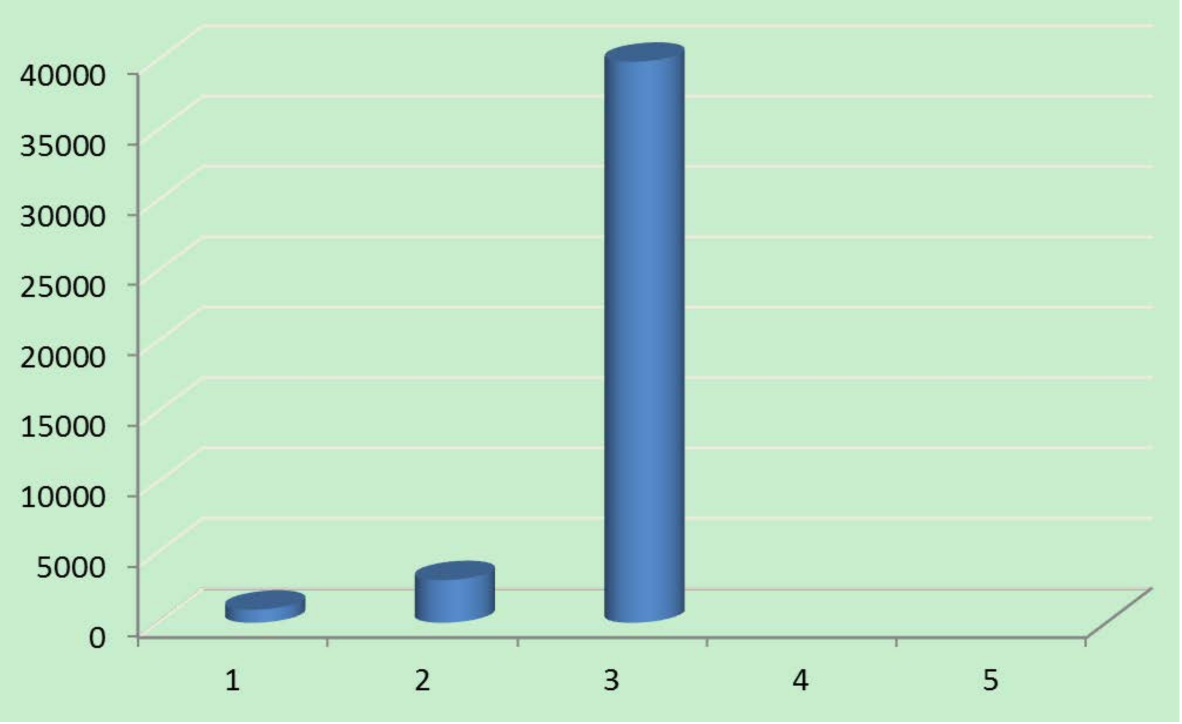






Resolution

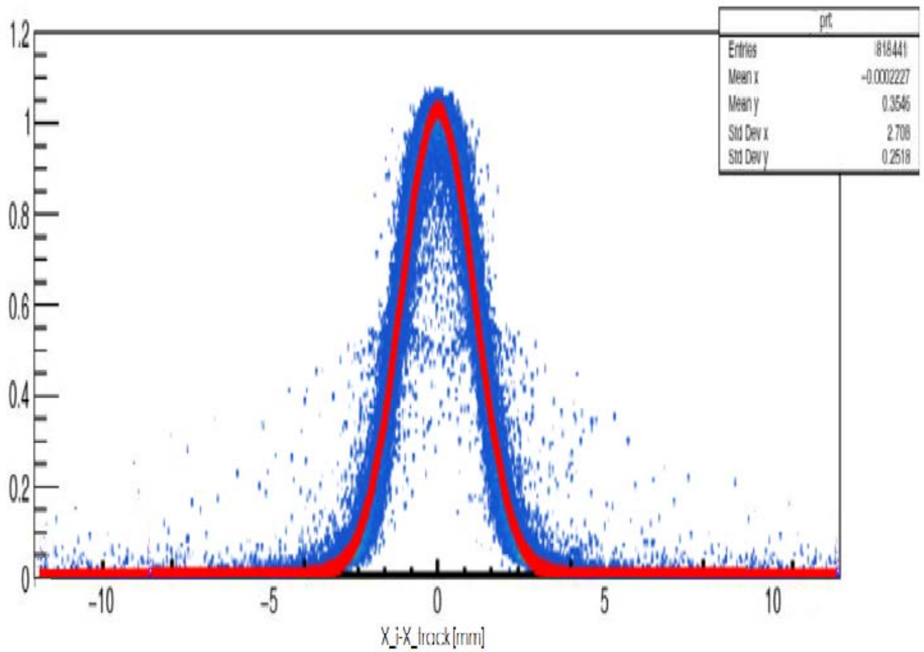
- Laser size: Φ0.75mm
- Gaussian laser profile
- Pad size: 0.95mm× 5.9mm
- Three adjacent pads : >92%

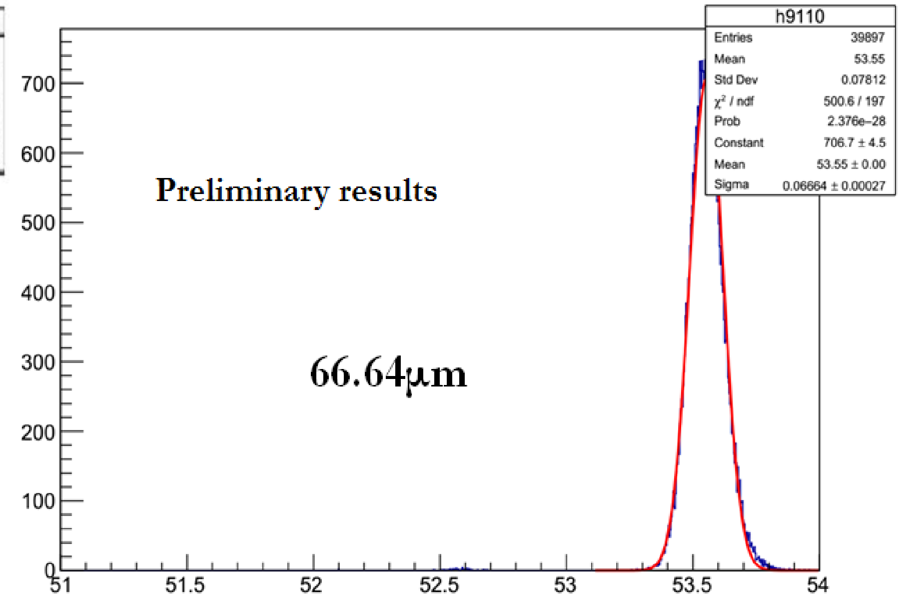


PRF analyzing (first step)

- **Pad Response Function (PRF)**
- **Drift length: 33mm**
- **Laser size: Φ0.75mm**
- **Gaussian laser profile**

$$PRF(x, r, w) = \frac{\exp[-4\ln 2(1-r)x^2/w^2]}{1+4rx^2/w^2}$$

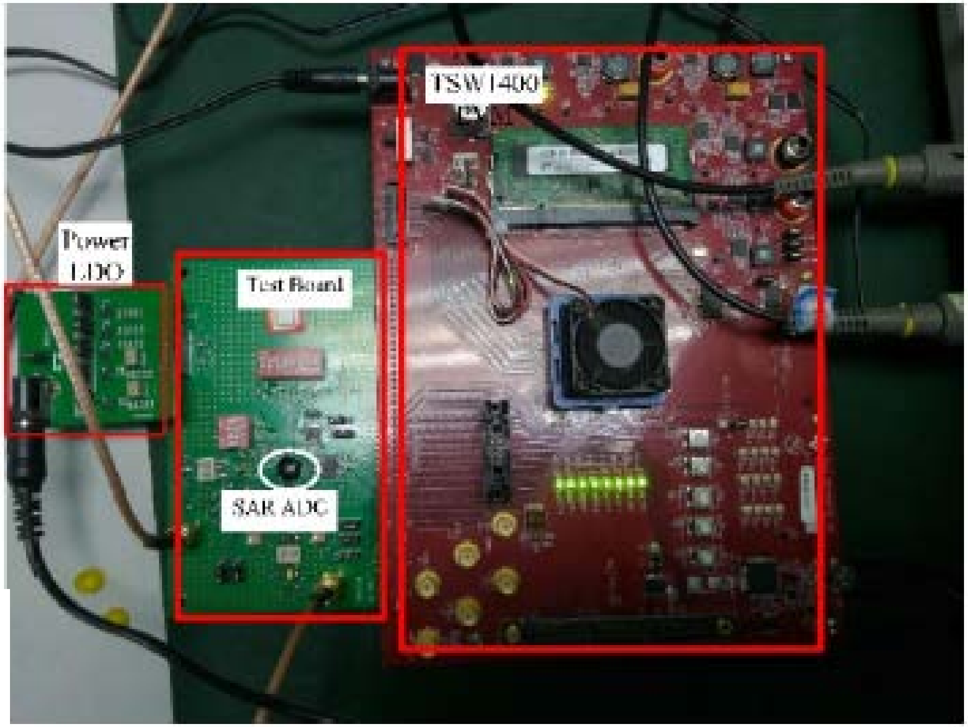




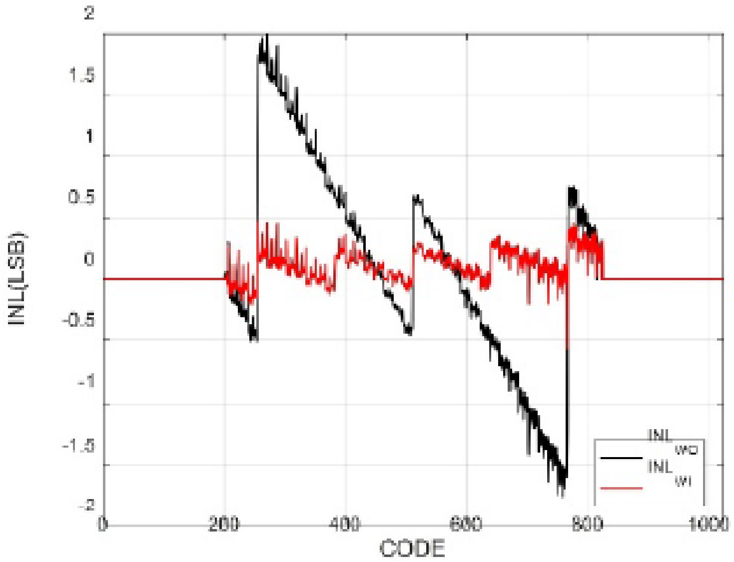
- **Status of ASIC R&D**

ASIC in 65nm CMOS

- Power consumption distribution of SAR ADC
- INL of SAR ADC with and without calibration
- Less than 0.6 LSB after calibration



The test setup for the SAR ADC



Module Name	Power (mW)
Total Chip	4.0
Reference Buffer	0.25
SAR ADC Core	1.0
Clock Generation	2.75

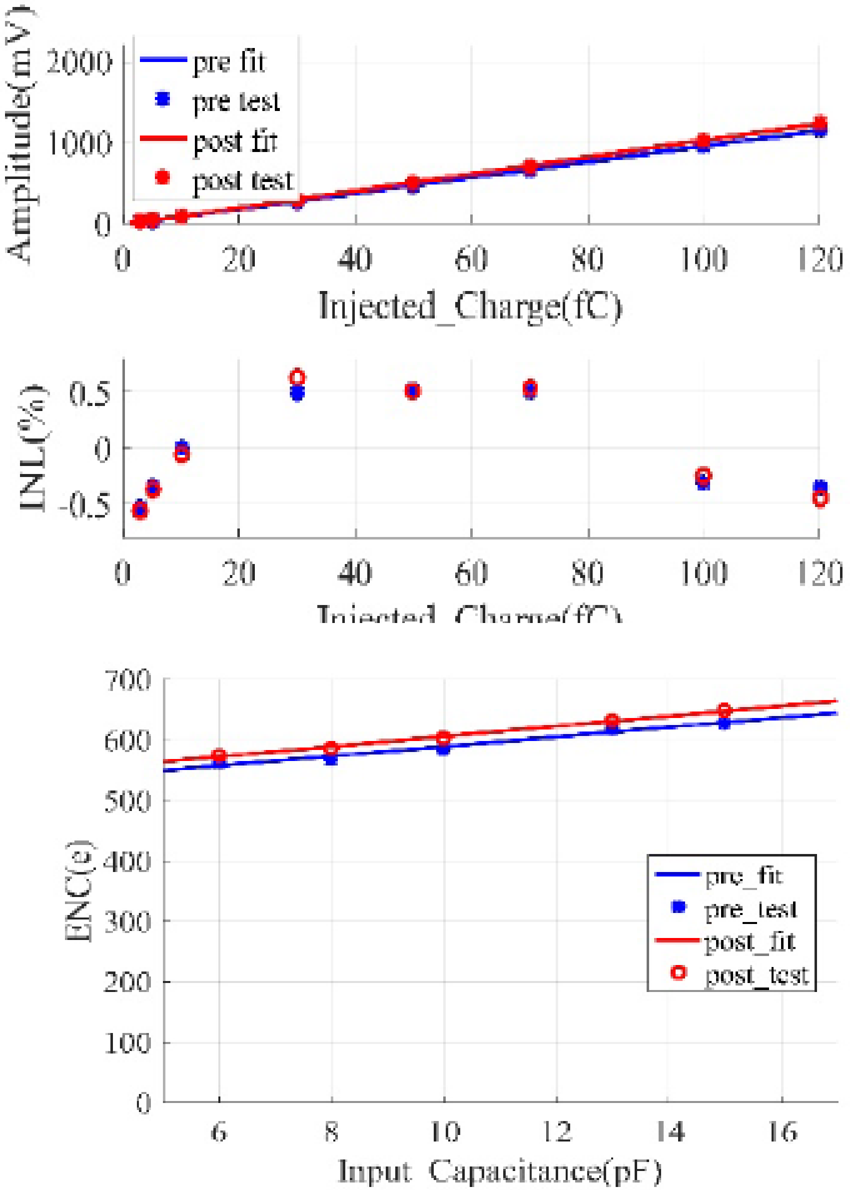
Total ionizing dose test

- Current Progress
  - Using the 60Co source
  - Three AFE and SAR ADC chips were exposed to the radiation source
  - These chips were irradiated at a dose rate of 50 rad (Si)/s at room temperature with the total dose up to 1 Mrad(Si)
  - The components were then annealed at room temperature for 168 hours (7 days)

TID test setup for AFE

TID test results

- **Current Progress**
  - All the performances of three chips remained almost the same after irradiation with the total dose of 1 Mrad (Si).
  - The change of the gain the linearity were neglectable
  - The ENC was lightly increased
  - Preliminary : the requirement for CEPC track detector (<1 krad) from CDR



Gain/INL/ENC before and after irradiation

- Status of the collaboration

Contribution for Snowmass of LOI LCTPC

A Time Projection Chamber using Advanced Technology for the International Large Detector at the International Linear Collider

submitted by the LCTPC collaboration

Project Plans

The work plan has been divided into three phases. In a first phase the principle of an MPGD TPC has been studied with small prototypes, several ideas like MWPC readout could be ruled out and important measurements could confirm the performance of MPGDs also in high magnetic fields. In the second phase, which is still ongoing, the studies are being consolidated by studying increasingly advanced modules resulting in a close to final design for the three baseline technologies. The three technologies are tested at a common setup at DESY and at the end of phase two a technology decision will be made. In phase three, a final design of the readout modules will follow.

The next steps in the consolidation phase are the design of a common module where a large fraction of the module is identical for all technologies, including a gating GEM and readout electronics based on the SALTRO-16 ASIC. These modules should be produced in a small pre-series with as much standardized industrial processes as possible. The comparison of these results will then lead to the technology choice, which should be taken once the green light for the ILC project is given by the Japanese government.

Until such decision can be reached, a number of tasks are still remaining among which are full simulations of the TPC performance in the ILC environment, cooling, further design of the readout electronics, and the calibration methods.

Future MPGD Technology Challenges

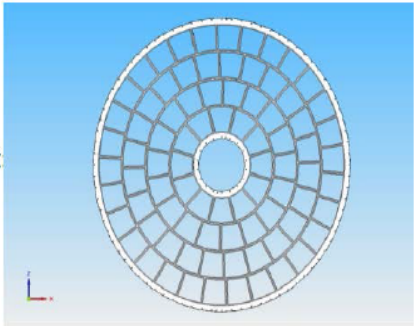
The MPGD technology, though quite far advanced in some aspects, still needs a significant effort in others. For example, the performance in a high magnetic field (B = 4.0 T) needs confirmation for all performance parameters, the ion blocking of the gating GEM has to be verified and development of modern readout electronics should be continued. The efficient and precise construction of a large number of GridPixes and the analysis of the large amount of data they produce are still challenges to be solved. Similarly, the calibration and alignment methods of the narrow UV laser beams are still to be considered for further R&D. Therefore, anyone interested in this project is sincerely invited to join the project and to stimulate further progress by new ideas.

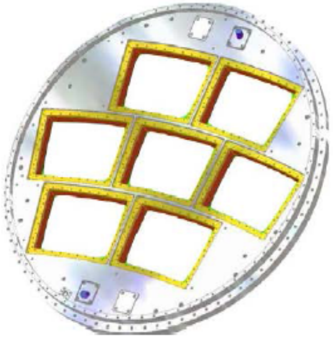
Overview of two readout options

Pad TPC and Pixel TPC

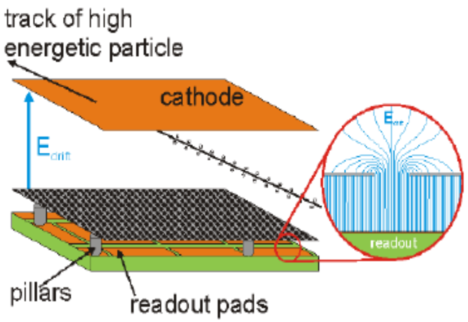
Pad TPC for collider

- Active area: 2×10m^2
- One option for endplate readout
  - GEM or Micromegas
  - 1×6 mm^2 pads
  - 10^6 Pads
  - 84 modules
  - Module size: 200×170mm^2
  - Readout: Super ALTRO
  - CO_2 cooling





Pixel TPC for collider



For Collider @cost:
But to readout the TPC with GridPixes:
→100-120 chips/module
240 modules/endcap (10 m^2)
→50k-60k GridPixes
→ 10^9 pixel pads

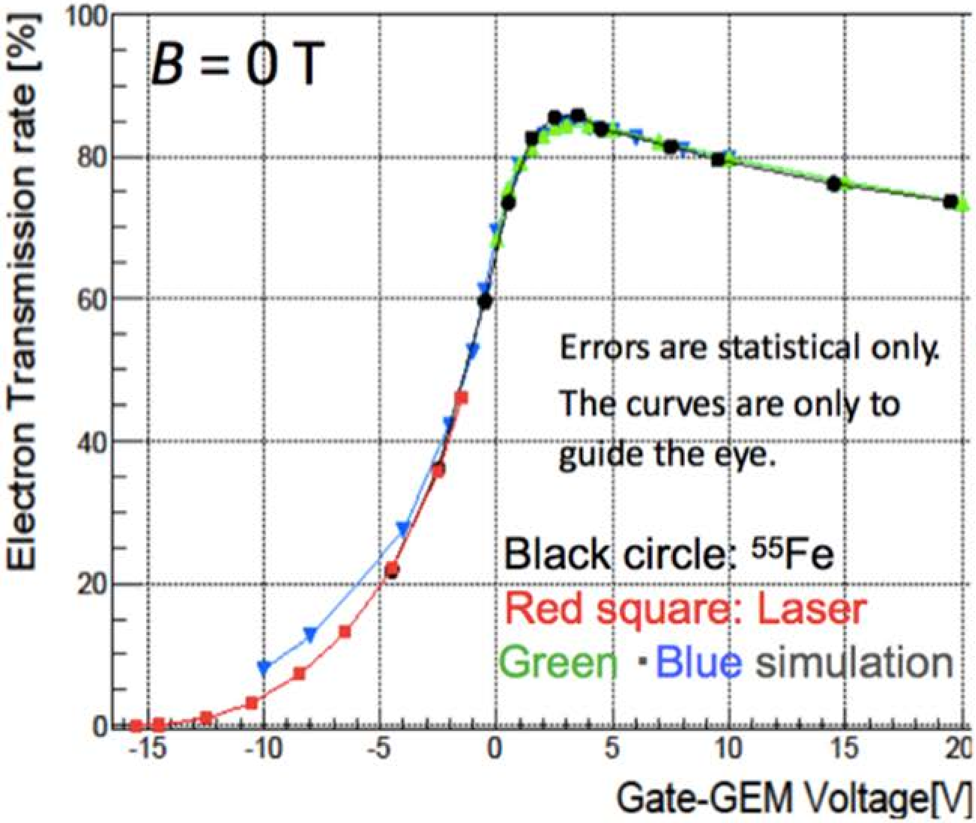
Benefits of Pixel readout:

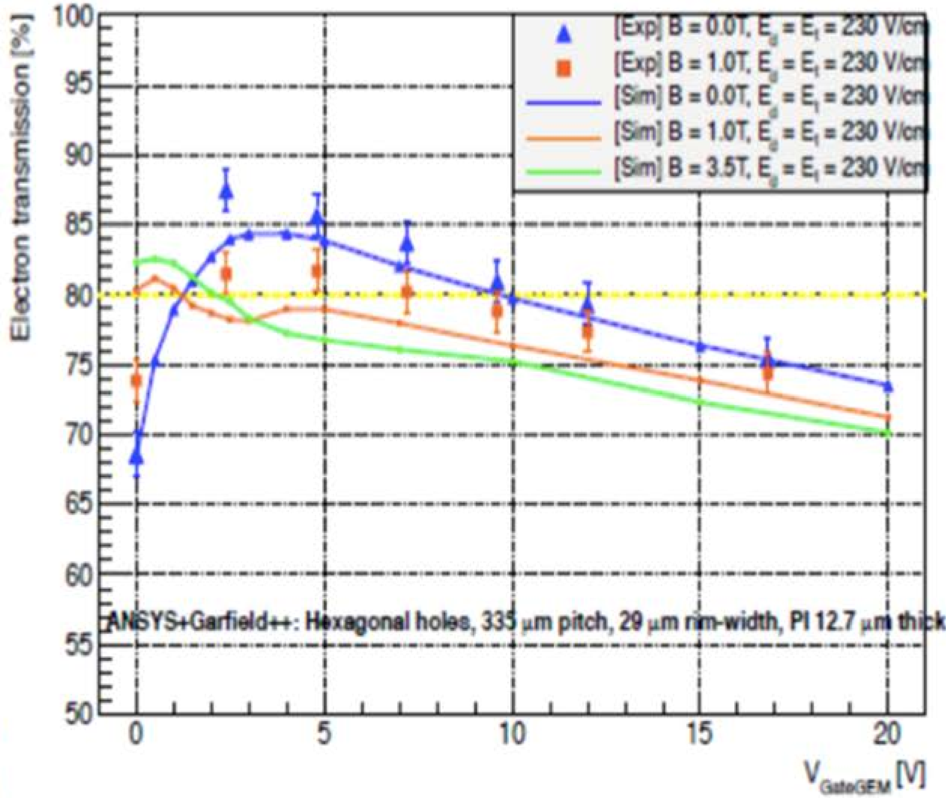
- Lower occupancy
  - → 300 k Hits/s at small radii.
  - → This gives < 12 single pixels hit/s.
  - → With a read out speed of 0.1 msec (that matches a 10 kHz Z rate)
  - → the occupancy is less than 0.0012
- Improved dE/dx
  - → primary e- counting
  - Smaller pads/pixels could result in better resolution!
  - Gain <2000
  - Low IBF*Gain<2
  - CO_2 cooling

Comparison of the different concepts

Pixel TPC with double meshes	Triple or double GEMs	Resistive Micromegas	GEM+ Micromegas	Double meshes Micromegas
IHEP, Nikehf	KEK, DESY	Saclay	IHEP	USTC
Pad size: 55um-150um square	Pad size: 1mm×6mm	Pad size: 1mm×6mm	Pad size: 1mm×6mm	Pad size: 1mm×6mm (If resistive layer)
Advantage for TPC: Low gain: 2000 IBF×Gain: -1	Advantage for TPC: Gain: 5000-6000 IBF×Gain: <10	Advantage for TPC: Gain: 5000-6000 IBF×Gain: <10	Advantage for TPC: Gain:5000-6000 IBF×Gain: <5	Advantage for TPC: High gain: 10^4 Gain: 5000-6000 IBF×Gain: 1-2
Electrons cluster size for FEE: About Ø200um	Electrons cluster size for FEE: About Ø5mm	Electrons cluster size for FEE: About Ø8mm	Electrons cluster size for FEE: About Ø6mm	Electrons cluster size for FEE: About Ø8mm
Integrated FEE in readout board Detector Gain：2000	FEE gain: 20mV/fC Detector Gain：5000-6000	FEE gain: 20mV/fC Detector Gain：5000-6000	FEE gain: 20mV/fC Detector Gain：5000-6000	FEE gain: 20mV/fC Detector Gain：5000-6000

Transparancy Gating device





Ion backflow for a double grid(Preliminary)

- Calculations for the IBF of the two meshes in case one has a total FR240 – normal GridPix operation. The lower Grid(Pix) was at FR16 too.

Ion backflow	Hole 30 μm	Hole 25 μm	Hole 20 μm
Top grid	2.2%	1.2%	0.7%
GridPix	5.5%	2.8%	1.7%
Total (IBF)	12×10^{-4}	3×10^{-4}	1×10^{-4}
Electron transparency	100%	99.4%	91.7%

- In order to reach IBF×Gain≈1 (Gain 10^3) below one has to choose a slightly
- Smaller hole size of 25 or 20 microns. (460LPI- 510LPI)
- The new meshes delivered to Nikehf and tests will be collaborated.

Further collaboration R&D

- This would be significantly reduced the issue of IBF at high luminosity in collider.
- This could reach to high counting rate environment using 150um square pad.
- It will be tested at Nikhef mounting this grid on top of the Gridpix (holes 30 μm) and measure the electron transparancy and the IBF. Some requirement parameters of the pad size, high voltage, pitch size will be inputted by IHEP.
- The update results will be reported in next CEPC workshop in October.

Summary

- Some update progress and experimental studise of TPC prototype R&D in last three months.
- Some update progress of the TPC ASIC chips R&D and the results of the power consumption and TID.
- Some update discussion and collaboration R&D with Nikehf and LCTPC.

Thanks!