Digital Pixel Measurement of TaichuPix1

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17-08-2020

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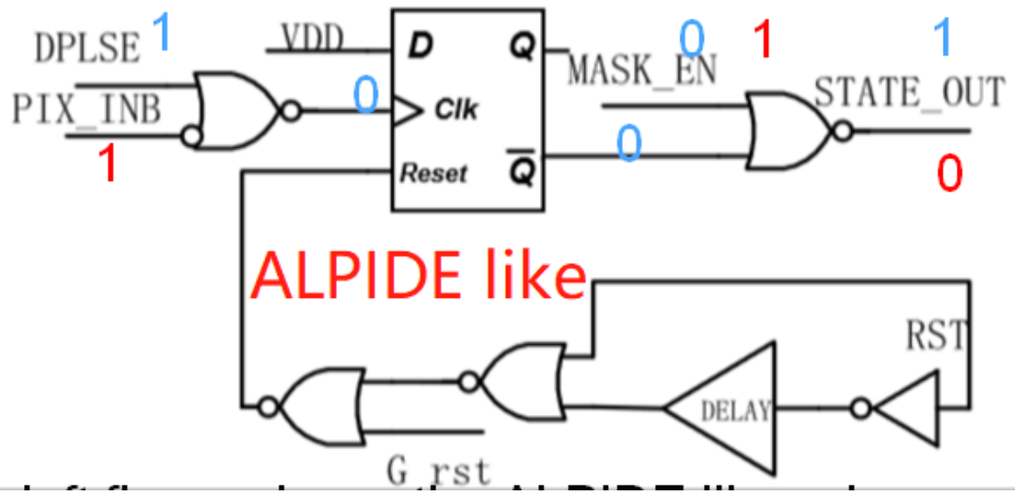
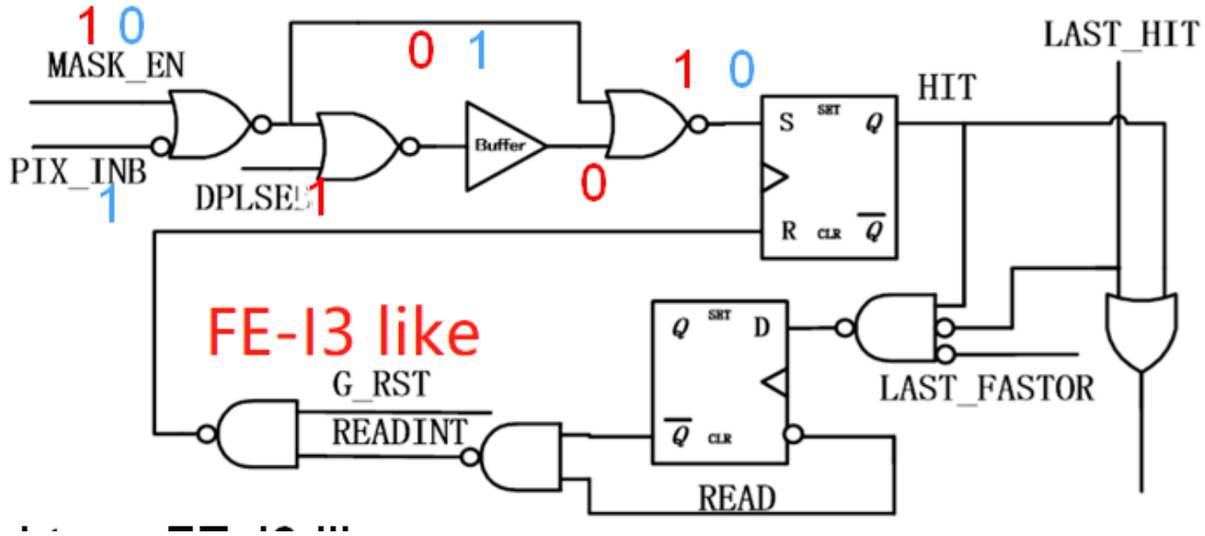
Digital logics inside pixel of TaichuPix1





◆The left figure shows the ALPIDE like scheme and the right are the FE_I3 like one.

◆ With the default state of the analog front end, PIX_INB="1", then DPLSE="1",

→When MASK_EN="1", ALPIDE like part will be shielded; FE-I3 like part is working fine.

→ When MASK_EN="0", FE-I3 like part will be shielded; ALPIDE like part is working fine.

No matter what the status of MASK_EN, half part of the pixel array should be working with DPLSE.

Testing results of masking digital pixels

◆40MHz chip system CLK，10MHz SPI speed，with digital pulse injection.

→MASK_EN="1", spi_write('00110','00000000');MASK_EN="0",spi_write('00110','01111111');

MSAK_EN= "1" to FE-I3
MSAK_EN= "0" to ALPIDE

```
DPULSE opened
..........next read...........
valid=  1,ts=254,col= 95,row=  0,pat=  0
valid=  1,ts=254,col= 31,row=127,pat=  0
valid=  1,ts=254,col= 95,row=  1,pat=  0
valid=  1,ts=254,col= 31,row=126,pat=  0
valid=  1,ts=254,col= 95,row=  2,pat=  0
valid=  1,ts=254,col= 31,row=125,pat=  0
valid=  1,ts=254,col= 95,row=  3,pat=  0
valid=  1,ts=254,col= 31,row=124,pat=  0
valid=  1,ts=254,col= 95,row=  4,pat=  0
valid=  1,ts=254,col= 31,row=123,pat=  0
valid=  1,ts=254,col= 95,row=  5,pat=  0
valid=  1,ts=254,col= 31,row=122,pat=  0
valid=  1,ts=254,col= 95,row=  6,pat=  0
valid=  1,ts=254,col= 31,row=121,pat=  0
valid=  1,ts=254,col= 95,row=  7,pat=  0
valid=  1,ts=254,col= 31,row=120,pat=  0
valid=  1,ts=254,col= 95,row=  8,pat=  0
valid=  1,ts=254,col= 31,row=119,pat=  0
valid=  1,ts=254,col= 95,row=  9,pat=  0
valid=  1,ts=254,col= 31,row=118,pat=  0
valid=  1,ts=254,col= 95,row= 10,pat=  0
valid=  1,ts=254,col= 31,row=117,pat=  0
valid=  1,ts=254,col= 95,row= 11,pat=  0
valid=  1,ts=254,col= 31,row=116,pat=  0
valid=  1,ts=254,col= 95,row= 12,pat=  0
valid=  1,ts=254,col= 31,row=115,pat=  0
```

MSAK_EN= "0" to all

```
DPULSE opened
..........next read...........
valid=  1,ts= 19,col= 95,row=  0,pat=  0
valid=  1,ts= 19,col= 63,row=  0,pat=  0
valid=  1,ts= 19,col= 95,row=  1,pat=  0
valid=  1,ts= 19,col= 63,row=  1,pat=  0
valid=  1,ts= 19,col= 95,row=  2,pat=  0
valid=  1,ts= 19,col= 63,row=  2,pat=  0
valid=  1,ts= 19,col= 95,row=  3,pat=  0
valid=  1,ts= 19,col= 63,row=  3,pat=  0
valid=  1,ts= 19,col= 95,row=  4,pat=  0
valid=  1,ts= 19,col= 63,row=  4,pat=  0
valid=  1,ts= 19,col= 95,row=  5,pat=  0
valid=  1,ts= 19,col= 63,row=  5,pat=  0
valid=  1,ts= 19,col= 95,row=  6,pat=  0
valid=  1,ts= 19,col= 63,row=  6,pat=  0
valid=  1,ts= 19,col= 95,row=  7,pat=  0
valid=  1,ts= 19,col= 63,row=  7,pat=  0
valid=  1,ts= 19,col= 95,row=  8,pat=  0
valid=  1,ts= 19,col= 63,row=  8,pat=  0
valid=  1,ts= 19,col= 95,row=  9,pat=  0
valid=  1,ts= 19,col= 63,row=  9,pat=  0
valid=  1,ts= 19,col= 95,row= 10,pat=  0
valid=  1,ts= 19,col= 63,row= 10,pat=  0
valid=  1,ts= 19,col= 95,row= 11,pat=  0
valid=  1,ts= 19,col= 63,row= 11,pat=  0
valid=  1,ts= 19,col= 95,row= 12,pat=  0
valid=  1,ts= 19,col= 63,row= 12,pat=  0
```

MSAK_EN= "1" to all

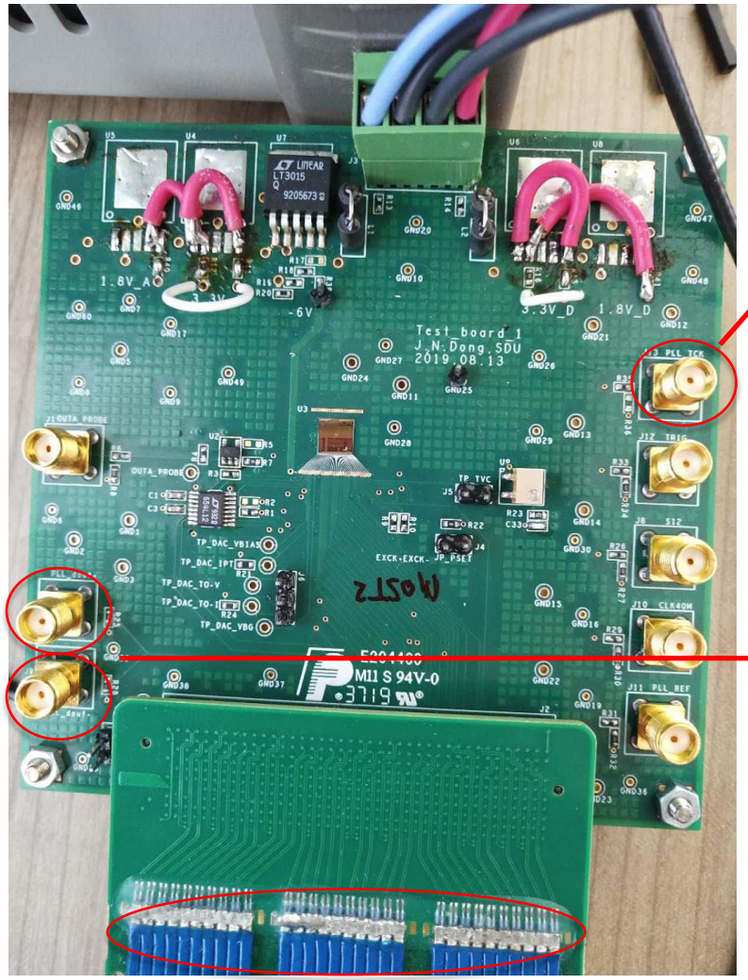
```
DPULSE opened
..........next read...........
valid=  1,ts= 45,col= 31,row=127,pat=  0
valid=  1,ts= 45,col= 95,row=  0,pat=  0
valid=  1,ts= 45,col= 31,row=126,pat=  0
valid=  1,ts= 45,col= 95,row=  0,pat=  0
valid=  1,ts= 45,col= 31,row=125,pat=  0
valid=  1,ts= 45,col= 95,row=  0,pat=  0
valid=  1,ts= 45,col= 31,row=124,pat=  0
valid=  1,ts= 45,col= 95,row=  0,pat=  0
valid=  1,ts= 45,col= 31,row=123,pat=  0
valid=  1,ts= 45,col= 95,row=  0,pat=  0
valid=  1,ts= 45,col= 31,row=122,pat=  0
valid=  1,ts= 45,col= 95,row=  0,pat=  0
valid=  1,ts= 45,col= 31,row=121,pat=  0
valid=  1,ts= 45,col= 95,row=  0,pat=  0
valid=  1,ts= 45,col= 31,row=120,pat=  0
valid=  1,ts= 45,col= 95,row=  0,pat=  0
valid=  1,ts= 45,col= 31,row=119,pat=  0
valid=  1,ts= 45,col= 95,row=  0,pat=  0
valid=  1,ts= 45,col= 31,row=118,pat=  0
valid=  1,ts= 45,col= 95,row=  0,pat=  0
valid=  1,ts= 45,col= 31,row=117,pat=  0
valid=  1,ts= 45,col= 95,row=  0,pat=  0
valid=  1,ts= 45,col= 31,row=116,pat=  0
valid=  1,ts= 45,col= 95,row=  0,pat=  0
valid=  1,ts= 45,col= 31,row=115,pat=  0
valid=  1,ts= 45,col= 95,row=  0,pat=  0
valid=  1,ts= 45,col= 31,row=114,pat=  0
```

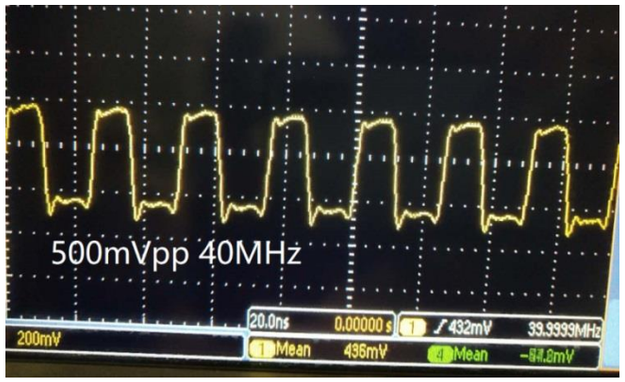
MSAK_EN= "1" to ALPIDE
MSAK_EN= "0" to FE-I3

```
DPULSE opened
..........next read...........
valid=  1,ts=148,col= 95,row=  0,pat=  0
valid=  1,ts=148,col= 63,row=  0,pat=  0
valid=  1,ts=148,col= 95,row=  0,pat=  0
valid=  1,ts=148,col= 63,row=  0,pat=  0
valid=  1,ts=148,col= 95,row=  0,pat=  0
valid=  1,ts=148,col= 63,row=  0,pat=  0
valid=  1,ts=148,col= 95,row=  0,pat=  0
valid=  1,ts=148,col= 63,row=  0,pat=  0
valid=  1,ts=148,col= 95,row=  0,pat=  0
valid=  1,ts=148,col= 63,row=  0,pat=  0
valid=  1,ts=148,col= 95,row=  0,pat=  0
valid=  1,ts=148,col= 63,row=  0,pat=  0
valid=  1,ts=148,col= 95,row=  0,pat=  0
valid=  1,ts=148,col= 63,row=  0,pat=  0
valid=  1,ts=148,col= 95,row=  0,pat=  0
valid=  1,ts=148,col= 63,row=  0,pat=  0
valid=  1,ts=148,col= 95,row=  0,pat=  0
valid=  1,ts=148,col= 63,row=  0,pat=  0
valid=  1,ts=148,col= 95,row=  0,pat=  0
valid=  1,ts=148,col= 63,row=  0,pat=  0
valid=  1,ts=148,col= 95,row=  0,pat=  0
valid=  1,ts=148,col= 63,row=  0,pat=  0
valid=  1,ts=148,col= 95,row=  0,pat=  0
valid=  1,ts=148,col= 63,row=  0,pat=  0
valid=  1,ts=148,col= 95,row=  0,pat=  0
valid=  1,ts=148,col= 63,row=  0,pat=  0
valid=  1,ts=148,col= 95,row=  0,pat=  0
valid=  1,ts=148,col= 63,row=  0,pat=  0
```

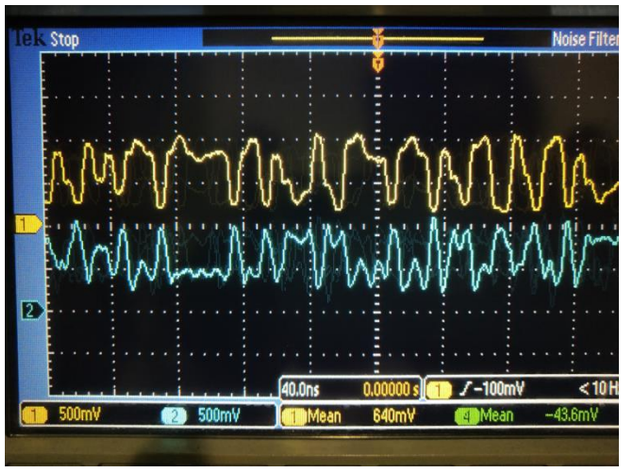
COL=31→FE-I3 like part　　COL=63/95→ALPIDE like Part

PLL & Serializer preliminary test results



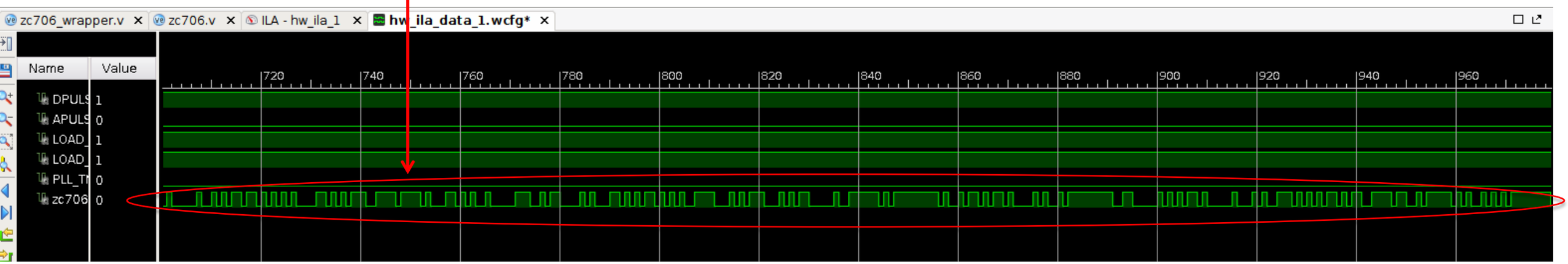


- With the 40MHz Reference Clock, the PLL will generate a 40MHz and 500mVpp signal at the PIN of TCK.



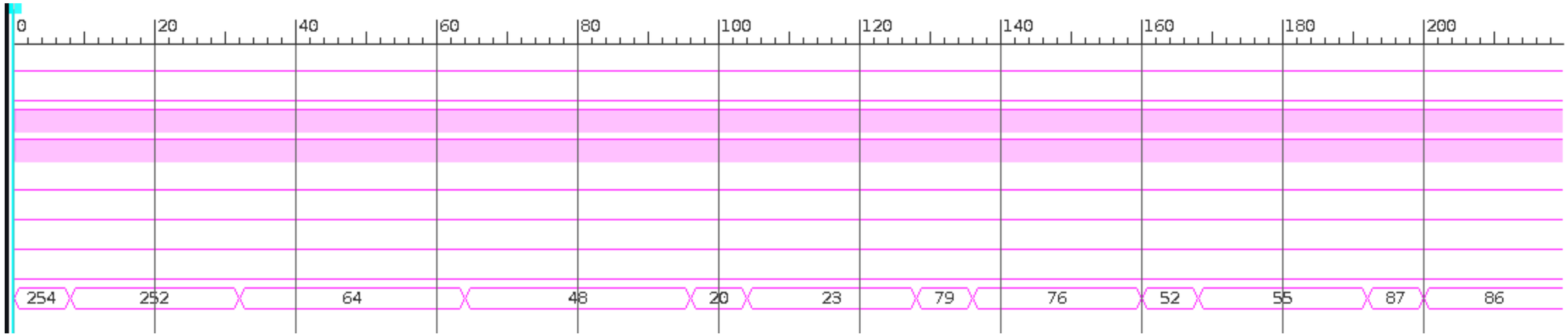
- The Oscilloscope could receive the differential signal but hard to recognize the digital sequences information.

- Use the FPGA hardware debug core to check the data. It could show the digital sequences, but the frame header is hard to recognize.

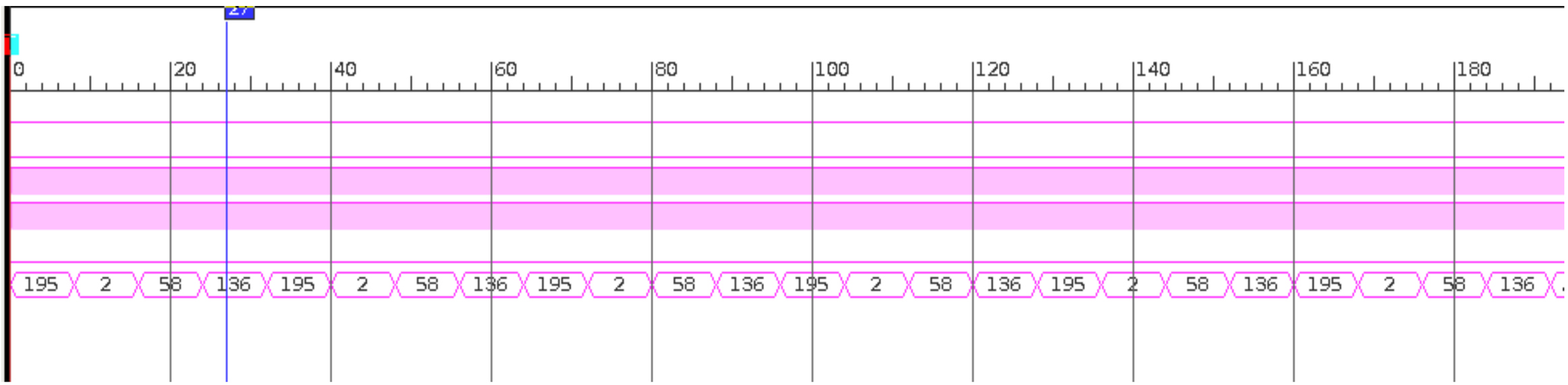


PLL & Serializer preliminary test results

- The last line is the serial to parallel conversion output, this is the result of DSEL=1, data is from the internal generator, but it mismatch the PRBS-2^7 pattern? And the time period of each data is different.



- This is the result of DSEL=0, data is from the periphery, the time period of each data is the same, but the repeat result (136-195-2-58) not so sure where is the header of byte ?



Summary and outlook

- The principle of digital logics shows the pixel array will be response with digital pulse injection no matter the masking state.
- It proves the function of masking signal is working fine.
- Even all the pixels are shielded by the masking blocks, the noisy signal will still come from the COL95_ROW0 and COL63_ROW0.
- The strategy to test serializer blocks will need to be optimize.

→ Next step is to improve the firmware on deserializing the LVDS signal.

→ Do final test together with the analog front end

Thanks for your attention.