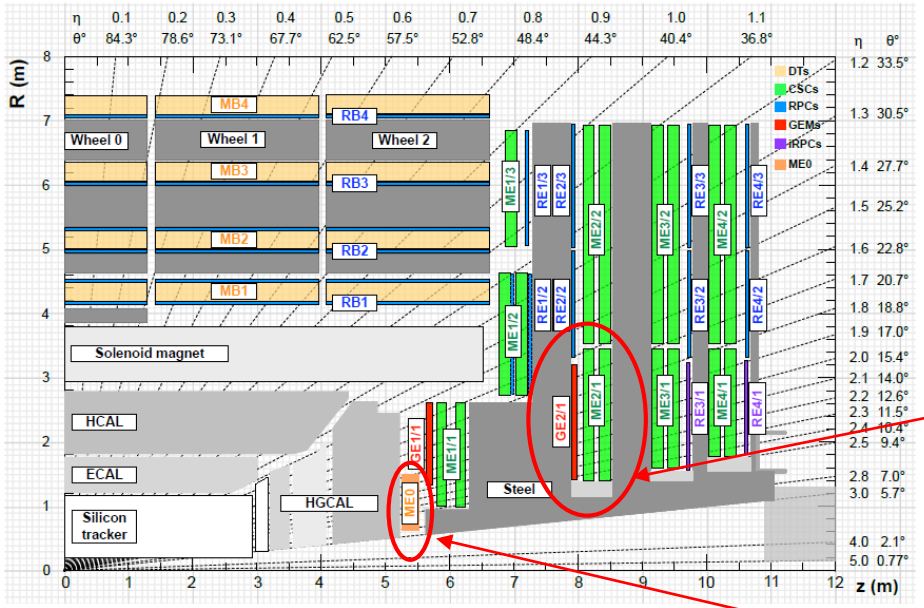
Development of the front-end electronic board for CMS-GEM detector

Li Zhe, Xue Zhihua, Ban Yong, Wang Ke, Wang Dayong, PKU, 2020.11.2

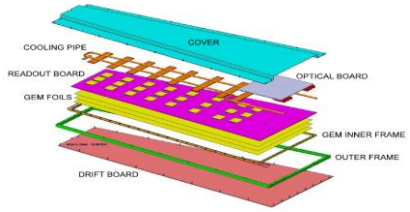
- Introduction to GEM Electronic Board
- GE2/1 GEB design and summary
- ME0 GEB development

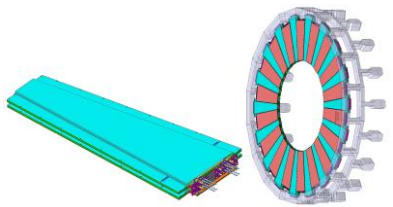
1. Introduction of GEB



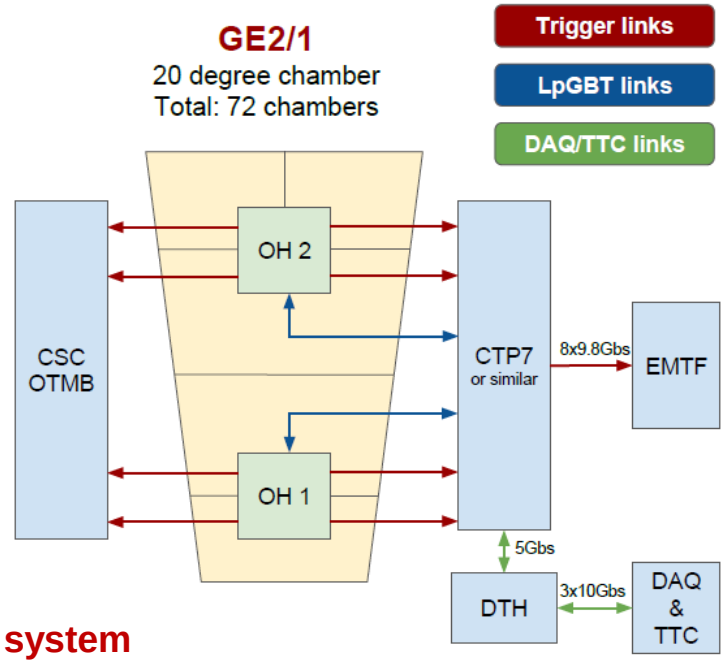
GEB is the key element in the readout system of GEM, which has three main functions:

1. **Transmission of signals between front-end VFAT and OH board.**
2. **Power drive and distribution.**
3. **Providing electrical shielding to signal of GEB**

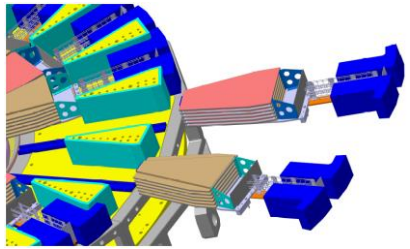




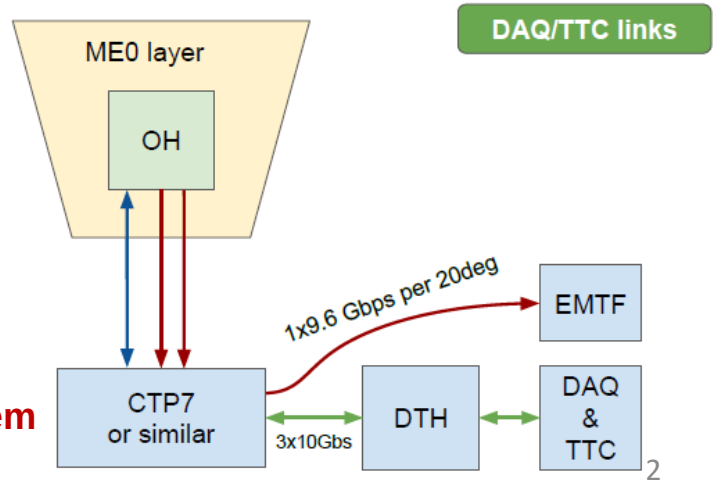
GE2/1
20 degree chamber
Total: 72 chambers



GE2/1 electronics readout system



ME0
20 degree layer
Total: 216 layers



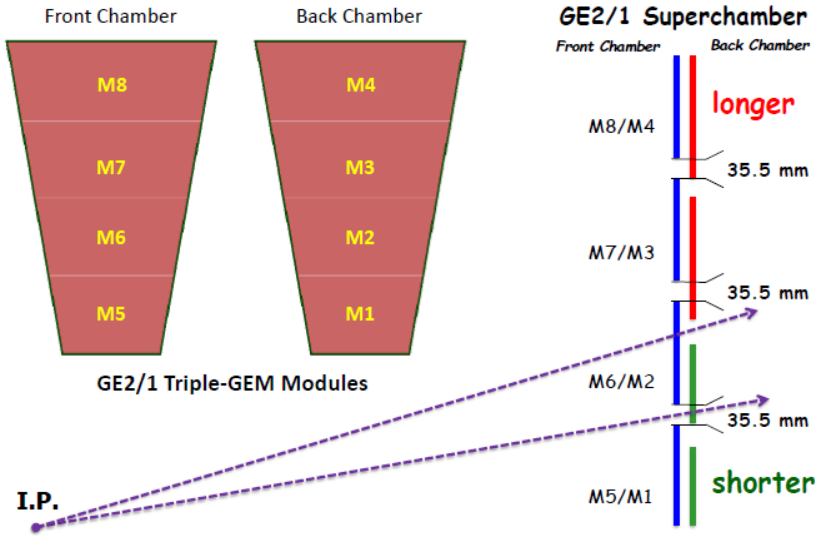
ME0 electronics readout system

There are 8 types GEB, from M1-M8, each GEB has **12 VFATs**, corresponding **to 1 OH board**.
M1-M4 in the back, M5-M8 in the front.
There is a total of 72 chambers, 288 GEBs.

VFAT trigger unit outputs **9 differential signals:**
8-bit data: data[8..1]
1 strobe signal: strobe
VFAT communication E-port has 3 pairs of differential signals
Receive clock: RDCLK
Receive data: RXD
Send data: TXD
VFAT reset signal
LVCMOS level signal: RESET

GE2/1

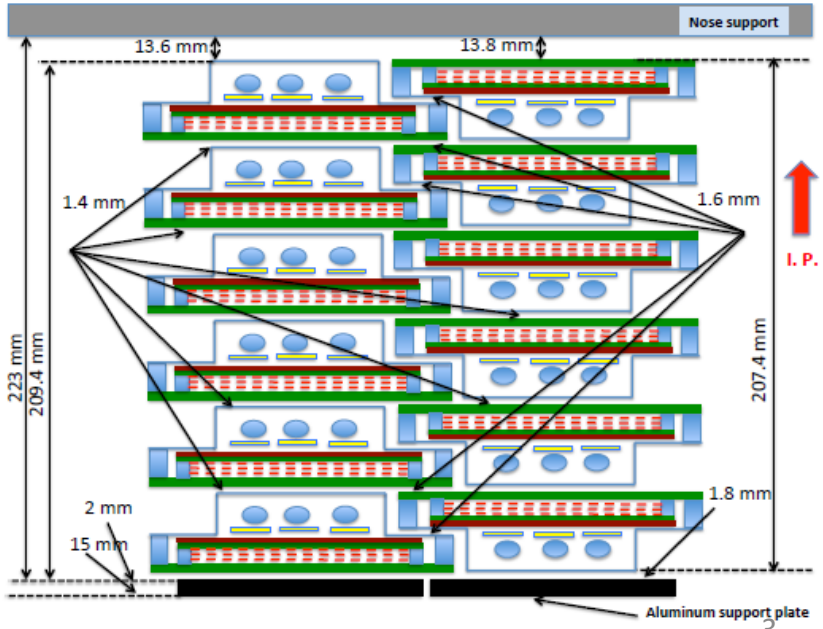
OH board power supply
1.5V power supply
1.8V power supply
2.5V power supply
VFAT power supply
1.2V digital power supply
1.2V analog power supply
2.5V power supply (shared with OH board)
Power current monitoring
Each power module
Shield
GEB board bottom layer (connected to the chamber shell)



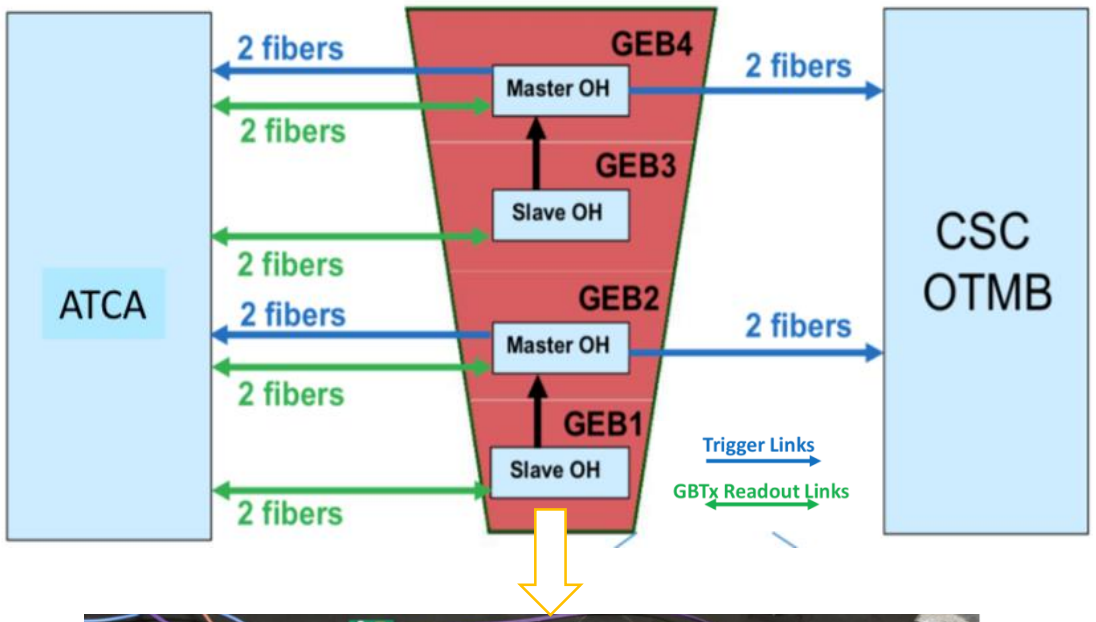
There are 2 types of GEB, narrow and wide ME0, each GEB has **12 VFATs**, corresponding to **2 OH boards** (ASIAGO), 216 GEBs
VFAT trigger unit outputs **9 pairs of differential** signals
8-bit data: data[8..1]
1 strobe signal: strobe **(some VFAT default)**
VFAT communication E-port has 3 pairs of differential signals
Receive clock: RDCLK
Receive data: RXD
Send data: TXD
VFAT reset signal
LVCMOS level signal: RESET

ME0

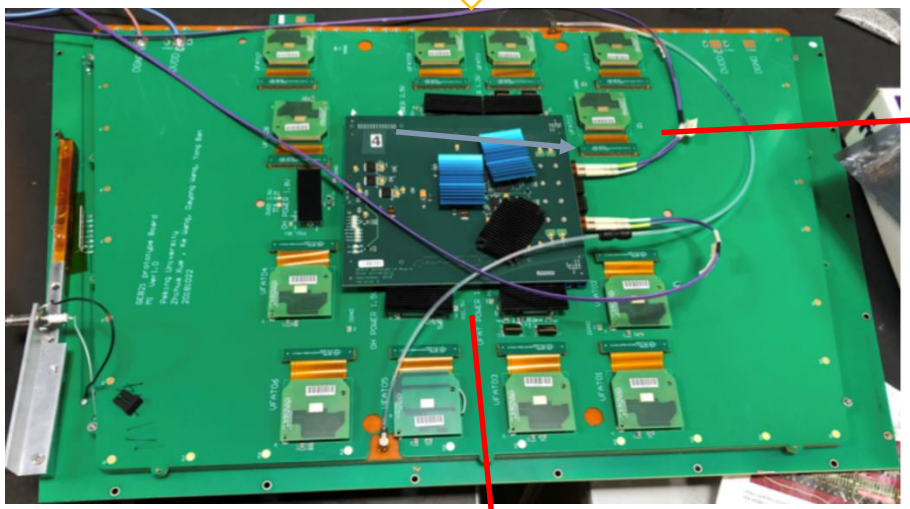
OH board power supply
1.2V power supply
2.5V power supply
VFAT power supply
1.2V digital power supply
1.2V analog power supply
2.5V power supply (shared with OH board)
GEB board monitoring
Current monitoring for each power module
Temperature measurement of each power module
Shield
GEB board bottom layer (connected to the chamber shell)

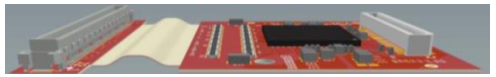


2.1 GE2/1 GEB design

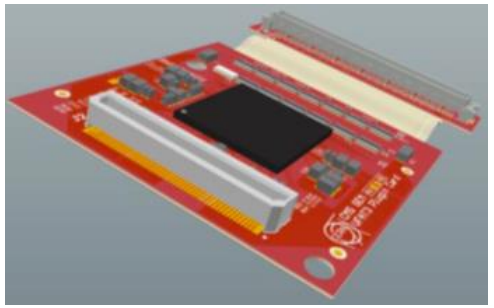


- GE2/1 detector system
- 72 detectors
  - Each detector is read by 48 VFAT3
- 288 GEB
- 288 OH boards
- 288 fibers to OTMB (3.2 Gbps)
- 288 fibers to ATCA (trigger signal)
- 576 fibers to ATCA (GBTx links)





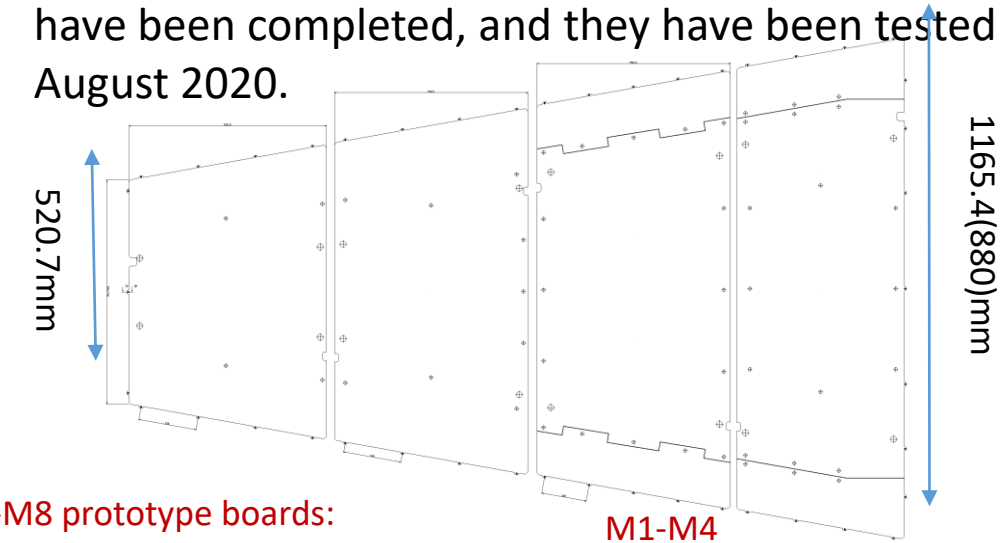
VFAT3 chip + flexible board



OH board： receive signals from GEB and transmit it to the back-end electronics

GEB2/1 design, production and test

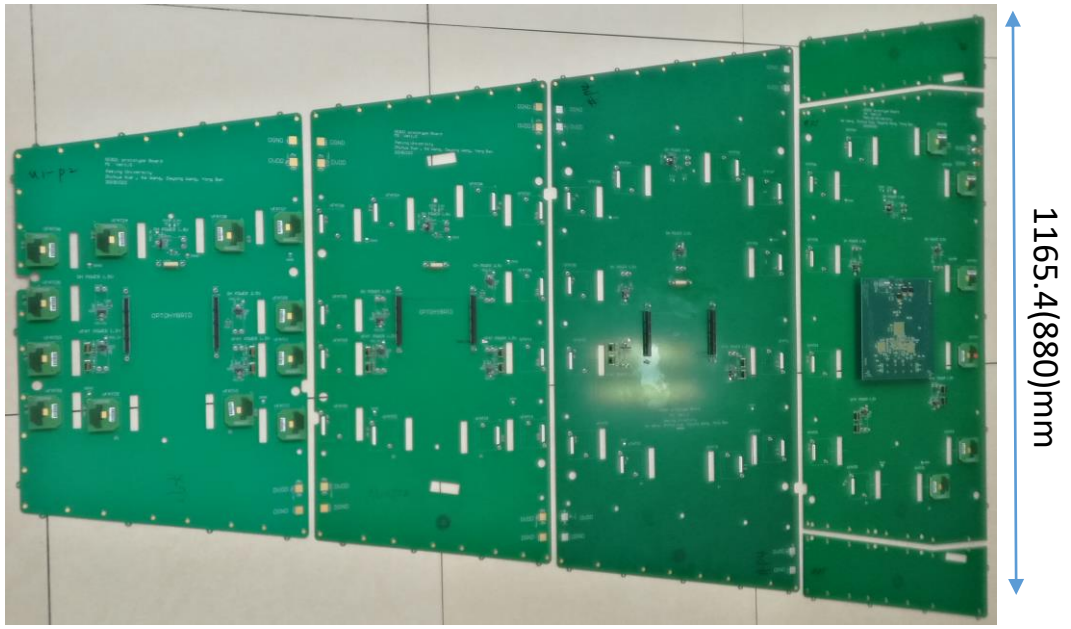
- The second round of GEM detector GE2/1 GEB will be designed, produced and tested by Peking University
- The design, production and testing of the **prototype board** of M1-M8 have been completed. The M7 has been tested in December 2019, and the M8 has been tested in January 2020. Both have been delivered for post-level debugging.
- Design and production of **production board** of M1-M4 have been completed, and they have been tested in August 2020.



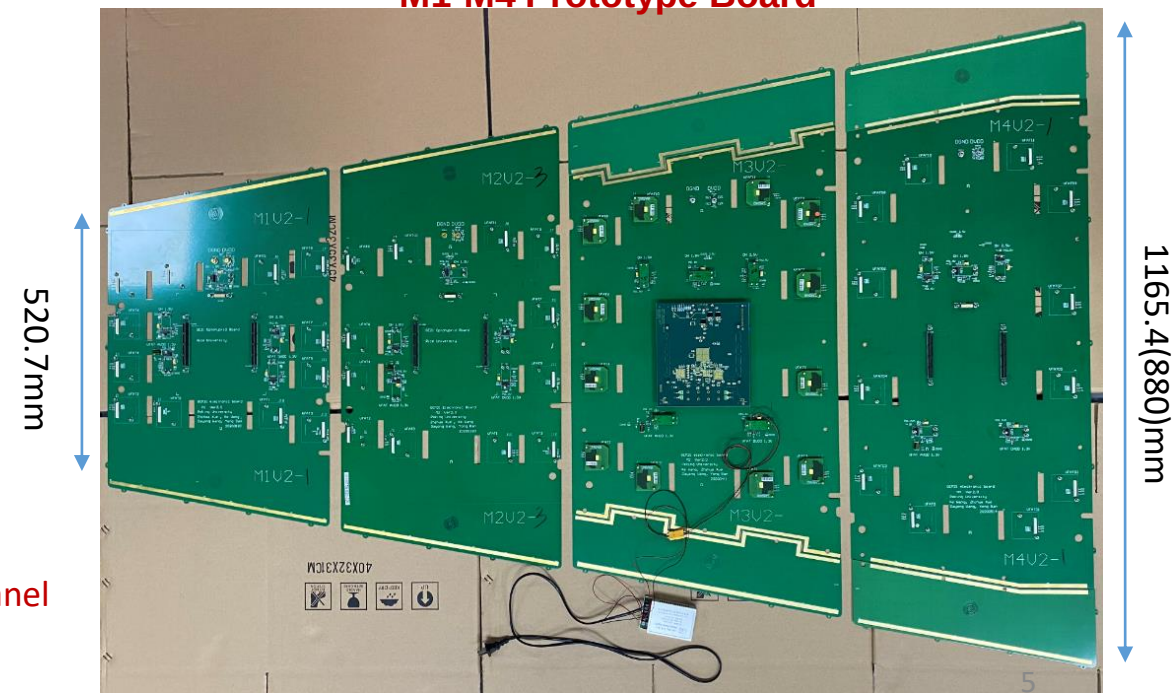
M5-M8 prototype boards:
M7、M8 are divided into 3 pieces, double panel on both sides.

M5-M8 Layout

M1-M4
Prototype boards
M4 is divided into 3 pieces, double panel on both sides, M3 is not divided.
Production board
M1-M4: M3、M4 are divided into 3 pieces



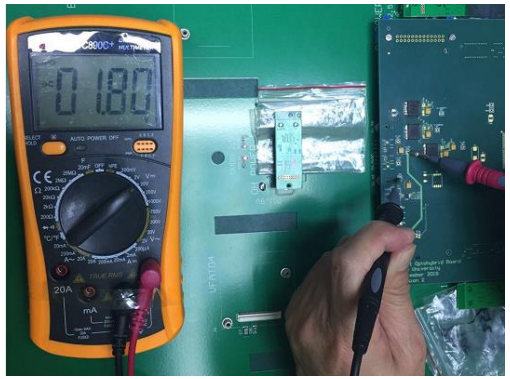
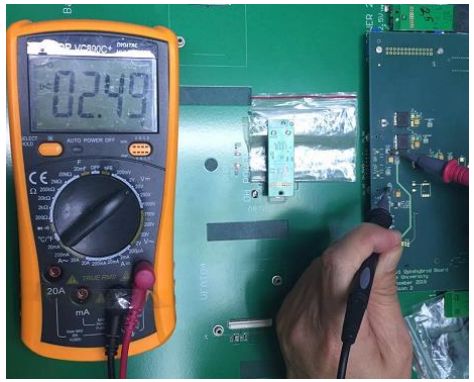
M1-M4 Prototype Board



M1-M4 Board Version2.0

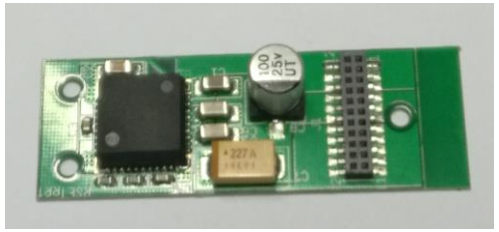
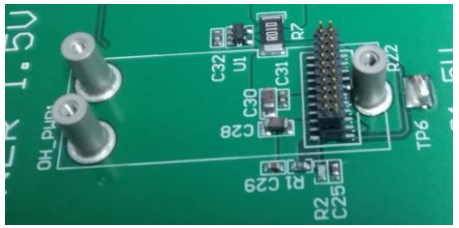
Peking University test in Sinofast Shenzhen

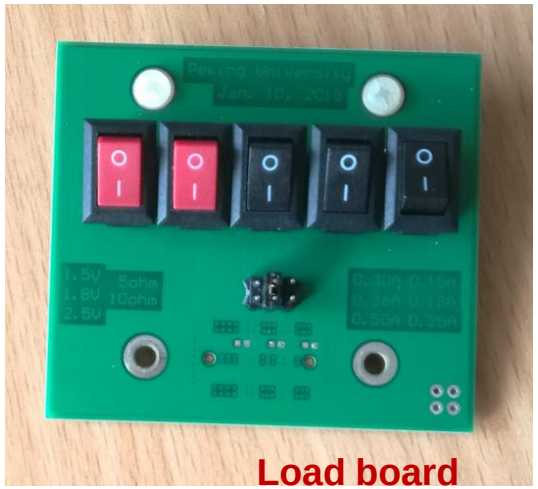
- Complete the test of prototype boards of M1-M8
- Production boards of M1-M4 has been tested in Shenzhen

- **Power module test**
- **Signal connectivity test**
- **Characteristic impedance test**
- **Bending degree test**
- **Mechanical compatibility test**

- Power module test:
  - Voltage and current test of 5 power modules
    - 1.5V,1.8V and 2.5V on OH board
    - 1.2V digital power、1.2V analog power supply on VFAT



- **The power test results meet the GEB design requirements, and the error is within a reasonable range**

➢ Power module test

	Measure Voltage			
DVDD	5.06V	5.06V	5.06V	5.06V
PWR1V5	1.508V	1.508V	1.508V	1.508V
PWR1V8	1.807V	1.807V	1.807V	1.807V
PWR2V5	2.50V	2.50V	2.50V	2.50V
1V2AVFAT	1.210V	1.210V	1.210V	1.210V
1V2DVFAT	1.206V	1.206V	1.207V	1.207V
PG1.8V	1.791V	1.791V	1.791V	1.791V
PG1.5V	1.495V	1.495V	1.495V	1.495V
PG2.5V	2.47V	2.47V	2.47V	2.47V
PG1.2V(A)	1.199V	1.199V	1.199V	1.199V
PG1.2V(D)	1.196V	1.196V	1.196V	1.196V

- Power test result of M4V2

GEB No.	GEB: 1		GEB: 2		GEB: 3		GEB: 4	
Monitor1	3.4mV	181.0mV	2.7mV	179.5mV	1.6mV	174.9mV	4.1mV	182.0mV
Monitor2	0.7mV	146.9mV	3.0mV	150.4mV	8.7mV	157.1mV	1.3mV	148.6mV
Monitor3	6.8mV	0.250V	0.8mV	0.245V	0.6mV	0.248V	1.3mV	0.243V
Monitor4	25.2mV		7.9mV		8.8mV		5.2mV	
Monitor5	0.6mV		0.3mV		14.2mV		0.6mV	

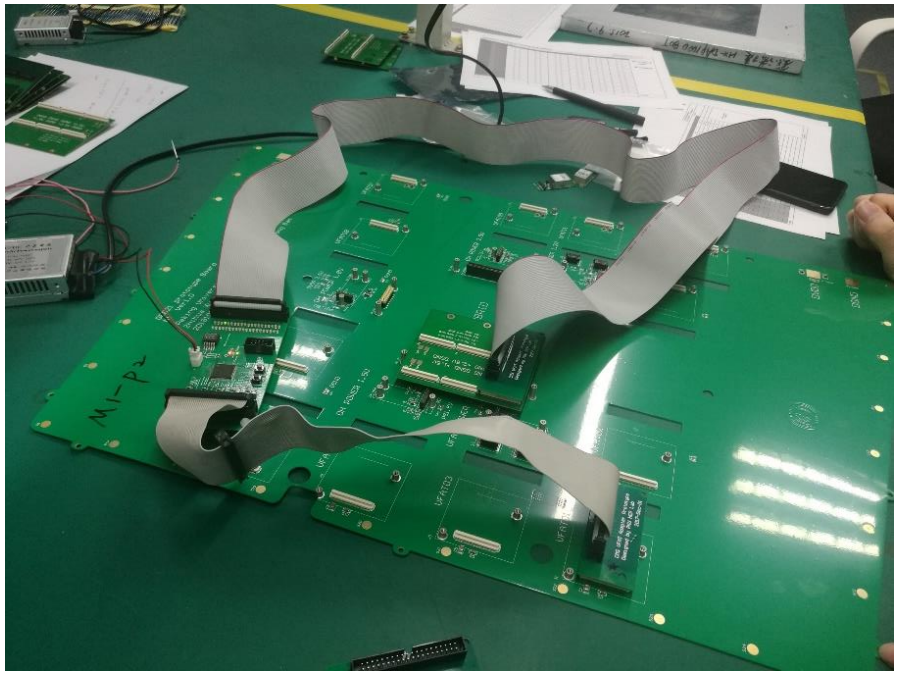
Monitor1-3 load resistor： ∞/2 ohm
Monitor4-5 load resistor： ∞ ohm

Monitor1 monitor PWR1V8, Monitor2 monitor PWR1V5, Monitor3 monitor PWR2V5, Monitor4 monitor 1V2AVFAT, Monitor5 monitor 1V2DVFAT

- Current test result of M4V2

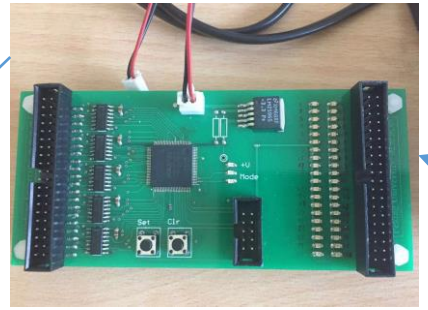
➢ Signal connectivity test

- Test whether the 25 outputs from 12 VFAT3 are successfully transmitted to the back-end OH board.



Drive Side(VFAT)

Show status of OH



LEDs display
(FPGA auto test)
IDC40 IDC40

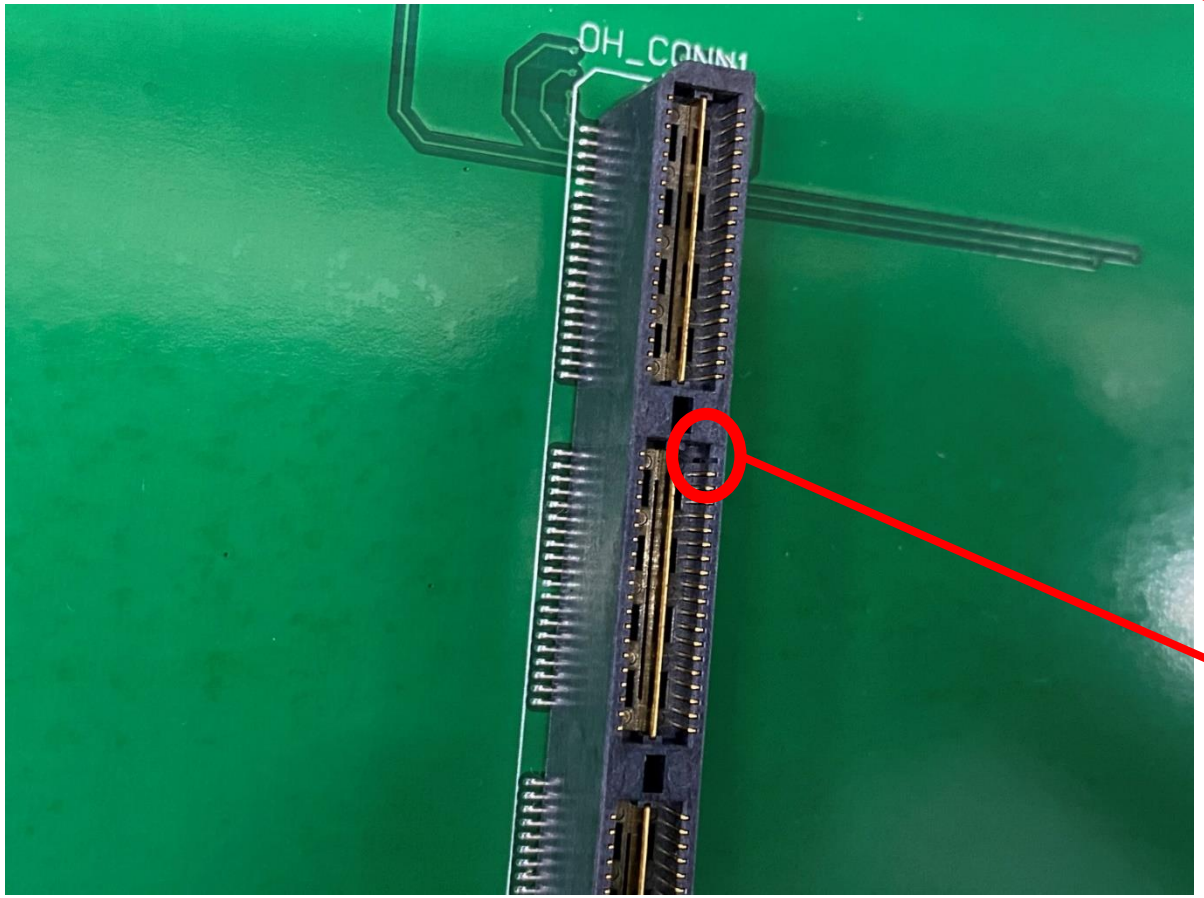
IDC40
Adapter1
Panasonic-100

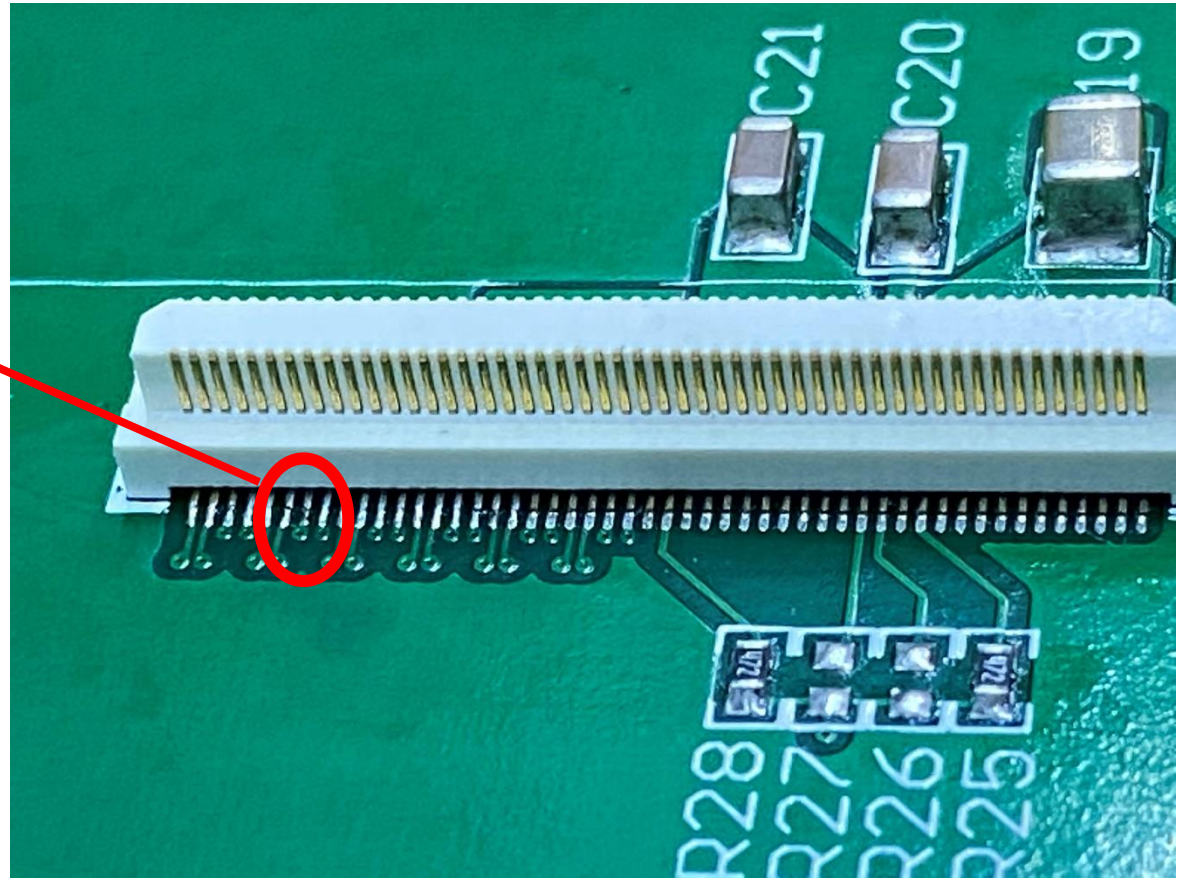
IDC40
Adapter1
Panasonic-100

Panasonic-100
Adapter2
Samtec-160

Panasonic100(VFAT)
GEB-prototype
Samtec-160

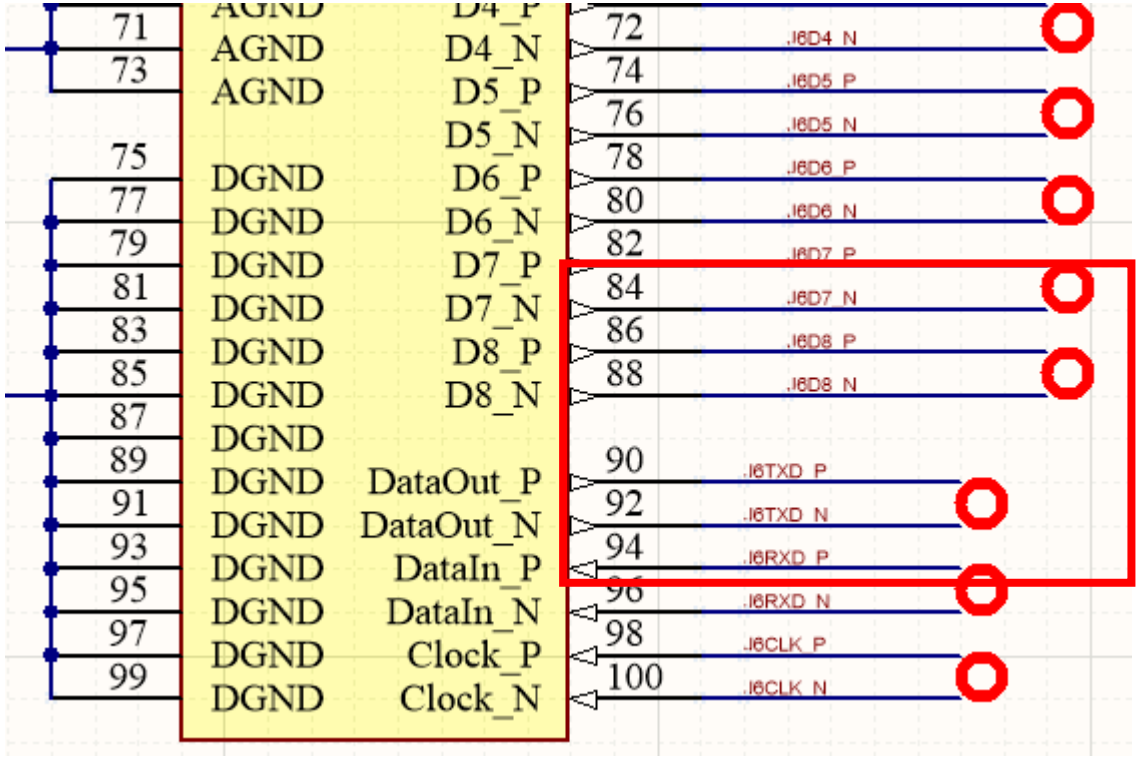
- M3V2
- The size of the circuit board is too large, and the unevenness of solder paste (solder paste: solder powder, flux, surfactant, thixotropic agent, etc.) is difficult to avoid, resulting in an open circuit.

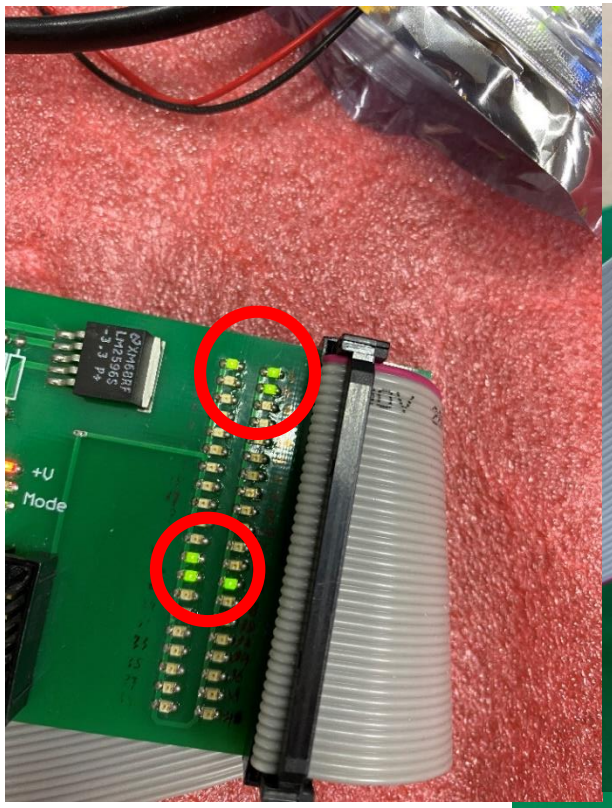


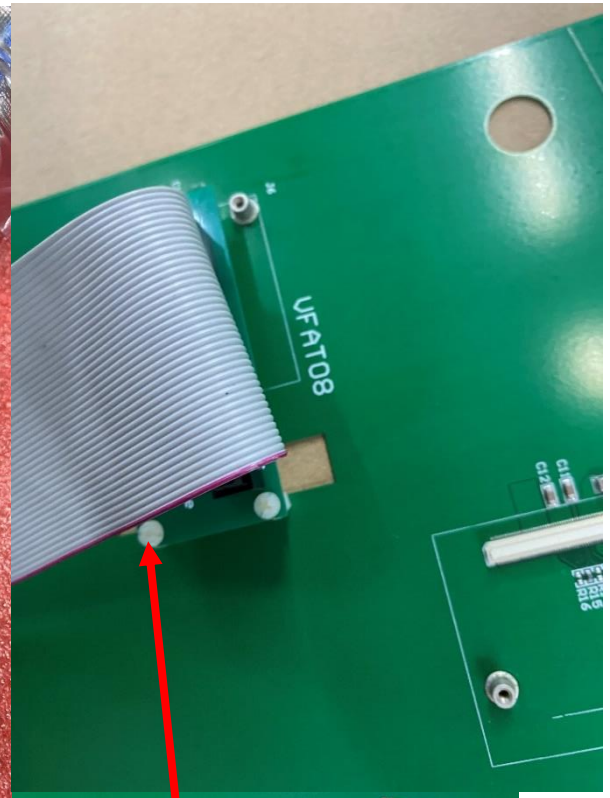


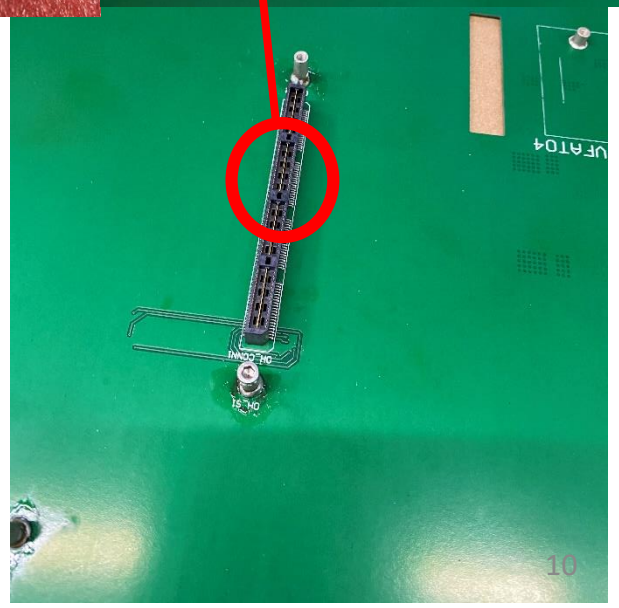
M3V2-3： OH-CONN1 misses a pin.
This is a very rare defect from factory components.

- 2.M4V2-2: 6 signal(pin84 86 88 90 92 94) line of J6(VFAT08) are shorted.
- **Reason： Solder of Panasonic is shorted.**







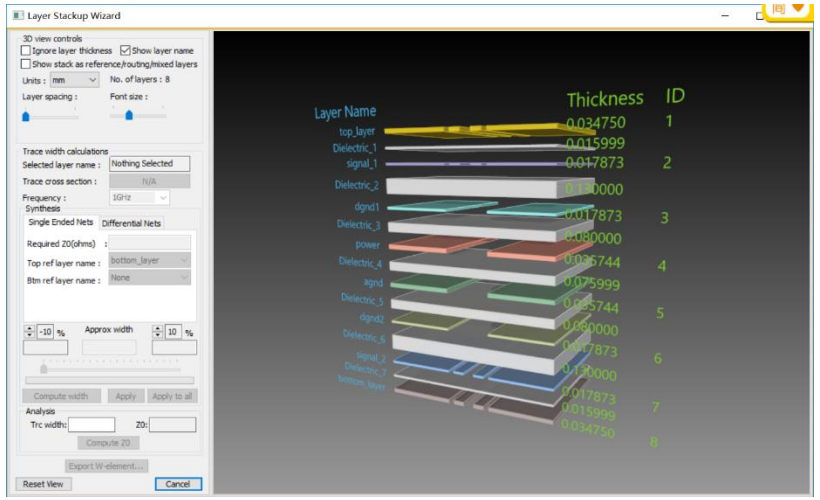


- Find problems and solve to ensure the transmission of signal lines.

➢Characteristic impedance

Characteristic impedance meets the standard

Design the line width and separation of differential lines according to the laminated structure of PCB (the **dielectric constant** of the plane, the **thickness** of each plane, the **thickness** of the copper, etc.). Meet the characteristic impedance requirement.



Plane	Signal_1/Signal_2
Single-end Wire	45.1373Ohm
Differential Wire	98.9679Ohm

24 Differential Pairs (0 Highlighted)

Designator	Average Length (mm)
J1CLK	248.94
J1RXD	248.94
J2CLK	248.94
J2RXD	248.94
J3CLK	248.94
J3RXD	248.94
J4CLK	248.94
J4RXD	248.94
J5CLK	248.94
J5RXD	248.94
J6CLK	248.94
J6RXD	248.94
J7CLK	248.94
J7RXD	248.94
J8CLK	248.94
J8RXD	248.94
J9CLK	248.94
J9RXD	248.94
J10CLK	248.94
J10RXD	248.94
J11CLK	248.94
J11RXD	248.94
J12CLK	248.94
J12RXD	248.936

M5 Prototype Board diff pairs Length Matching

IMPEDANCE MEASUREMENT REPORT

阻 抗 测 量 报 告

TESTING QTY: 1 DATE CODE: 2820

Measuring Equipment 测量仪器及型号: Agilent E5071C (TDR Time Domain Reflectometer)时域反射仪

Impedance Measurement 阻抗测量于: Finished Board 成品板

SampleNo. 样品编号	Layer 层号	Line Width 线宽(mm) +/-10%	Type of Impedance 阻抗类别		Impedance Requirement (ohm) 阻抗值要求	Tolerance		Impedance Value 阻抗测试数值	Result 结果
			Single Ended 单端	Differential 差动		+	-		
1	L1	0.204	/	√	100	10	10	102.14	ACC
	L2	0.104	/	√	100	10	10	101.53	ACC
	L7	0.104	/	√	100	10	10	98.76	ACC

Remarks:

Disposition: Acc ☑ Rej ☐

TESTED BY: YLI3 DATE: 2020.07.20

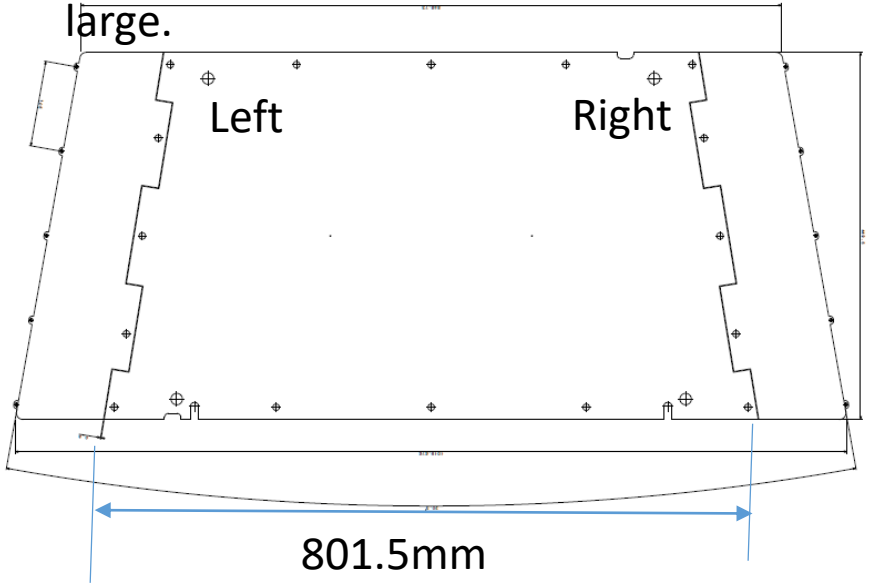
APPROVED BY: DQCAI DATE: 2020.07.20

Documentation NO.QA-2019-08 Rev:1.2

M4 Version2.0 Board

➢ Bending degree test

- Choose 4 corners of GEB (8-layer board part) as the main test points, measure the distance between these 4 points and the horizontal plane with a micrometer, **the ratio of this distance to the length of the curved side is the curvature.** We take 4 test values or other The maximum value of the position is calculated to get the maximum curvature of the GEB (due to the limitation of the measurement conditions, the measurement error is large.



GEB	Highest Point（mm）	Curvature
GEB 1	0.59	0.06%
GEB 2	0.29	0.03%
GEB 3	1.40	0.15%
GEB 4	0.25	0.03%
GEB 5	0.30	0.03%
GEB 6	0.77	0.08%
GEB 7	0.71	0.08%

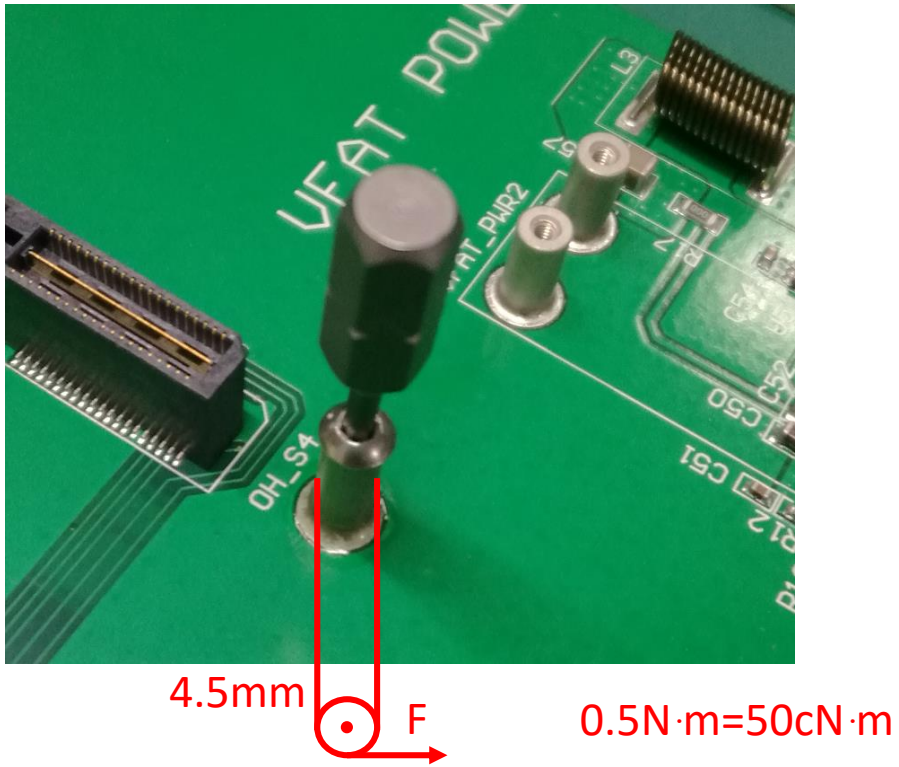
IPC standard curvature<0.75%

- M7 test results show that the maximum bending value of GE2/1 GEB usually does not exceed 1mm (the measured value minus the plate thickness), and the bending degree meets the requirements.

➢ Mechanical compatibility test

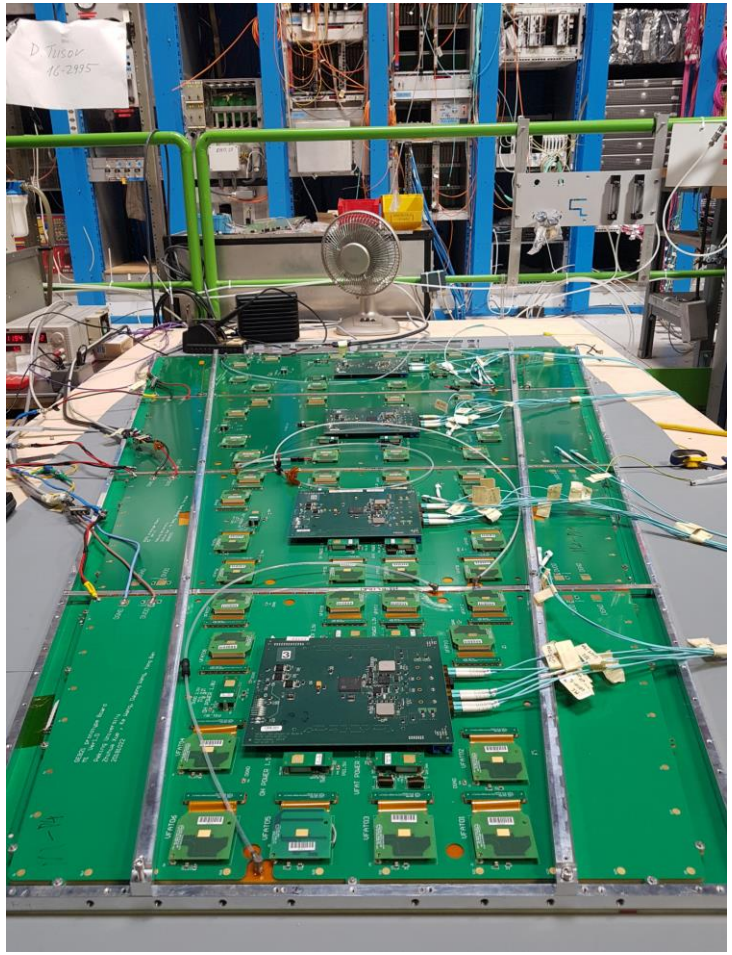
- Install VFAT (PlugIn Card), OH board, and FEAST on GEB to check the collimation of Standoff.
- Test stand-off torque for OH board

- Test results show that Standoff has good collimation
- The standoff torque of the OH board all passed the **0.5NM** test, and the test of part of the standoff showed that the torque can **reach 1NM** (no damage).

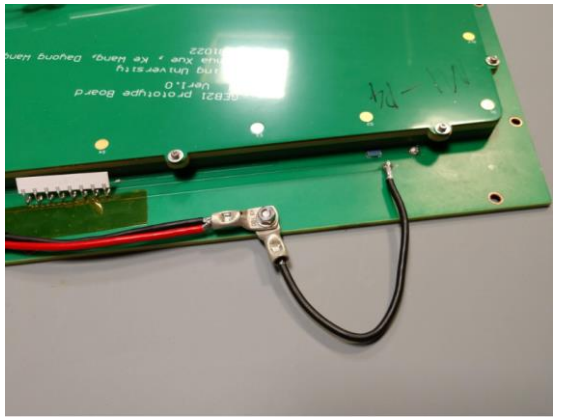


CERN 904 test (M1-M4)

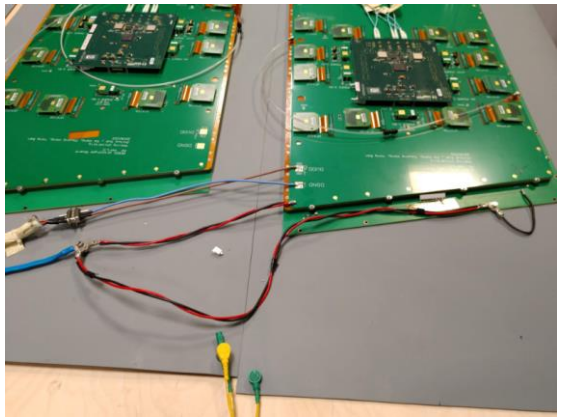
Below are pictures of the 904 GE2/1 electronics integration test stand. All four chambers (M1-M4) are fully instrumented and working. Grounding wires run from a pad on the GEB, a point in contact with the drift board, and the HV ground to a common point for each individual chamber. From here, the chambers are all connected to a common ground. Optical fibers for both GBTs and the GEM trigger are connected on all optohybrids.



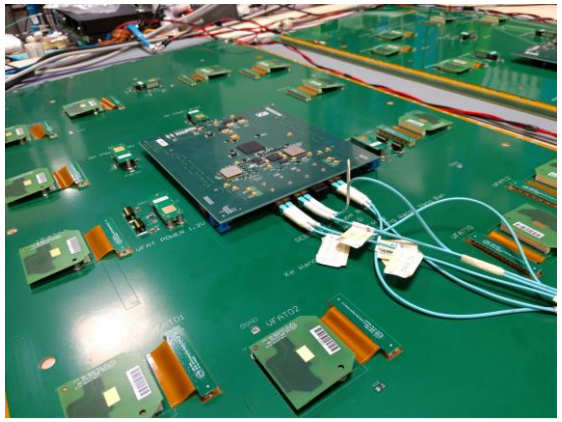
M1-M4 Prototype Board Test



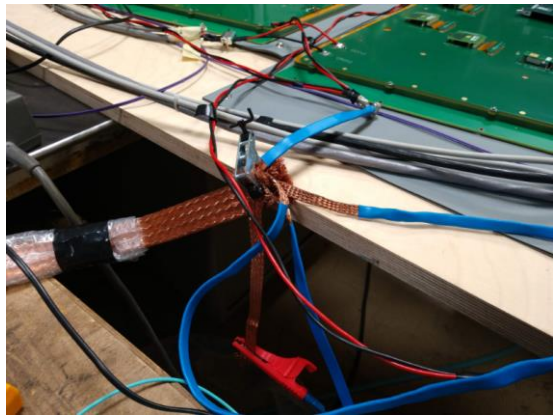
Grounding point for HV and drift board



Grounding point for GE21-M1

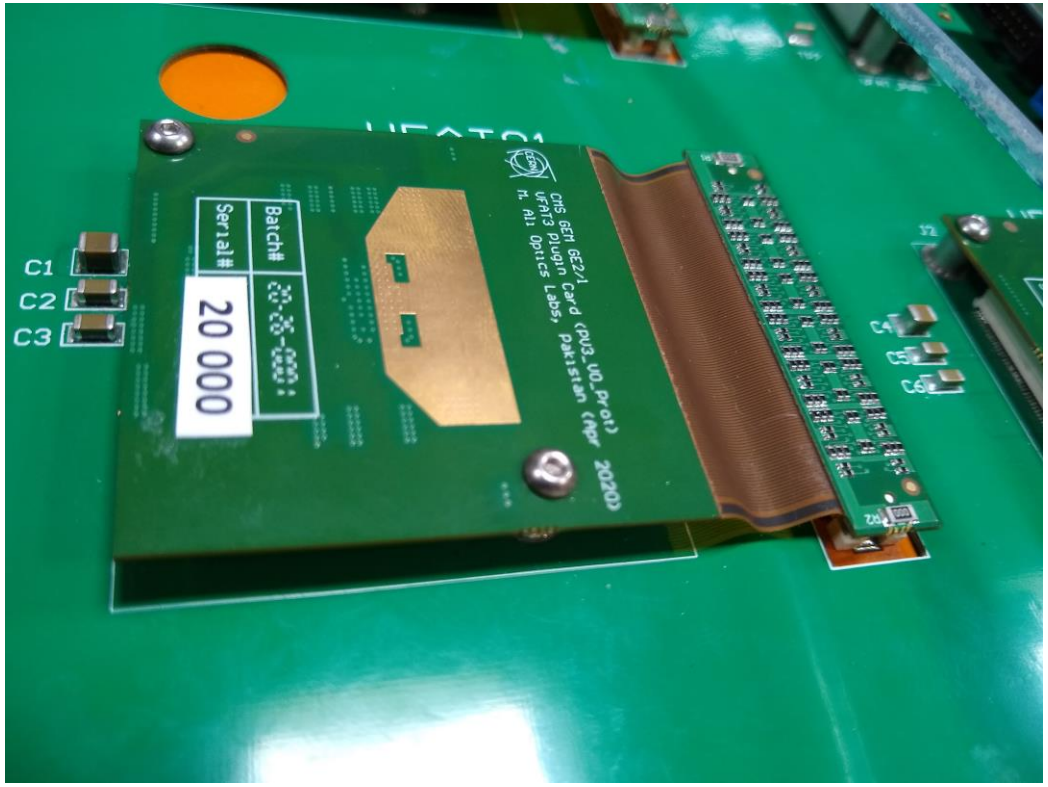


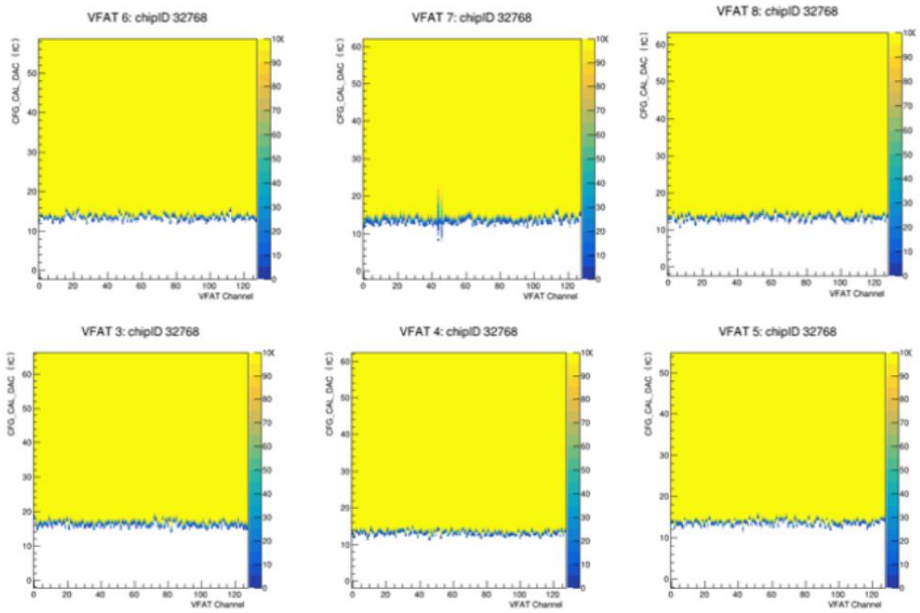
Optical Fibers for both GBTs and the GEM trigger

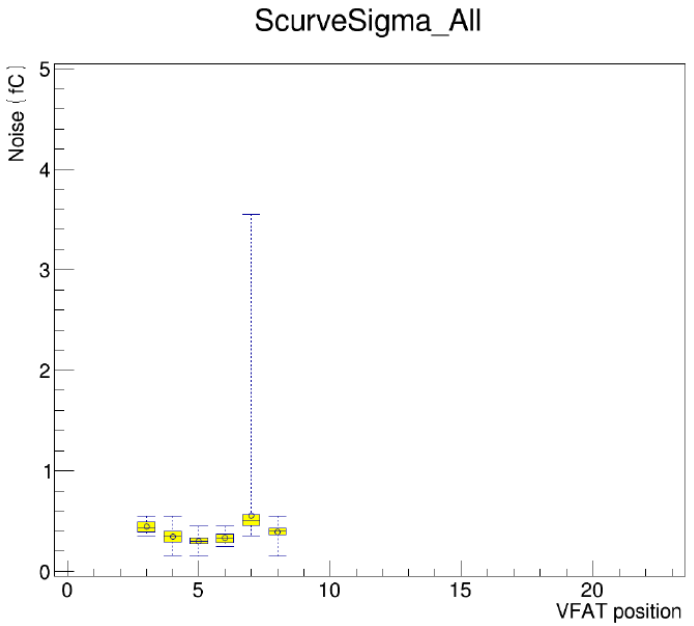


Common grounding point for all modules

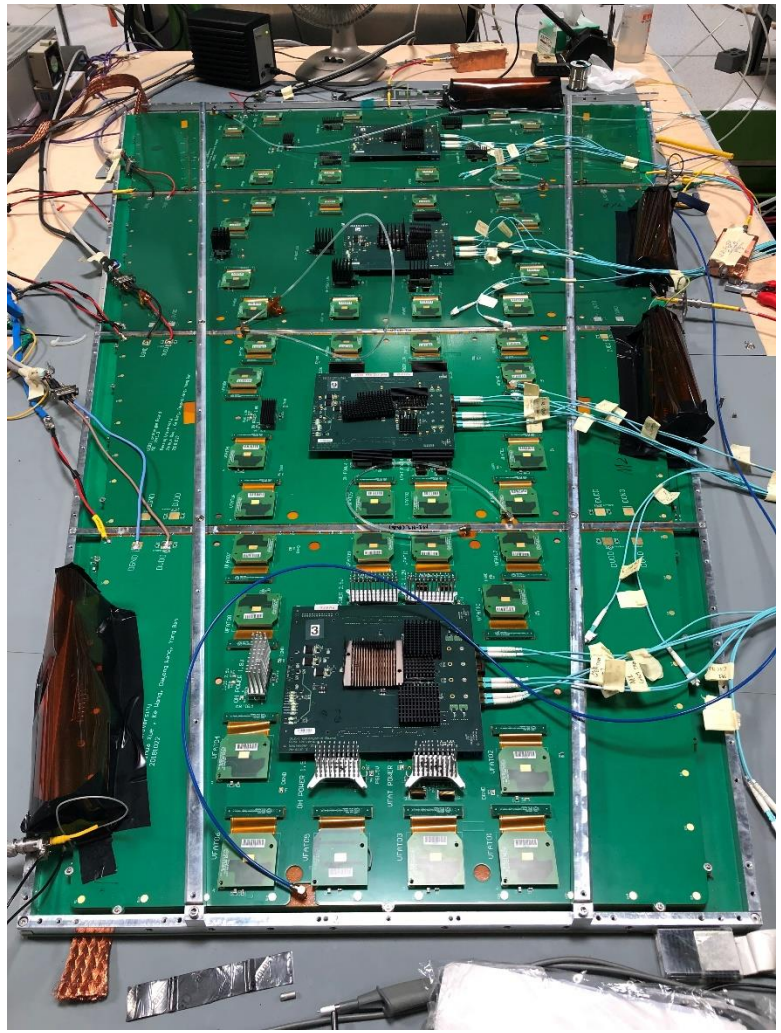
➢ Noise test

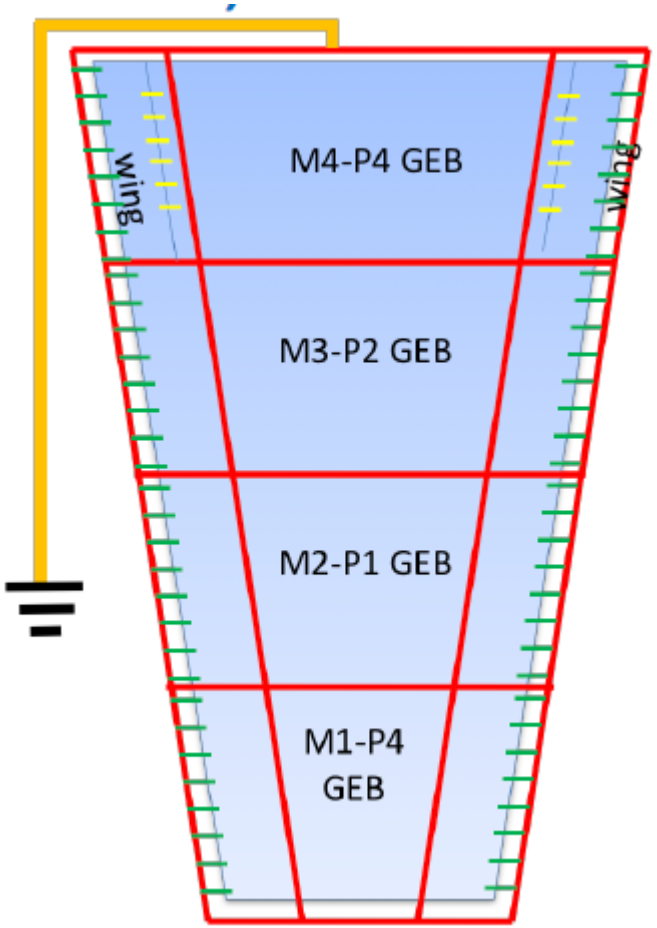

C1
C2
C3
Serial#
Batch#
20 000
CMS GEM GE2/1
VFAT3 Plugin Card (PV3_V0_Prot)
ft. All Optics Labs, Pakistan (Apr 2020)

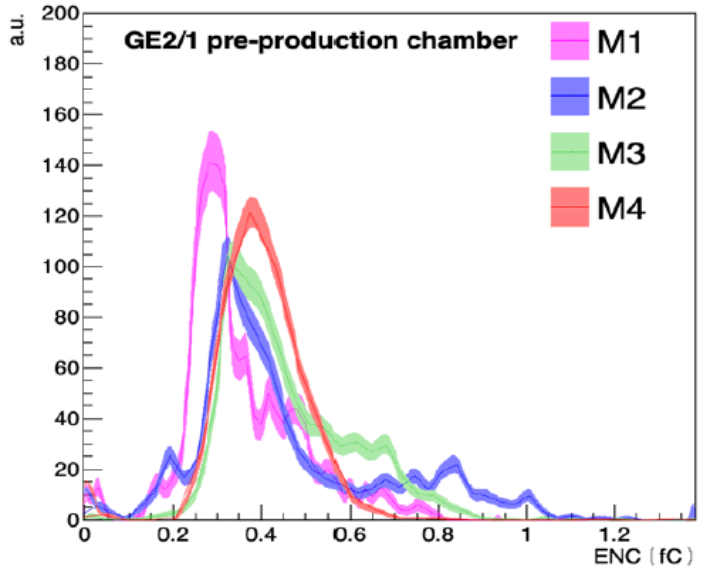

VFAT 6: chipID 32768
VFAT 7: chipID 32768
VFAT 8: chipID 32768
VFAT 3: chipID 32768
VFAT 4: chipID 32768
VFAT 5: chipID 32768
CFG_CAL_DAC (fC)
VFAT Channel

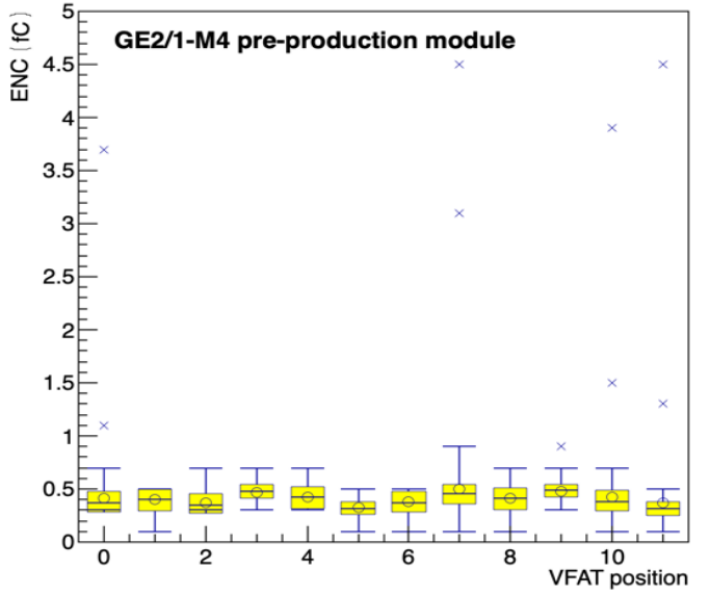

ScurveSigma_All
Noise (fC)
VFAT position
0
1
2
3
4
5
0
5
10
15
20

➢ Noise test of M1-M4 installed on the detector







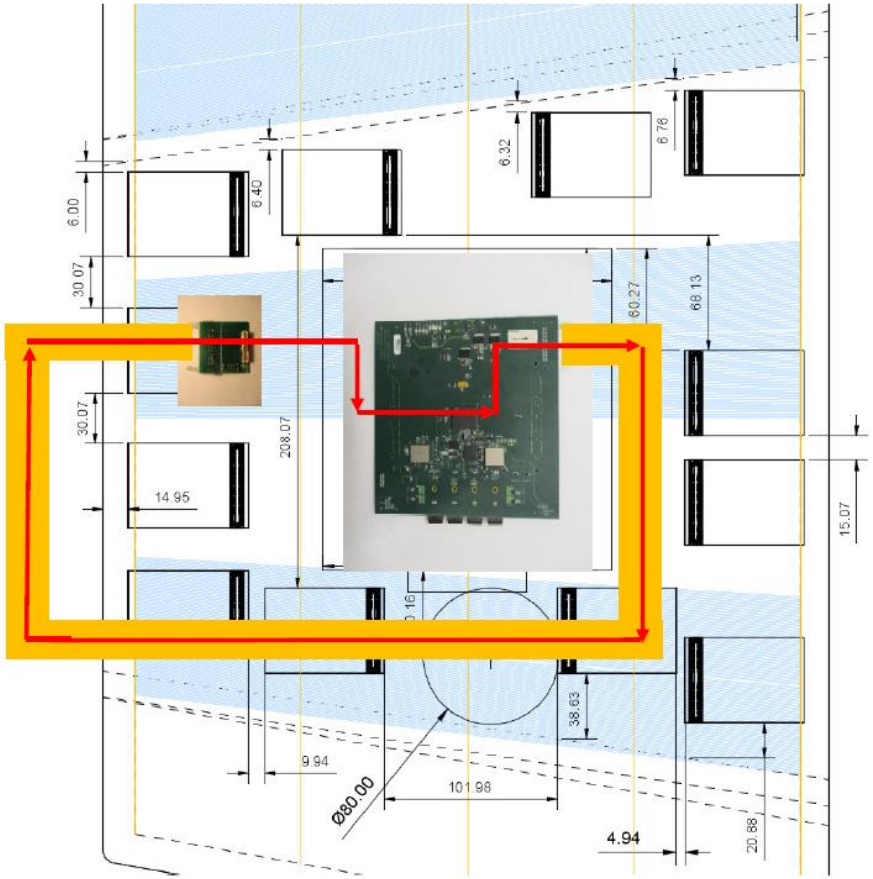


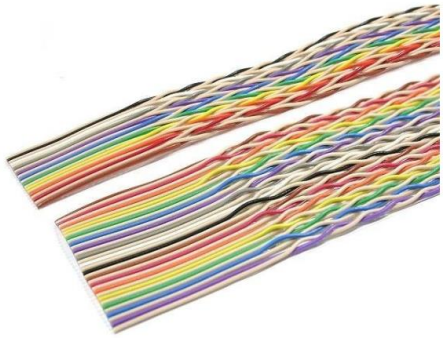
- **The level of noise is 0.3～0.5fC**

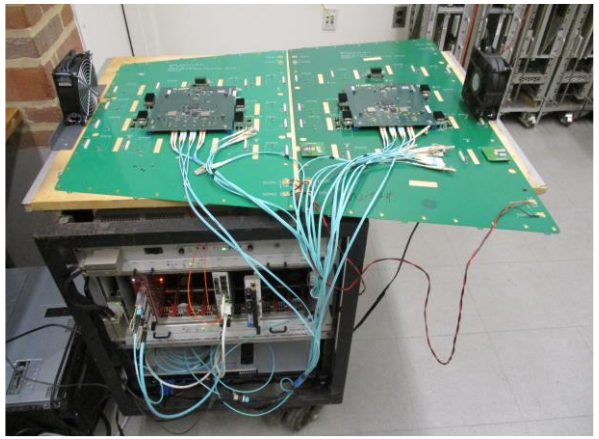
Test by Rice University

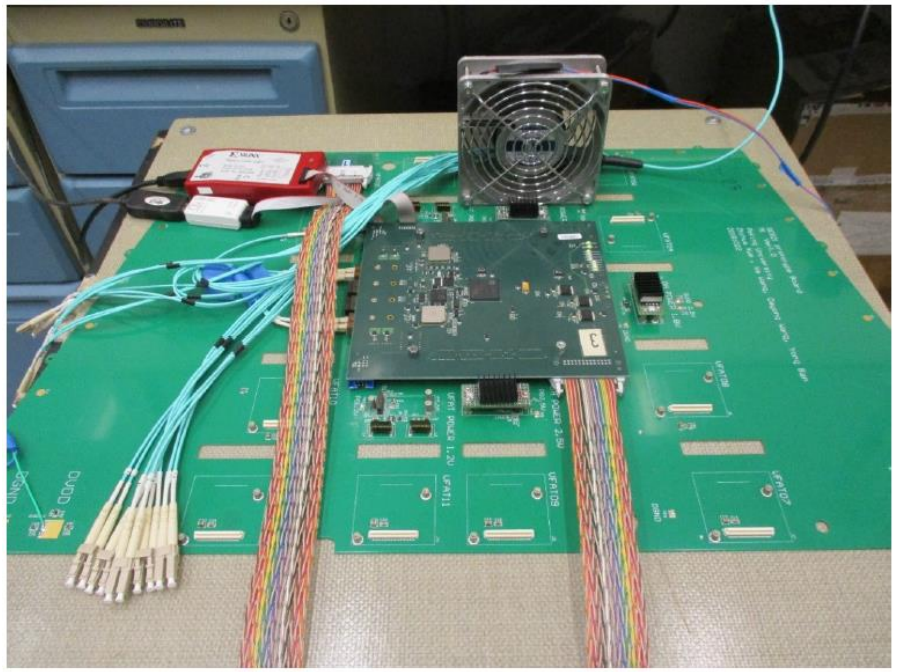
➢ Data transmission test

Slow software driven data transmission test
• All differential inputs from VFAT connectors to Artix-7 FPGA are OK









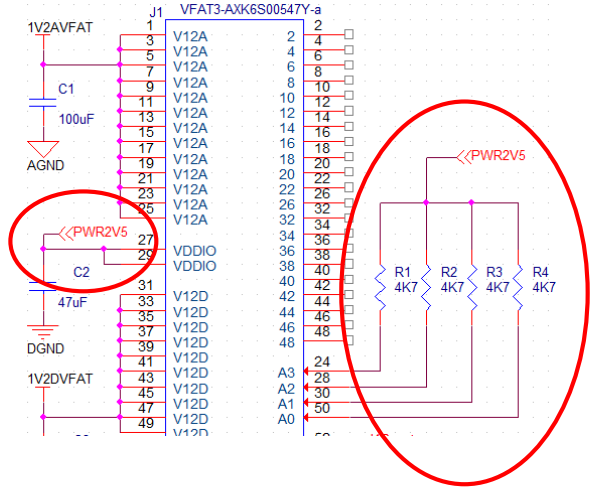
Data Transmission Test **on M1 GEB**

The goal: check data transmission at 320MHz via twisted pair cable
- 2 m long cable (much longer than the real Master-Slave connection)
- PRBS patterns from the Master/Slave connector to one of the VFAT slots
- **no errors in ~1 hour (BER<10^{-13})**

PRBS: Pseudo-Random Binary Sequence

2.2 GE2/1 GEB summary

- The first round of M1-M4 principle model design, production and testing
  - Design requirements and goals of GEB.
  - Determine the connection sequence and method of interface signals.
  - Understand the difficulties of large-size circuit board production.
  - The impedance control design parameters are limited.



PlugIn Card (VFAT)

- The second round of M5-M8 principle model design, production and testing
  - **Modified VFAT interface, added location address and 2.5V power supply. (GBTx in August last year)** To achieve 320MHz differential signal transmission.
  - Mechanical strength and shielding.

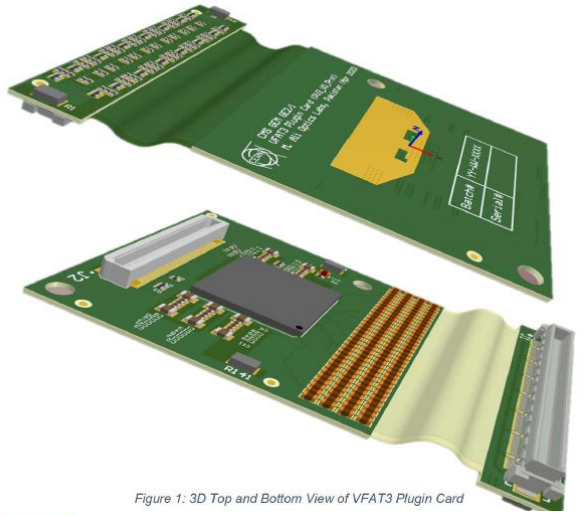


Figure 1: 3D Top and Bottom View of VFAT3 Plugin Card

- The third round of M1-M4 production model design and production
  - Modified VFAT interface
  - Improve the production quality of circuit boards and improve the yield rate

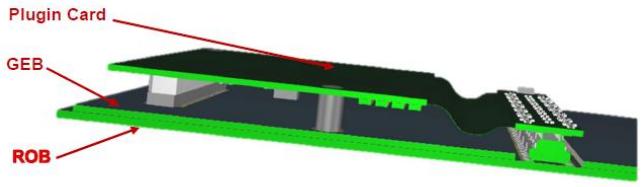
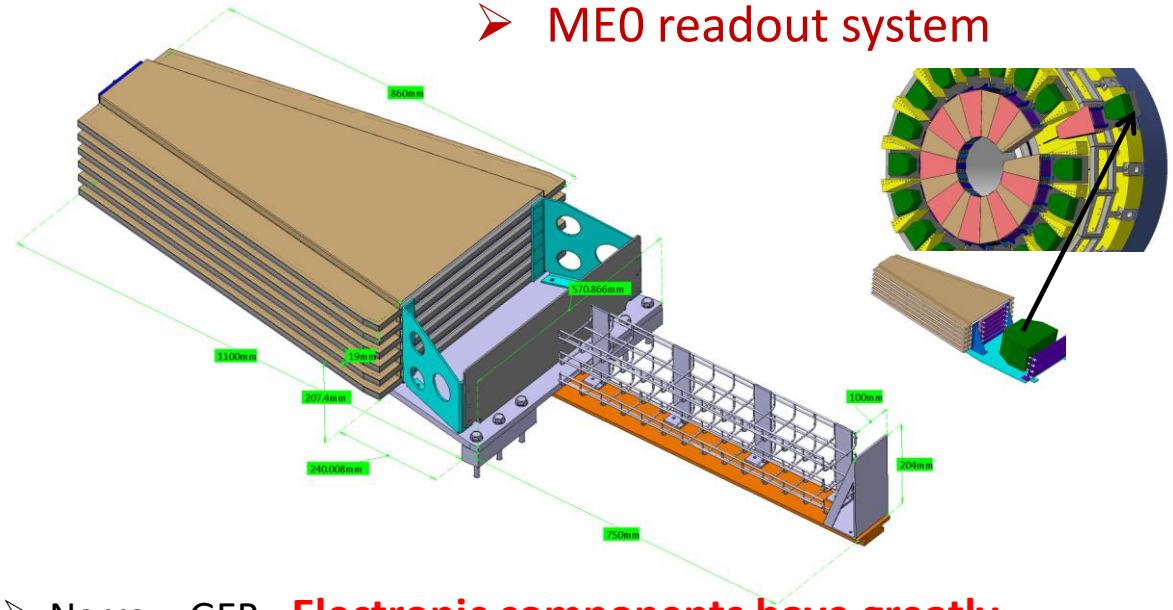


Figure 2: Assembly View of GEM Electronics

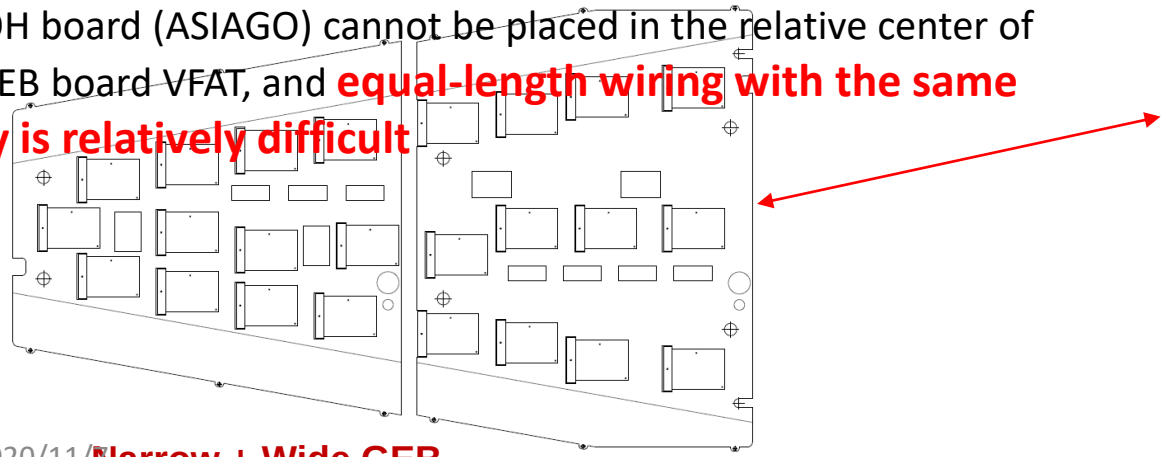
3. ME0 GEB development

➢ ME0 readout system



➢ Narrow GEB: **Electronic components have greatly increased in density**, making layout and wiring difficult

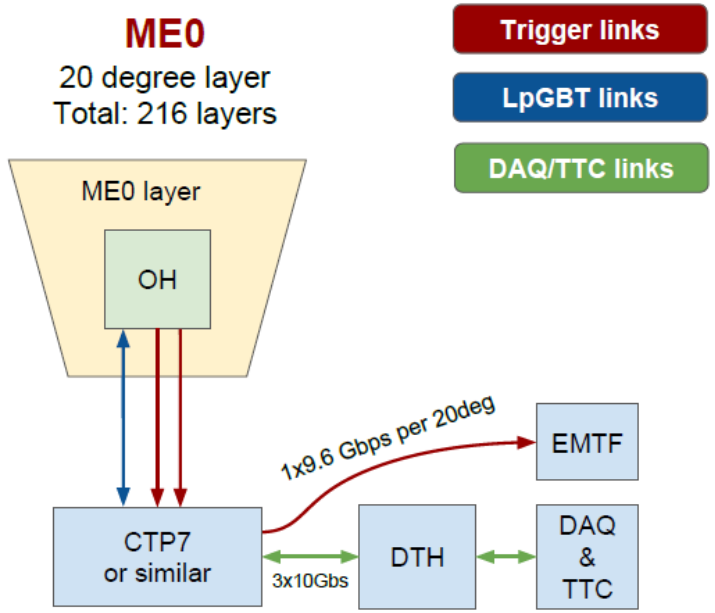
➢ The OH board (ASIAGO) cannot be placed in the relative center of the GEB board VFAT, and **equal-length wiring with the same delay is relatively difficult**



Narrow + Wide GEB

The main hardware components required by ME0 (not including the spare module, the optical link is included in the corresponding board)

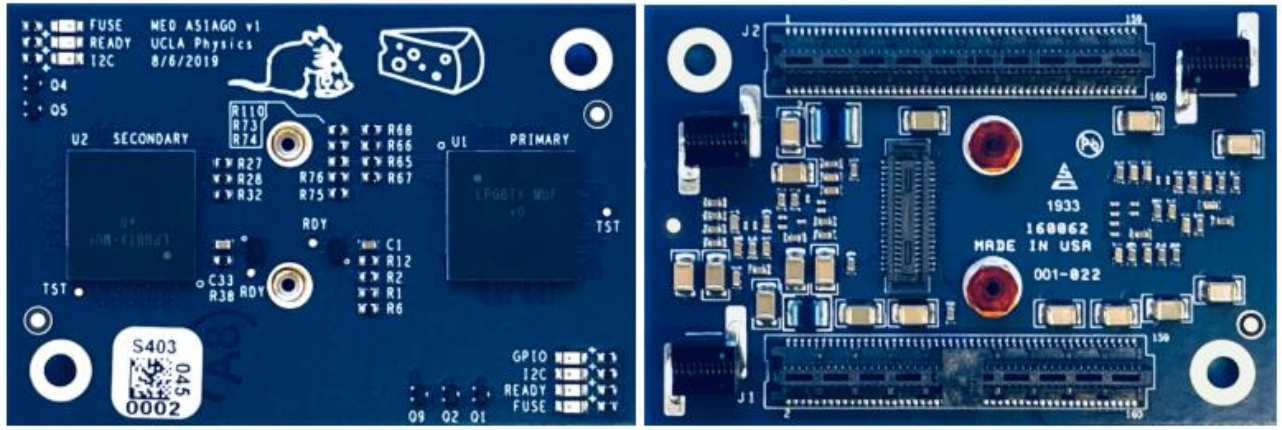
- **Triple ME0 module: 216**
  - **Each detector is read out by 48 VFAT3**
- **GEB: 216 （Narrow GEB+ Wide GEB）**
- **OH board: 216（ASIAGO: 864）**
- **VFAT(PlugIn Card) 5194**
- **HV board: 36**
- **LV board: 36**



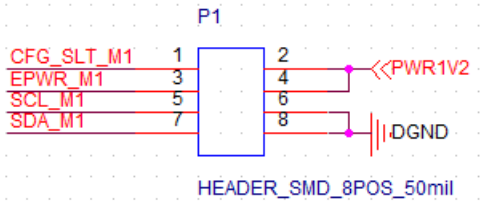
ME0 electronics readout system

ME0 GEB circuit design

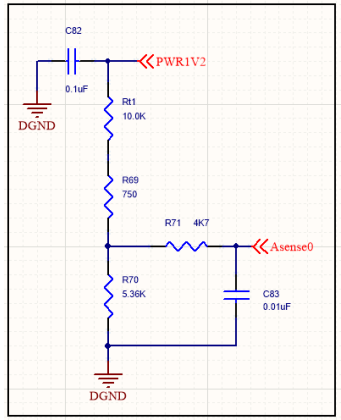
- First round design of Narrow and Wide prototype boards
  - Add OH interface
  - Add FPGA configuration interface
  - **Add temperature measurement circuit**
  - Increase current detection protection
  - **3 or 4 FEAST modules compatible design(in order to reduce production cost)**
  - Fixing of optical fiber(Zipline)

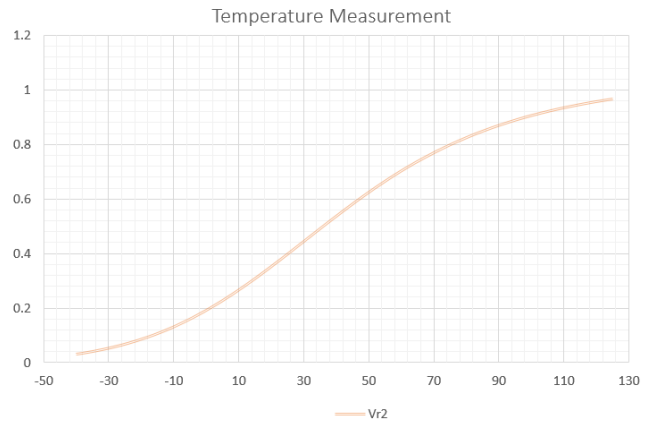


ME0 OH board (ASIAGO)

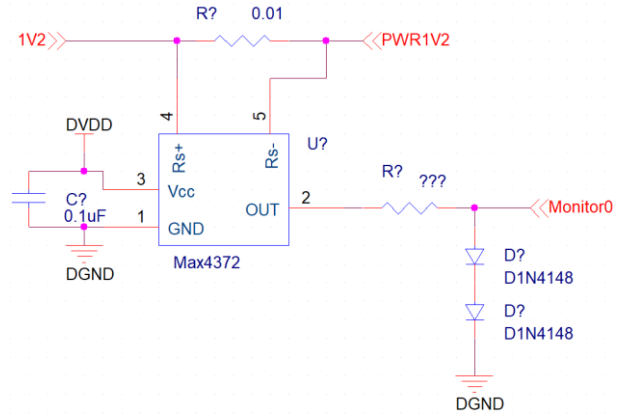


OH configuration interface





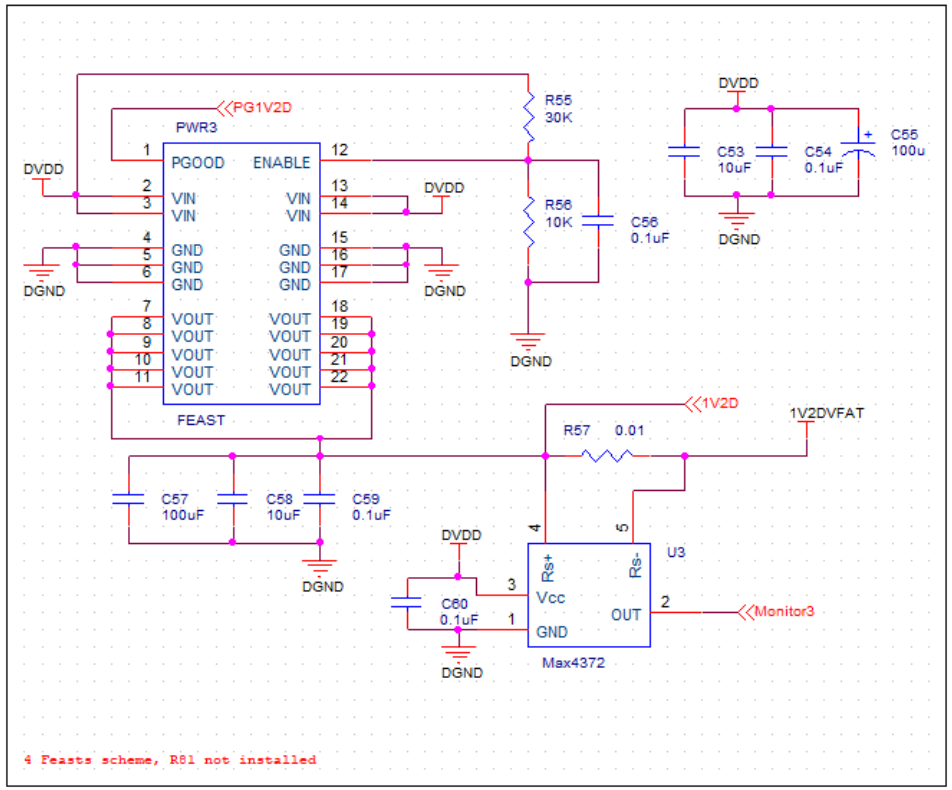
NTC thermistor

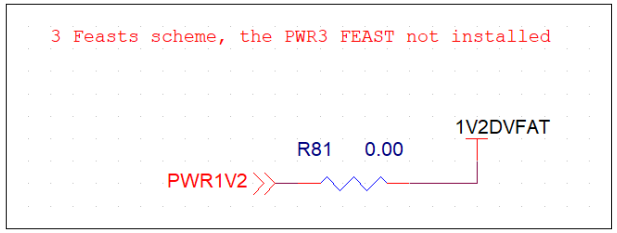


Input protection using clamp

➢ FEAST module: 3 or 4 compatible designs

- 4 Feast plan (R81 is not installed)
- OH power supply:
  - PWR1: PWR1V2 --- 1.3A/ASIAGO, total 2.6A
  - Each measurement is least than 1mA
  - PWR2: PWR2V5 --- 0.2A/ASIAGO,0.4A in total
  - EachVFAT is less than 1mA
- VFAT power supply:
  - PWR3: 1V2DVFAT --- 70mA/VFAT, total 840mA
  - PWR4: 1V2AVFAT --- 140mA/VFAT, total 1.68A
  - PWR2: PWR2V5 --- each VFAT is less than 1mA
- 3 Feast plan (PWR3 FEAST module is not installed)
- OH power supply:
  - PWR1: PWR1V2 --- 1.3A/ASIAGO, total 2.6A
  - Each temperature is less than 1mA
  - PWR2: PWR2V5 --- 0.2A/ASIAGO, total 0.4A
  - Each VFAT is less than 1mA
- VFAT power supply:
  - PWR4: 1V2AVFAT --- 140mA/VFAT, total 1.68A
  - PWR1: PWR1V2 --- 70mA/VFAT, total 840mA
  - PWR2: PWR2V5 ---VFAT is less than 1mA

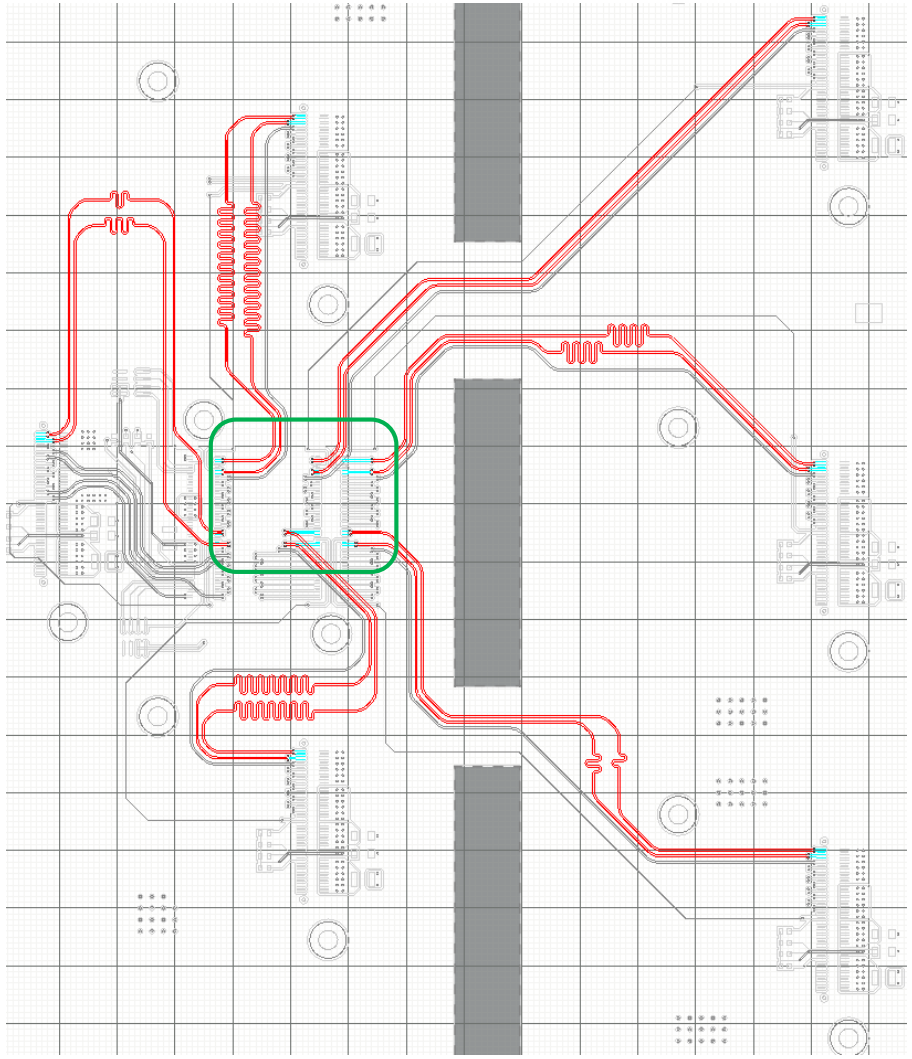




- 4 Feast plan:
- PWR1: PWR1V2 --- 2.6A
- PWR2: PWR2V5 --- 0.4A
- PWR3: 1V2DVFAT --- 0.84A
- PWR4: 1V2AVFAT --- 1.68A
- 3 Feast plan:
- PWR1: PWR1V2 --- 2.6A+0.84A ≈ 3.5A
- PWR2: PWR2V5 --- 0.4A
- PWR4: 1V2AVFAT --- 1.68A

R81、PWR3 module cannot be installed at the same time to avoid short circuit

Equal length wiring



Narrow ME0 GEB J1-J6 & OH1 (on the Left)

- Narrow ME0 GEB J1-J6 & OH1 (on the Left)

Designator	Average Length (mm)
J1CLK	128.501
J1RXD	128.501
J2CLK	128.501
J2RXD	128.501
J3CLK	128.501
J3RXD	128.501
J4CLK	128.501
J4RXD	128.501
J5CLK	128.501
J5RXD	128.501
J6CLK	128.501
J6RXD	128.505

- Narrow ME0 GEB J7-J12 & OH2 (on the right)

Designator	Average Length (mm)
J7CLK	143.067
J7RXD	143.067
J8CLK	143.067
J8RXD	143.067
J9CLK	143.067
J9RXD	143.067
J10CLK	143.067
J10RXD	143.067
J11CLK	143.067
J11RXD	143.067
J12CLK	143.063
J12RXD	143.067

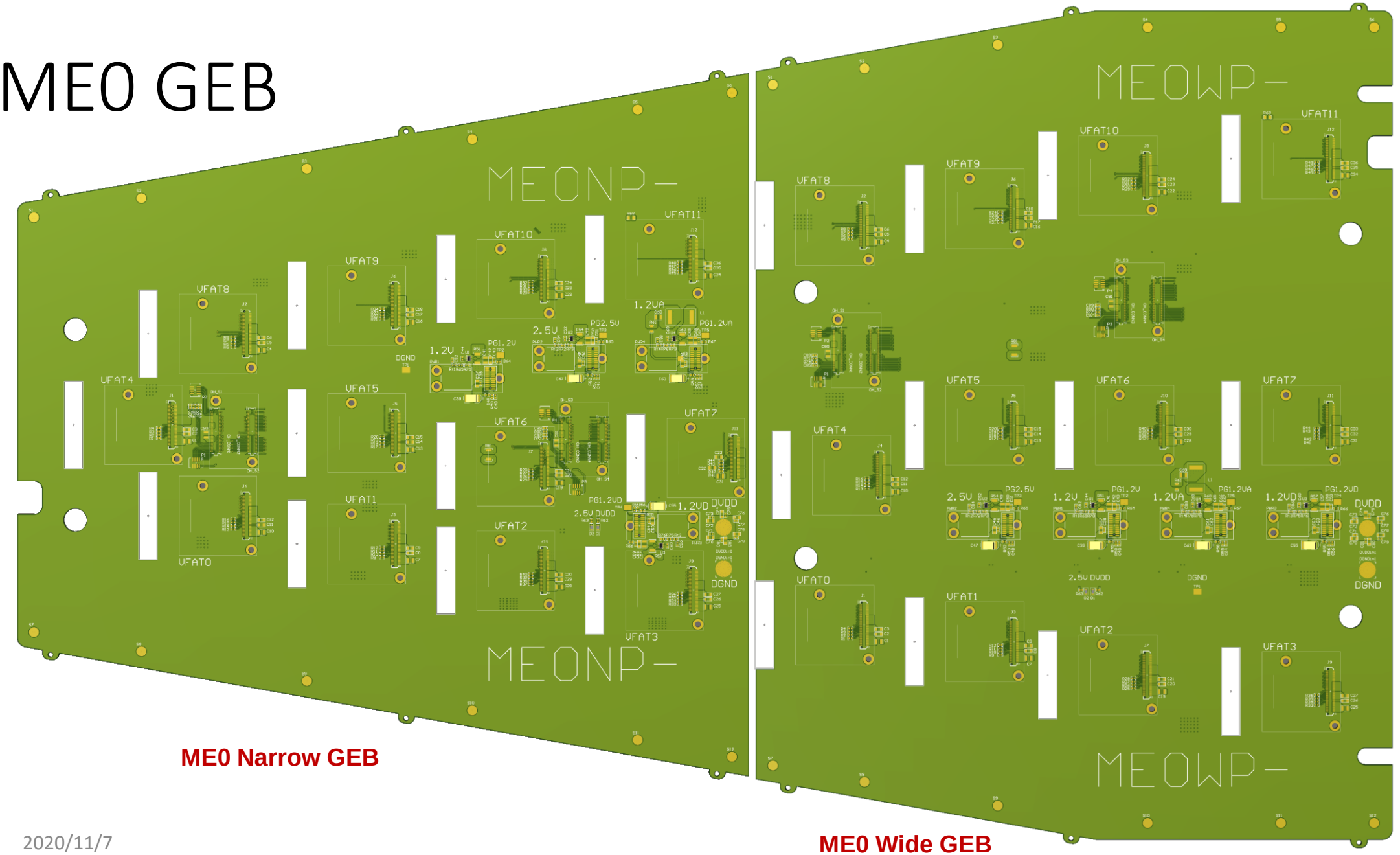
- Wide ME0 GEB J1-J6 & OH1 (on the Left)

Designator	Average Length (mm)
J1CLK	208.835
J1RXD	208.835
J2CLK	208.835
J2RXD	208.835
J3CLK	208.835
J3RXD	208.83
J4CLK	208.835
J4RXD	208.835
J5CLK	208.835
J5RXD	208.835
J6CLK	208.835
J6RXD	208.835

- Wide ME0 GEB J7-J12 & OH2 (on the right)

Designator	Average Length (mm)
J7CLK	276.24
J7RXD	276.24
J8CLK	276.24
J8RXD	276.24
J9CLK	276.24
J9RXD	276.236
J10CLK	276.24
J10RXD	276.24
J11CLK	276.24
J11RXD	276.24
J12CLK	276.24
J12RXD	276.24

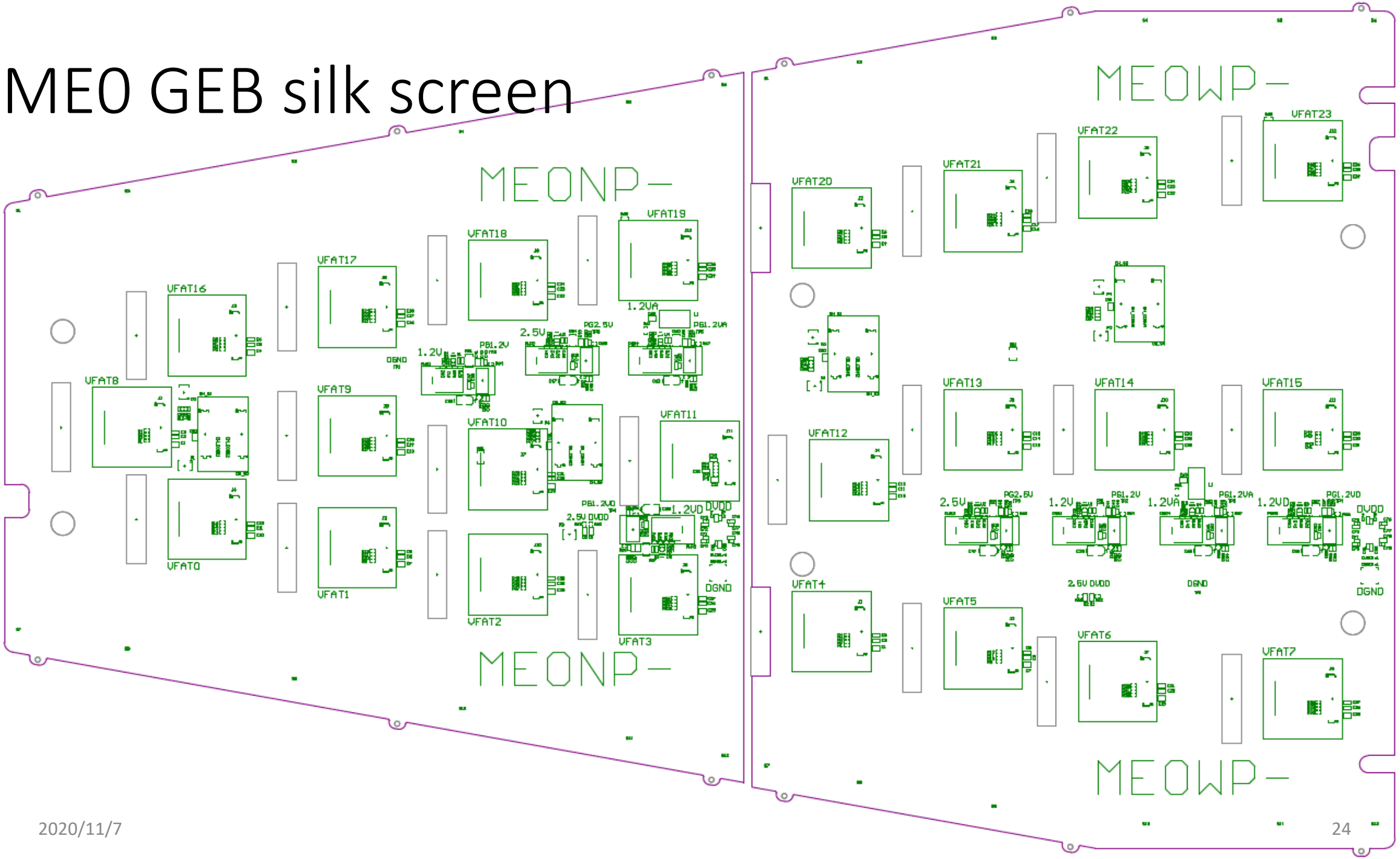
ME0 GEB



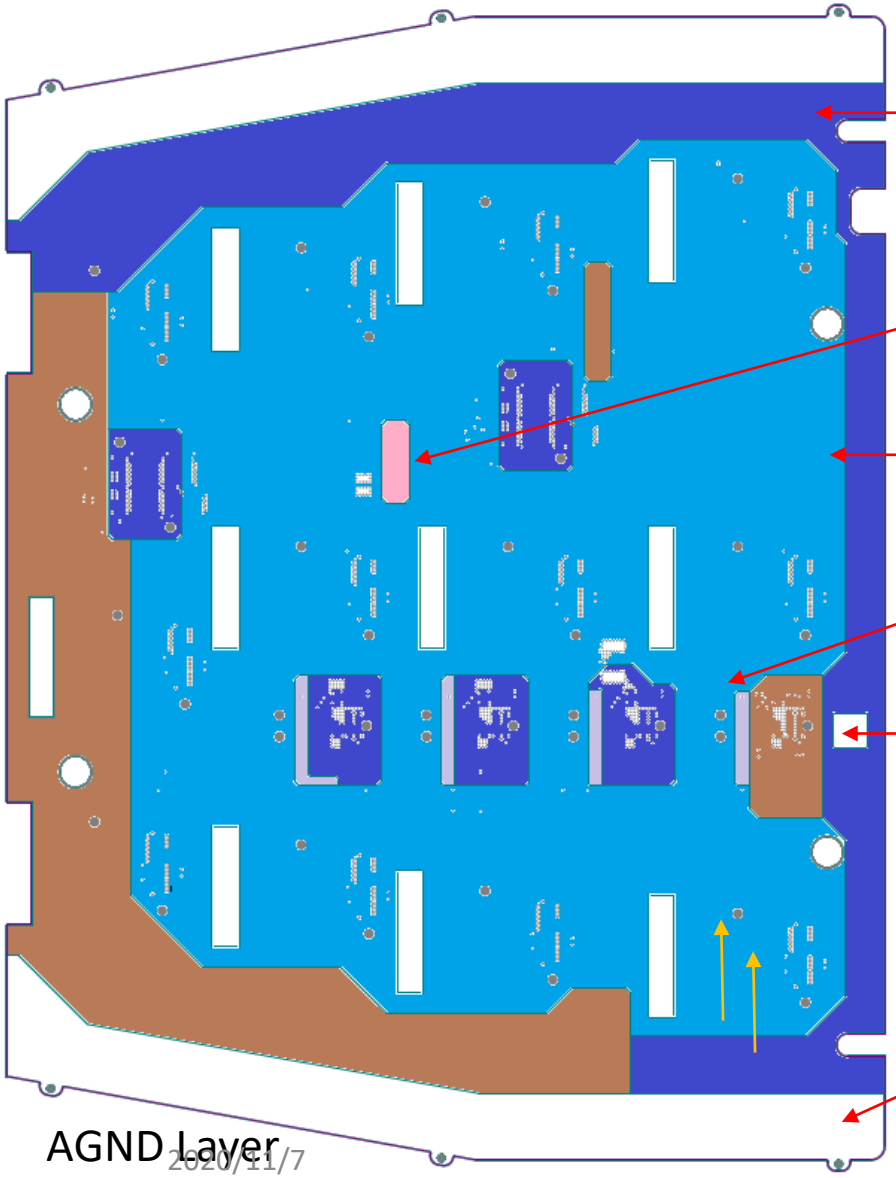
ME0 Narrow GEB

ME0 Wide GEB

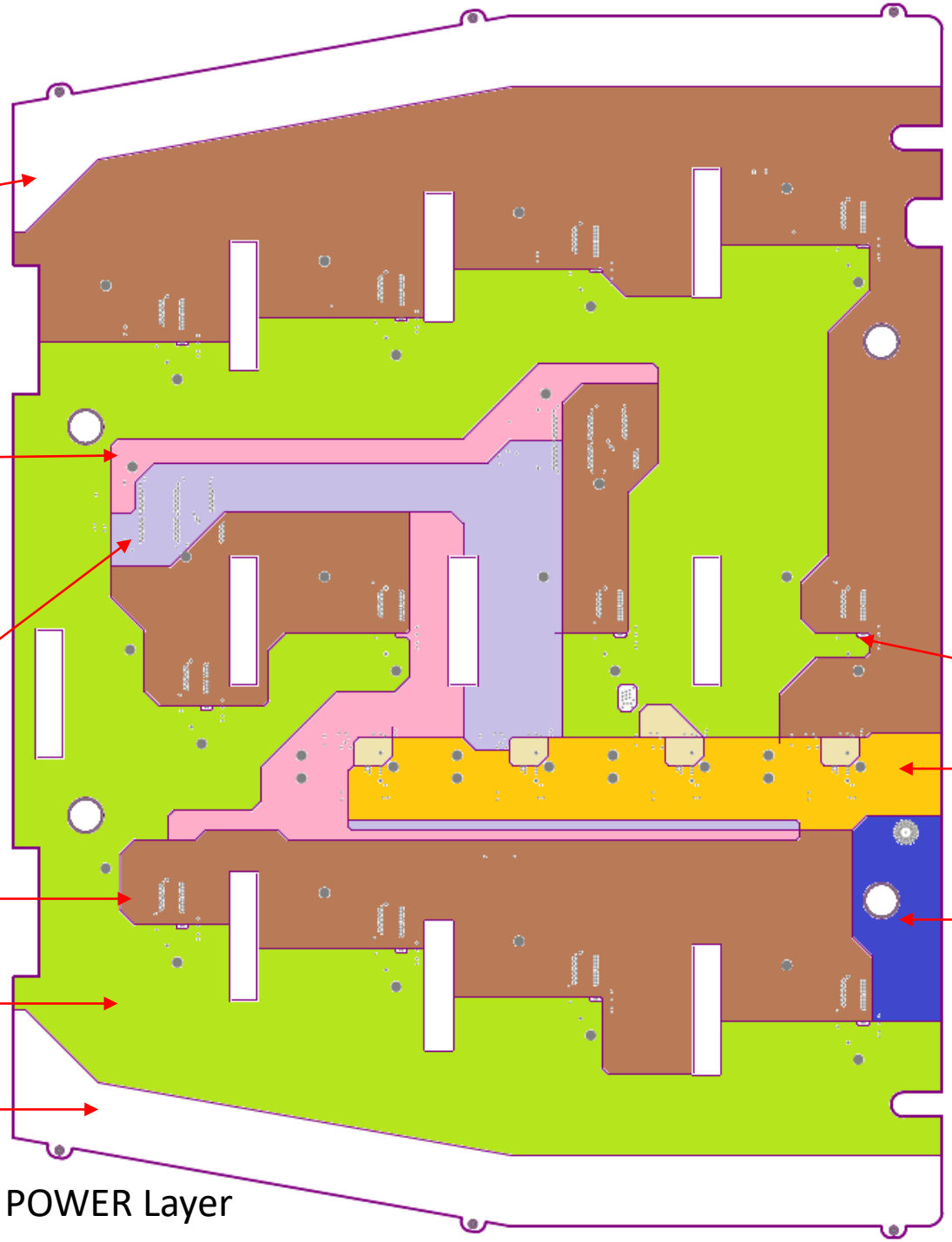
ME0 GEB silk screen

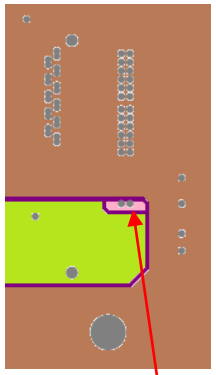


- ME0 Wide GEB power split



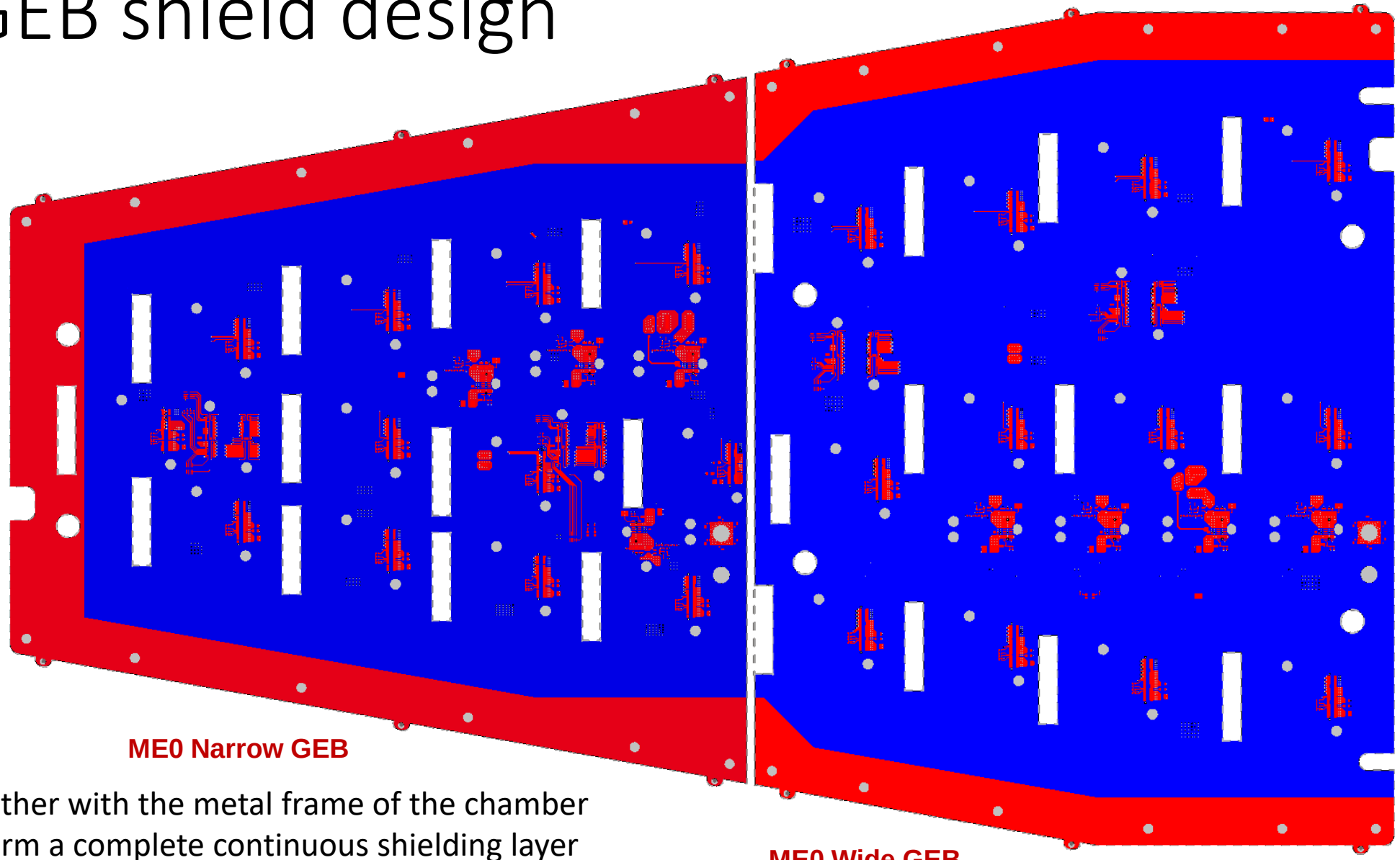
AGND Layer





POWER Layer

ME0 GEB shield design



ME0 Narrow GEB

ME0 Wide GEB

Together with the metal frame of the chamber
to form a complete continuous shielding layer

Simulation of M1-M8 and ME0

➢ Reflection loss, insertion loss and TDR

The change of the signal line will cause the characteristic impedance of the signal line to change, thereby causing reflection.

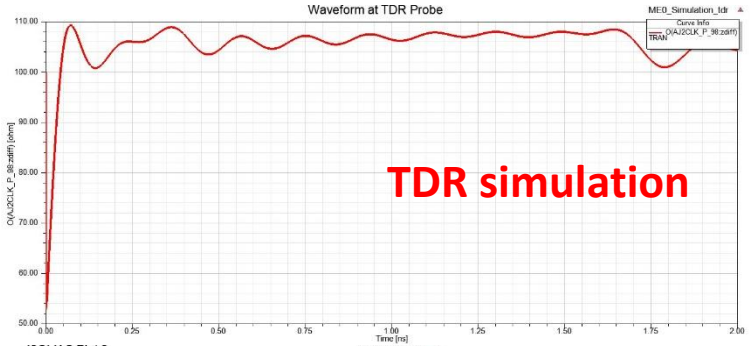
$$\Gamma = \frac{Z-1}{Z+1}$$

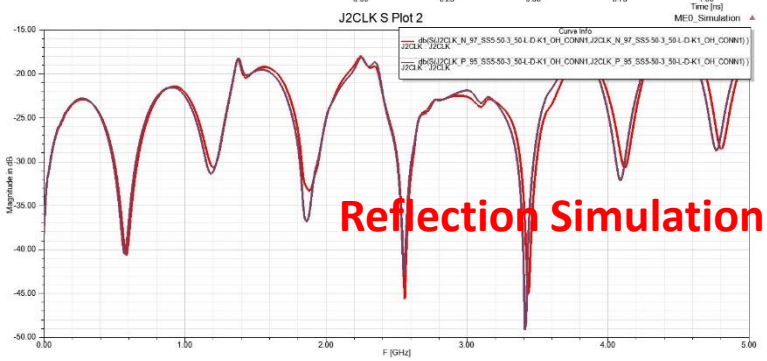
Signal may be reflected. The reflection and loss of signal for the differential line may have a greater impact on signal transmission and may cause bit errors. So we simulate M1-M8 and ME0.

Simulation includes reflection loss, insertion loss and TDR.

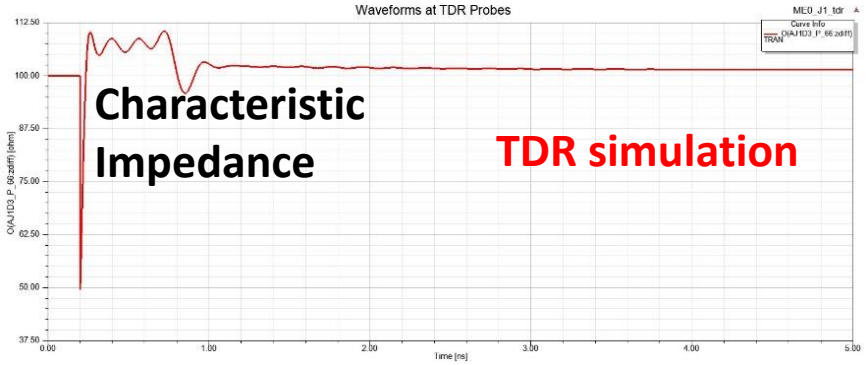
TDR: Time domain reflectometry, can detect the change of characteristic impedance the differential line at different positions.

Some simulation results of ME0

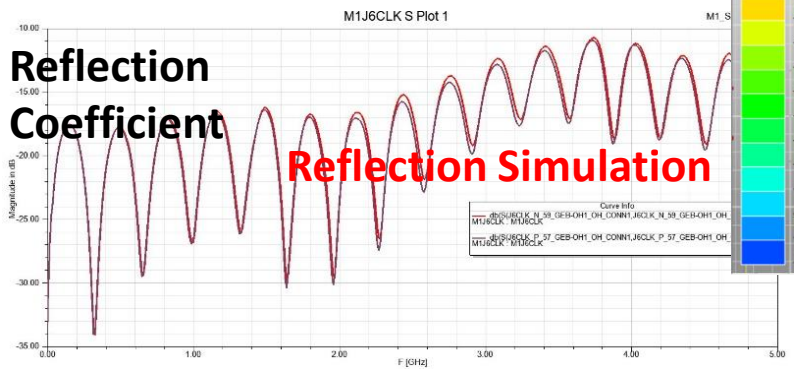




Some simulation results of M1-M8



Time



Frequency

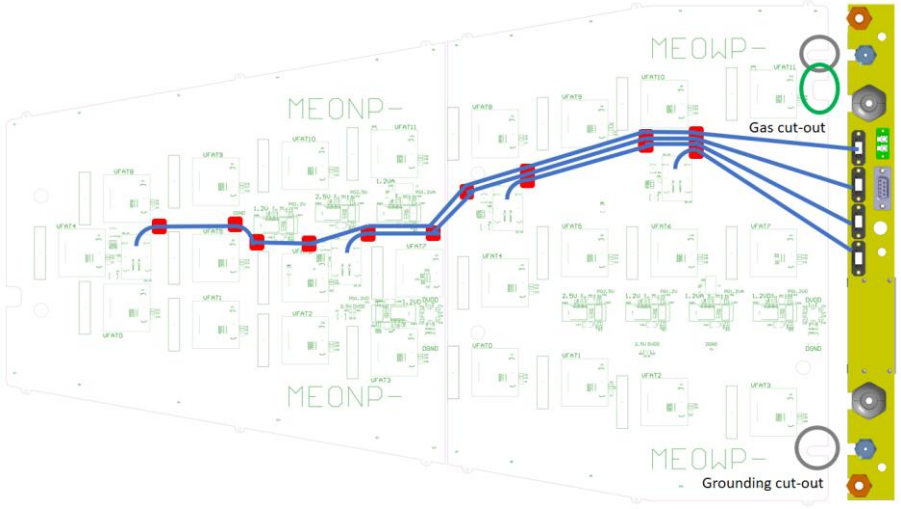
DC voltage drop simulation

PWR2V5

We found that the characteristic impedance fluctuation is within 12.5%, and the reflection loss is around -25dB, which can meet the bit error rate requirement of the M1 test.

Summary of ME0

- First round design of Narrow and Wide prototype boards
  - 3 or 4 FEAST modules compatible design(in order to reduce production cost)
  - Fiber Routing & Fiber Fixing ME0 GEB
  - FEAST Arrangement
- Simulation of ME0
  - Reflection loss, insertion loss and TDR
  - DC voltage drop
  - Characteristic Impedance
- ME0 work schedule
  - Pass the 3D inspection as soon as possible and deliver to the factory to start production.



Thank you!