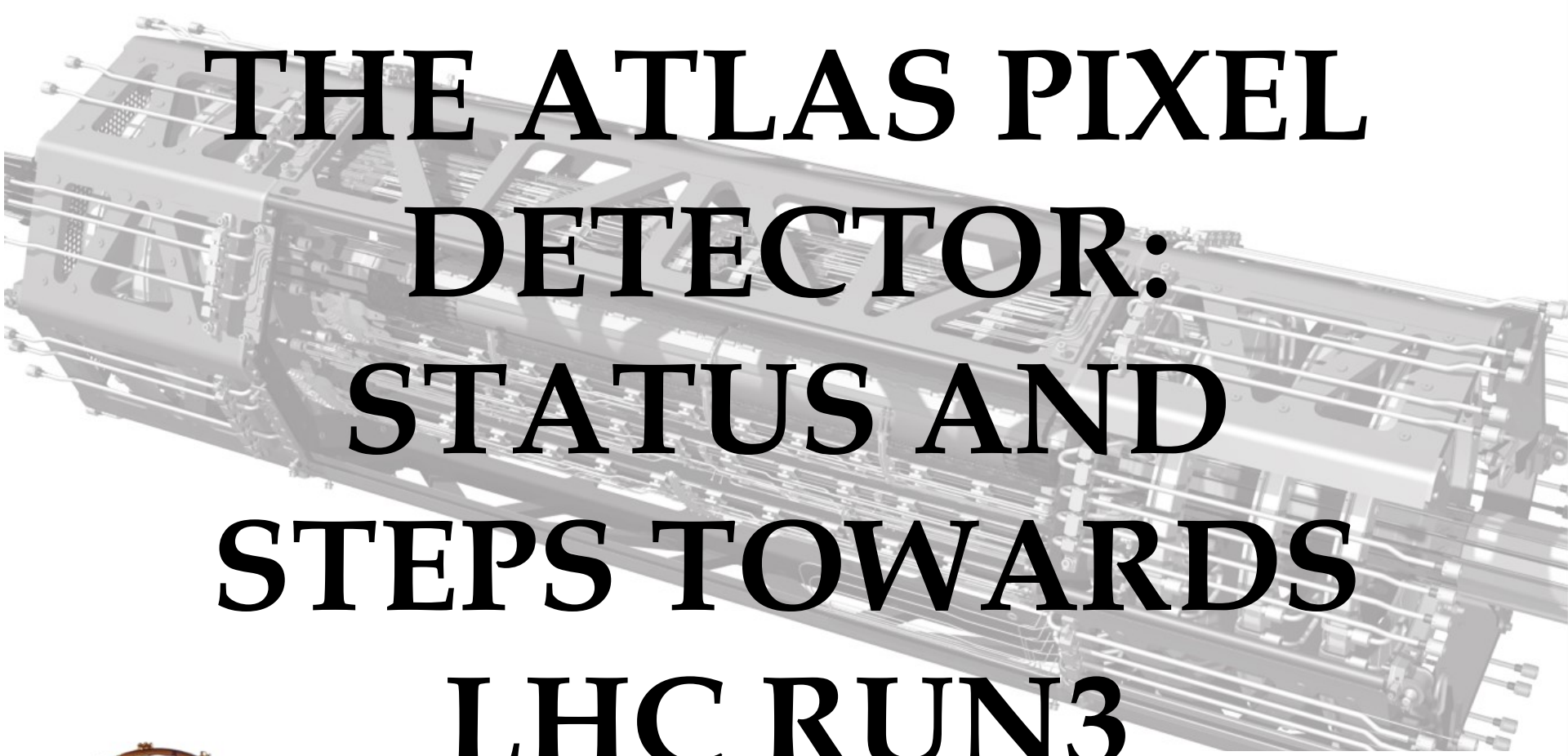
THE ATLAS PIXEL DETECTOR: STATUS AND STEPS TOWARDS LHC RUN3



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6th November 2020

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INTRODUCTION

Involved in ATLAS Pixel operation since 2016:

- Pixel DAQ Coordinator (2017)
- Pixel Run Coordinator (2018)
- Pixel Technical Coordinator (2019-current)

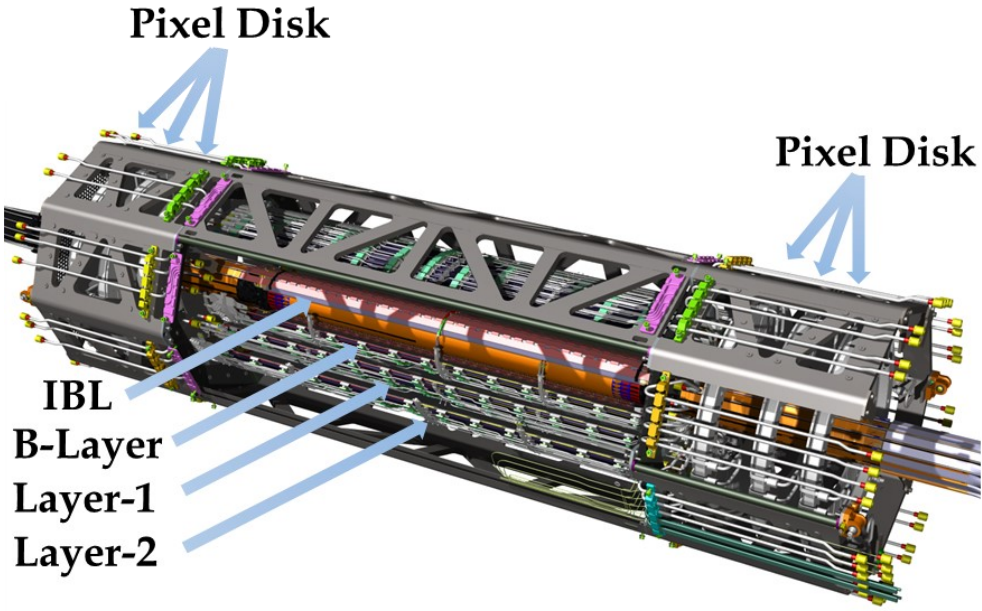
Working with a team of colleagues from IHEP:

- Xiaotong Chu
- Lianyou Shan
- Da Xu
- Han Cui

THE ATLAS PIXEL DETECTOR

4 cylindrical layers (**Insertable B-Layer**, **B-Layer, Layer1, Layer2**) and 2 end-caps (3 **Disk** layers each) with different detector technologies:

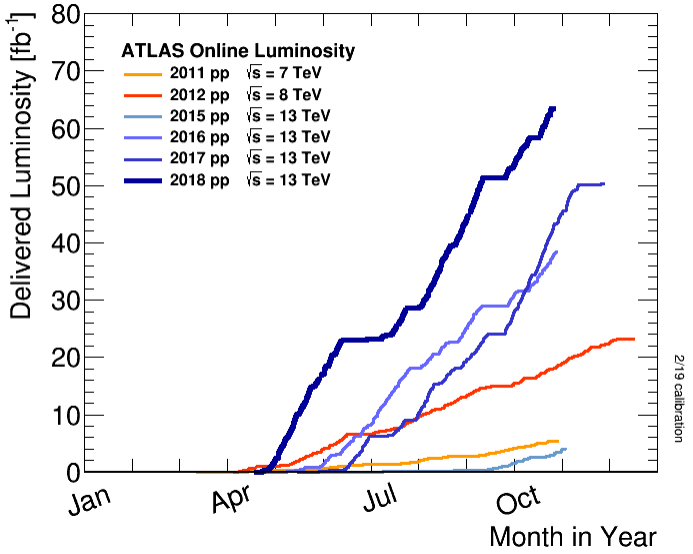
- **FE-I3** installed during 2007:
  - Technology: standard 250 nm CMOS
  - Radiation hardness: 50 Mrad
  - Sensor: 250 μm n+-in-n
- **FE-I4** installed during LS1 in 2014 (IBL):
  - Technology: 130 nm CMOS
  - Radiation hardness: 250 Mrad
  - 2 sensors technologies:
    - Planar: 200 μm n+-in-n
    - 3D: 230 μm n+-in-p

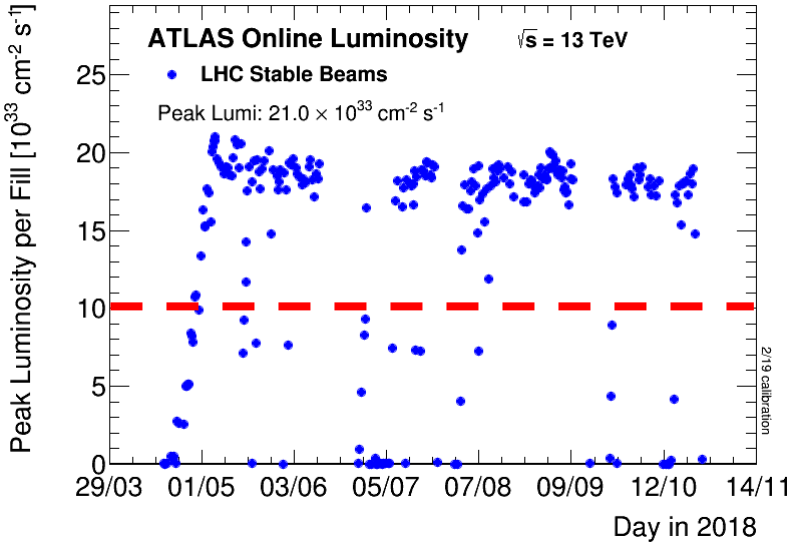


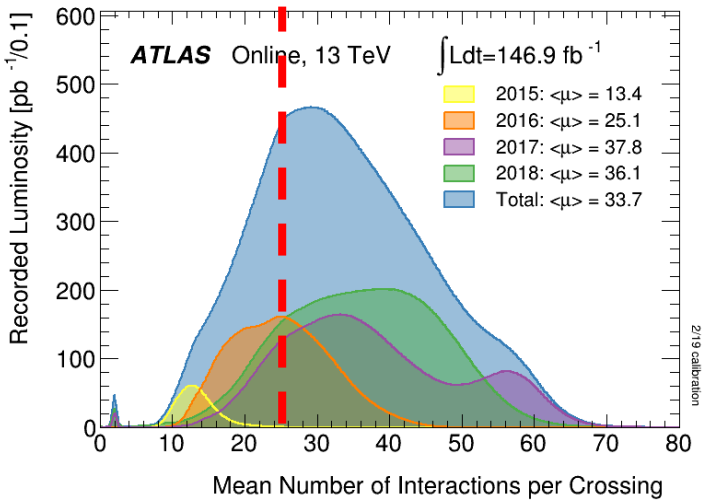
	FE-I3	FE-I4
Pixel size [μm^2]	50x400	50x250
Pixel array	18x160	80x336
Chip size [mm^2]	7.6x10.8	20.2x19.0
No. of transistors [millions]	3.5	87
Active fraction	74%	89%
Analog/digital current [μA/pix]	26 / 17	10 / 10
Digital current [μA/pix]	17	10
Analog/digital voltage [V]	1.6 / 2.0	1.5 / 1.2

SUMMARY AND PERFORMANCE OF THE LHC

Design conditions for the ATLAS Pixel Detector (peak luminosity of $L = 1x10^{34}$ cm^{-2} s^{-1} and pile-up of $\mu \approx 25$) were largely exceeded during Run 2.







LHC performance:

- Challenging conditions with peak $L \approx 2x10^{34}$ cm^{-2} s^{-1} and $\mu \approx 60$
- Similar challenging conditions are expected for LHC Run3

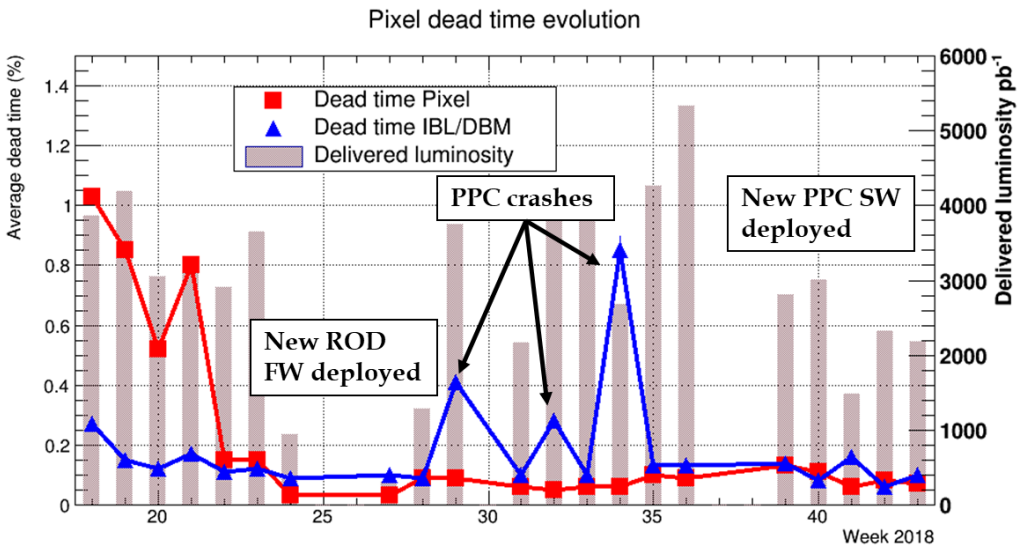
SUMMARY OF RUN2 DATA TAKING

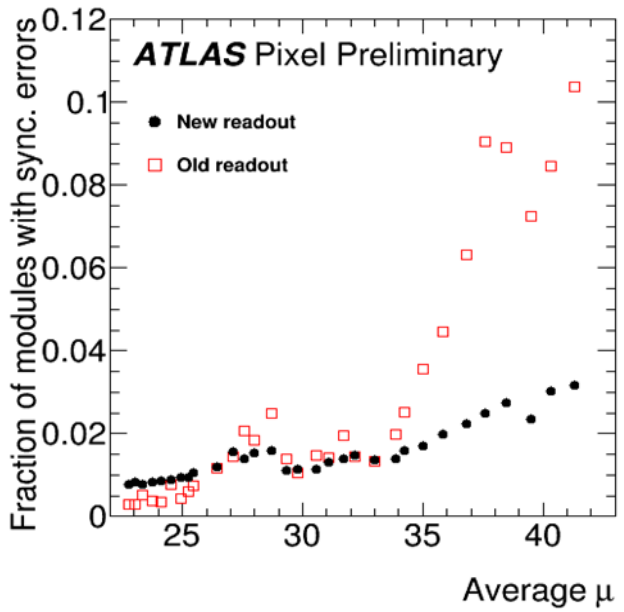
Off detector electronics were upgraded during Run2:

- Increase bandwidth
- New firmware recovery mechanism deployed → Improvement of detector desynchronization
- New software recovery tools deployed → Great improvement of the dead time

Module Link Occupancy at 100kHz L1					
	μ	B-Layer 160Mbps	Layer-1 160Mbps	Layer-2 80Mbps	Disks 80Mbps
Maximum in 2016	40	60%	81%* → 41%	119%* → 59%	75%
Maximum in Run 2	60	81%	103%* → 52%	159%* → 79%	96%
Maximum in Run 3	80	101%	125%* → 63%	188%* → 94%	115%

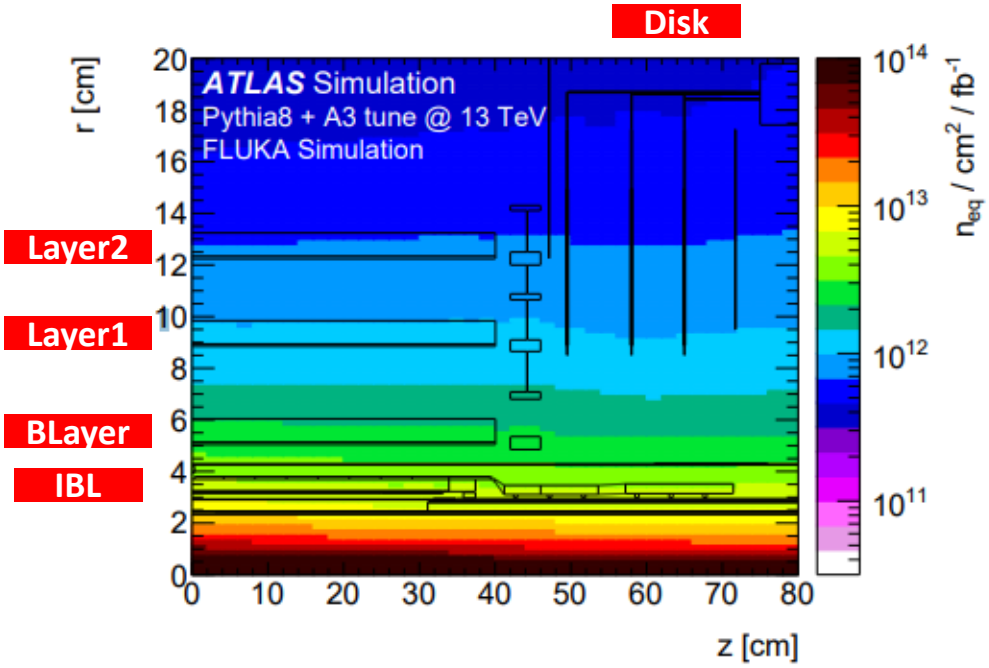
* Before upgrade

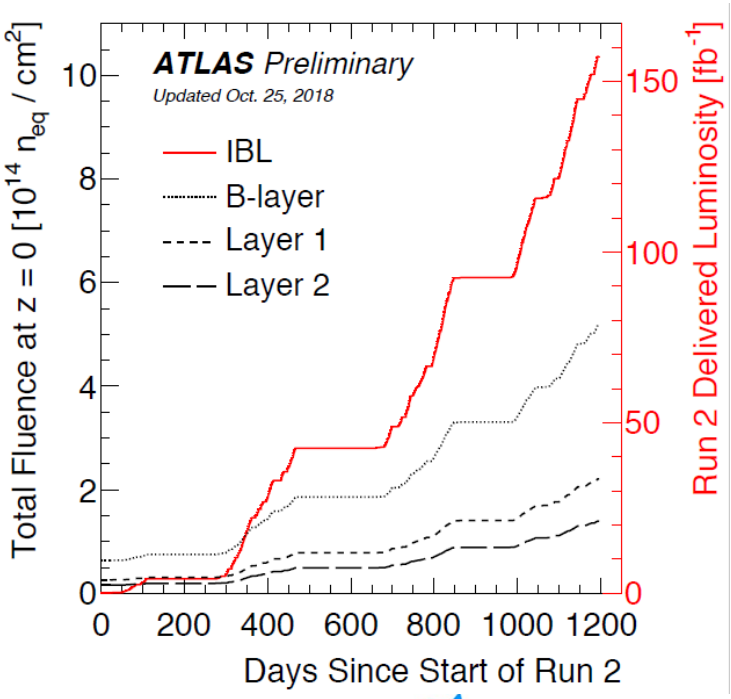




RADIATION EFFECTS IN THE ATLAS PIXEL DETECTOR

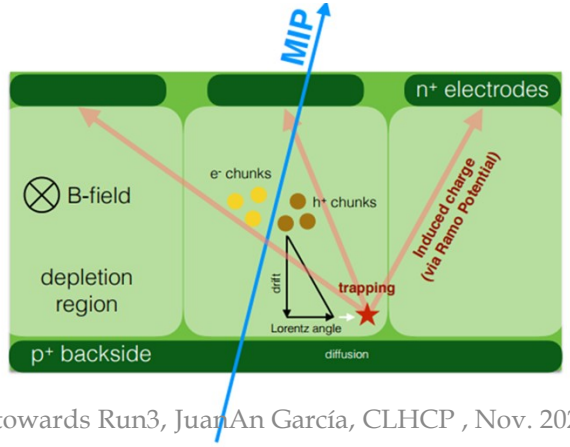
Radiation effects are visible in the Pixel detector: Fluences up to ~10^{13} hadrons (E>20 MeV) cm^{-2} fb^{-1} according to PYTHIA/FLUKA simulations.





Different types of radiation effects:

- Single Event Effects
- Radiation damage

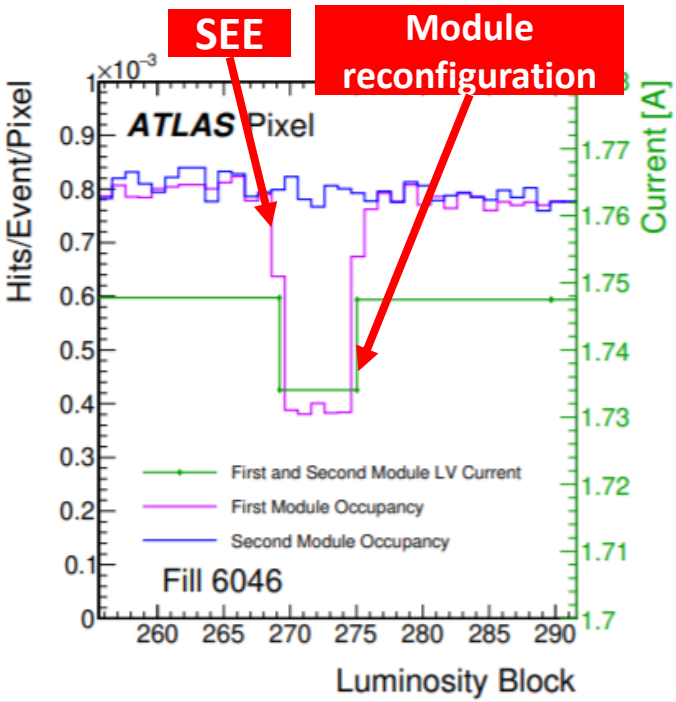


SINGLE EVENTS EFFECTS IN FE-I4

Single Event Effects (SEE) cause memory corruption in the FE registers.

Impact of SEE in the global registers:

- Step on the LV current consumption on the FE chip.
- Drop on the module occupancy being a source of inefficiency.
- Induces dead time and timeout affecting data taking efficiency.

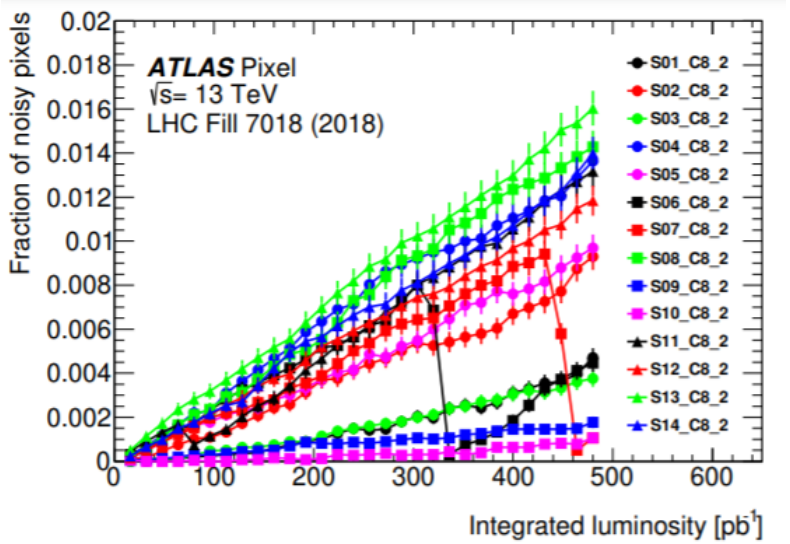


Impact of SEE in single pixel registers:

- Increase of noisy pixels.
- Increase of broken clusters and quiet (not firing) pixels.
- No major impact on tracking performance.

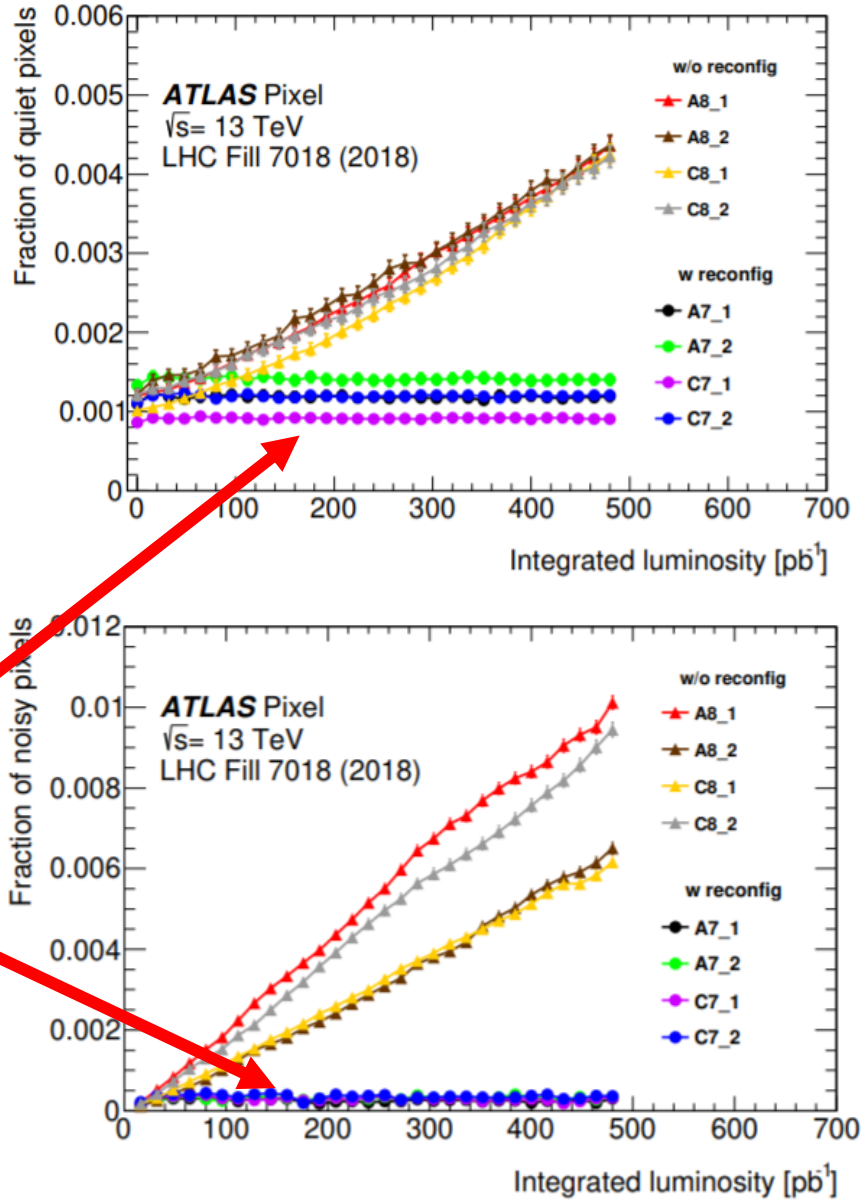
The effect of SEE have been measured during high luminosity LHC fills, a paper has been recently published: [JINST 15 (2020) 06, P06023]

Measurements of Single Event Upset in ATLAS IBL



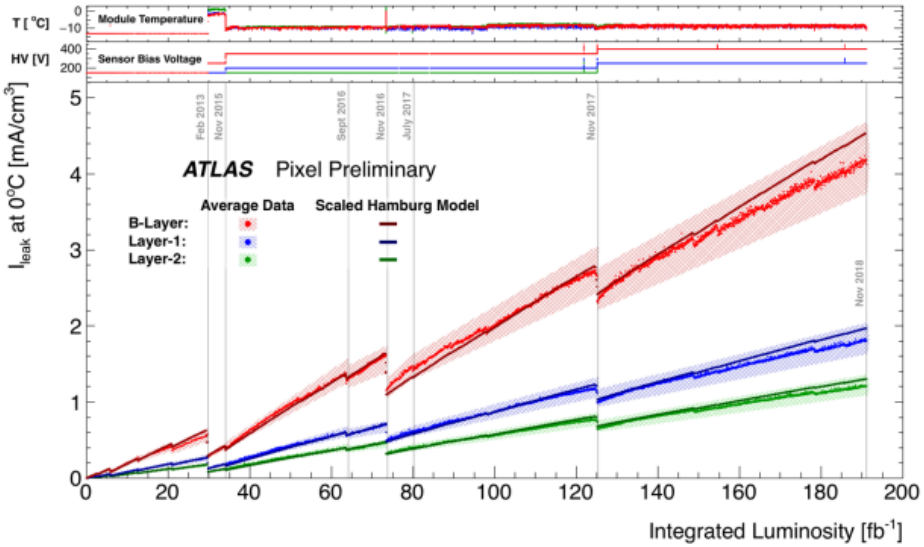
CORRECTIVE ACTIONS ON SEE

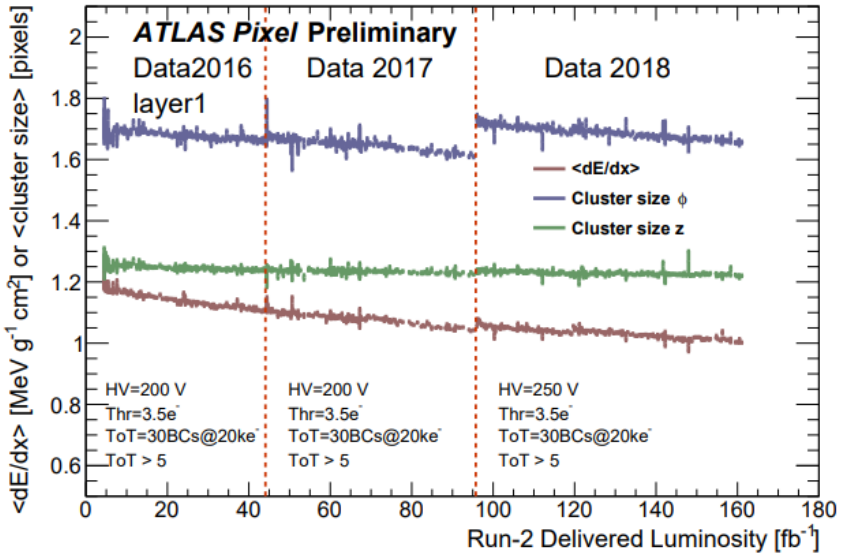
- Periodic reconfiguration of global registers implemented during Run2 (sent every ~5 s)
  → No dead time induced in data taking
- Single pixel register reconfiguration implemented but not fully deployed:
  - Full reconfiguration performed every ~11 min.
  - Tested during 2018
    → Improvement on the quiet pixel and noise level already seen
  - To be fully deployed during Run3

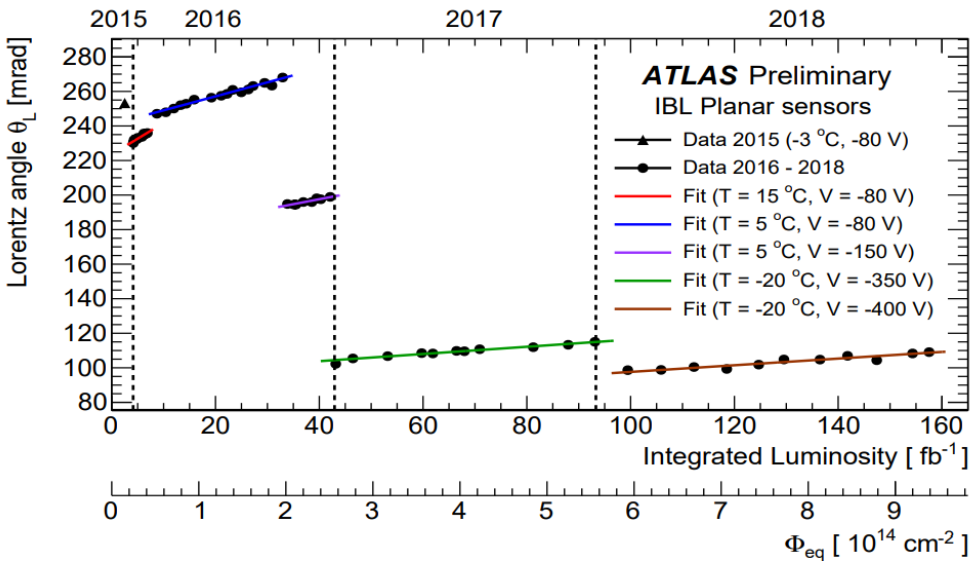


RADIATION DAMAGE

- Increase of the HV leakage current → Model predictions in agreement with measured data
- Charge trapping affecting collected charge and dE/dX
- Changes in the electric field profile affecting the cluster charge distribution and the Lorentz Angle





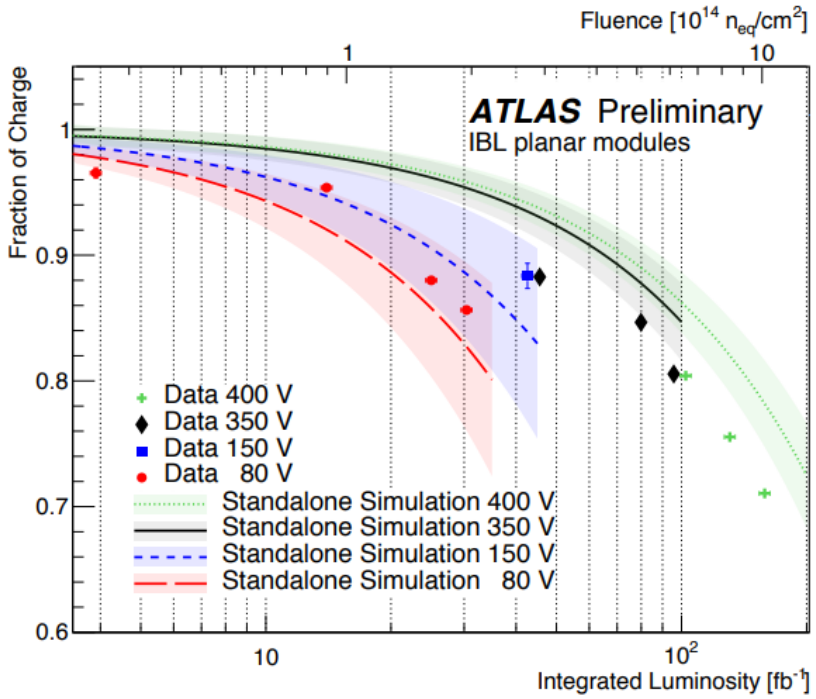


RADIATION DAMAGE

- Affect the depletion voltage.
- **Bias voltage** in the different layers increased ~yearly to partially recover full depletion area and charge collection efficiency
- Lowering of analog and digital (ToT cut) threshold during 2018 to compensate charge collection efficiency → To be revisited for Run3

Threshold	2017	2018
IBL	2500e, ToT>0	2000e, ToT>0
B-layer	5000e, ToT>5	4300e(*), ToT>3
Layer-1	3500e, ToT>5	3500e, ToT>5
Layer-2	3500e, ToT>5	3500e, ToT>5
Endcap	4500e, ToT>5	3500e, ToT>5

(*) M1A/M0/M1C : 4300e, otherwise : 5000e

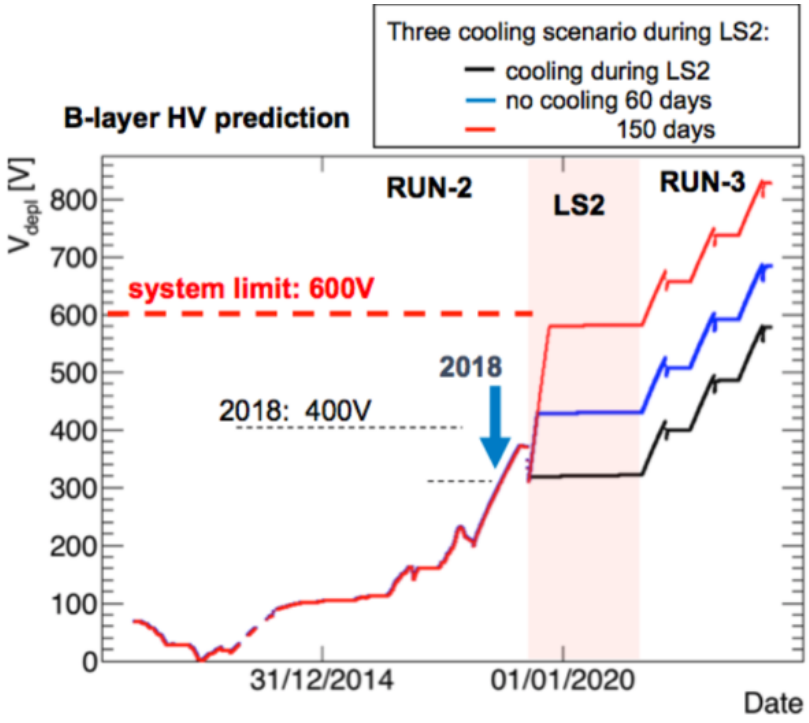


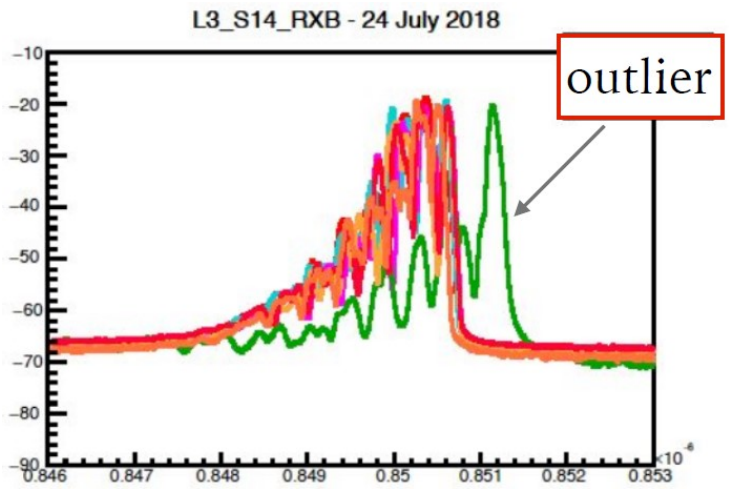
A radiation damage model has been developed for the ATLAS Pixel Detector → JINST 14 (2019) no.06, P06012

Modelling radiation damage to pixel sensors in the ATLAS detector

LS2 OPERATION

- Detector kept cold -5ºC to avoid reverse annealing.
- Detector turned on periodically:
  - Monitoring and calibration scans
  - Investigation of problematic modules
  - Test DAQ developments
  - Combined ID cosmic runs
- VCSEL (transceiver) array on opto-boards was one of the major HW failures during Run2:
  - Channel failures can be predicted from shift in the optical spectrum ~50 problematic channels identified
  - Optoboard replacement planned in February 2021





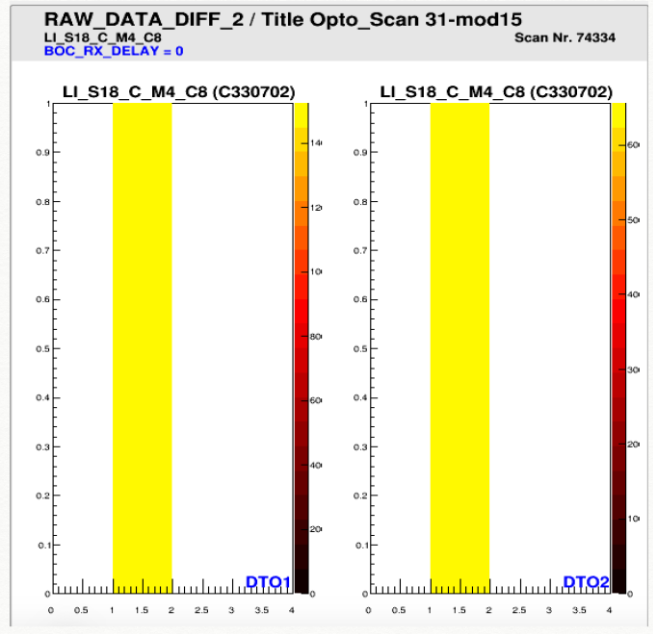
LS2 DEVELOPMENTS

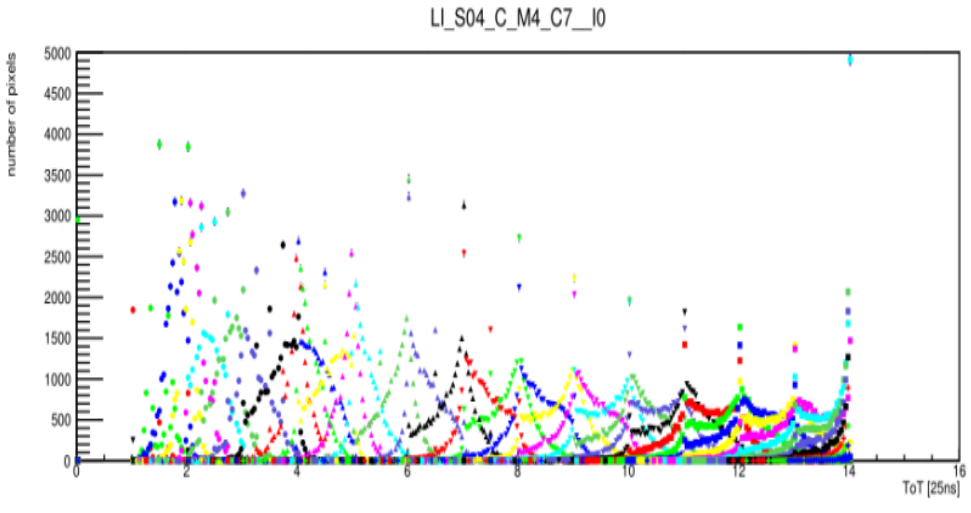
- Large number of software and firmware updates during LS2:
  - DAQ consolidation after 3 years of readout upgrade
- Firmware developments:
  - Resolved long-standing data corruption (rate ~10-6)
  - Mitigation of desynchronization in high-rate/high-occupancy runs
- ROD software migration to run under embedded Linux OS
  - Stability improvement and debugging capabilities wrt old Xilinx kernel
- Further improvements:
  - Expand global register configuration to FE-I3
  - Parallel ROD recovery
  - Migration to CC7, TDAQ9, integration of ALTI trigger interface

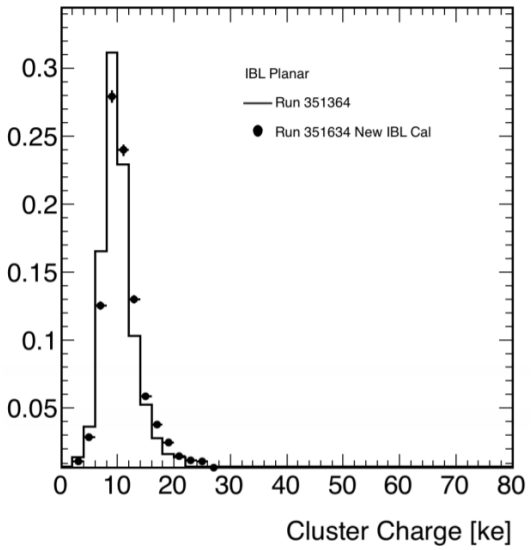
LS2 DEVELOPMENTS

Pixel tasks from IHEP colleagues:

- Development of IBL opto-scan → **Da Xu**
- New ToT to charge conversion in FE-I4 using average charge per ToT → **Xiaotong Chu**
- New ToT to charge conversion in FE-I3 using interpolation method → **Han Cui**
- Implementation in Athena of the new calibration methods → **Lianyou Shan**







SUMMARY AND CONCLUSIONS

- Pixel data taking over LHC Run2 was particularly challenging due to peak luminosity and pile-up record beyond the designed value.
- Off detector electronics were upgraded during Run2:
  - Improvement of desynchronization and dead time.
- Single Event Effects cause memory corruption in the FEI-4 global and single pixel register latches:
  - Periodic reconfiguration of the global FE-I4 registers developed in 2017, single pixel reconfiguration to be deployed in Run3.
- Radiation damage effects are visible in the Pixel detector:
  - Damages on the sensor bulk requires regular increase of the bias voltage and revisit the threshold parameters in the different layers.
- Currently preparing for Run3:
  - Opto-board replacement.
  - DAQ software improvements.
  - Study of the operational parameters towards Run3.

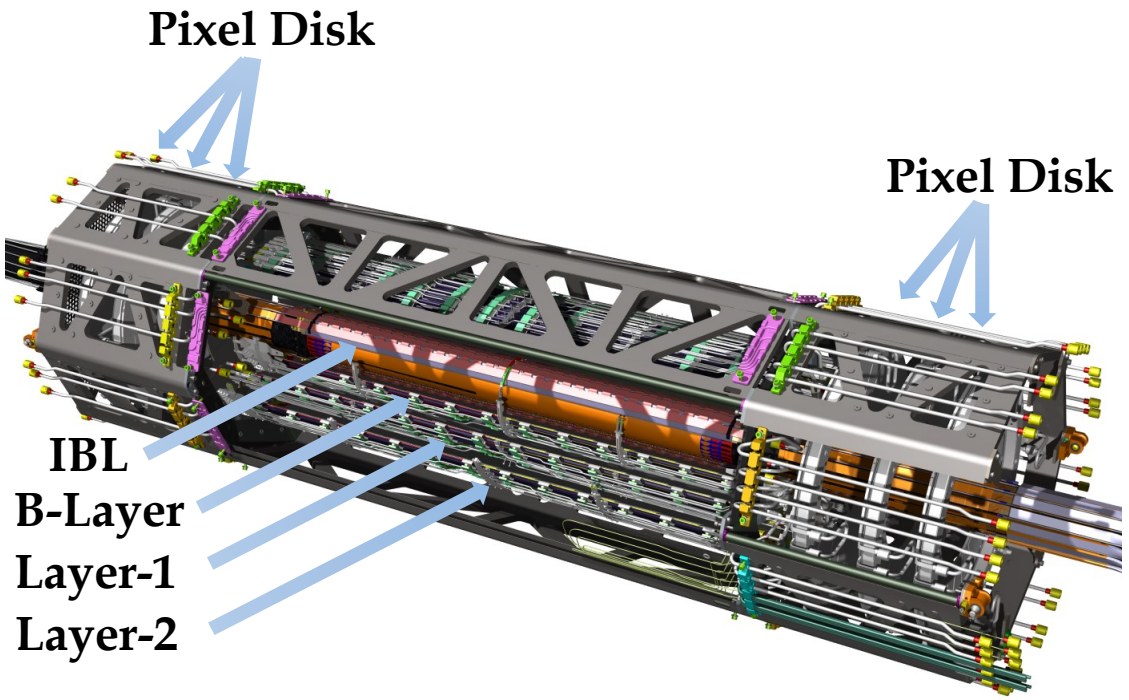

Thank You

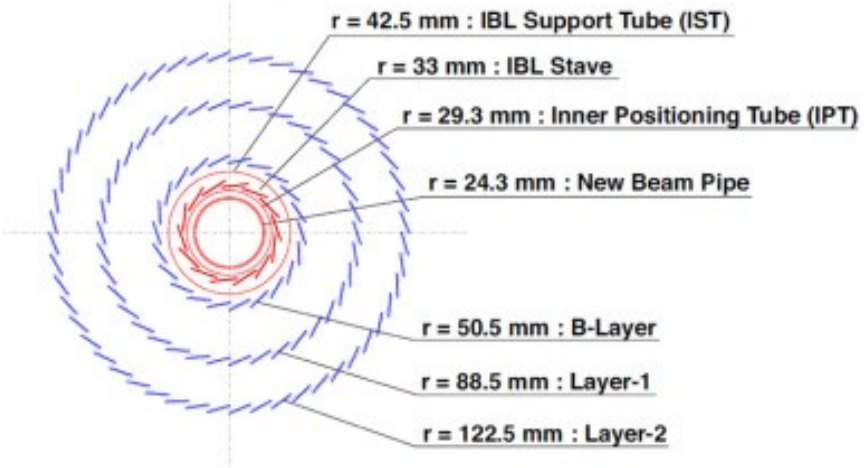
BACKUP

The ATLAS Pixel Detector is situated in the innermost part of ATLAS.

Main features:

- Excellent spatial resolution for track and vertex reconstruction
- Radiation hardness matching LHC requirements
- 4 Barrel layers + 3x2 end caps Disk

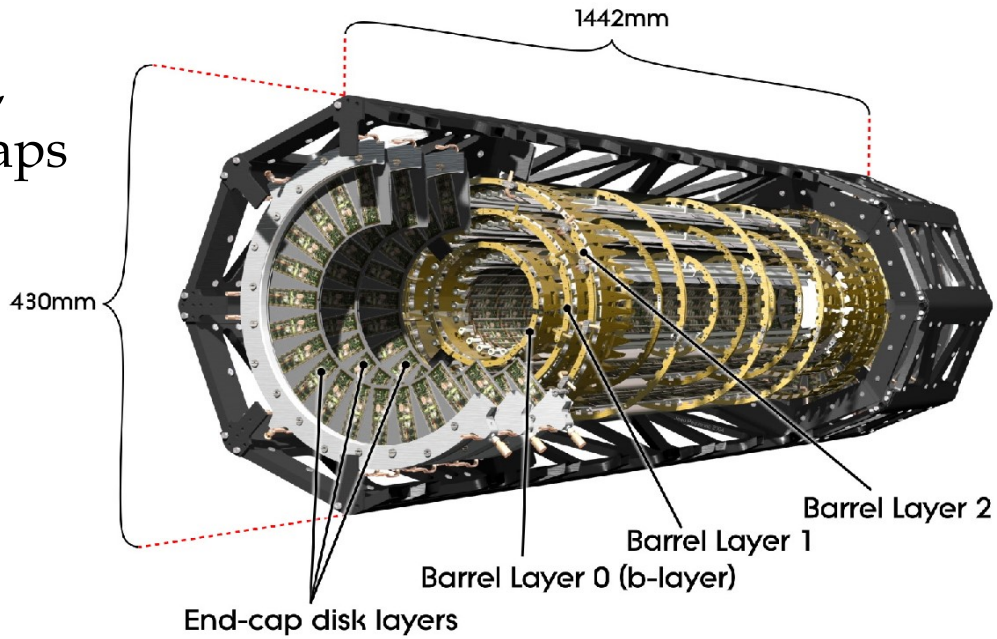




BACKUP

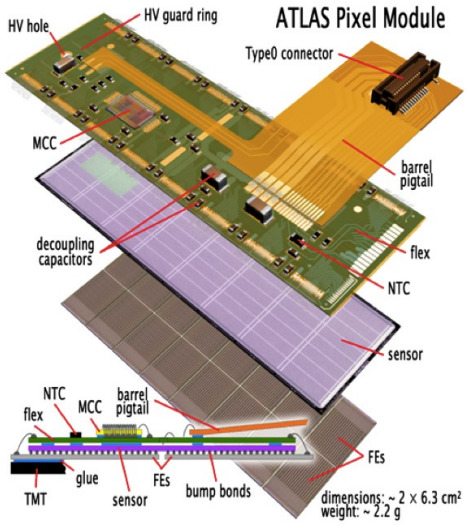
Pixel:

- 3 cylindrical layers (B-Layer, Layer1, Layer2) and 2 end-caps (3 Disk layers each)
- 80M of electronic channels ~95% operational



Front-end chip FE-I3

- Standard 0.25 µm CMOS
- 2880 (18x160) channels
- Analog: amplification and programmable threshold discriminator
- Digital: pixel address, time info, ToT (Time over Threshold)
- Radiation hardness 50Mrad



Sensor:

- n+-on-n; 250 µm tick
- 328 columns (50 µm r-Φ pitch)
- 144 rows (400 µm η pitch)

BACKUP

Insertable B-Layer (IBL):

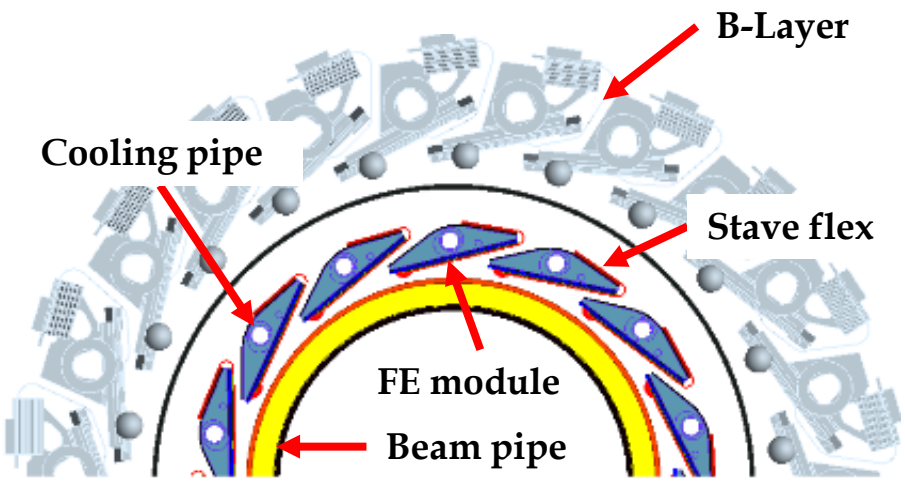
- New innermost layer
- Installed and commissioned during LS1 in 2014
- 14 staves at r = 3.27 cm
- Two sensor technologies:
  - Planar (central region)
  - 3D (high- η)
- 12M channels
  → ~99.3% operational

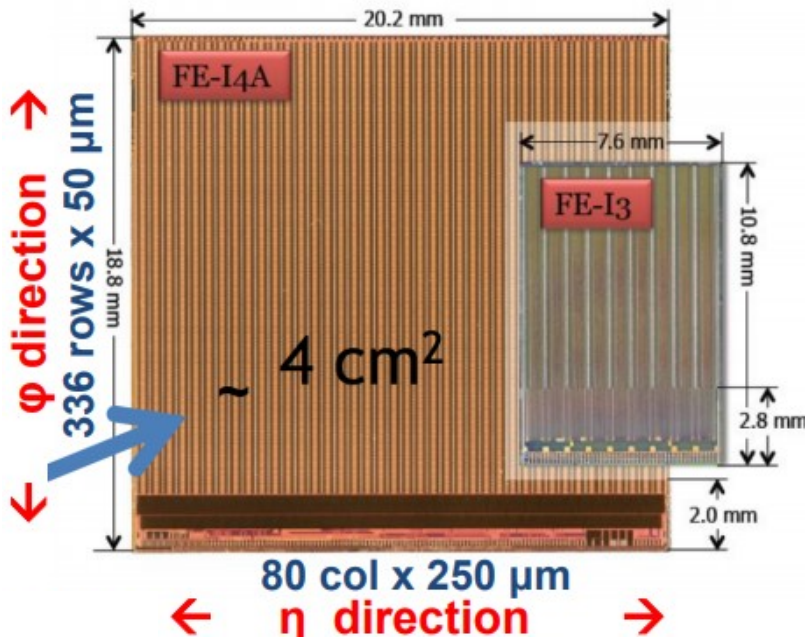
Front-end chip FE-I4

- 0.13 µm CMOS
- 26880 (80x336) channels
- Radiation hardness 250 Mrad

Sensors:

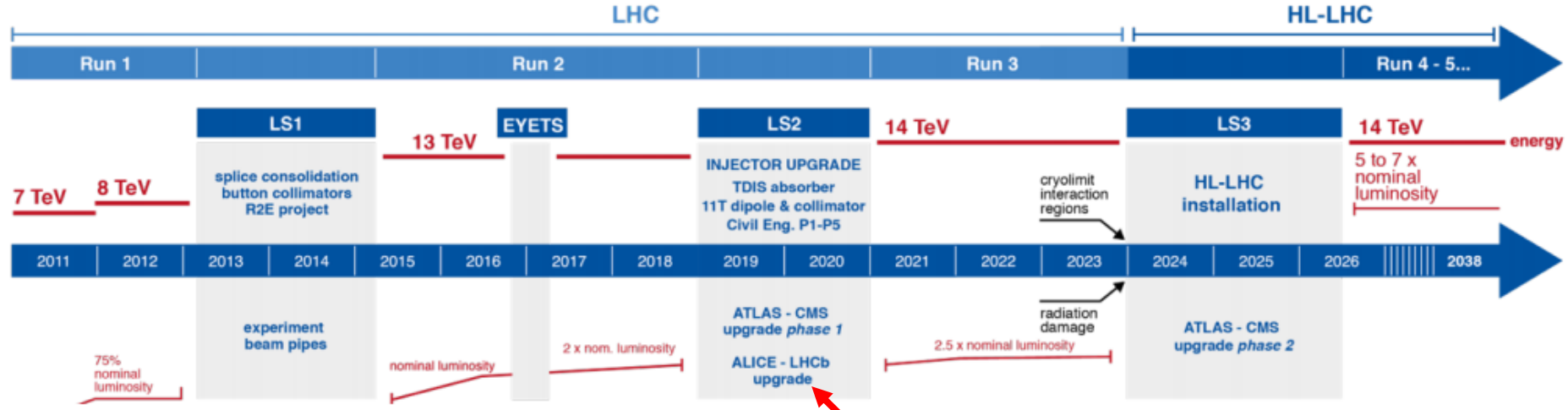
- Planar: 200 µm n+-in-n
- 3D: 230 µm n+-in-p

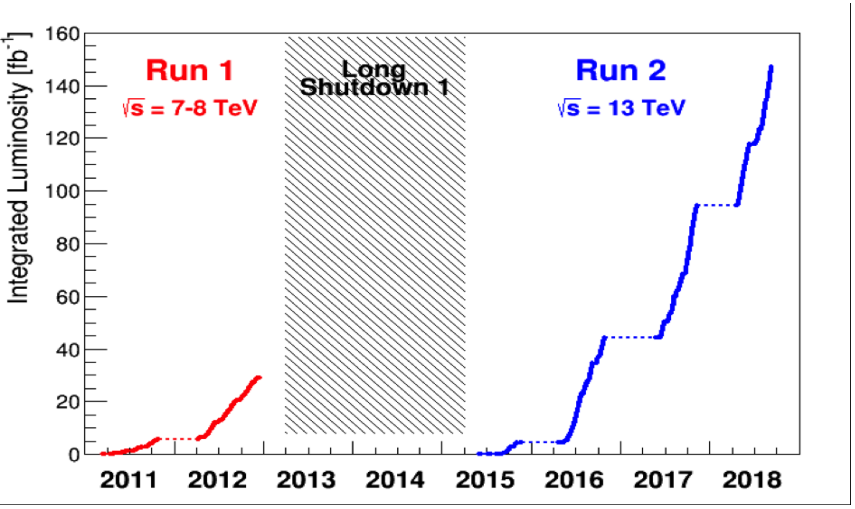




BACKUP

LHC roadmap:





We are here

BACKUP

Excellent Run2 data taking with 99.5% of data quality efficiency.

ATLAS pp Run-2: July 2015 – October 2018

Inner Tracker			Calorimeters		Muon Spectrometer				Magnets	
Pixel	SCT	TRT	LAr	Tile	MDT	RPC	CSC	TGC	Solenoid	Toroid
99.5	99.9	99.7	99.6	99.7	99.8	99.6	100	100	99.8	98.8

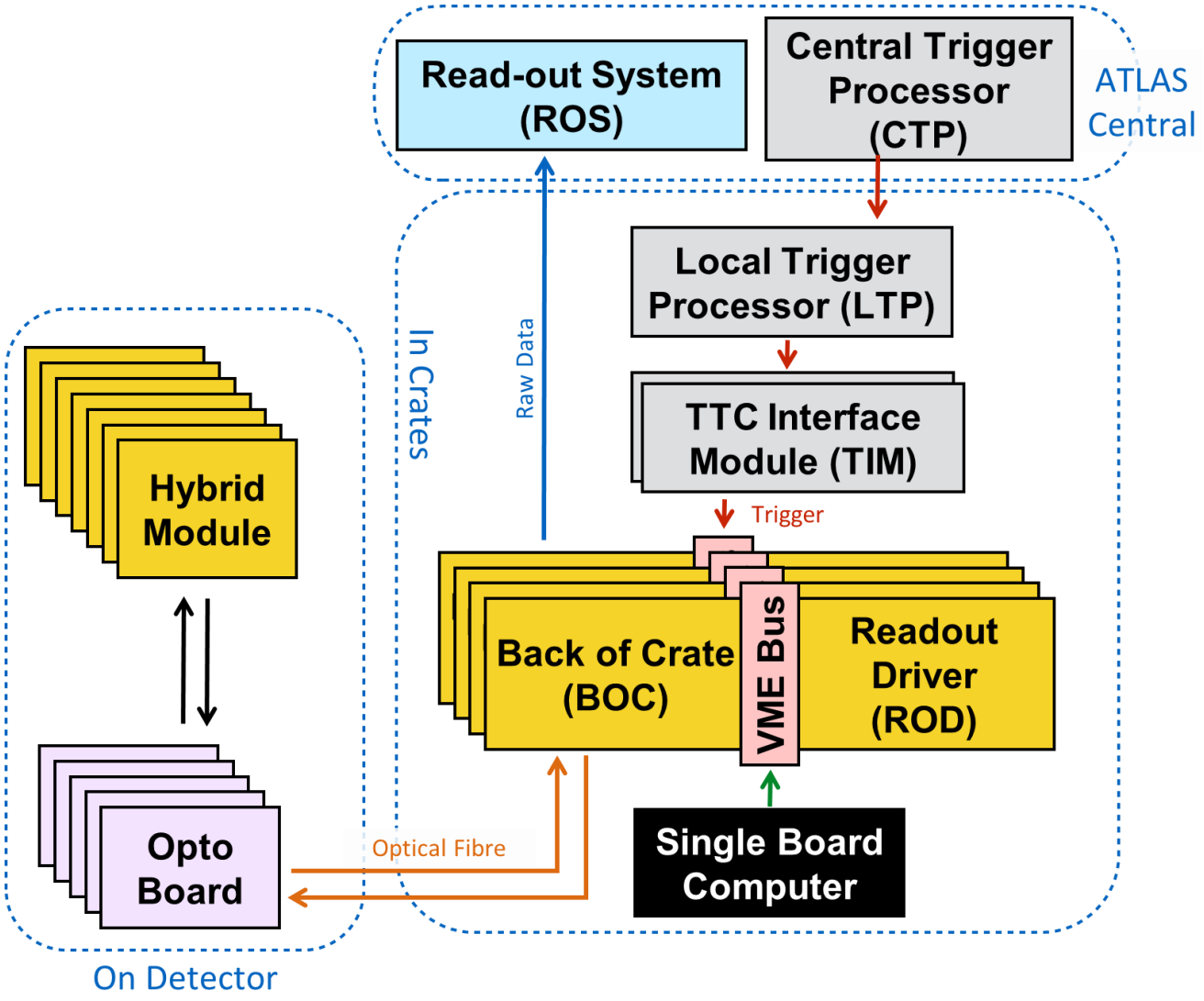
Good for physics: 95.6% (139 fb^{-1})

Luminosity weighted relative detector uptime and good data quality efficiencies (in %) during stable beam in pp collision physics runs with 25 ns bunch-spacing at $\sqrt{s}$=13 TeV for the full Run-2 period (between July 2015 – October 2018), corresponding to a delivered integrated luminosity of 153 fb^{-1} and a recorded integrated luminosity of 146 fb^{-1}. Runs with specialized physics goals are not included. Dedicated luminosity calibration activities during LHC fills used 0.6% of recorded data in 2018 and are included in the inefficiency. Trigger-specific data quality problems (0.4% inefficiency at Level-1) are included in the overall inefficiency. When the stable beam flag is raised, the tracking detectors undergo a so-called "warm start", which includes a ramp of the high-voltage and turning on the pre-amplifiers for the Pixel system. The inefficiency due to this, as well as the DAQ inefficiency, are not included in the table above, but accounted for in the ATLAS data taking efficiency.

BACKUP

Pixel/IBL Readout system:

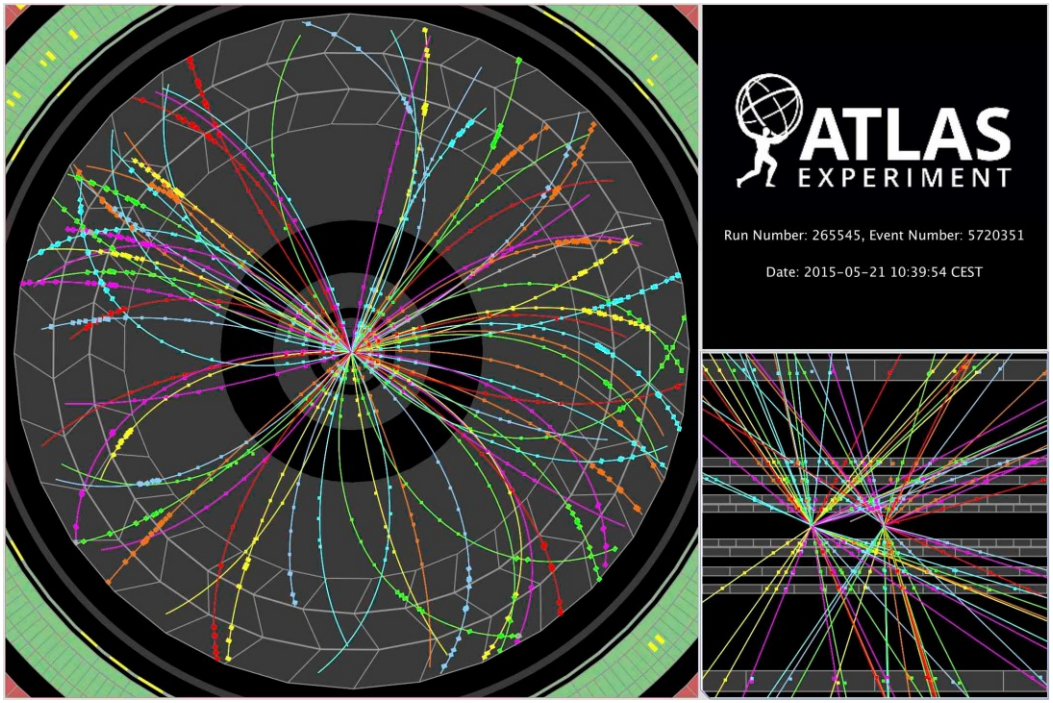
- Off-detector (In Crates): The readout back-end electronic chain consists of: ROD, BOC and TTC interfacing to ATLAS TDAQ while optical transceivers are interfacing to the on-detector part.

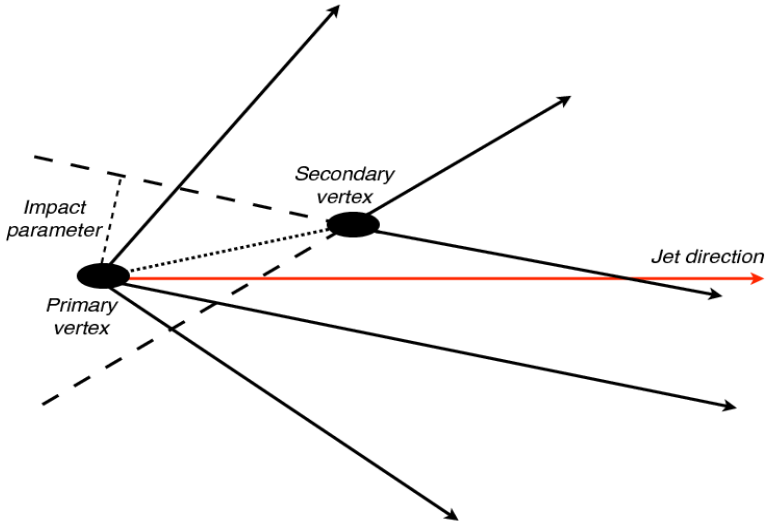


BACKUP

Pixel and IBL are fundamental for particle reconstruction:

- Accurate reconstruction of tracks (charged particle trajectories)
- Determination of the position of primary and secondary interaction vertices.
- Track impact parameters d_0 and z_0
- Flavour tagging
- Exotic tracking signatures
- Resolution of tracks inside jet cores. Tracking in dense environment (TIDE)



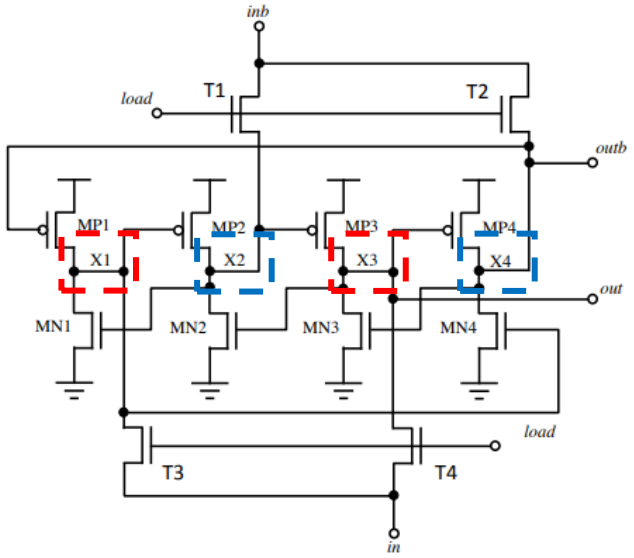


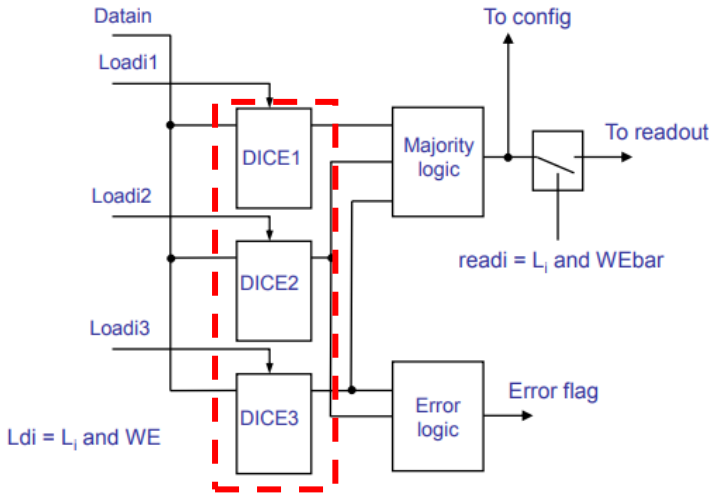
BACKUP

Single Event Effects (SEE) can cause memory corruption in the global and single pixel registers. This effect is seen in IBL (FE-I4 chip).

Radiation hard design:

- FE-I4 configuration (global and single pixel) is stored in Dual Interlocked CElls (DICE) latches.
- FE-I4 global configuration has triple redundancy logic (not possible at single pixel register level due to space constraints in the FE chip).





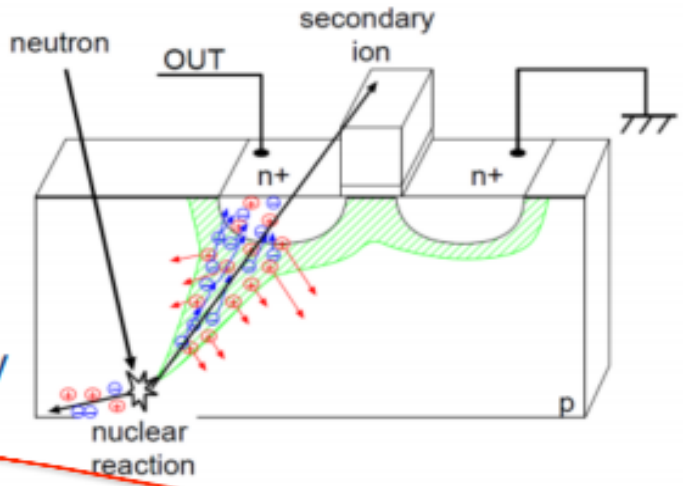
BACKUP

Single Event Effects: Single Event Transients and Single Event Upsets:

Single Event Upset (SEU)

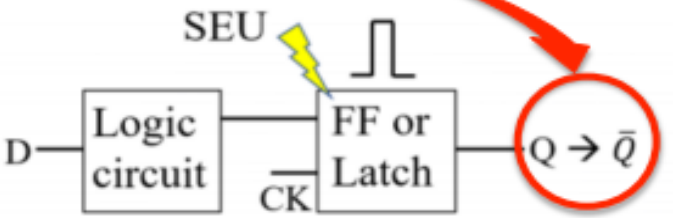
- Circuit with two stable states, 0 or 1 (latch), used to store each configuration bit.
- A relevant amount of charge into a latch **can flip its logic state.**
- In case of highly ionizing recoil nuclei and showers from nuclear interactions of the MIPs in the proximity of the memory cells:

➔ **memory corruption.**



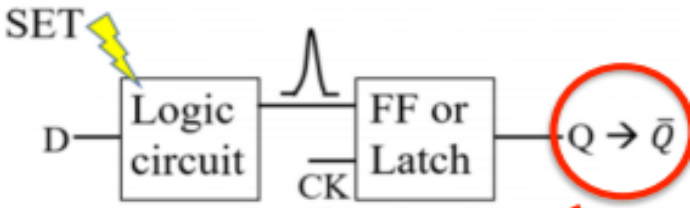
Single Event Transient (SET)

- Transient pulse caused by single event effect (SEE) that propagates in a combinatorial circuit path and eventually be latche in a storage cell.



- Glitch on the "LOAD" line of Shift Register (SR):

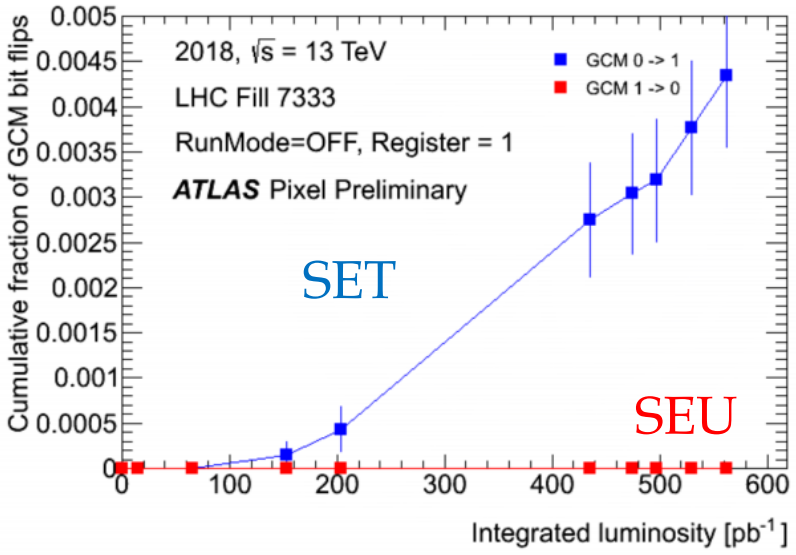
➔ **memory corruption.**



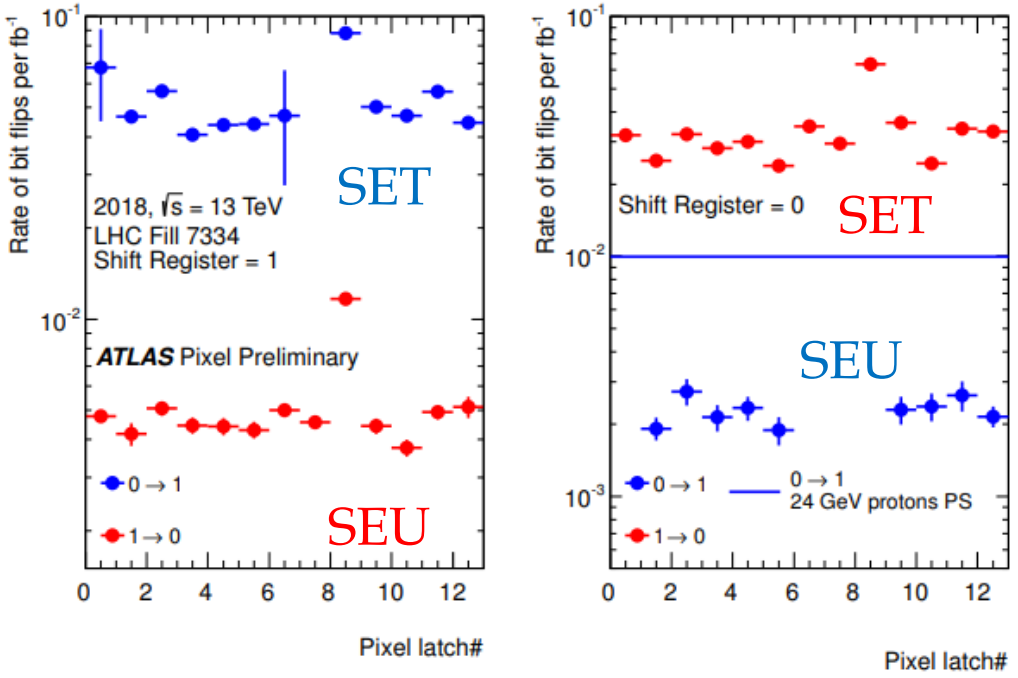
BACKUP

Measurements on SEE by reading back FE-I4 registers:

Global registers



Single Pixel registers



Different measurements while loading shift registers (LOAD line) to 0 and to 1 for single pixel registers → measument of bit-flips using register readback.

SET:

SR=1 : 0 → 1

SR=0 : 1 → 0

SEU:

SR=1 : 1 → 0

SR=0 : 0 → 1

Rate of bit-flips dominated by SET!

BACKUP

Corrective actions on SEE:

L1A Trigger (Level 1 trigger Accept)

ECR Error Counter Reset

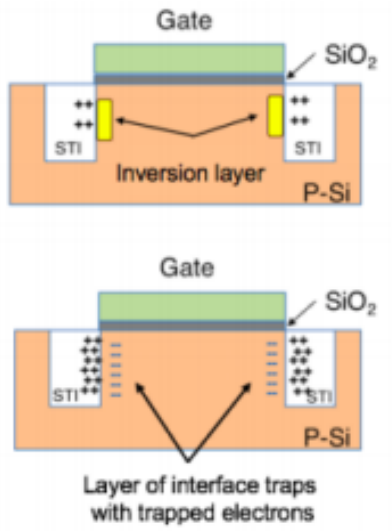
BCR Bunch Crossing Reset

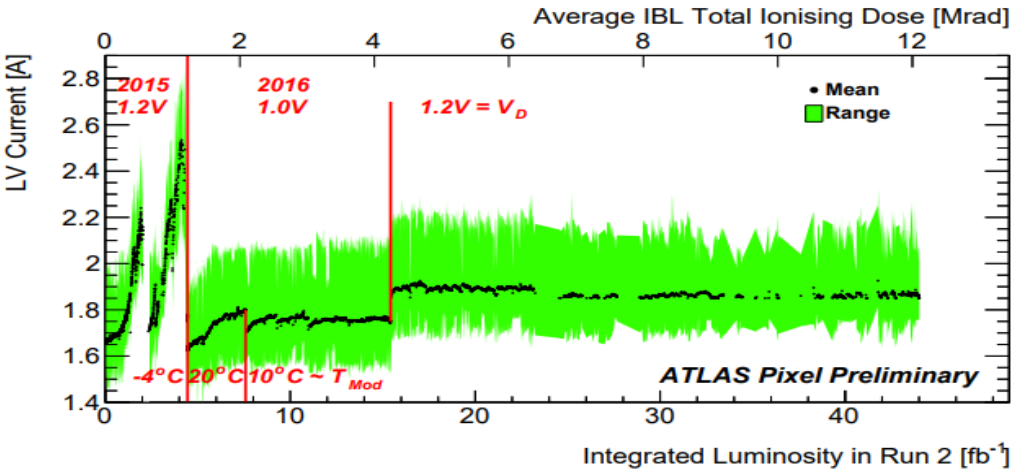
- Periodic reconfiguration of FE registers.
- No dead time induced in data taking, performed at the ECR (1 ms gap withouth triggers)
- Global register configuration (32x16 bits) send every 5 s.
- Pixel register configuration send partially every ~5 s (3 out of 13 latches and 1 double column out of 40). Full FE reconfiguration performed every ~11 min. Not yet deployed, but tested during 2018 → Improvement on the noise level and fraction of "quiet" Pixels seen.

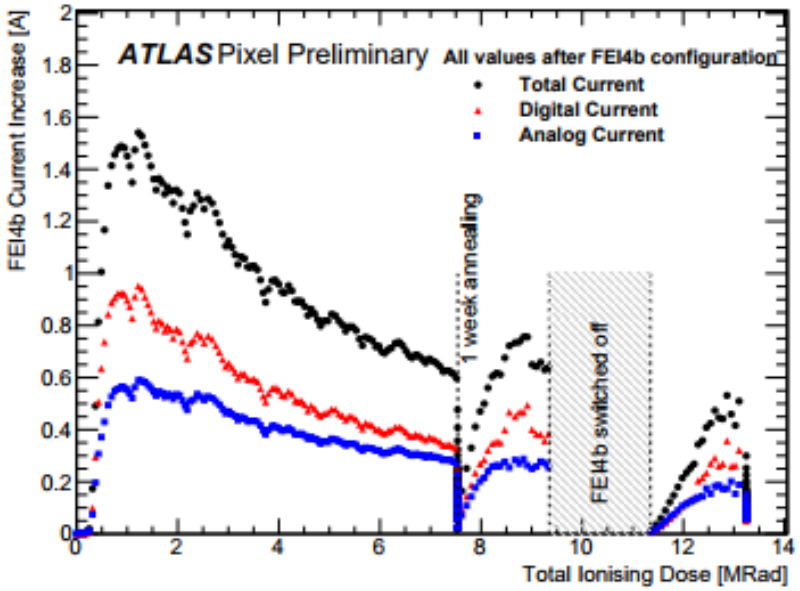
BACKUP

IBL LV current increase due to radiation damage:

- **Trapped positive charge**: in the bulk of the Shallow-Trench-Isolation (STI) oxide gives origin to the source-drain leakage current → function of TID with peak at $\sim 2-3$ Mrad.
- **Interface traps**: filled with electrons in the NMOS structures → compensates the trapped holes → decrease of leakage current
- **Dose and temperature dependence** and annealing of trapped positive charges at low temperature during sensors OFF.

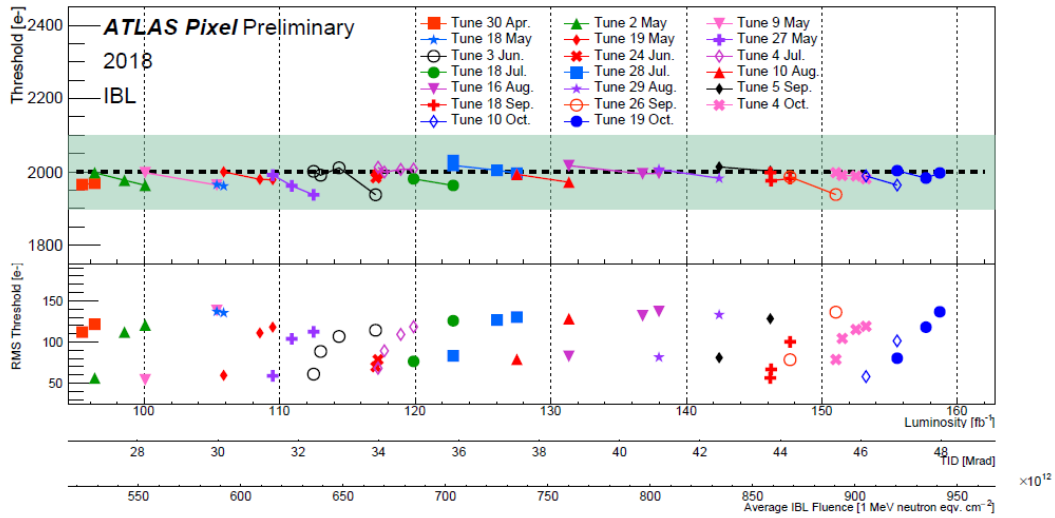


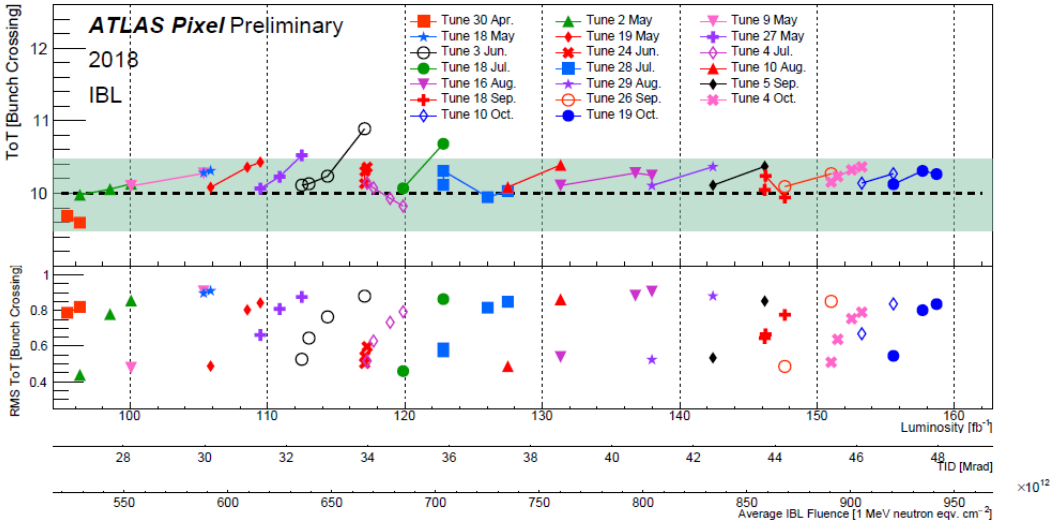




BACKUP

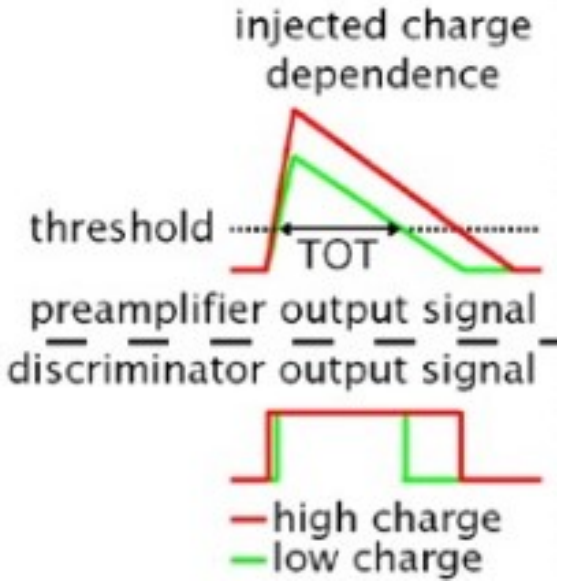
ToT and threshold drift due to radiation damage:





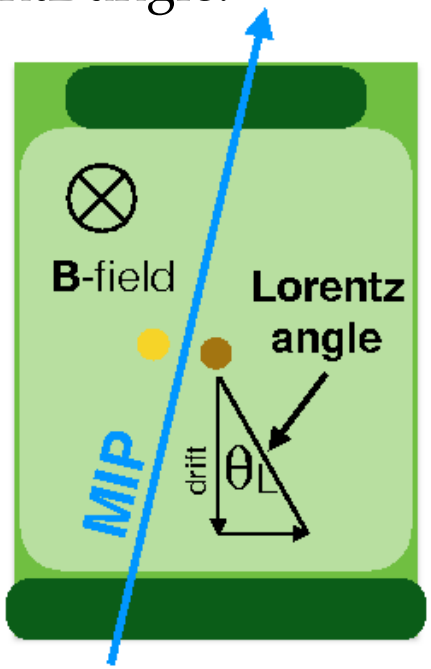
Threshold: analog cut on signal amplitude:

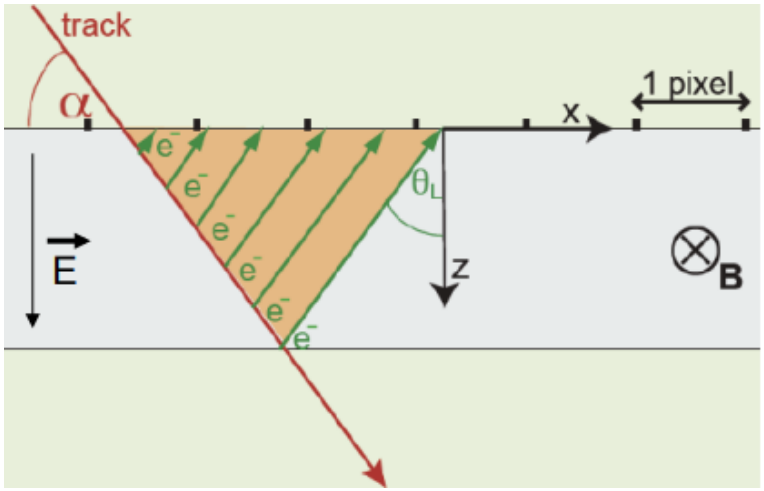
ToT: Time over threshold, measured in Bunch Crossing units (1 BC = 25 ns)



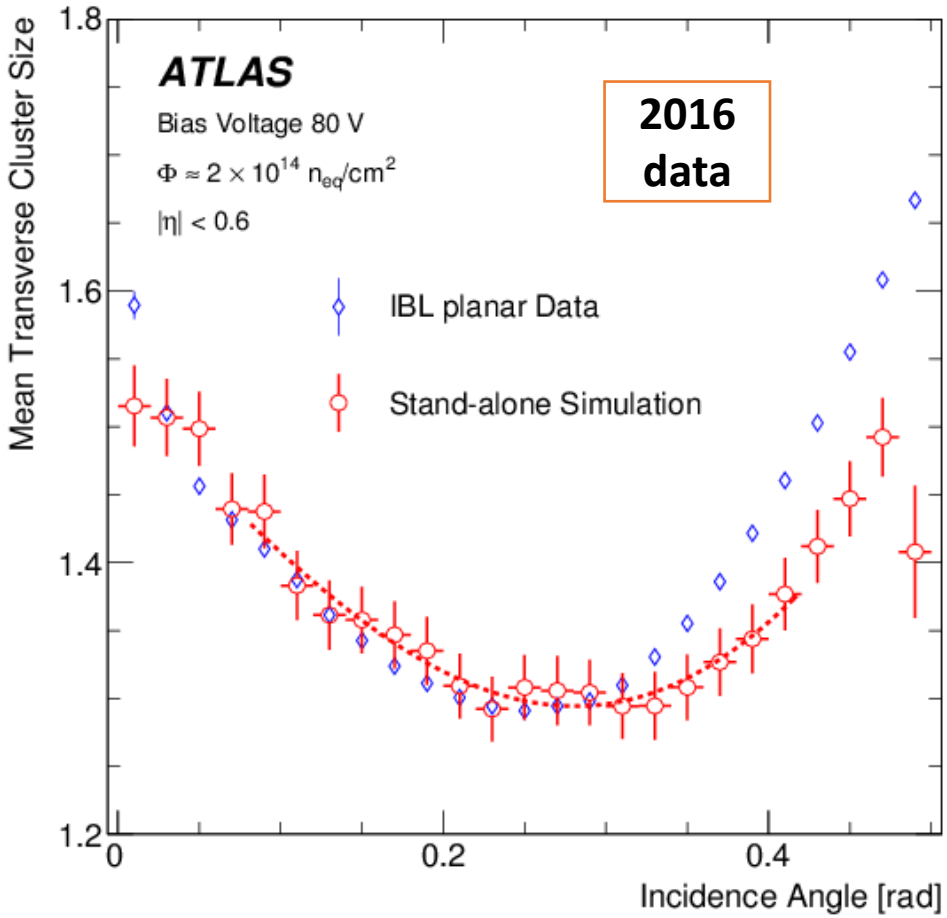
BACKUP

Lorentz angle:



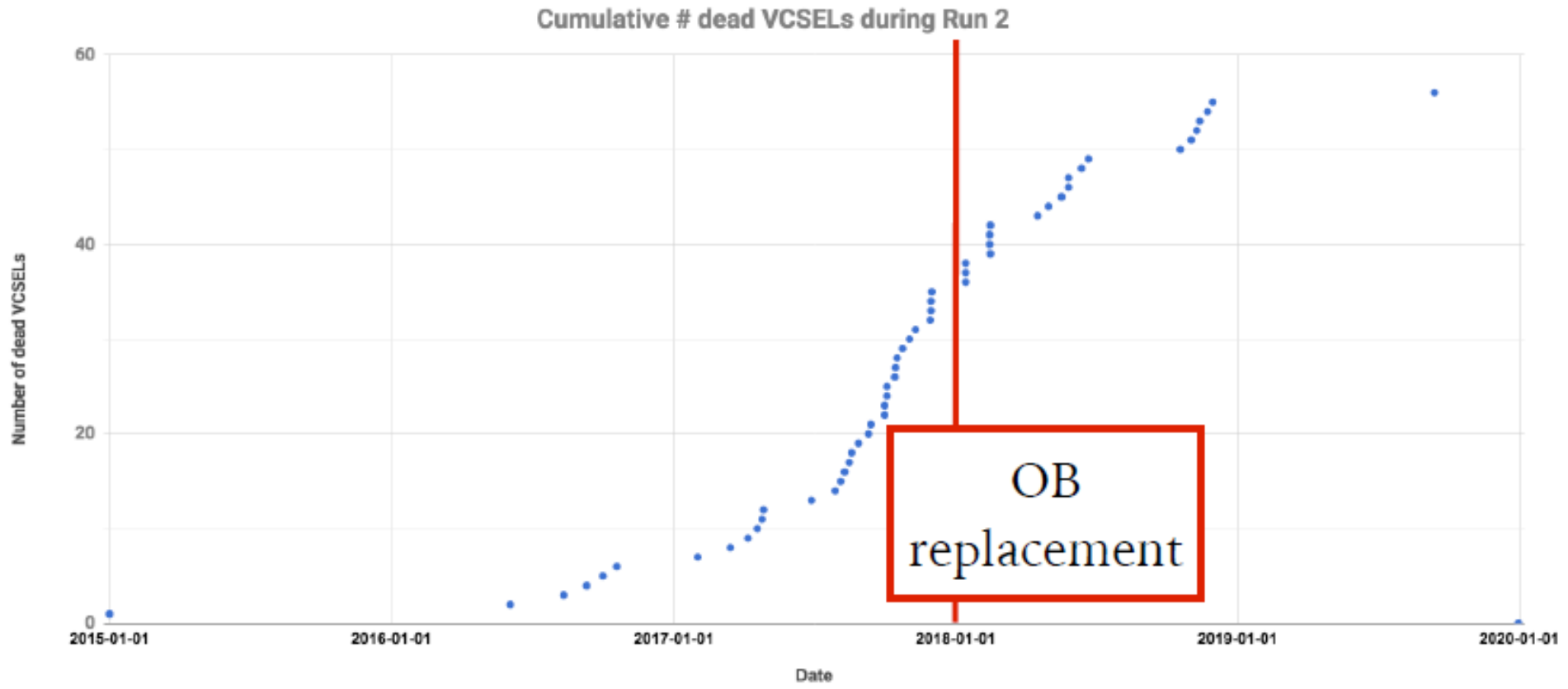


Mean transverse cluster size versus transverse incidence angle near the end of the 2016 run (about 2×10^{14} neq/cm2) with a bias voltage of 80 V

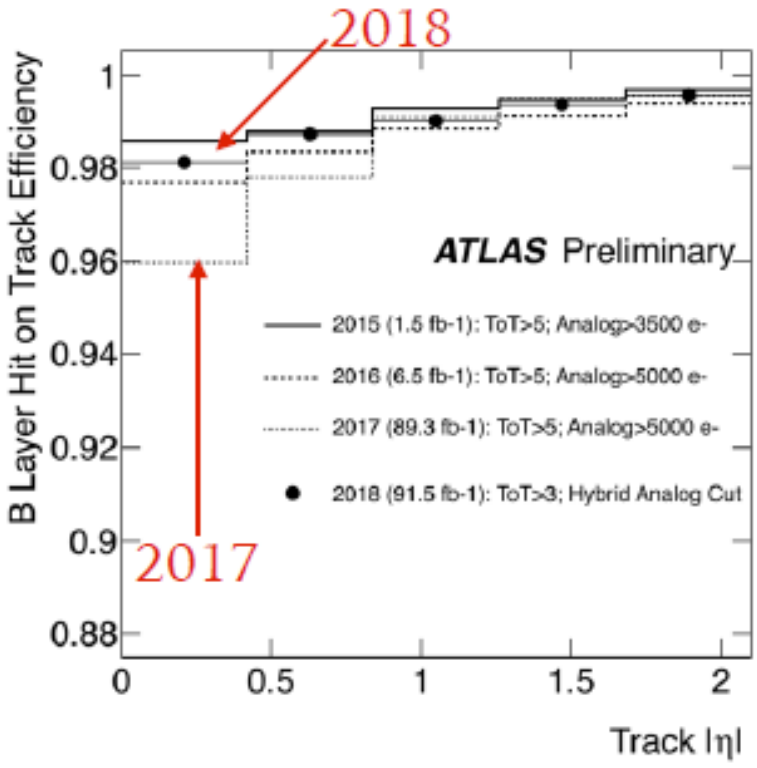


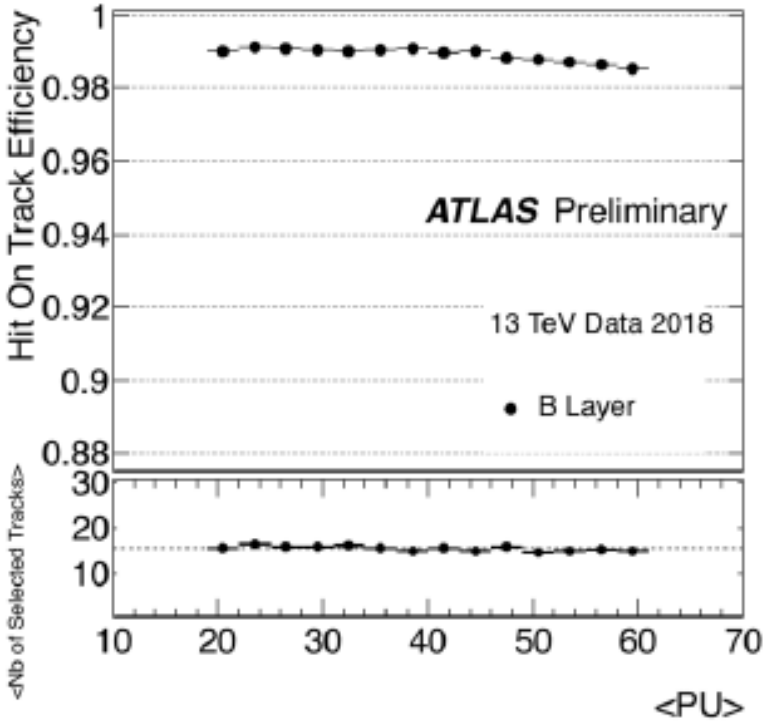
BACKUP

VCSEL failures evolution:



BACKUP





- B-Layer (2nd inner-most) has largest threshold due to bandwidth considerations
- More radiation damage than other Pixel layers -> efficiency decreases
- |η| dependent threshold adjustment; at low |η| largest dose -> largest beneficial adjustments
- Significant efficiency recovery after lowering thresholds
- Efficiency stable for high pile-up