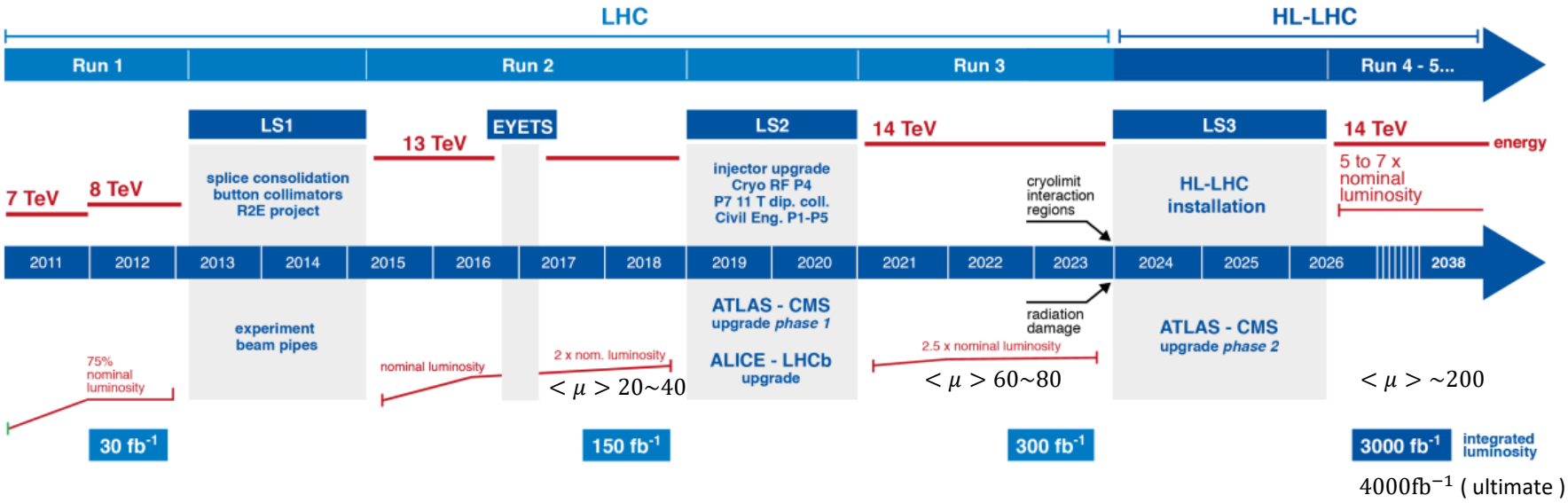
ATLAS Detector Upgrade

Peilian LIU（IHEP）

On behalf of the ATLAS Chinese Clusters

The 6th CLHCP workshop, 6 -9 Nov 2020, Zoom

Roadmap to High Luminosity LHC



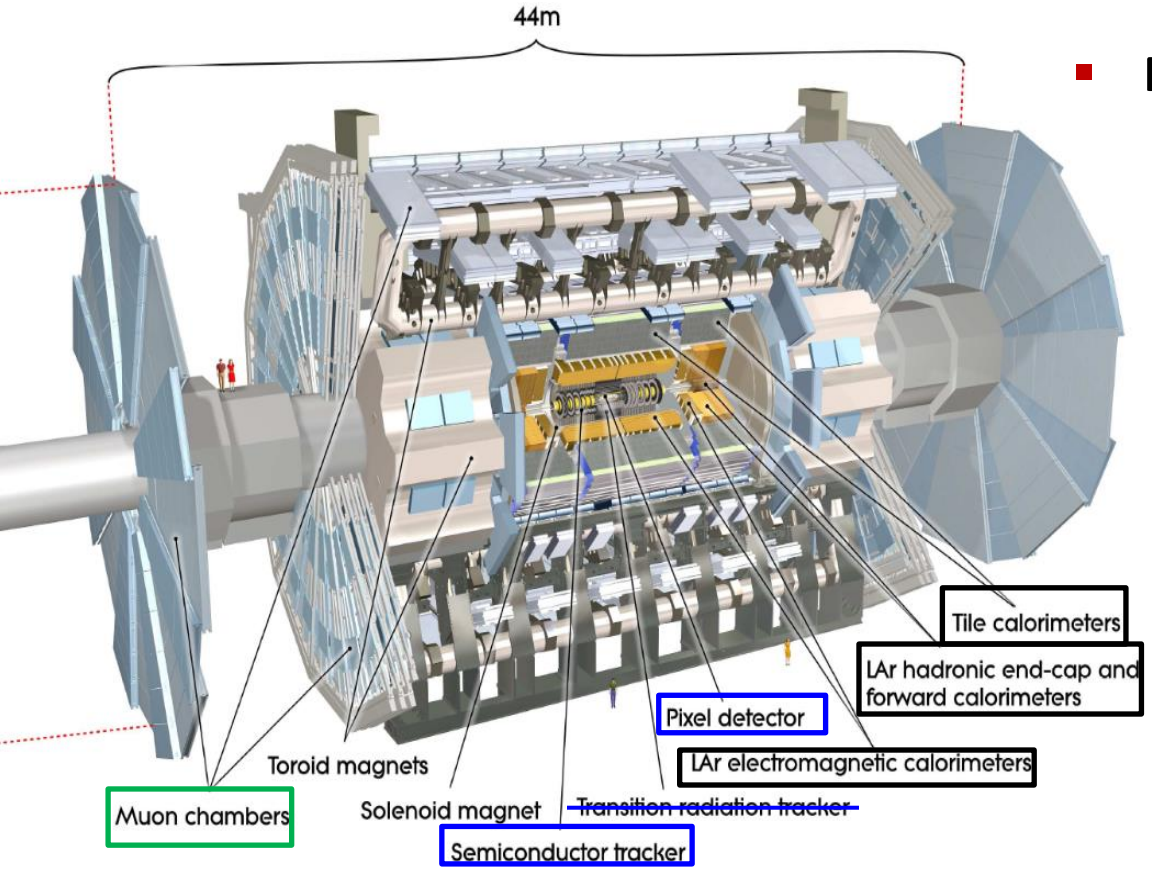
4000fb^{-1} (ultimate)

- The high-luminosity LHC (HL-LHC) is intended to provide $300\ \text{fb}^{-1}$ of data each year during an operating period of roughly 10 years.
  - An instantaneous luminosity of $\mathcal{L} \sim 7.5 \times 10^{34}\text{cm}^{-2}\text{s}^{-1}$
  - An average of 200 inelastic proton-proton interactions per bunch crossing (pile-up, $< \mu > = 200$)
- The ATLAS detector will be upgraded to cope with the increased occupancy and data rate.

The Upgrades of ATLAS Detector

- **Phase-I (happening)**

  New small wheels of Muon Spectrometer (the only upgrade)



- **Phase-II (foreseen in 2026)**

  All-silicon new Inner Tracker (ITk)

  New inner Muon barrel trigger chambers

  High-η muon tagger

  New High-Granularity Timing Detector

  Calorimeters (only TDAQ)

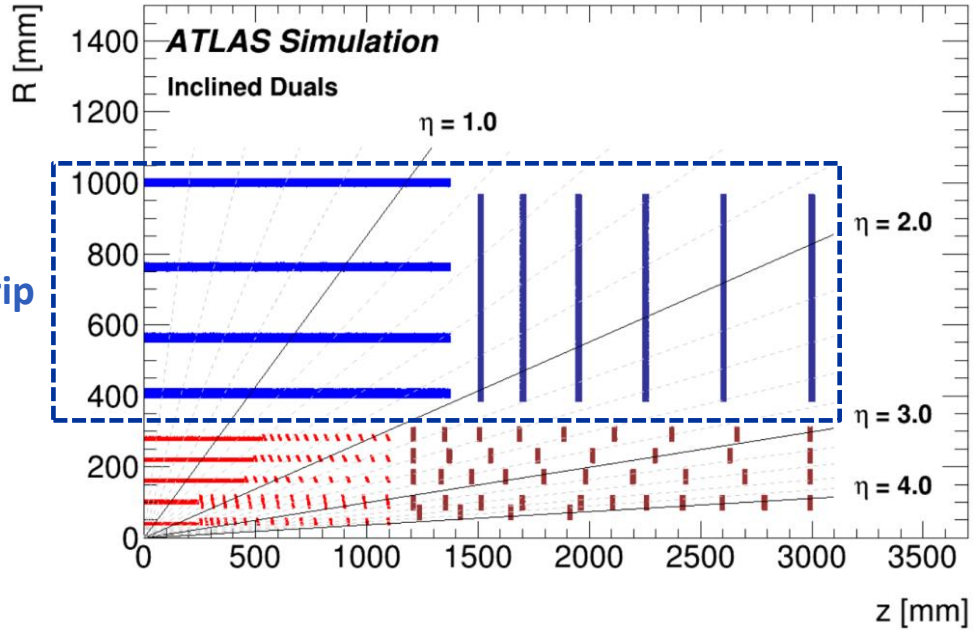
  New readout electronics for all systems

Upgrade projects the Chinese clusters are involved in

- **Inner Tracking Detector**
- **Muon Spectrometer**
- **High Granularity Timing Detector**

Inner Tracker

Inner Tracker Strip Detector



Strip

All-silicon Inner Tracker (ITk) with extended coverage ($|\eta| < 4$)to improve the tracking performance

IHEP and THU committed to deliver 1000 strip barrel modules (10m² of sensor surface)

- 10% of the total strip barrel modules (US 50% + UK 40%)
- Additional contributions to strip barrel system integration, installation and commissioning

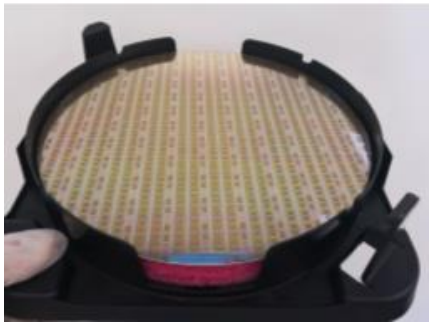
Objectives

- **Radiation hard frontend readout ASIC design**
- **High performance Strip detector module production**
- **Novel CMOS pixelated strip sensor characterization**

- In close collaboration with RAL and UK community

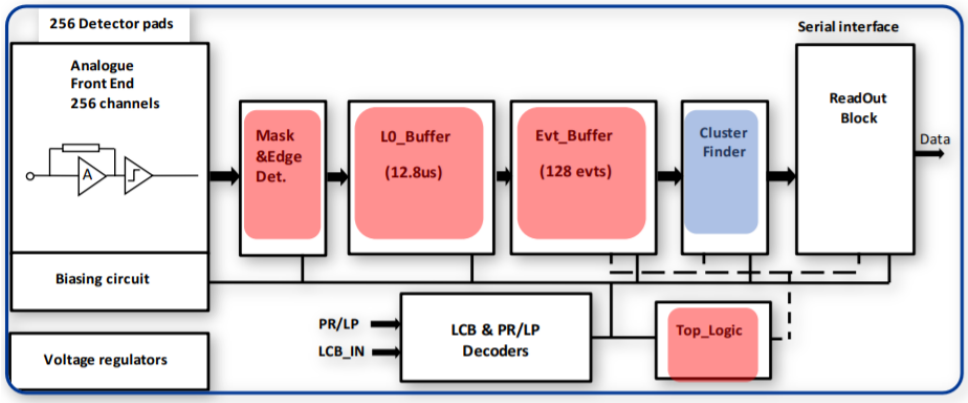
Radiation Hard FE ASICs

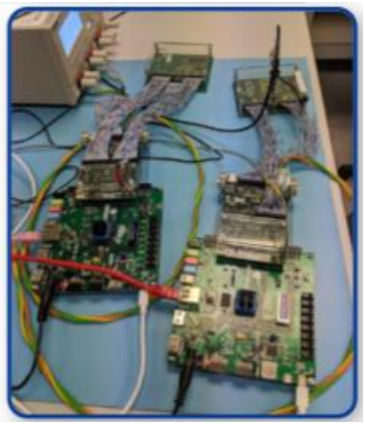
- ABC-STAR chips with readout architecture redesigned to cope with the increased trigger rate
- **Significant contributions to design & verification of digital blocks.**
- Prototype chips already tested and used for module assembly



IHP contributed to design and verification

IHP contributed to verification



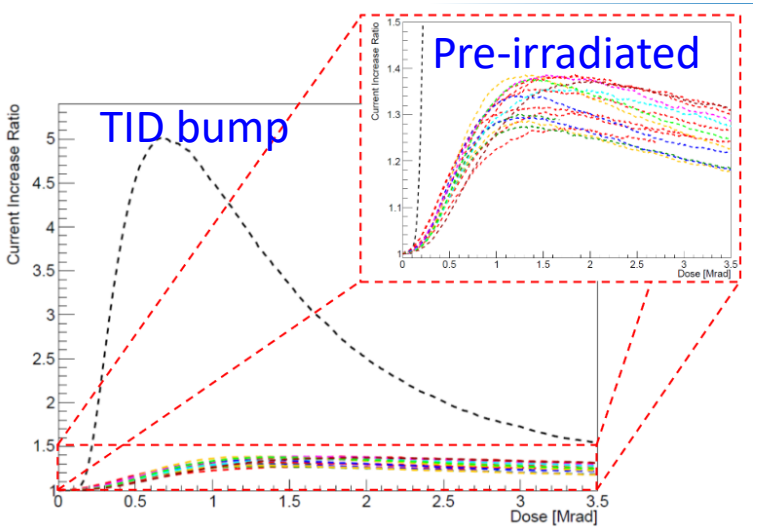


W. Lu et al, 2017 JINST 12 C04017

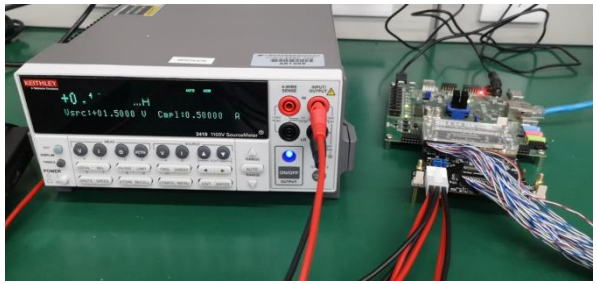
- Export license available for shipment of chips from CERN to IHEP

TID “Bump”

- **Higher current draw with radiation due to Total Ionizing Dose (TID)**
  - Undesired capacity redundancy on powering and cooling design
  - Cannot be easily eliminated by design
- **System level solution: chips pre-irradiated to pass the TID bump.**

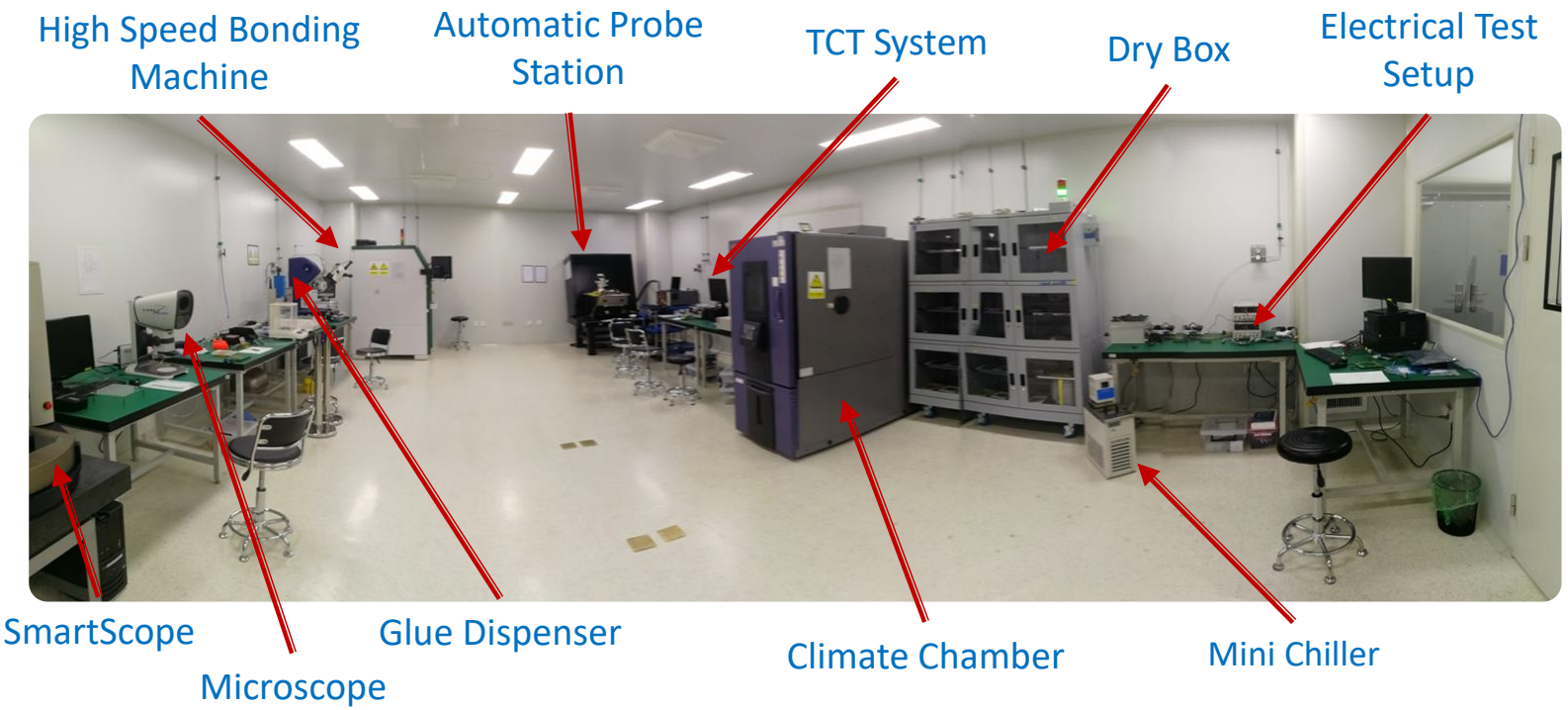


- Quality Assurance: at batch level, TID measurements of pre-irradiated chips with x-ray machine (setup at IHEP)



Infrastructure Readiness

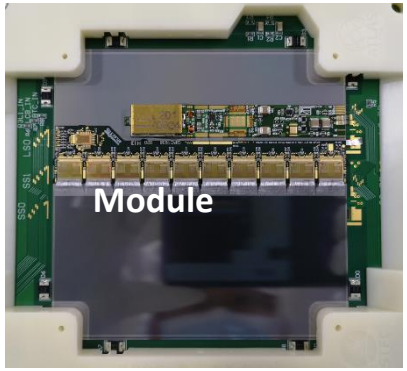
- Constructed ISO Class 7 clean room at IHEP dedicated for the ITk upgrade project



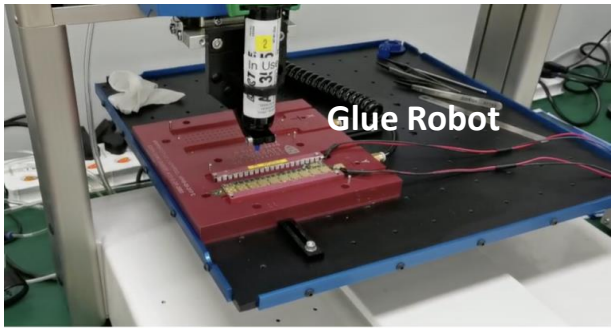
- Nearly all instruments required for module production in place

Module Prototyping

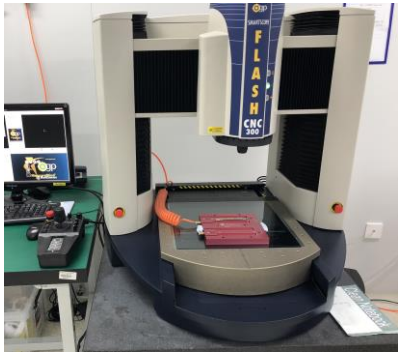
- Producing module prototypes exactly following the QC steps
  - Precision control at each step to deliver high quality modules: e.g. glue amount and thickness, wire strength → impacts on module performance (heat dissipation, mechanical support, wire bonding)

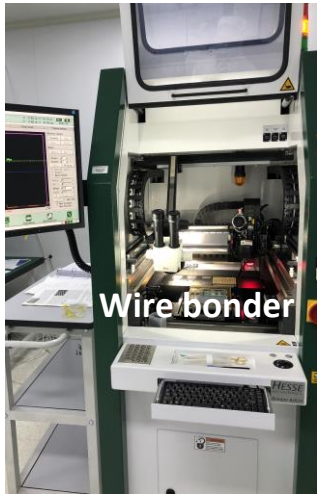


Calibration of glue amount

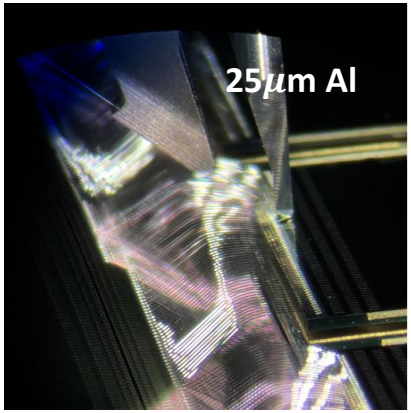


Metrology of glue thickness

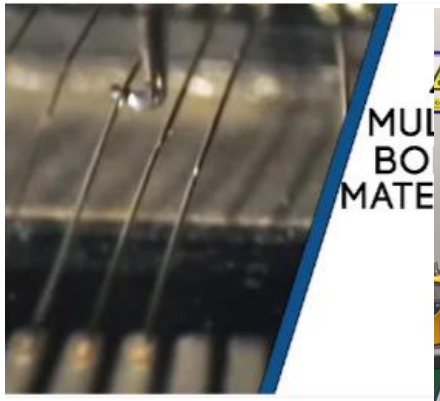




Wire bonding



Pull force test

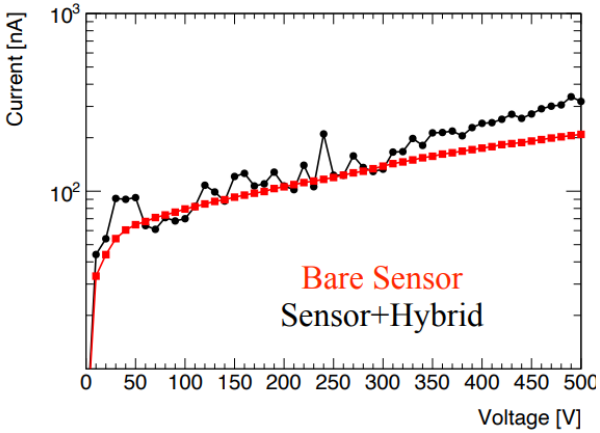


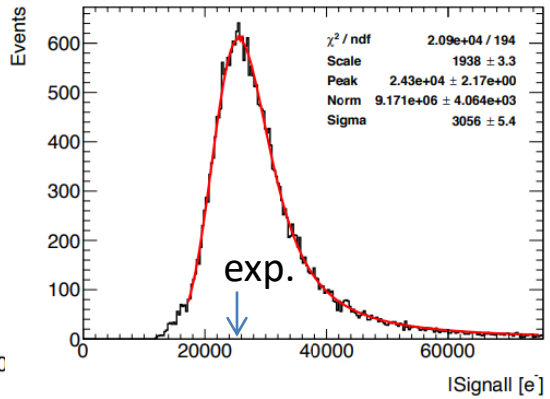
See Dengfeng Zhang's talk

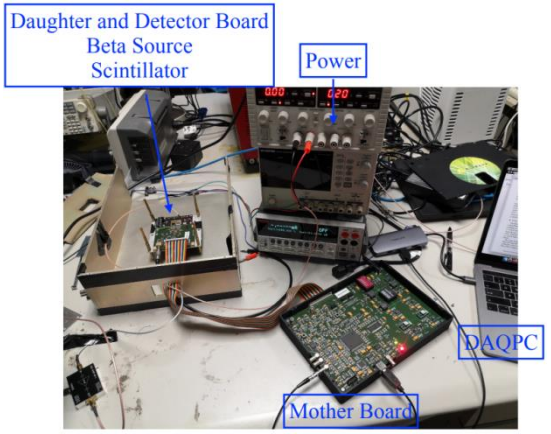
L. Poley et al 2020 JINST 15 P09004

Testing the Module

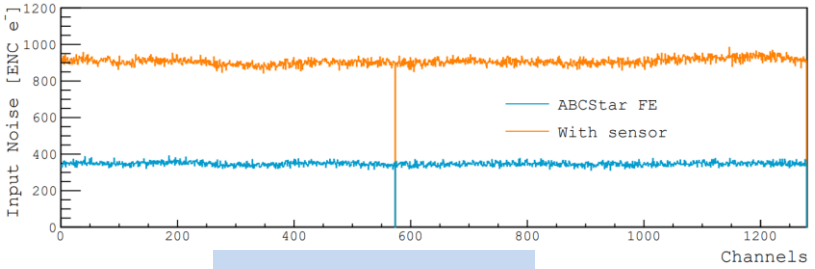
- Sensor
  - I-V characteristic of sensor before and after assembly
  - charge collection study of sensor prototype (mini sensor) using Sr90 with the ALiBaVa system

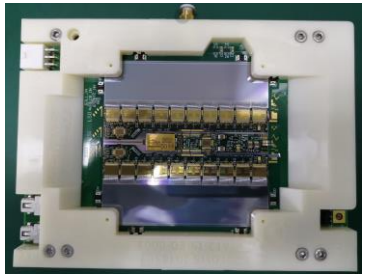






- Full electrical test of modules: measured gain, noise and noise occupancy → **fully functional**

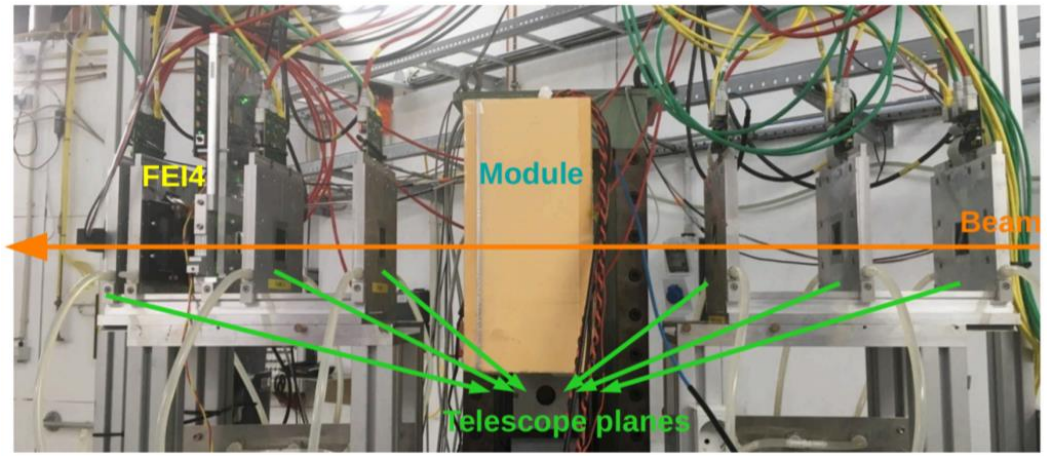


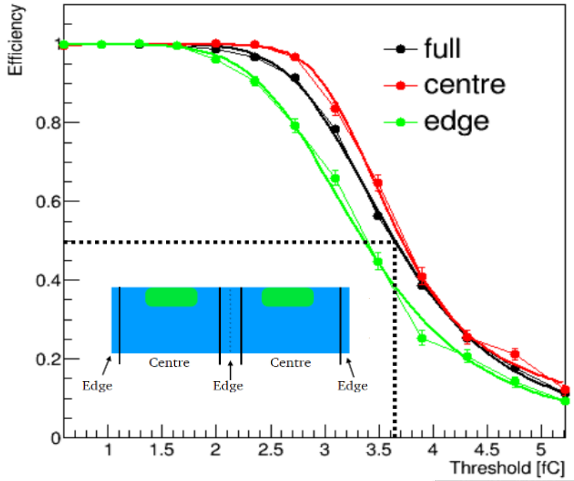


See Kai Liu's talk

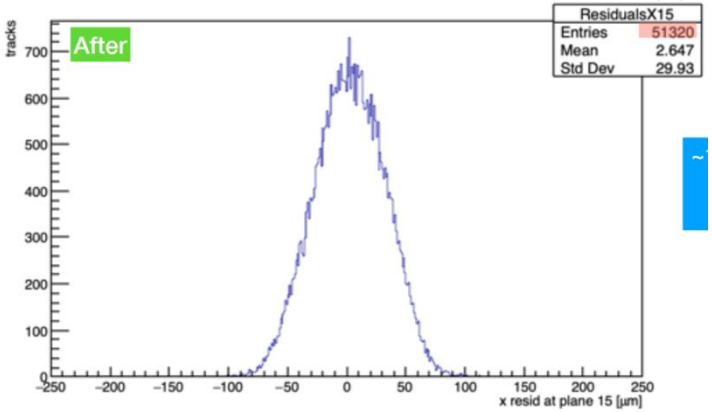
Testbeam Measurements

- **Decisive performance evaluation of prototype modules using DESY beam**
- **Significant contributions to beam test campaigns**
  - Test setup, data taking, data analysis and reconstruction software development





  - Data desynchronisation problem during analysis
    - Only 29.5% of events synchronised
  - The number of synchronised events is around 96.8% after the **desync correction**.

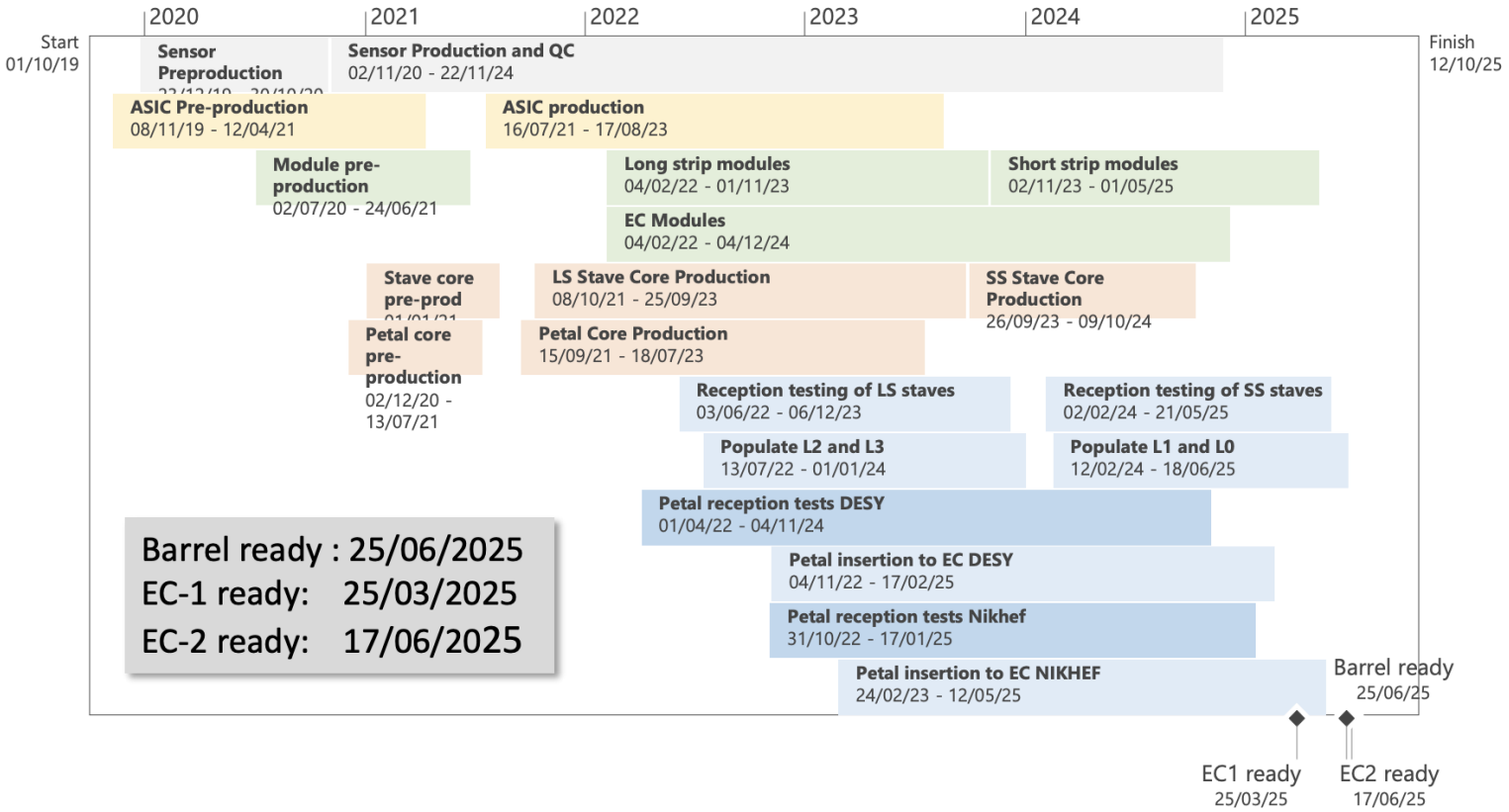


- Developing new software for future ITk strip beam test reconstruction and analysis

NIMA 924 (2019) 108-111
NIMA 979 (2020) 164430

See Emma Buchanan's talk

Site Qualification and Pre-production

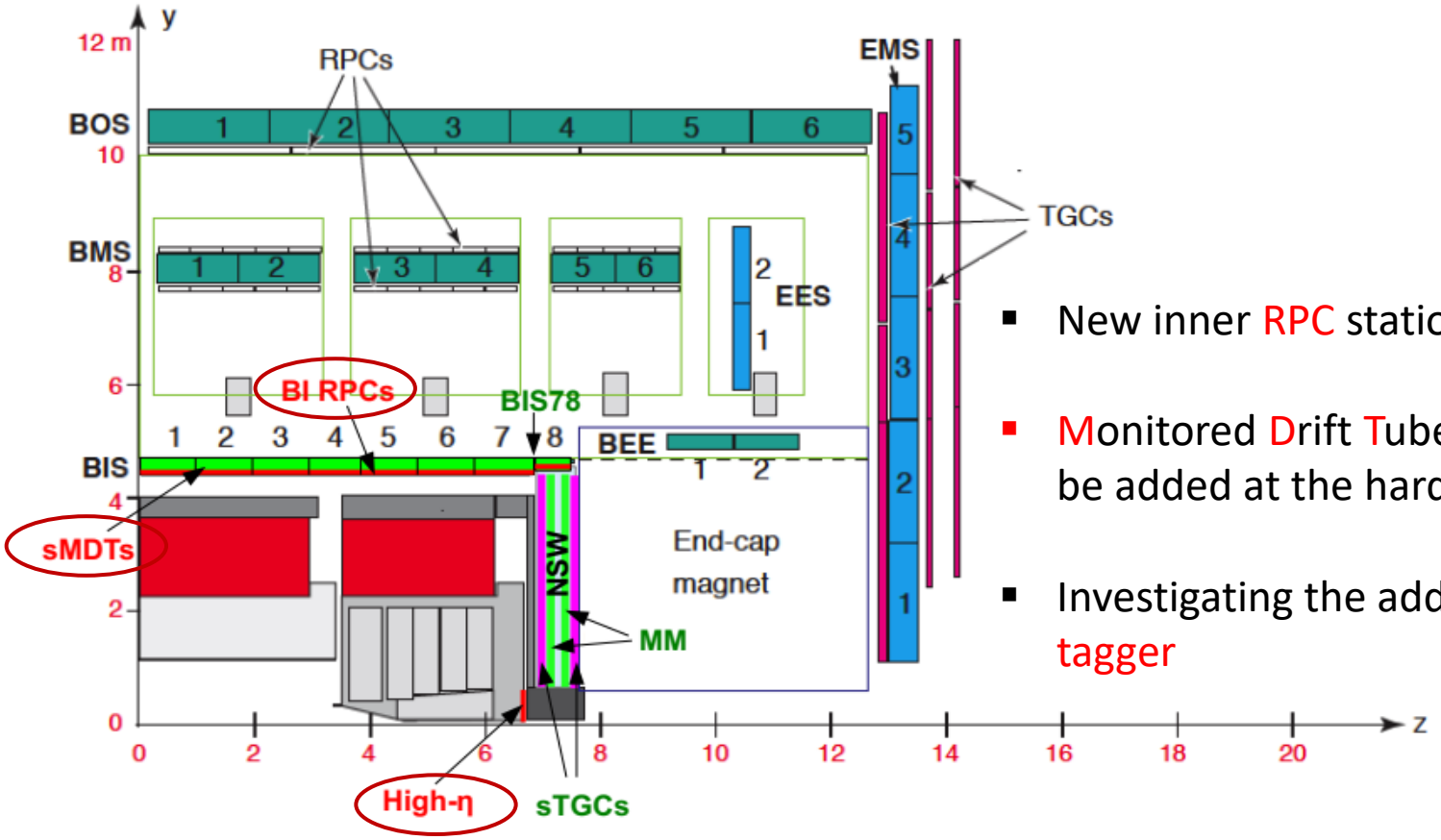


- Preparing for site qualification (postponed, likely by video)
- After being qualified, we will start the pre-production (5% of modules)

Muon Spectrometer

Muon Spectrometer

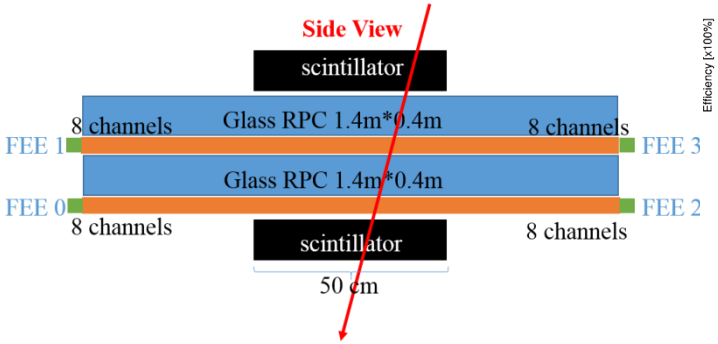
- **Phase-II** mainly about trigger

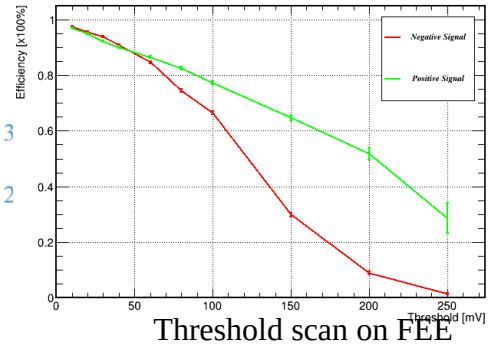


- New inner RPC stations
- Monitored Drift Tubes information to be added at the hardware trigger
- Investigating the addition of a high-η tagger

Test on Two-end Readout RPC

- **8-channels FEE with Amplifier & Discriminator developed at USTC**
  - Equipped on both ends of the honeycomb readout panel

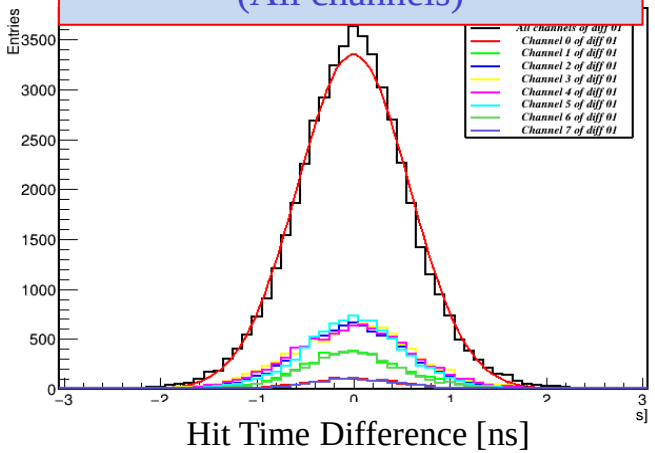




Threshold scan on FEE

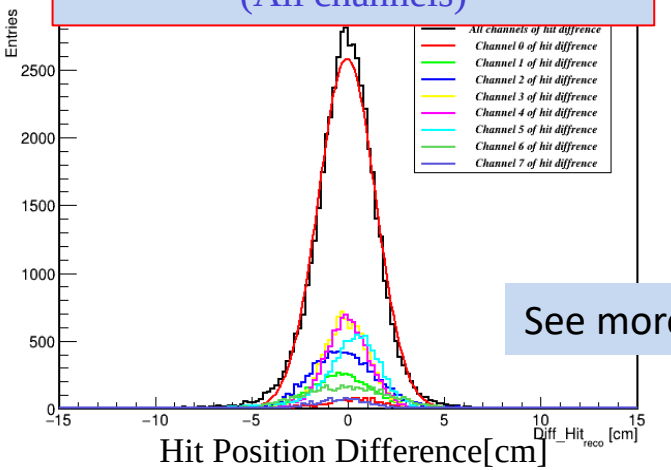
- **Two identical glass RPCs (1.4x0.4m) tested together with cosmic ray**

Time resolution: 411 ± 1.6 ps
(All channels)



Hit Time Difference [ns]

Spatial resolution: 1.05±0.004 cm
(All channels)

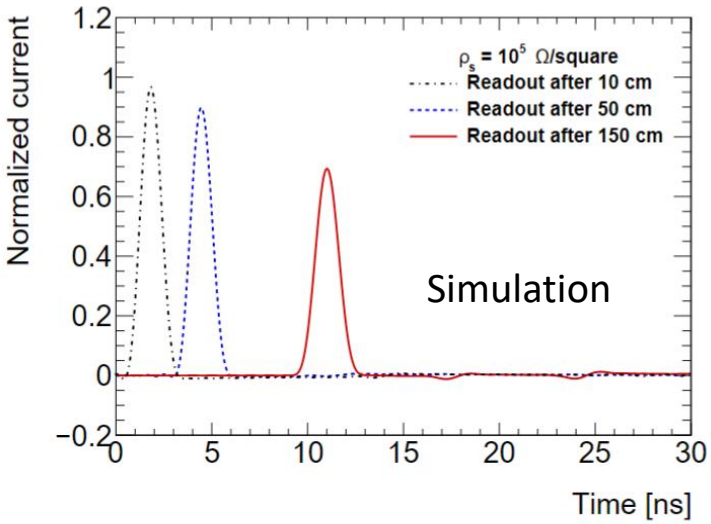


Hit Position Difference[cm]

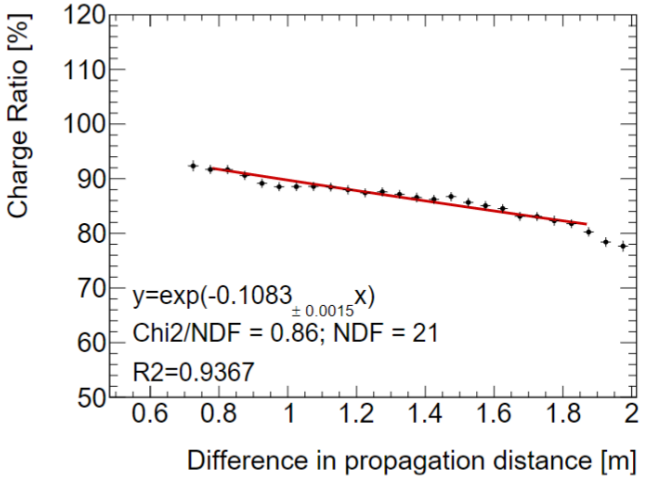
See more in Quanyin Li's talk

RPC Signal Attenuation Study

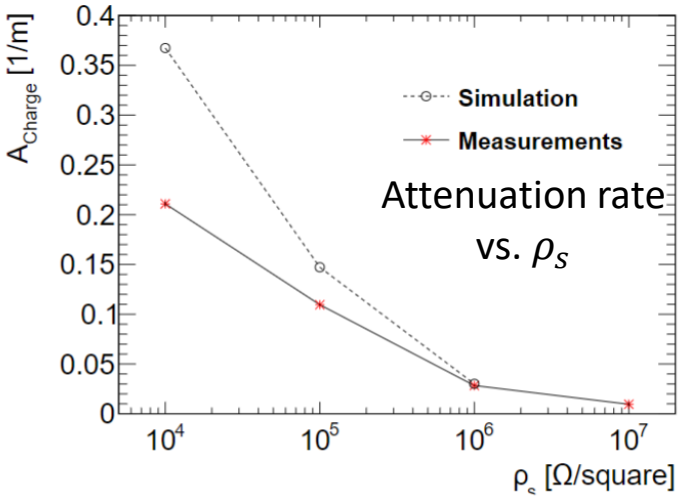
- Signal attenuation found in simulation



- Experimental setup to quantify the charge attenuation rate



- Lower graphite surface resistivity ρ_s leads to stronger attenuation

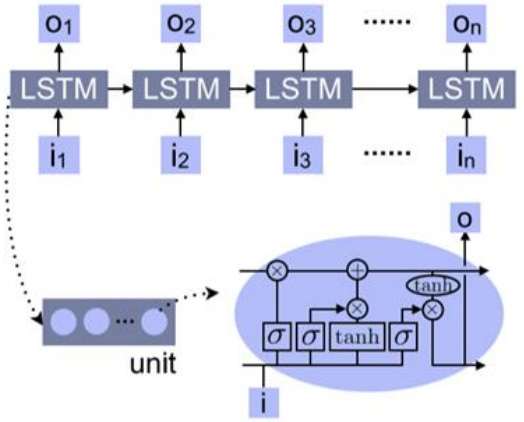


- Reported on RPC 2020, submitted to JINST

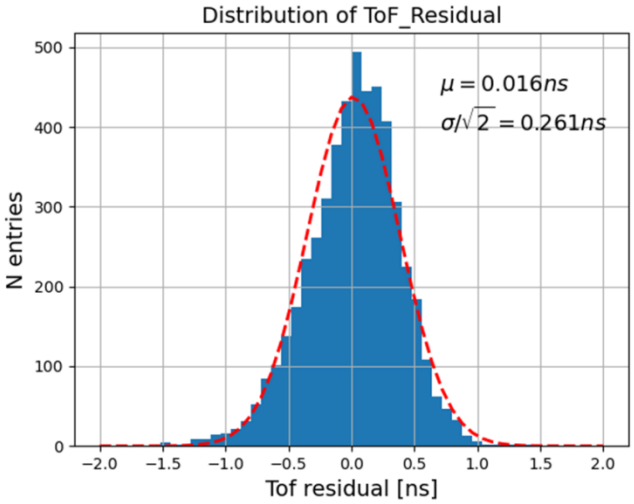
RPC Time Resolution Study using Machine Learning

- To study a more intrinsic σ_t of thin-gap RPC
- Neural network setup: (Long short term memory) LSTM and (Multi-Layer Perceptron) MLP
- Data augmentation method utilized to fully explore the data usage
- The network predict a $\sigma_t = 261\ ps$ (HV at 6300 V)
  - 50% leading edge method (CFD): $\sigma_t = 430\ ps$
- ML gives a better RPC intrinsic σ_t, compared to 50% point method.
- Further optimization is ongoing. Will study relation between σ_t and gap size.

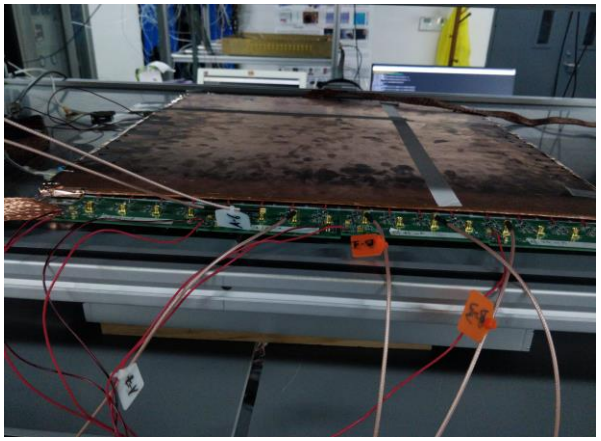
See more in Xiangyu Xie's talk



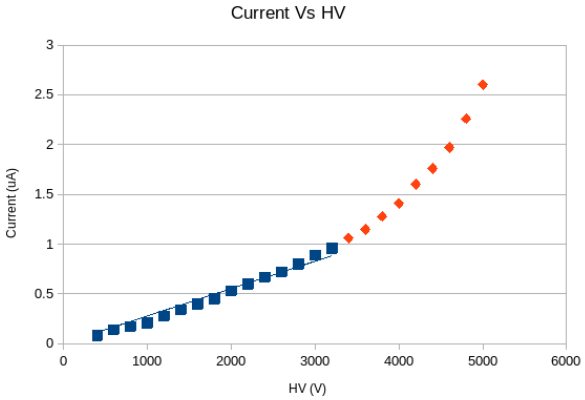
(b) Long Short Term Memory network

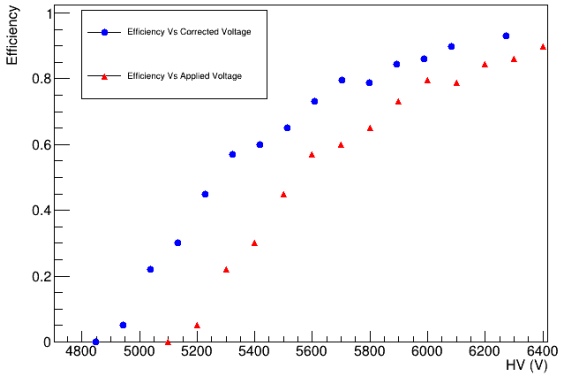


RPC R&D @ SJTU



- **Clean room has been built**
- **Cosmic ray test of glass RPC (30x33cm^2)**
  - efficiency reaching 95%, compatible with USTC result

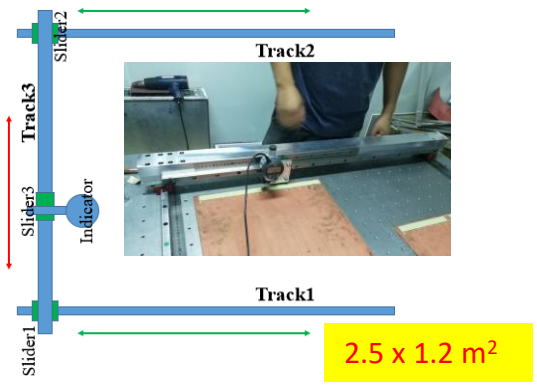




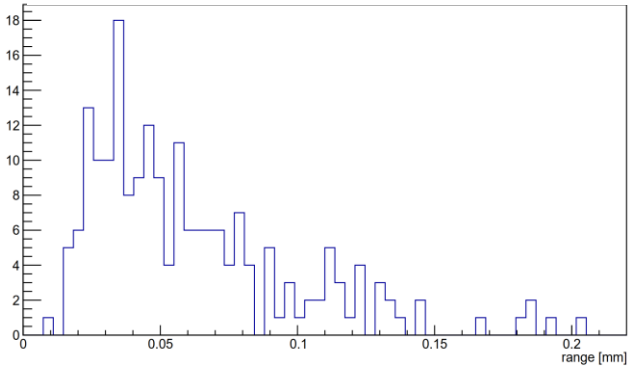
- **Gas flow simulation** to optimize gas velocity uniformity, and to minimize vorticity by adjusting positions of spacers, inlet, outlet, size of spacers, etc (preliminary results, to be further optimized)
- Will construct 1x1m^2 glass RPC chambers
- Will characterize 4 Bakelite prototype chambers with required humidity(~30-40%RH)
- Painting room for graphite coating is under investigation will be built soon.

QA&QC Facilities

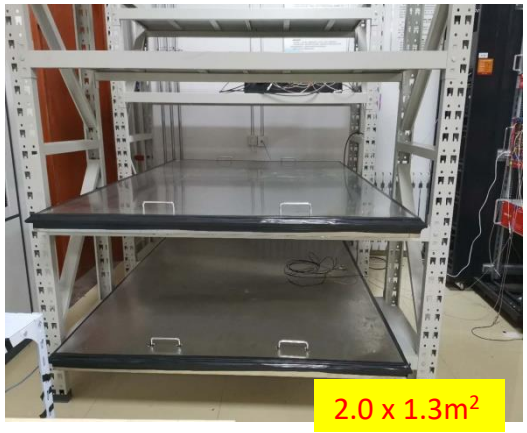
- **Panel flatness measurement system built @USTC**
  - For Quality Control in the mass production



flatness of a 140 x 40 cm² readout panel



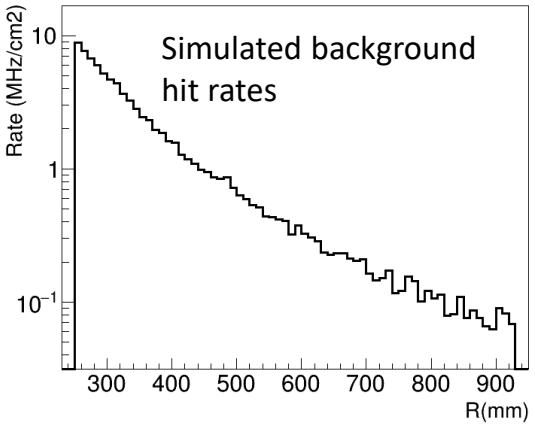
- **Large cosmic ray trigger system built @SDU**



- Two layers of scintillators
- Can fully cover the BIS type RPCs; Used for QC and QA in the mass production.

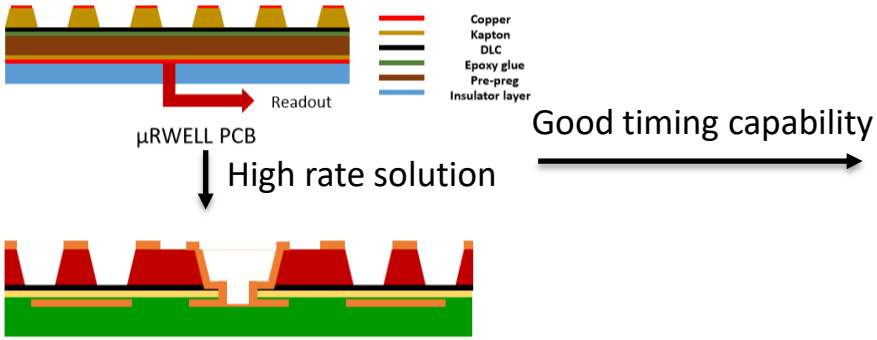
High-η muon tagger

- **To extend the angular acceptance for muon identification** (new inner tracking system extends the tracking coverage up to $|\eta| < 4$)
- **Detector requirements**
  - Compact: multiple layers with 5cm
  - High rate capability: 10 MHz/cm^2
  - Large detection area: a few ten m^2

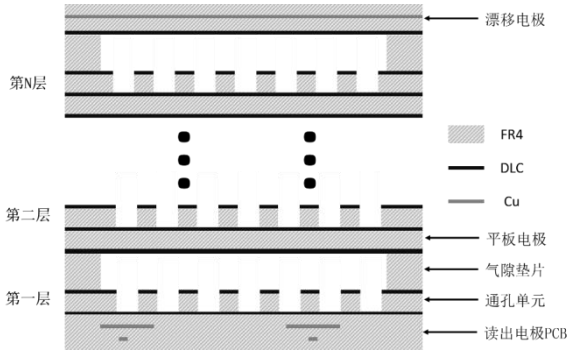


- **Novel micro-pattern gaseous detector (MPGD) concepts for the muon tagger are being explored @USTC**

Micro-resistive WELL detector (uRWELL)

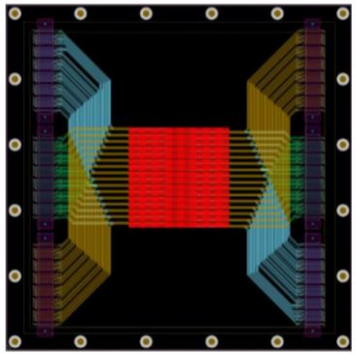


Multiple-gap resistive WELL detector

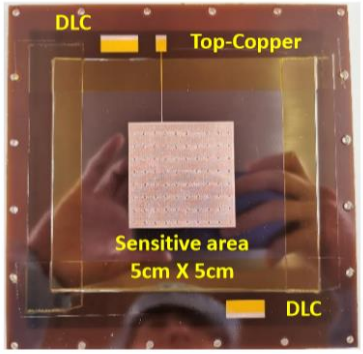


MPGD Development for the Muon Tagger

High-rate μRWELL prototype

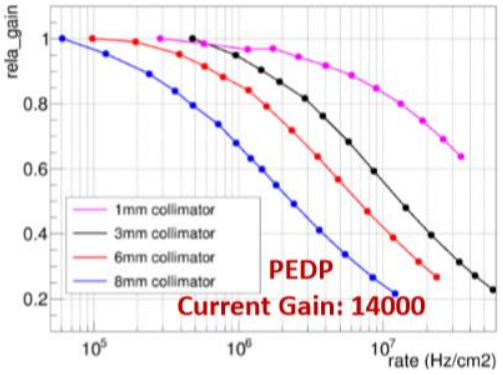


Small-pad readout

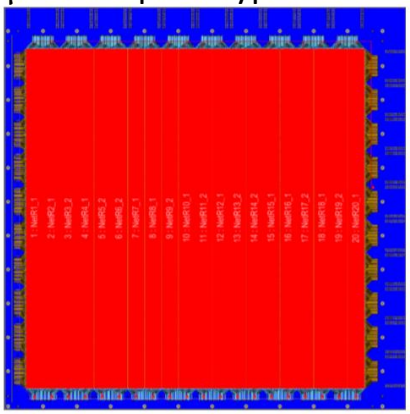


μRWELL PCB

Rate capability for 8 keV X-rays (×10 for MIP)

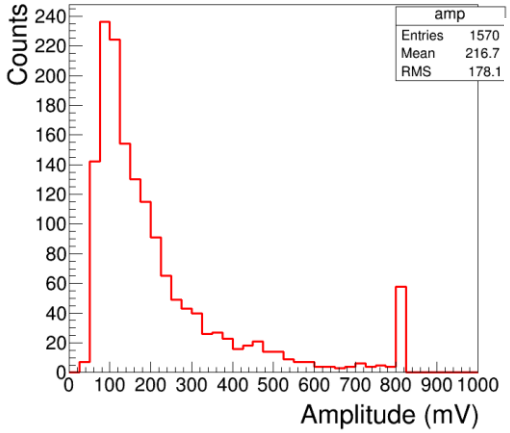


Designing a 50cm×50cm μRWELL prototype

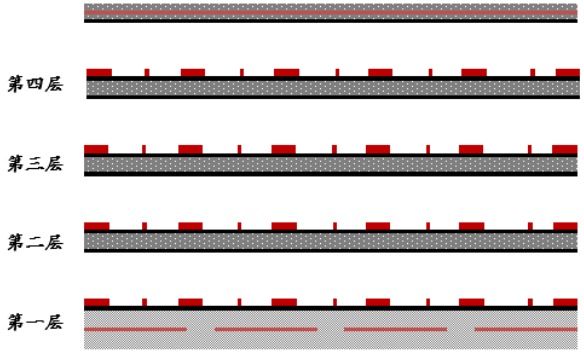


4-gap resistive WELL prototype

Amplitudes of cosmic-ray signals. Efficiency ~ 80%

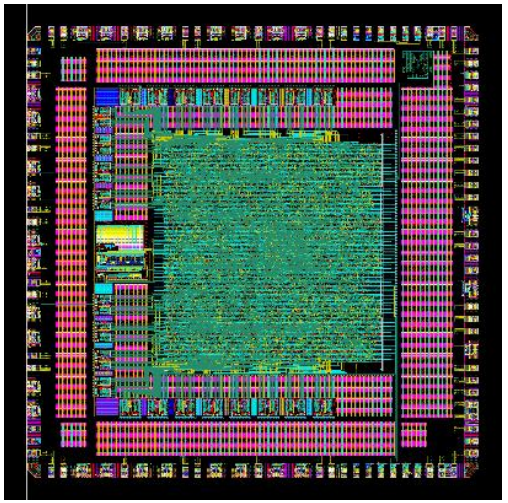


Designing a resistive Micro-Strip Gaseous Chamber (MSGC) for enhancement of efficiency

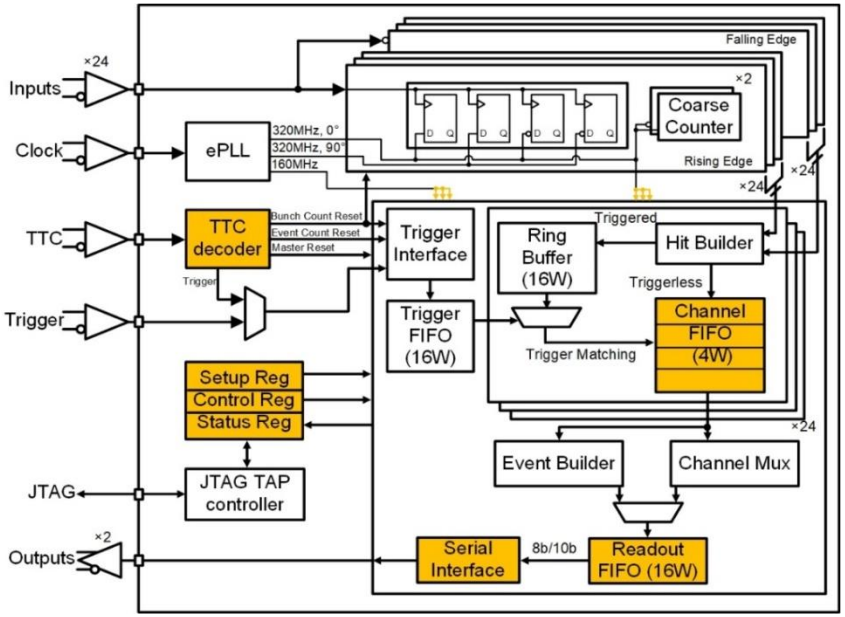


TDC ASIC in MDT

- **The 3rd version of the MDT TDC ASIC has been completed by USTC and University of Michigan in cooperation.**
  - Fabricated in 130 nm CMOS technology.
  - Triple Module Redundancy is implemented in the configuration registers and flow control logic blocks, to enhance the radiation tolerance of this ASIC.



Layout of the ASIC (3rd version)

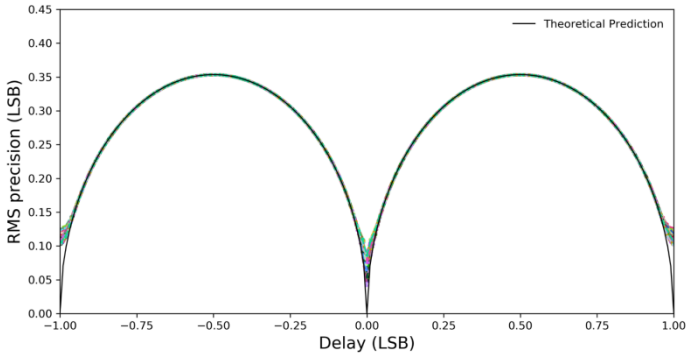


Block diagram of the TDC ASIC with TMR implemented

BGA144 package

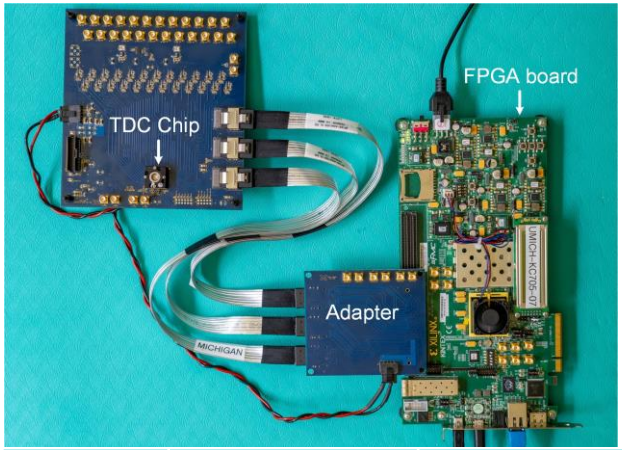
TDC ASIC in MDT

- **Time resolution** is similar with the 2nd version, better than 300 ps



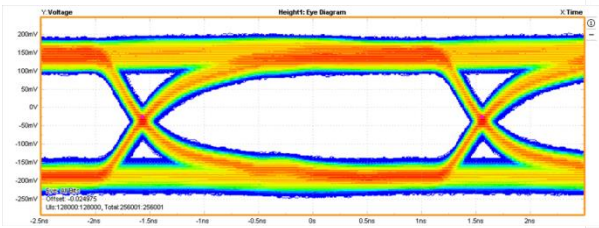
Time resolution (RMS)

Test setup of TDC V3

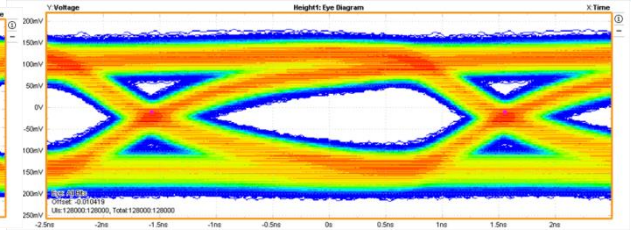


	TDC V2(mW)	TDC V3(mW)
Digital	146	152.6
Analog	104	105.2
Total	250	257.8

- **Power consumption** increase due to partially TMR is only 3%.
- **Cable driving ability** meets requirement (BER < 1e-14)



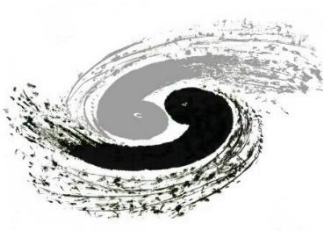
eye diagram of driving 1m cable



eye diagram of driving 4m cable

- **Combination tests with MDT front-end electronics** will be conducted before finalizing the design and production.

High Granularity Timing Detector

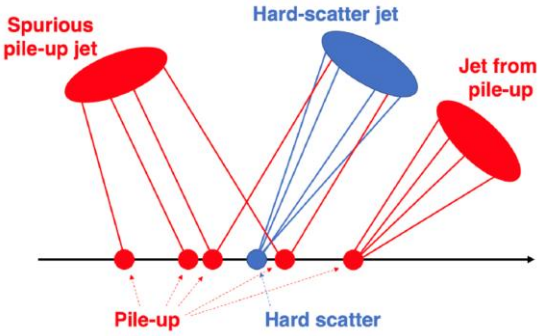


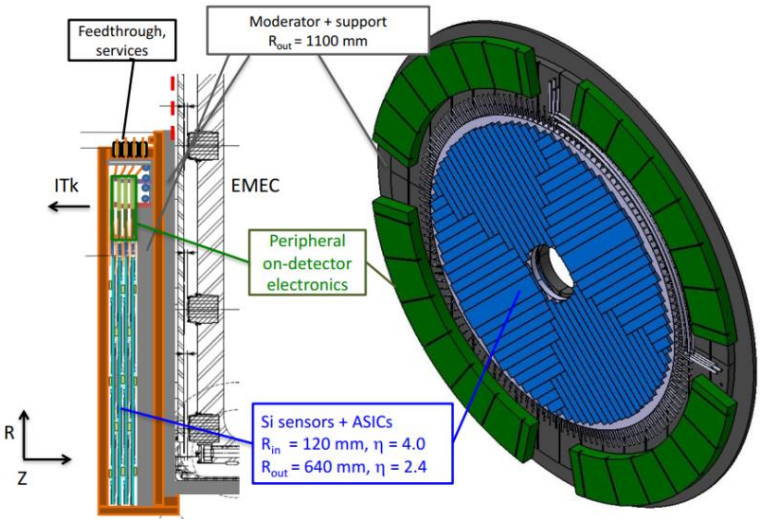
High-Granularity Timing Detector

Congratulations to HGTD people that this project got approved by CERN Research Board as official ATLAS Phase-II upgrade project on 18 Sep 2020

Very challenging to mitigate the pileup effects at HL

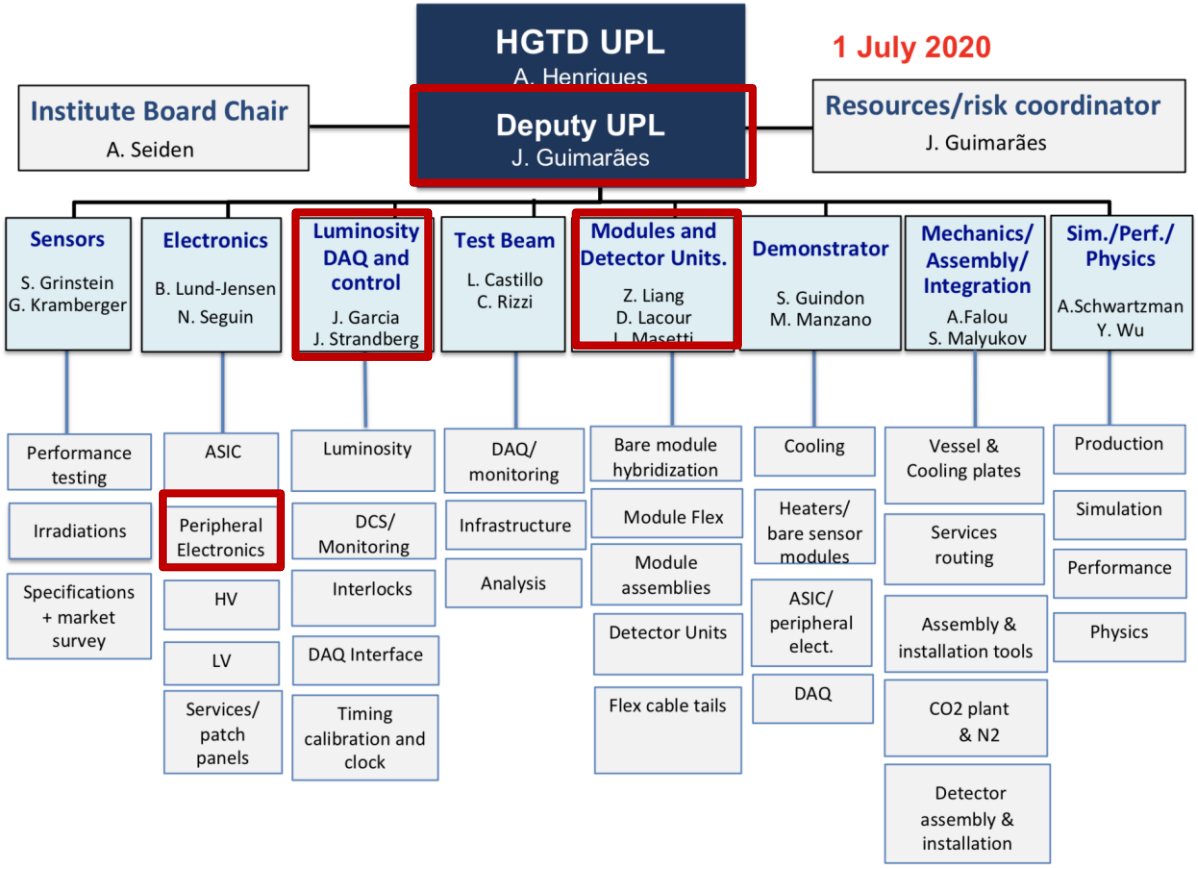
- Designed to distinguish between **collisions occurring very close in space but well separated in time**
- Located just outside of ITk covering the forward region $\mathbf{2.4 < |\eta| < 4.0}$
- Consisting of 4 silicon layers
  - 10% occupancy in $1.3 \times 1.3\ \mathrm{mm}^2$ pixels
- Expected **timing resolution of 30-50 ps** will greatly improve the pileup mitigation in the forward region
  - Compared to 180 ps RMS spread of collisions





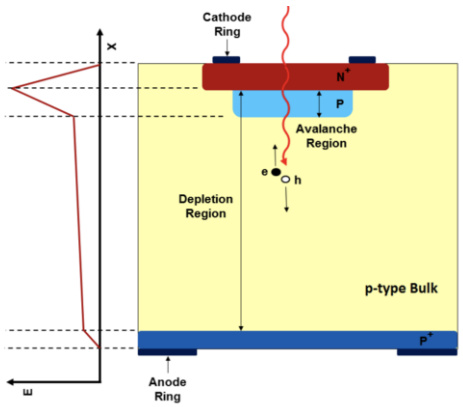
IHEP group in HGTD detector

- **IHEP takes Leading roles in HGTD project**
  - HGTD deputy project leader (Joao Guimaraes Da Costa)
  - Module group Level-2 coordinator(Zhijun Liang)
  - DAQ Level-2 coordinator (Juanan Garcia)
  - Peripheral electronics Level-3 coordinator (Jie Zhang)

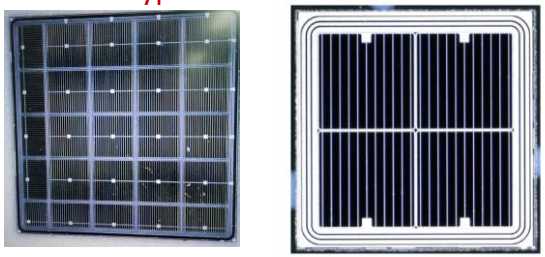


HGTD sensor R&D at IHEP

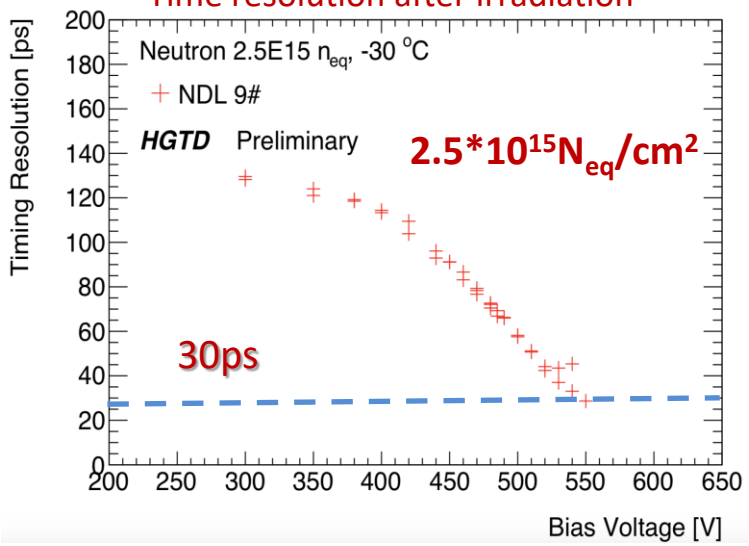
- **Low gain avalanche diode(LGAD) is developed for HGTD**
  - Radiation hard, thin active layer (fast timing)
  - High S/B, no self-triggering
- **IHEP & Beijing Normal University developed IHEP-NDL sensor**
  - Time resolution reach 30ps at high fluence 2.5*10^{15}Neq/cm^2
  - Collected around 30fC(4fC) charge before (after) irradiation
- **Next step (2021)**
  - Will develop full size (4*2cm^2) sensors
  - Will compete with HPK/FBK in market survey



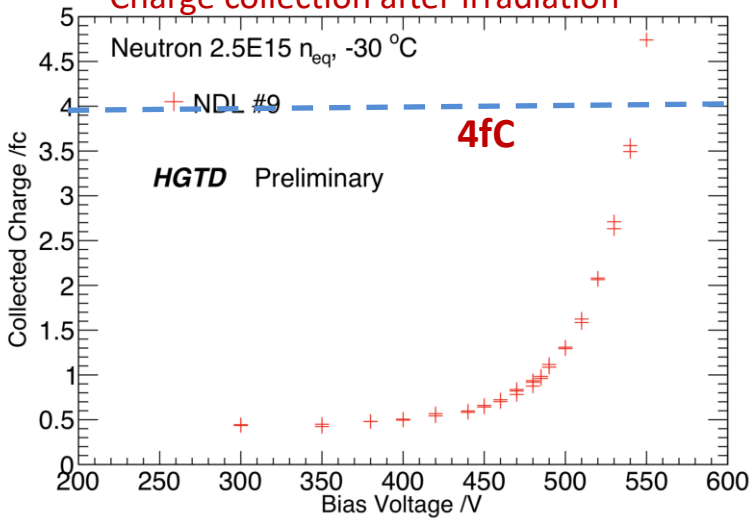
Prototype of IHEP-NDL sensors



Time resolution after irradiation

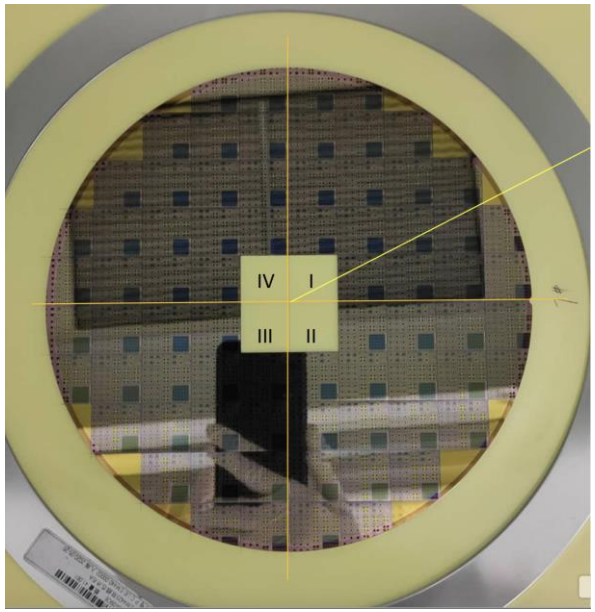


Charge collection after irradiation



HGTD sensor R&D at IHEP

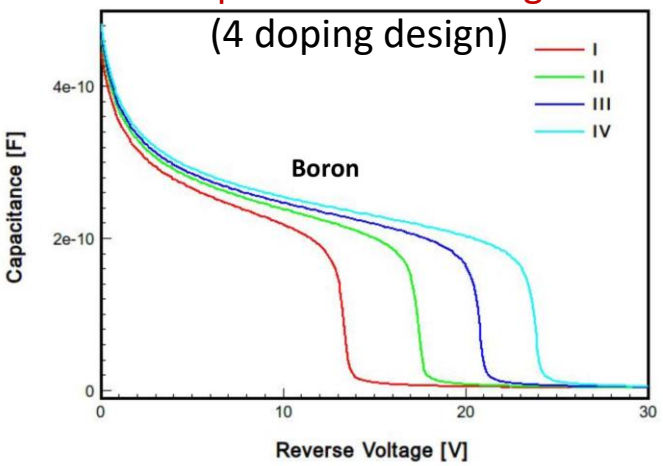
IHEP-IME sensors



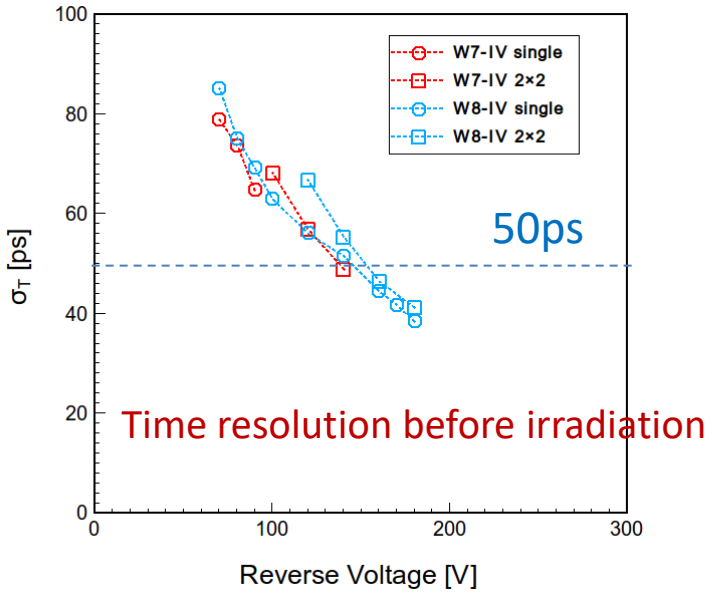
- **IHEP & Institute of micro-electronics (IME) LGAD sensor**
  - IHEP team designed and IME fabricated the 1st prototype this September.
  - Depletion voltage close to design value (4 doping design)
- **Good time resolution (30-40ps) and high charge collection (20-30 fC)**
- Will measure irradiation hardness and design full size sensor

Capacitance vs voltage

(4 doping design)



See Kewei Wu's talk



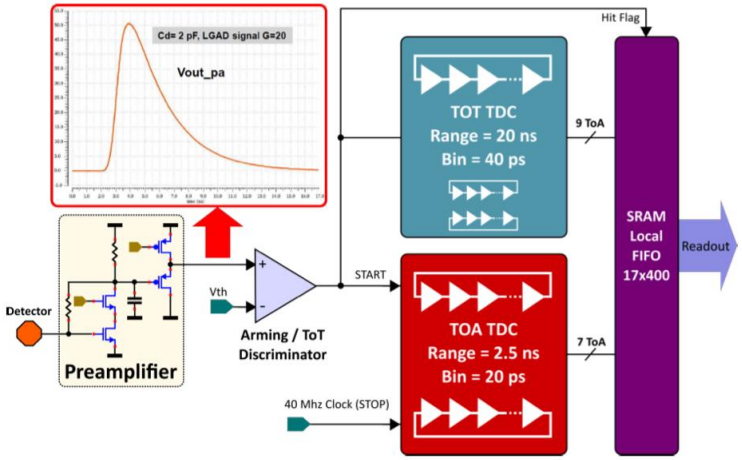
Fast readout ASIC R&D

- Fast readout ASIC (ALTIROC) R&D is one of the keys for HGTD
  - Time resolution is better than 10ps
  - Radiation hardness: >200MRad
  - Status: **Small prototype (ALTIROC1) under test**; Full-size ASIC in 2021

- **IHEP/NJU developed full-size ASIC emulator**
  - Study of the communication between ALTIROC emulator and FELIX DAQ system started

- **IHEP contributed to irradiation study of ALTIROC1_v3**

Schematic of ALTIROC

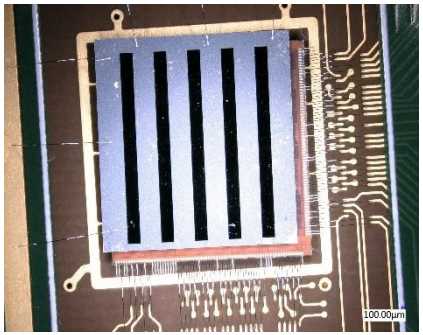


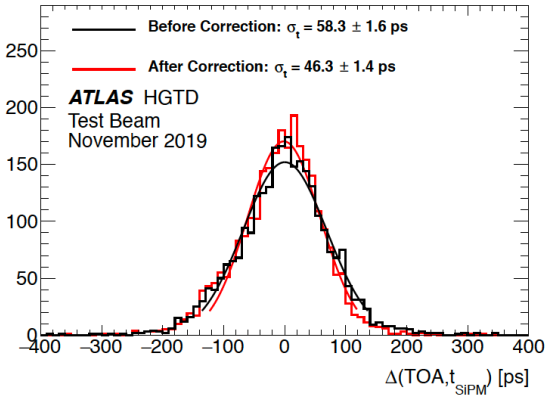
ASIC emulator

X ray machine in IHEP
For ASIC irradiation study

HGTD Module R&D at IHEP

- **IHEP performed 2 rounds of prototyping of mini-modules** (6.5x6.5mm^2)

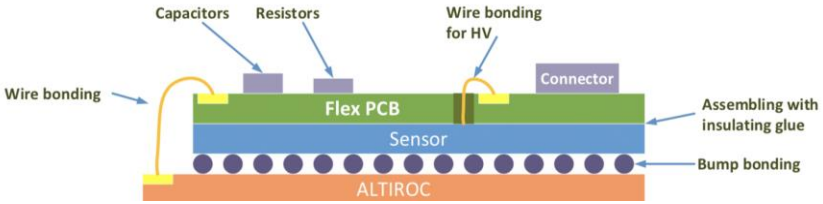




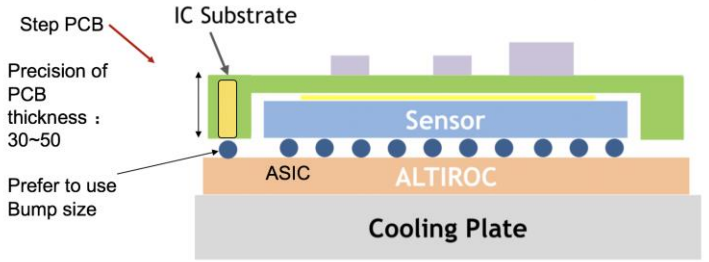
Time resolution
~46ps in beam test

- **Alternative module design with full bump bonding**
  - Avoid wire bonding, simplify the assembly process, more robust

Baseline module design

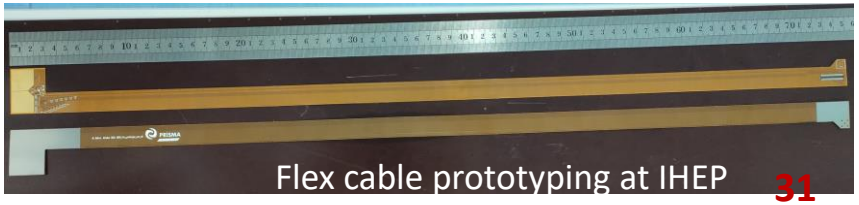


Alternative module design



- **Module flex design and flex cable prototyping**
- Full size (4 x 2 cm^2) module prototyping in 2021

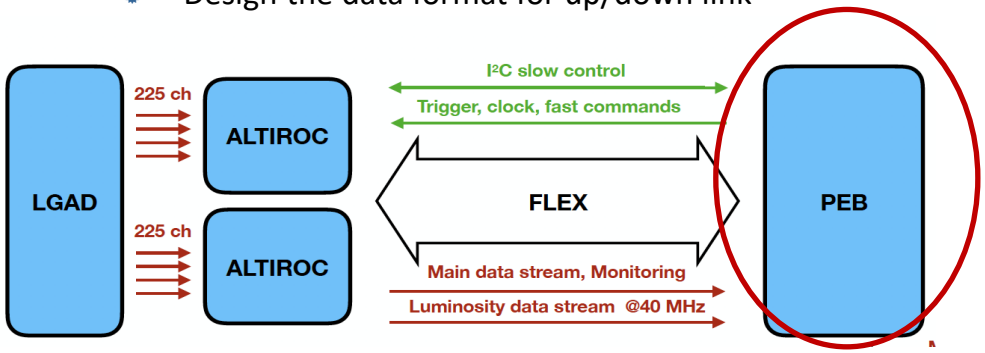
See Zhijun Liang's talk



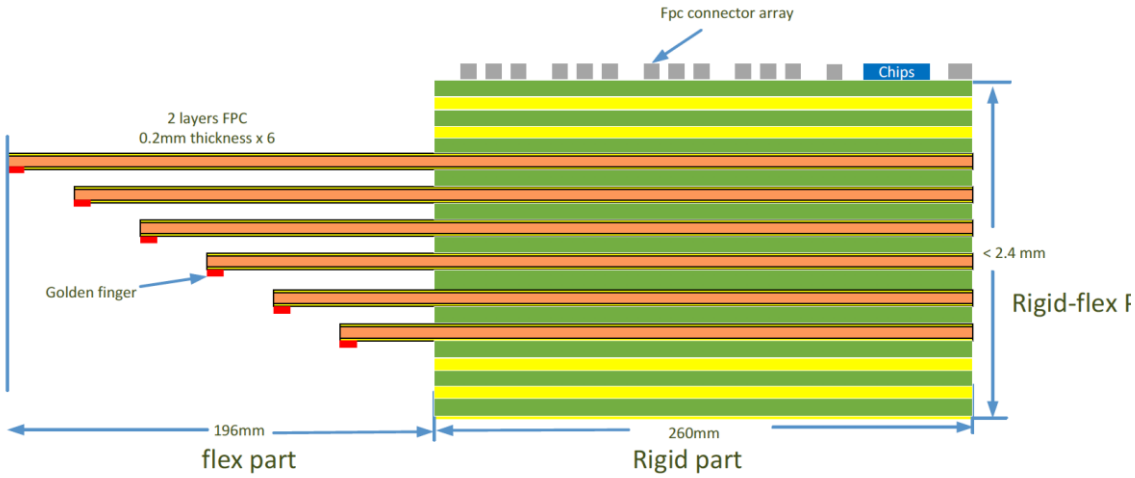
Flex cable prototyping at IHEP

Peripheral electronics and DAQ

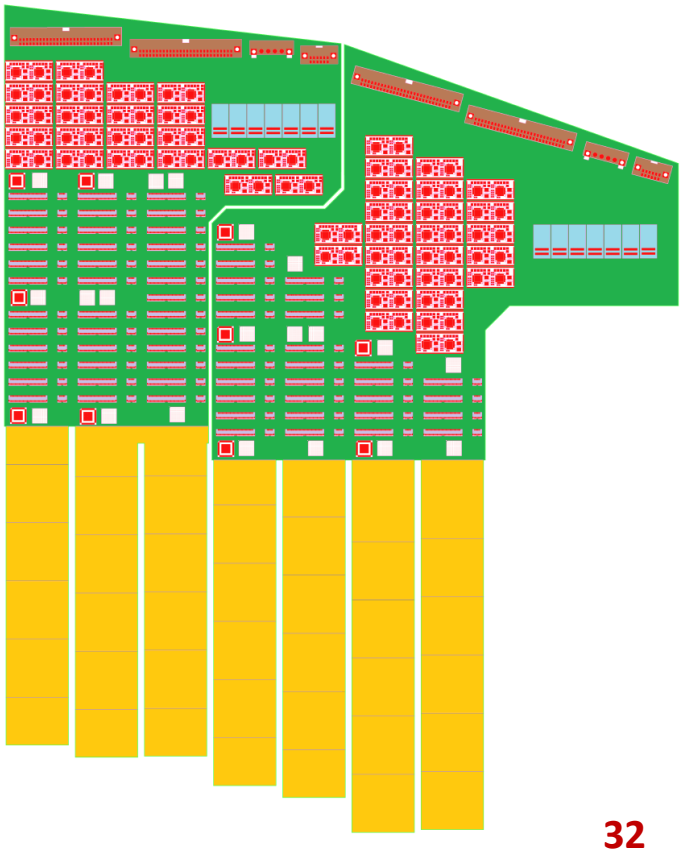
- **IHEP/NJU are leading the Peripheral board (PEB) design**
  - Proposed rigid board + flexible PCB design → Became baseline
- **IHEP is leading HGTD DAQ group**
  - Design the data format for up/down link



Peripheral board rigid-flexible PCB design



Peripheral Electronics



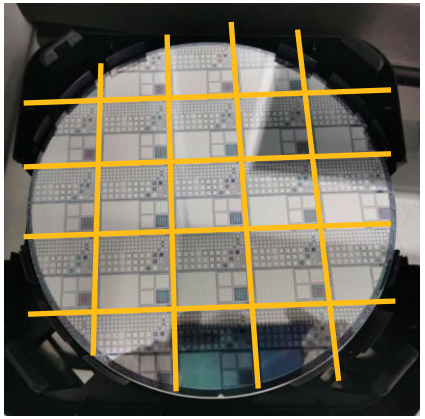
USTC HGTD activities overview

- Sensor design and “USTC-1” LGAD performance
- Beta scope TCT system
- Studies of large-area HPK prototype sensors
- ALTIROC1 test
- Software and performance

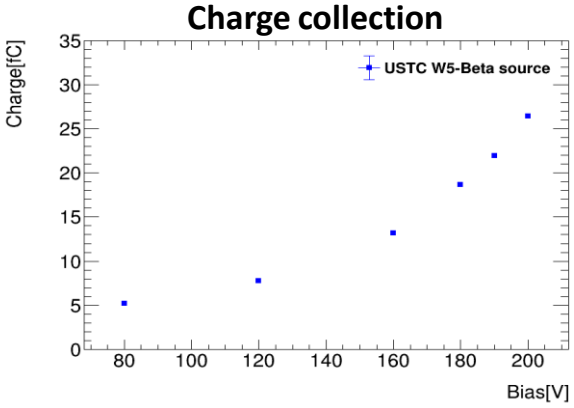
Sensor design and "USTC-1" performance

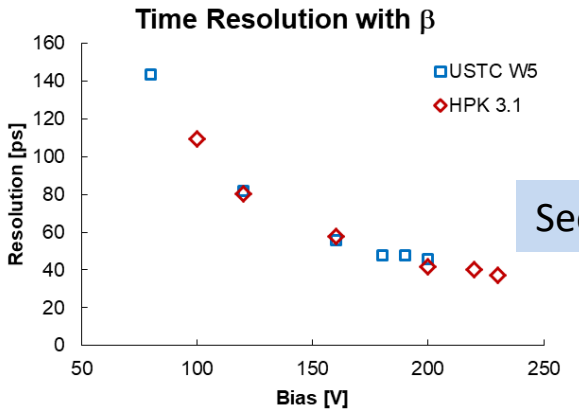
- **USTC-1 prototype designed at USTC and fabricated at IME**
  - 6 splits, including one with Carbon doping

Wafer	Designed VBD [V]	GL.Energy	GL.Dose	Implantation
W1	165	Medium	Medium	B
W2	165	Medium	Medium	B
W3	150	Low	High	B
W4	180	High	Low	B
W5	265	Medium	Low	B
W6	165	Medium	Medium	B+C



- **Promising results from first measurements**
- Measure time resolution and charge collection with Sr90 beta source

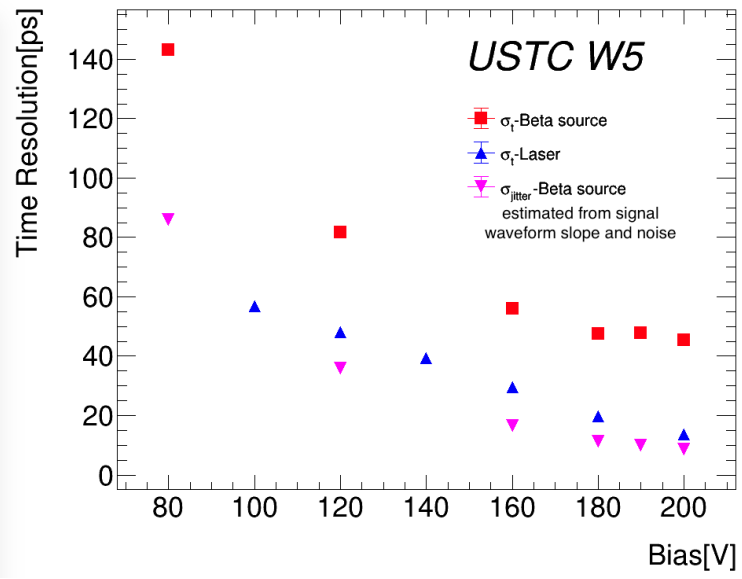


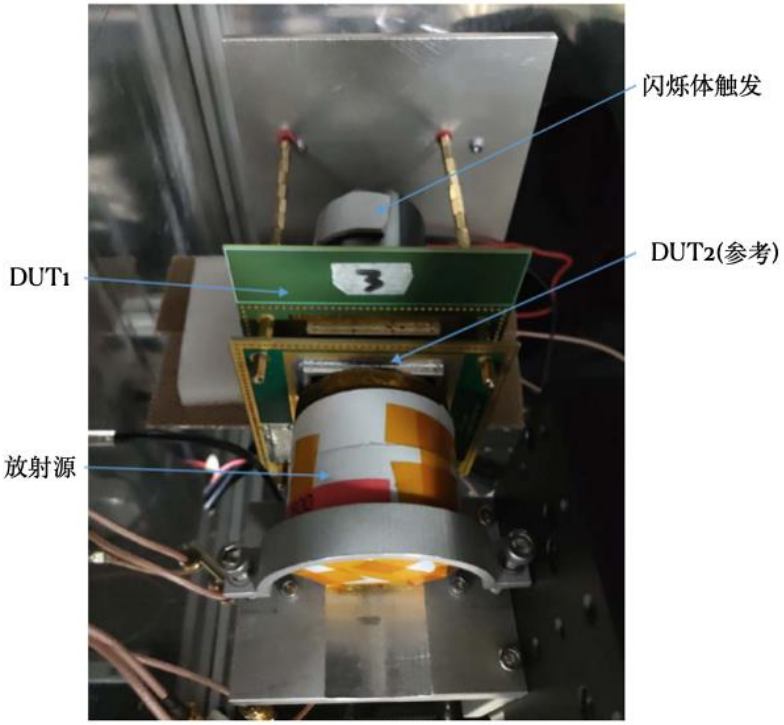


See Xiao Yang's talk

Beta-scope TCT at USTC

- Feature: Scintillator trigger and ref. detector, 2-stage amplification
- Infrared laser to check jitter

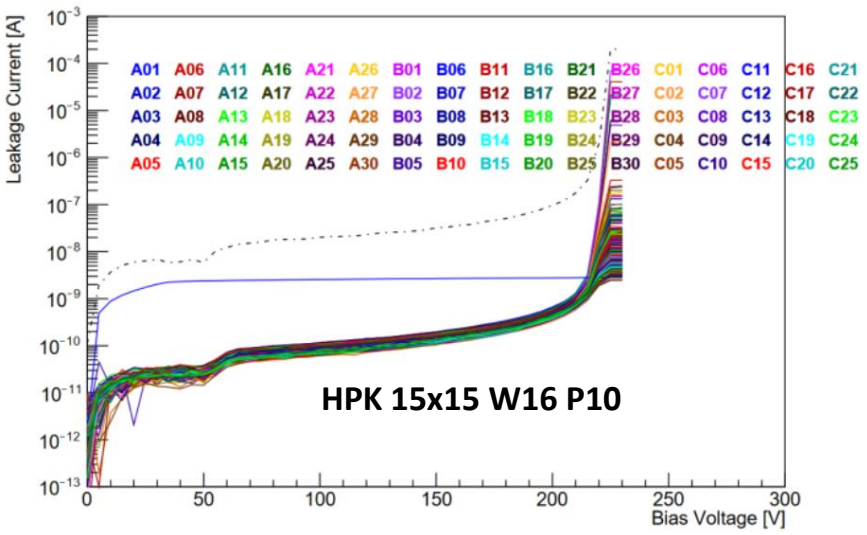


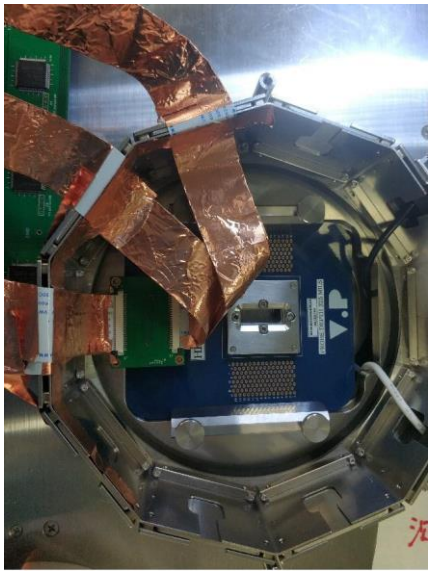


See Tao Wang's talk

Studies of large-array HPK sensors at USTC

- **Developed I-V, C-V measurement system** with probe cards for 5x5 and 15x15 arrays
- Studied the **effects of floating guarding/floating pads**: punch-through effect important to explain the different results obtained from different labs
- Study in progress: the implication of sparse mal-functioning pads in a large array for detector operations

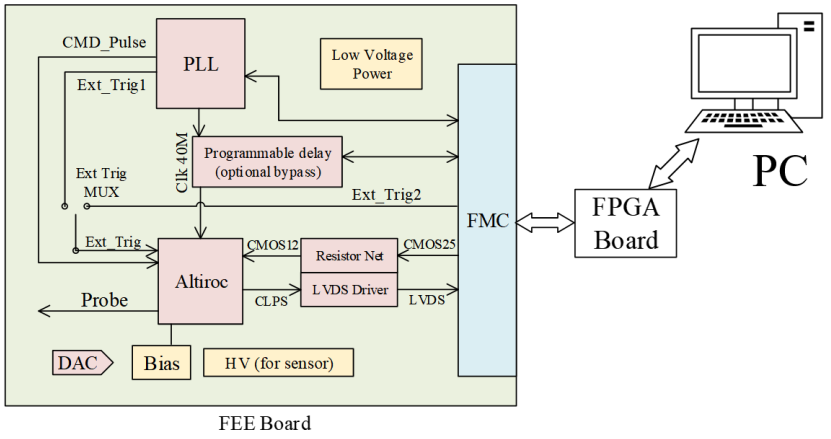




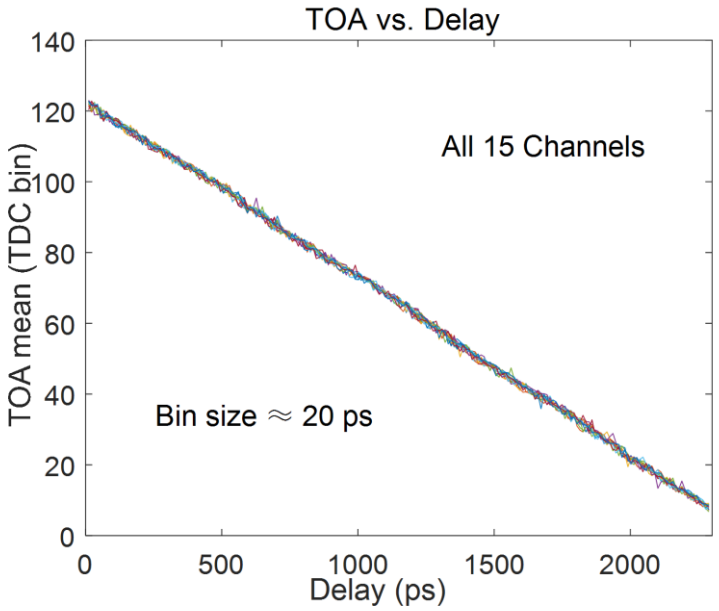
See Xiao Yang's talk

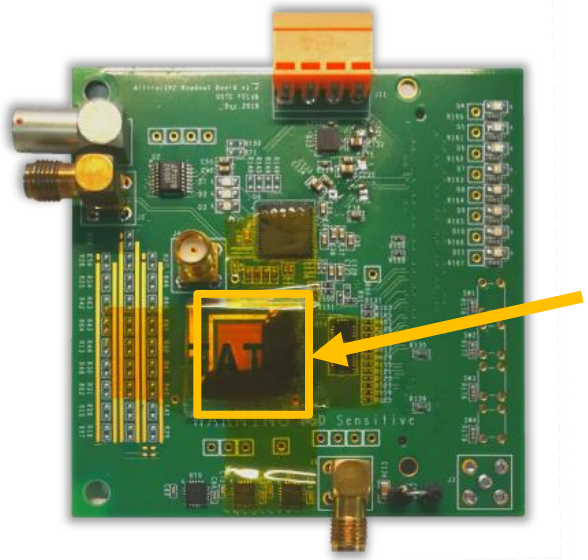
ALTIROC ASIC test at USTC

- Designed an ASIC test system
- “Re-discovered” the known issues of ALTIROC1_v2 chips
- Testing of ALTIROC1_v3 chips in progress



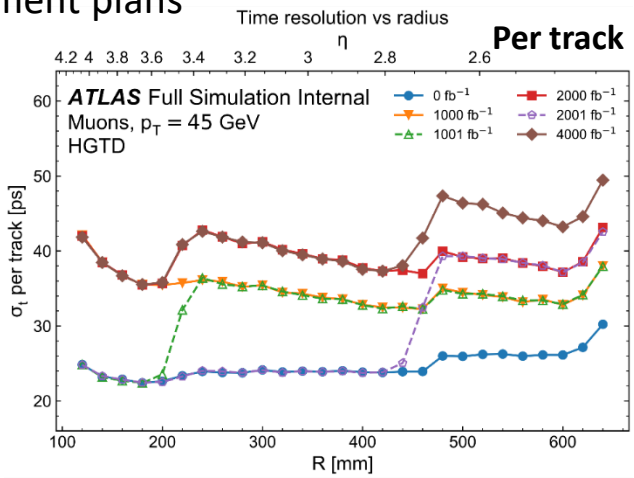
FEE Board

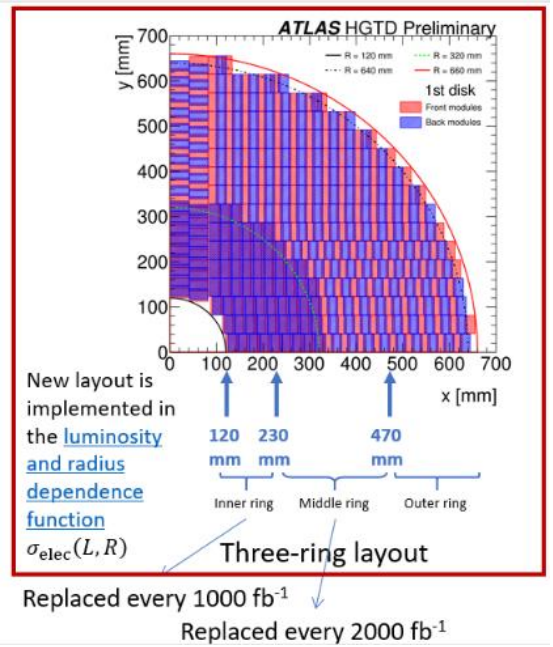




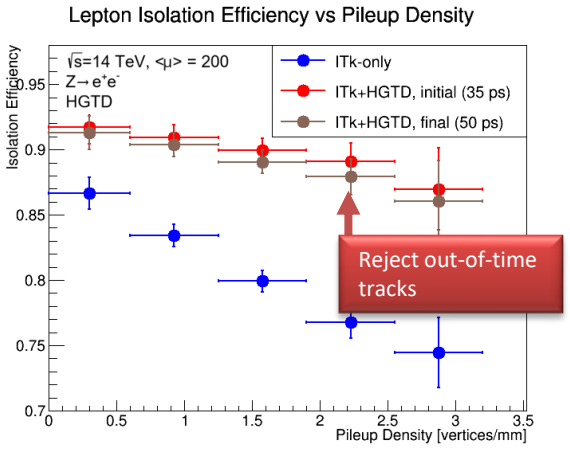
Software and Performance Studies at USTC

- Implemented the digitization in the HGTD simulation
- Implemented the 3-ring layout in the simulation
- Checked the resolution corresponding to the new replacement plans





- Studied the expected enhancement to lepton isolation by the HGTD detector
- Continuing to contribute to the HGTD software and performance studies



See Tao Wang's talk

Conclusions

- **Challenging to maintain or improve the performance in very dense environment with pileup up to 200**

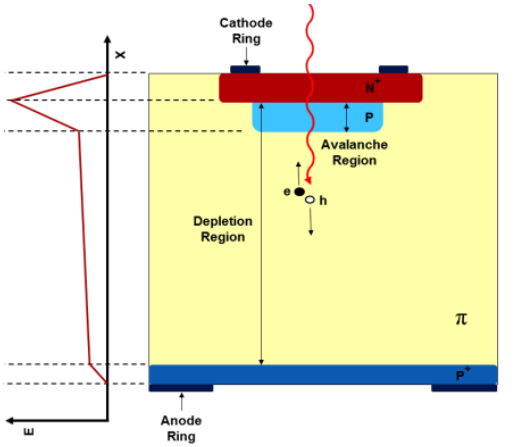
- **Chinese clusters have made and are continuing to make significant contributions to main upgrade projects**
  - All-silicon ITk with extended coverage to improve the tracking performance
  - HGTD to mitigate pile-up effects
  - Muon detector (Trigger system upgrade to keep lower trigger threshold)

- **Expecting good detector performance as reimbursement of big efforts we make**

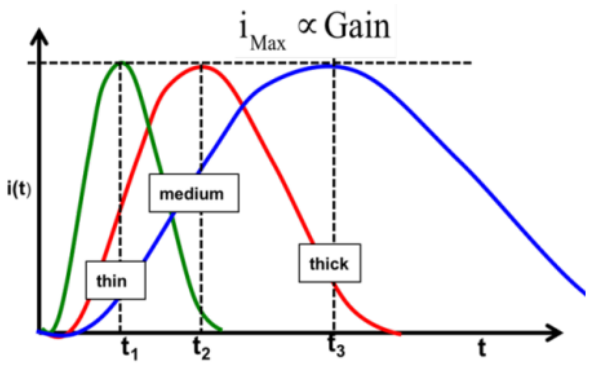
Backup

HGTD

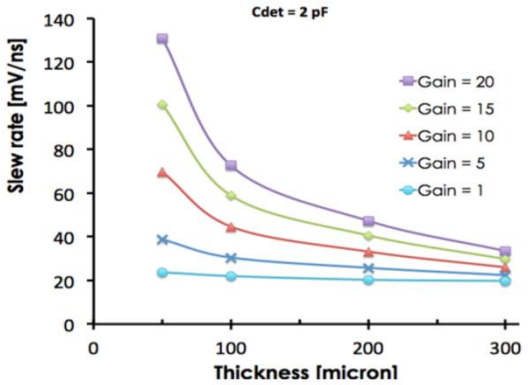
- The technology chosen for the HGTD sensors is Low Gain Avalanche Detectors (LGAD)
  - n-on-p silicon detectors containing a extra highly-doped p-layer below the n-p junction to create a high field which causes internal gain
  - an initial current is created from the drift of the electrons and holes in the silicon
  - When the electrons reach the amplification region, new electron/hole pairs are created and the holes drift towards the p^+ region and generate a large current



Cross section of an LGAD diode



Current signals for different thicknesses



Signal slope as function of thickness.

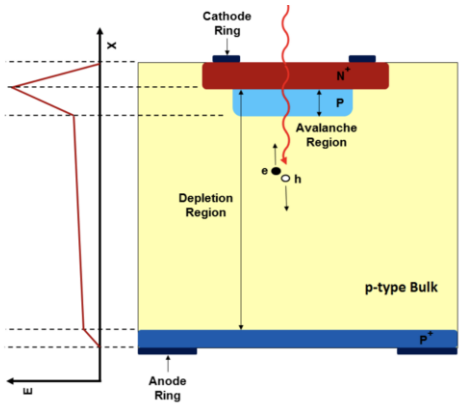
An LGAD thickness of 50 microns has been adopted.

The Trigger and DAQ Upgrade

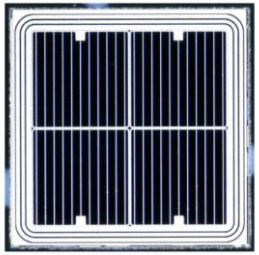
- **High instantaneous luminosity means higher data rates**
- **New designed trigger/DAQ system**
  - To cope with high rates while keeping **low trigger thresholds**
  - The baseline architecture: **a single-level hardware trigger + event filter**
  - **1 MHz trigger rate** instead of 100 kHz
    - A big challenge for the detector readout
  - **10 kHz output data rate** instead of 1 kHz
- **New readout electronics for all systems**
  - To cope with the increased occupancies and data rates

HGTD sensor R&D at IHEP

- **Low gain avalanche diode(LGAD) is developed for HGT**
  - Radiation hard, thin active layer (fast timing)
  - High S/B, no self-triggering

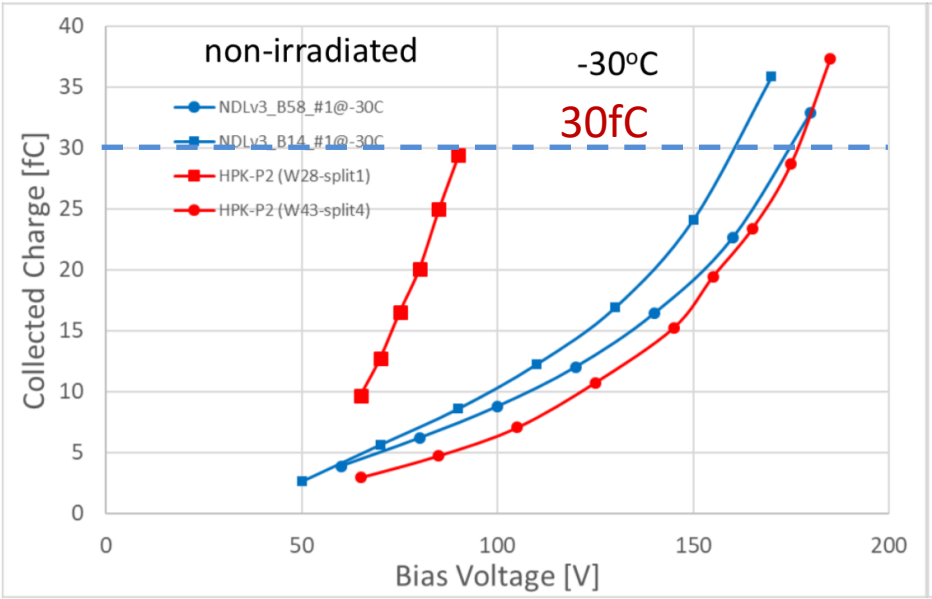


Prototype of IHEP-NDL sensors

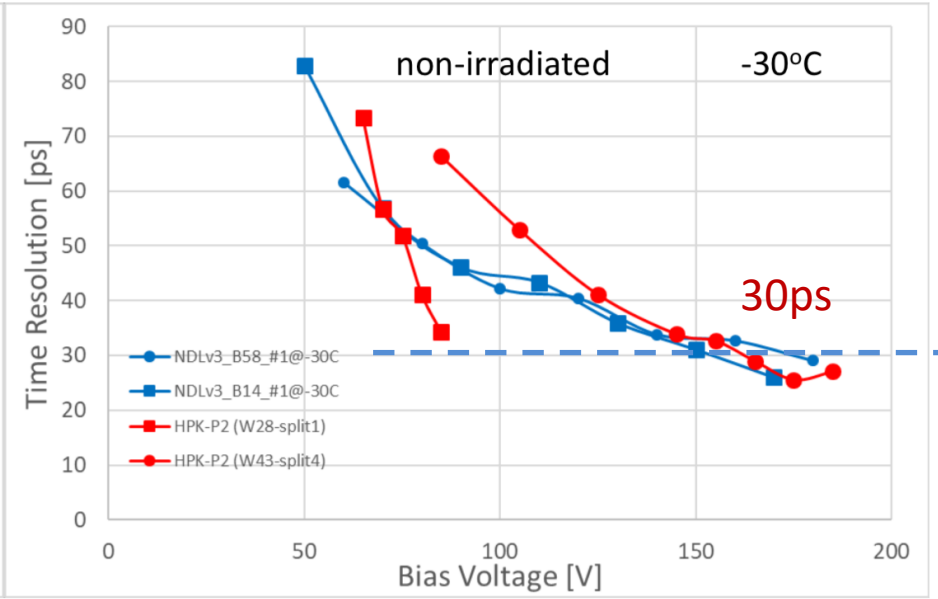


- **IHEP & Beijing Normal U. developed IHEP-NDL sensor**
  - Time resolution ~**30ps** at high fluence 2.5*10^{15}Neq/cm^2
  - Collected charge **~30 fC** (~**4fC**) before (after) irradiation

Collected charge before irradiation

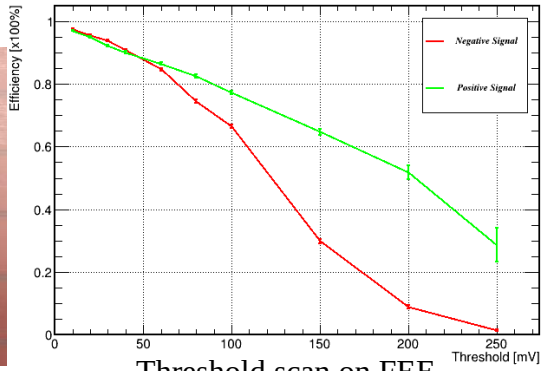


Time resolution before irradiation

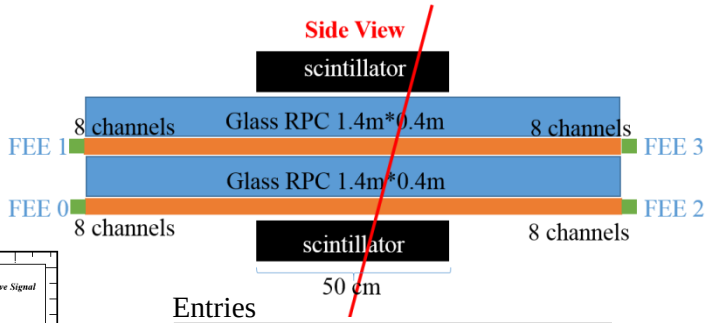


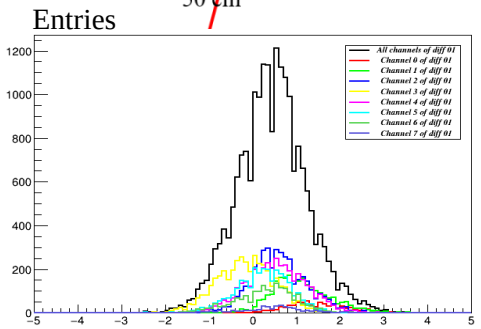
Test on two-end readout RPC

- 8-ch FEE with Amp + discriminator developed at USTC
- Equipped onto both ends of One honeycomb readout panel
- Two identical glass RPC (1.4x0.4m) tested together with cosmic ray

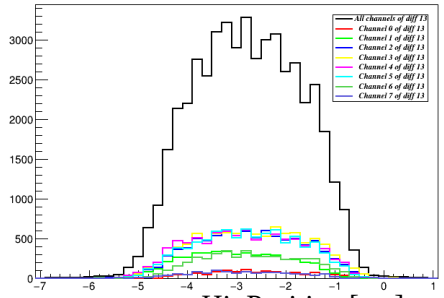


Threshold scan on FEE



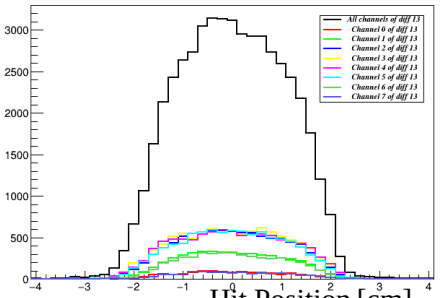


Distribution of time difference [ns]



Hit Position [cm]

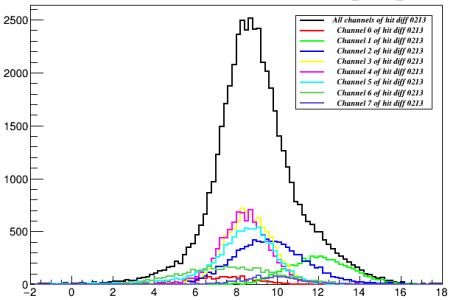
1. Get the mean value of distribution channel by channel
2. Shift the mean value of every channel to 0.



Hit Position [cm]

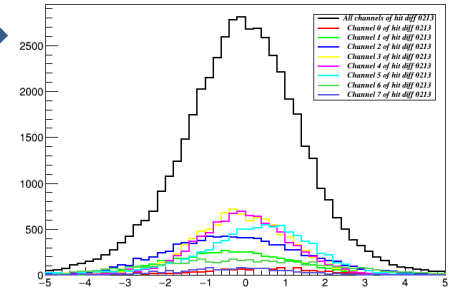
Time resolution:

- Channel 0: 433±16.5 ps
- Channel 1: 413± 8.2 ps
- Channel 2: 431± 5.9 ps
- Channel 3: 466± 5.3 ps
- Channel 4: 486± 5.8 ps
- Channel 5: 425± 5.9 ps
- Channel 6: 463± 9.8 ps
- Channel 7: 490±38.9 ps



Difference of Hit Position [cm]

Difference of hit position

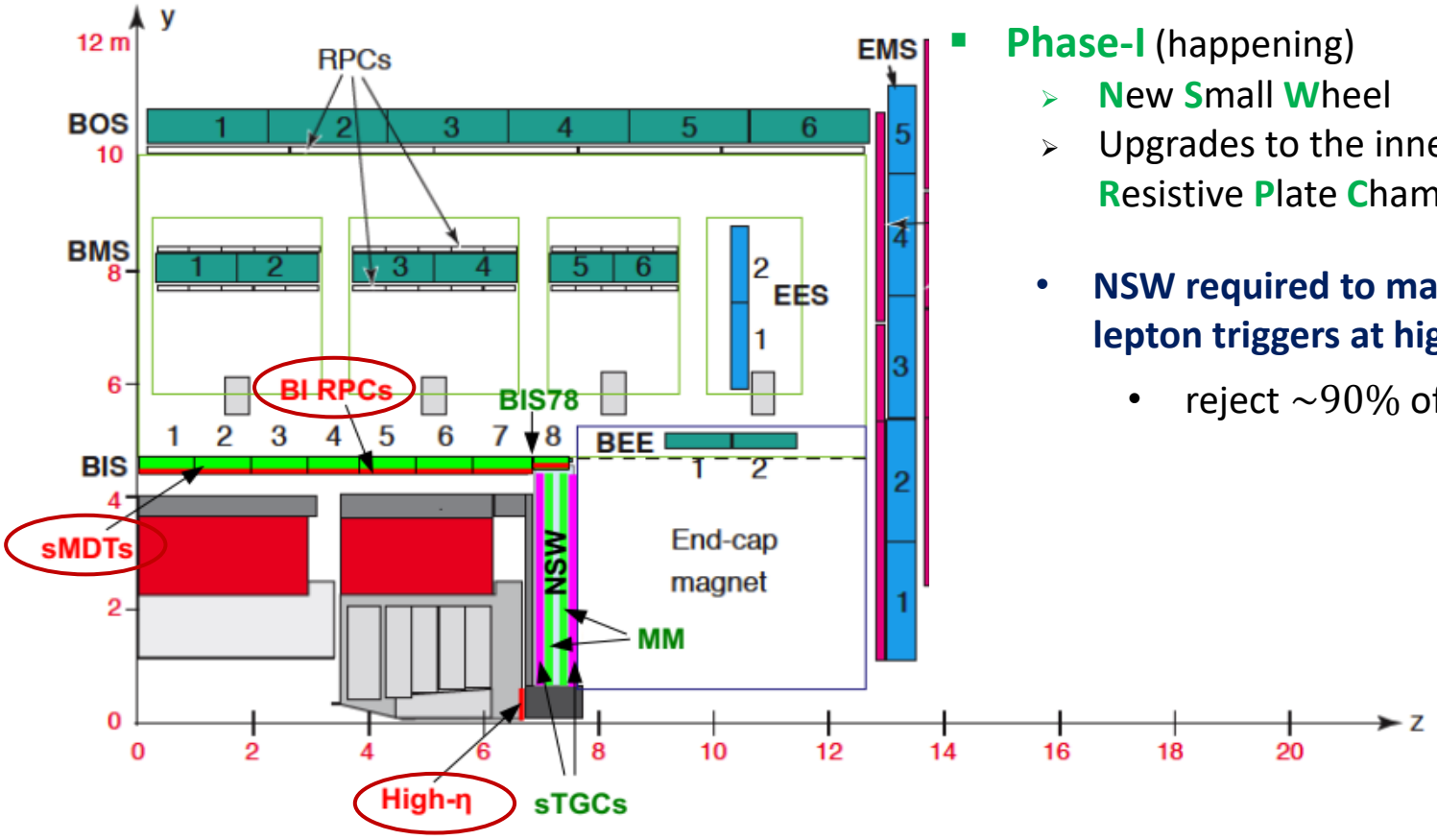


Difference of Hit Position [cm]

Spatial resolution: (cm)

All: resolution = 1.049 +- 0.004
Ch0: resolution = 1.066 +- 0.027
Ch1: resolution = 1.053 +- 0.010
Ch2: resolution = 1.206 +- 0.010
Ch3: resolution = 0.824 +- 0.007
Ch4: resolution = 0.815 +- 0.007
Ch5: resolution = 0.917 +- 0.009
Ch6: resolution = 1.506 +- 0.016
Ch7: resolution = 0.969 +- 0.023

Muon Spectrometer



- **Phase-I** (happening)
  - **N**ew **S**mall **W**heel
  - Upgrades to the inner barrel **R**esistive **P**late **C**hambers

- **NSW required to maintain low-p_T lepton triggers at high rates**
  - reject ~90% of fake triggers

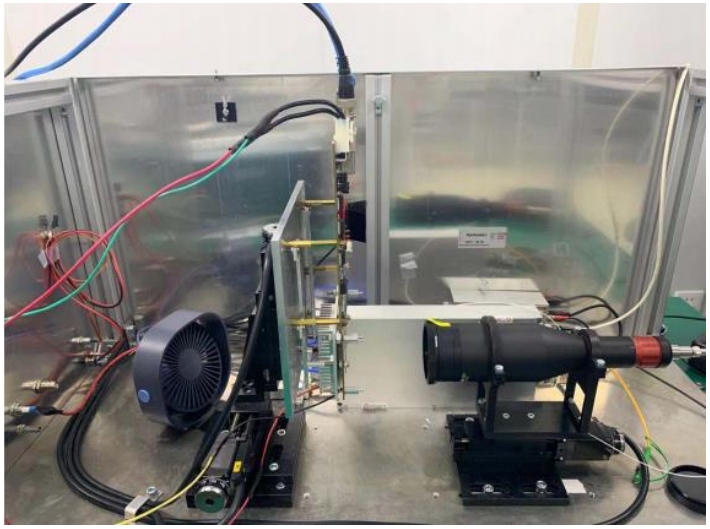
- **Phase-II** (2024 – 2026, mainly about trigger for Muon spectrometer)
  - New inner RPC stations (**USTC, SDU, SJTU**)
  - Monitored Drift Tubes information to be added at the hardware trigger (**USTC**)
  - Investigating the addition of a high-η tagger (**USTC**)

Irradiations at INER

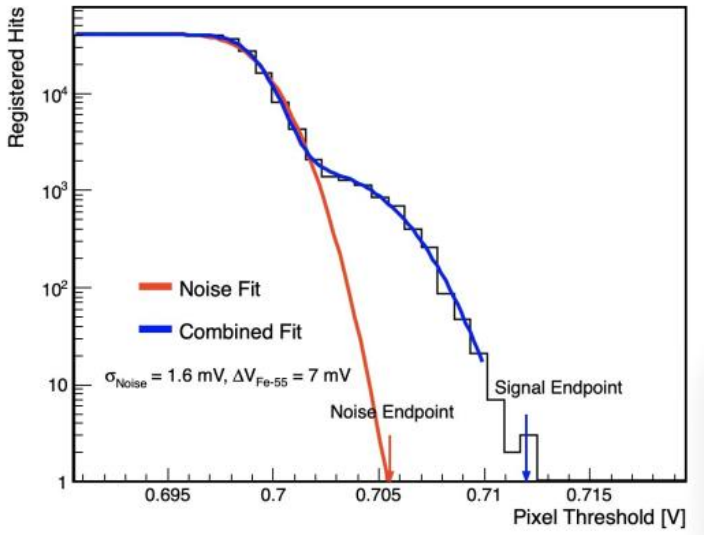
- Initial pre-irradiation studies were done with xrays at RAL
- All results shown here come from Co-60 irradiation at INER in Taiwan
  - Good relations with INER via ATLAS-Taiwan colleagues
  - Good experience using the site in the past
  - Attractively low price for full production pre-irradiation O(10k) plus shipping
  - Only negative is time for shipping and the export license
- Facility has a wall of Co-60 with a conveyor belt going around it
  - Irradiated to approx. 8 Mrad
- Drawer which we use allows boxes with dimensions of 40x30x7cm
- ABC130 pre-irradiation done as single 4” gel-pak
- ABCStar pre-irradiation done in waffle/gel-paks taped into standard 28x19x6 cm box
  - In Taiwan just had to take box, put on conveyor belt and take off when done
  - Takes about 24 hrs for actual irradiation

CHESS2 – CMOS HV Evaluation for Strip Sensors

- **HV-CMOS desirable for high performance tracking in harsh collision environment**
  - High position resolution, low material budget and low cost
- CHESS sensor initially developed to evaluate the HV-CMOS concept as an alternative solution to the strip detector for ATLAS ITk upgrade.
- Tests with laser and radioactive sources (Fe-55、Sr-90)



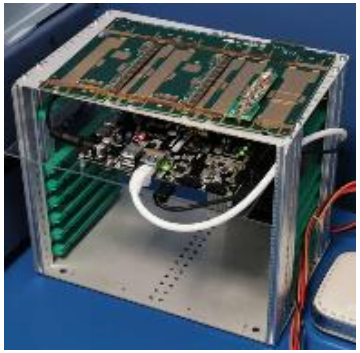
Threshold scan with Fe-55



- Published as a Hiroshima proceeding paper: NIMA 981 (2020) 164520

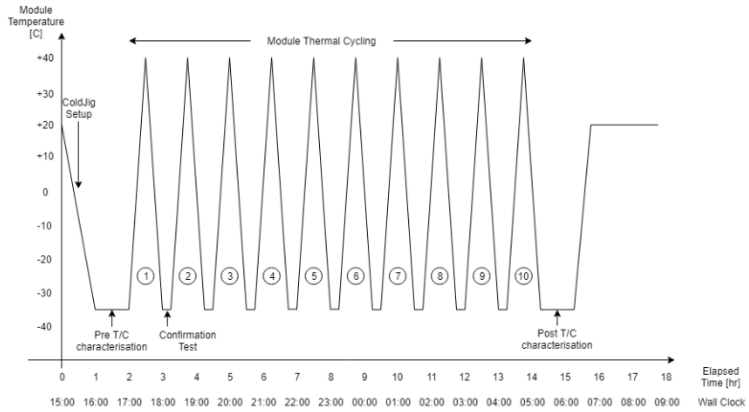
Foreseen measurements

- **Hybrid burn-in**
  - 36 hybrids at the same time
  - 100 hours@ 40℃
  - Waiting for the panel and crate



Oven

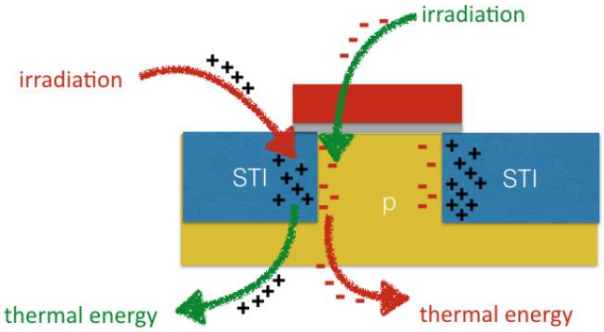
- **Module thermal cycling (-35℃ to +40℃， 10 cycles in 12 hours)**

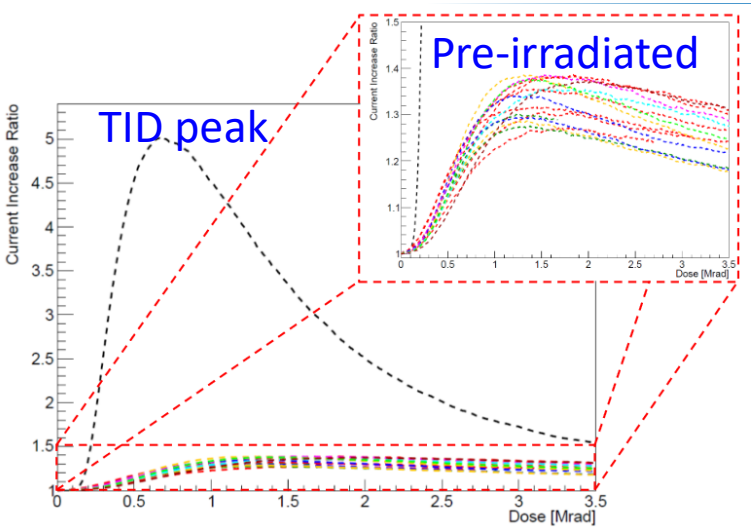


Cold Box assembled in Warwick, will be shipped to China after test

TID “Bump”

- **Higher current draw with radiation due to Total Ionizing Dose (TID)**
- Leakage current resulting from two competing mechanisms: radiation and thermal excitation.
  - Undesired capacity redundancy on powering and cooling design
  - Cannot be easily eliminated by design





- **System level solution: chips pre-irradiated to pass the TID peak.**
- Quality Assurance: at batch level, TID measurements of pre-irradiated single chips with x-ray machine (setup at IHEP)