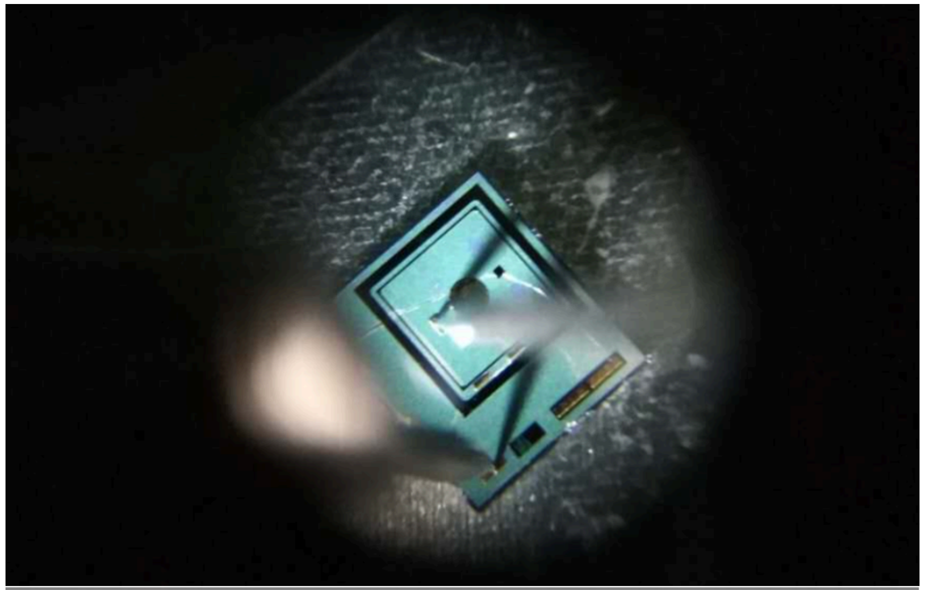
Characterization of the LGADs for the HGTD Upgrade at USTC

- *Large array test*
- *Punch-through model*
- *USTC-1 LGAD*



Xiao Yang, Xiangxuan Zheng

University of Science and Technology of China

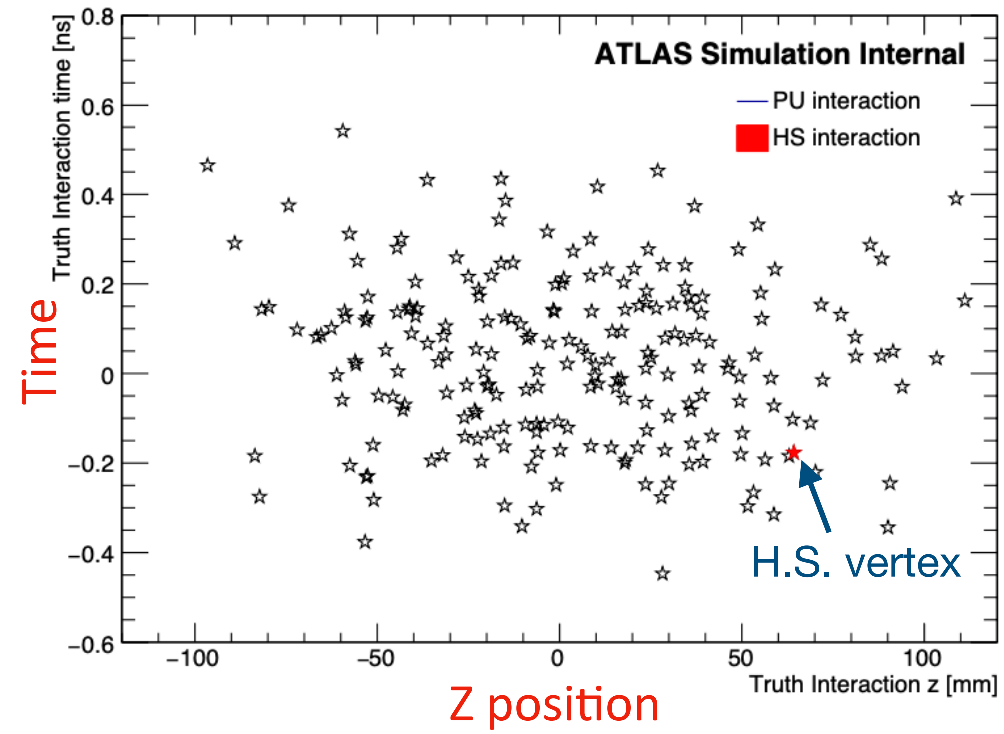
The 6th China LHC Physics Workshop,
November 8th, 2020

(i) HGTD TDR: https://cds.cern.ch/record/2719855/files/ATLAS-TDR-031.pdf

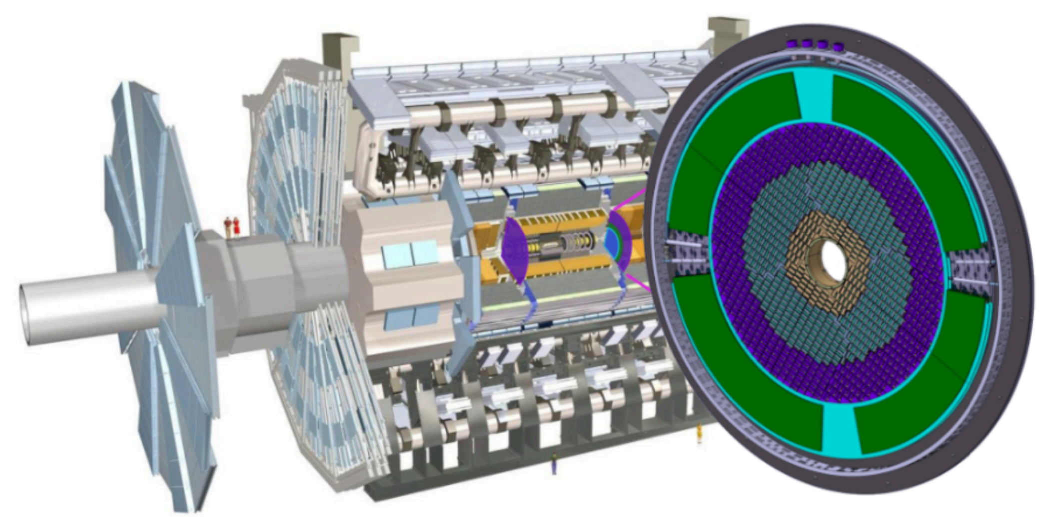
(ii) *Layout and performance of HPK prototype LGAD sensors for the High-Granularity Timing Detector*,NIMA,Volume 980, 11 November 2020
https://doi.org/10.1016/j.nima.2020.164379

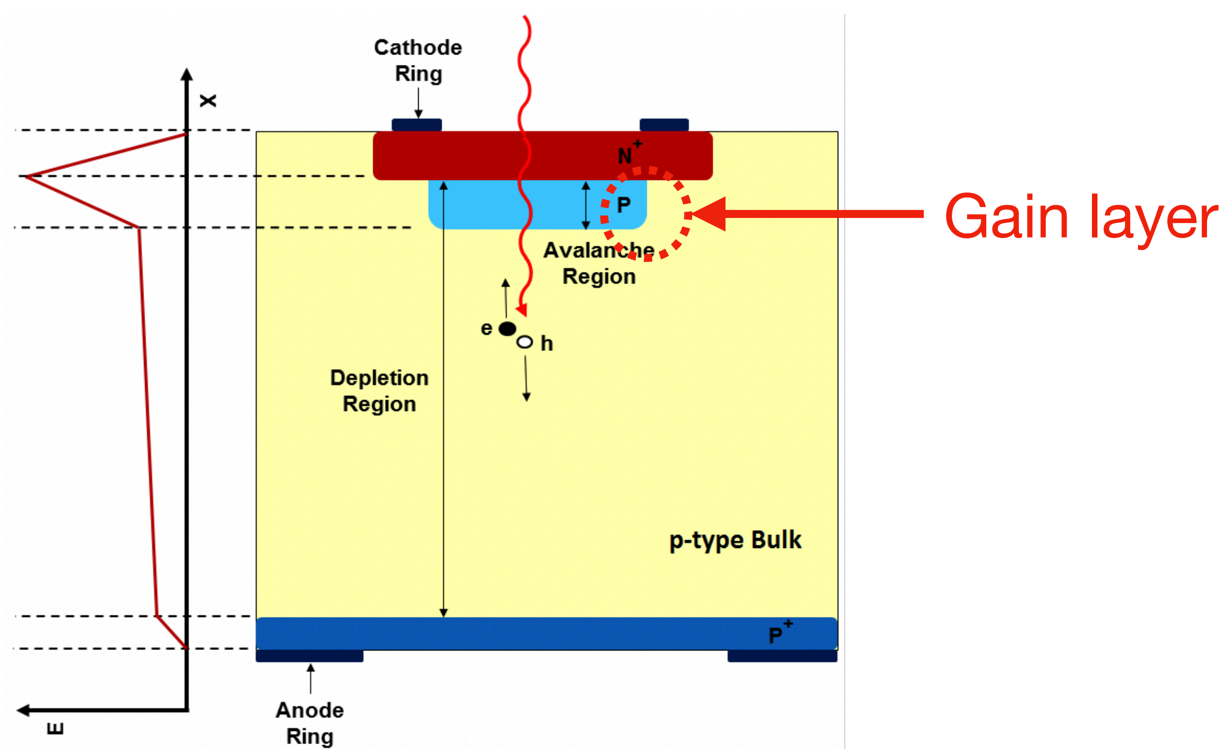
The High-Granularity Timing Detector(HGTD) for the ATLAS Phrase-II Upgrade

Motivation and Technique



- In the HL-LHC, Pile-up density would get so high that track to vertex association would be very hard, especially in the forward region
- Having a timing detector in forward region would allow us make the matching in "4-D" space.
- A novel technology: LGAD (**Low-Gain Avalanche Detector**), which have promising S/N and σ_t by inducing an internal gain layer.





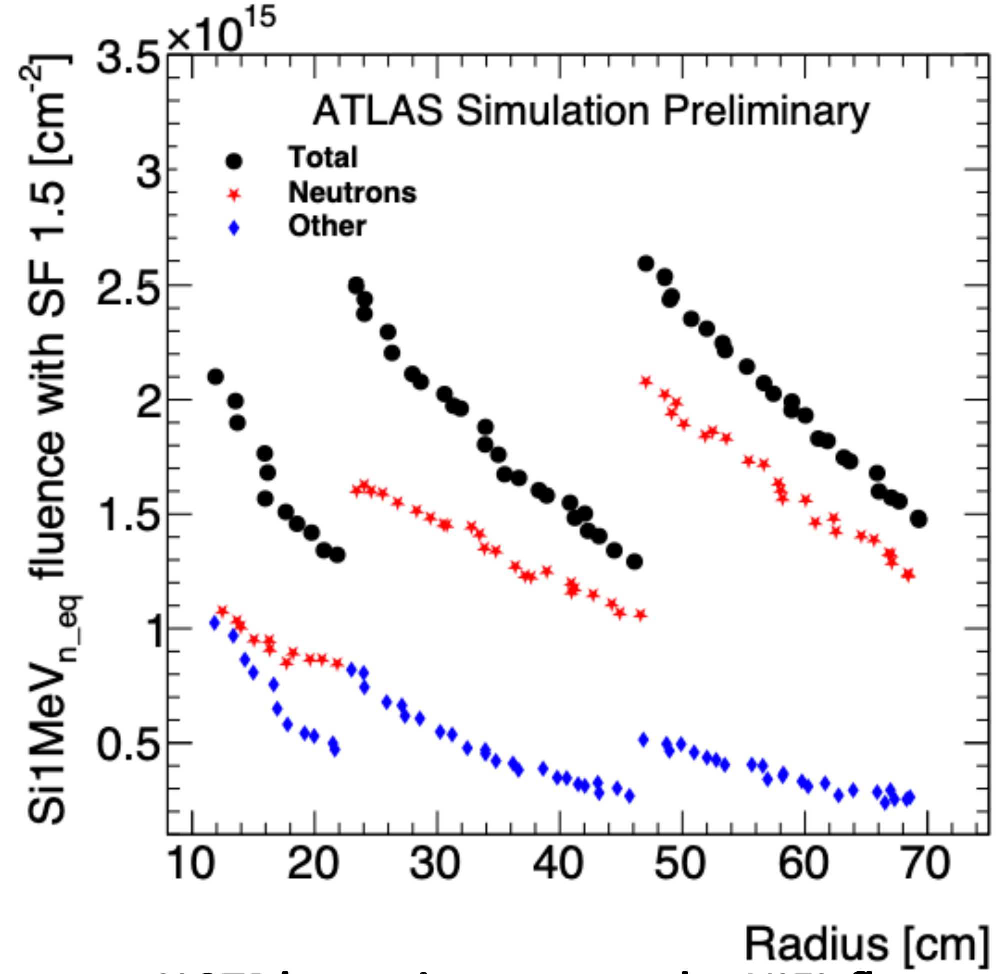
- σ_t ~30 ps per track

larger gain
↓
faster rising time and larger S/N
↓
better time resolution

LGAD Sensor R&D

Challenges on LGAD Design

- **Radiation Hardness:**
  - Acceptor removal[1]:
    acceptors could be "neutralized" by the defects created by the hadron irradiation. (intensively studied by RD50)
  - **Solutions:**
    - Narrow and deep implantation of boron
    - Carbon diffusion



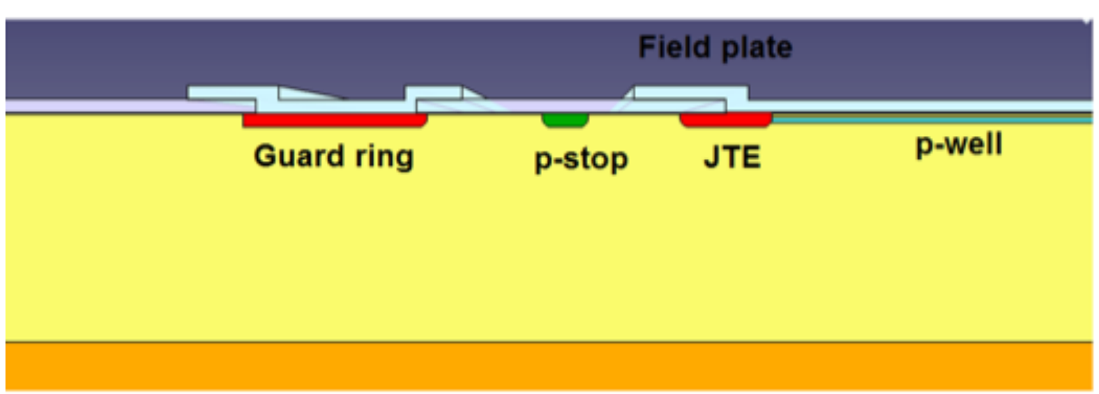
HGTD's requirement on the NIEL fluence

- **Premature breakdown:**
  - Optimization of the peripheral region to improve HV tolerance (to ~800V)
  - Implementation of the structures commonly used in ***power semiconductor device***:
    Guard ring, JTE, Field plate

$$\rho_A(\phi) = g_{eff}\phi + \rho_A(0)e^{-c\phi}$$

Acceptor density with NIEL fluence

➡ ***The I-V and C-V tests are powerful tools to obtain these parameters!***



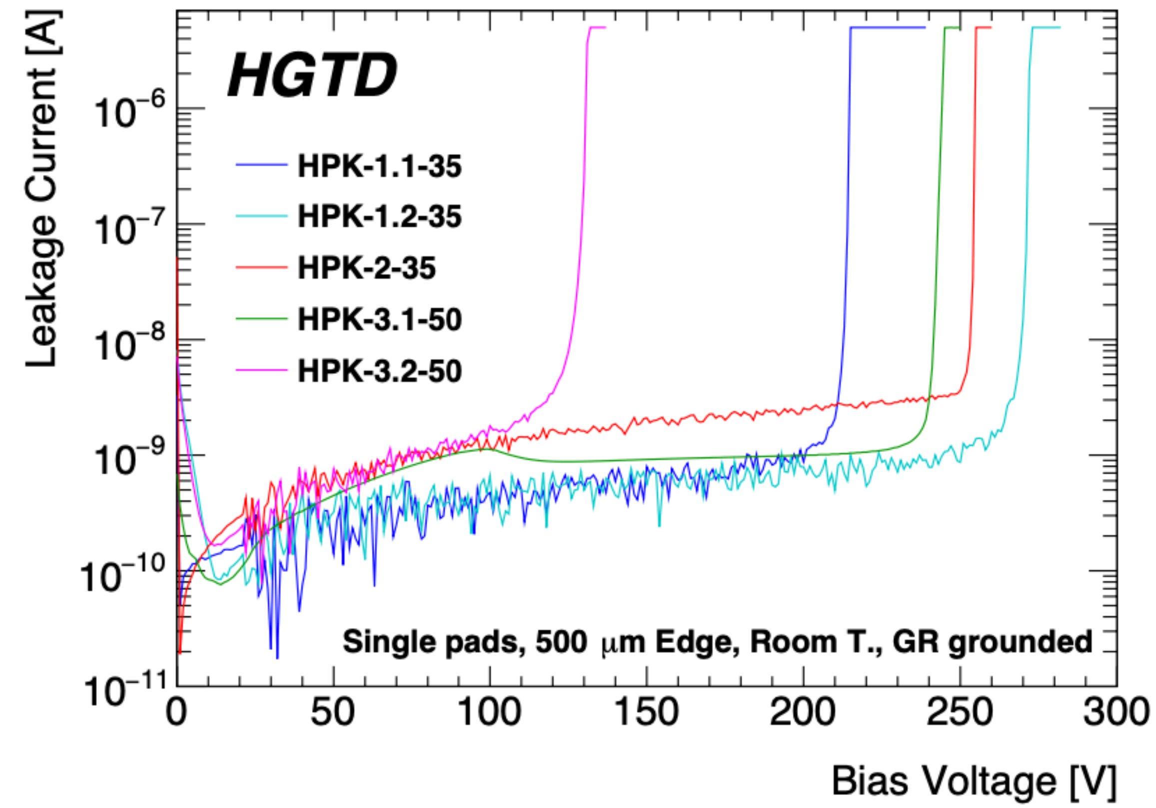
Structures to avoid premature breakdown

HPK Prototype LGAD Probe

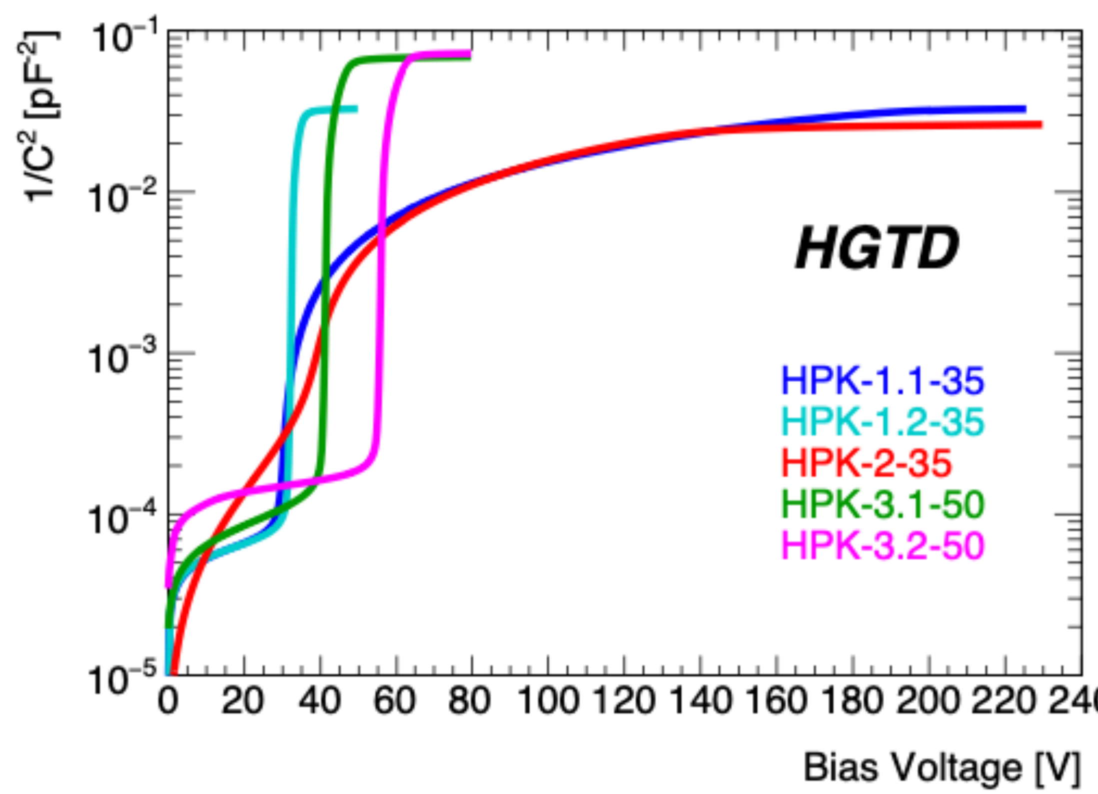
- With **I-V and C-V**:
  - We can extract the parameters like:
    - leakage current
    - breakdown voltage: VBD
    - depletion voltage: VGL(gain layer), VFD(bulk)
    - doping profile
  - Then we can determined the
    - power consumption
    - operation voltage
    - irradiation influence
    - uniformity of the array

Type	V_{GL} [V]	V_{FD} [V]
HPK-1.1–35	31	195
HPK-1.2–35	33	36
HPK-2–35	40	144
HPK-3.1–50	42	49
HPK-3.2–50	56	64

Measured depletion voltages (VGL,VFD) of different HPK prototype LGAD

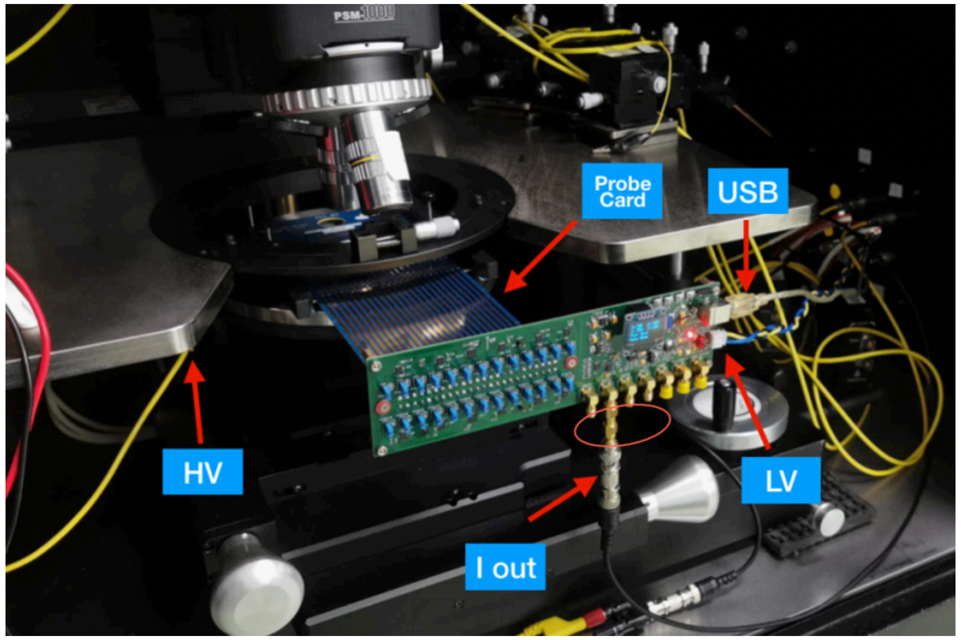


I-V curves of different HPK prototype LGAD

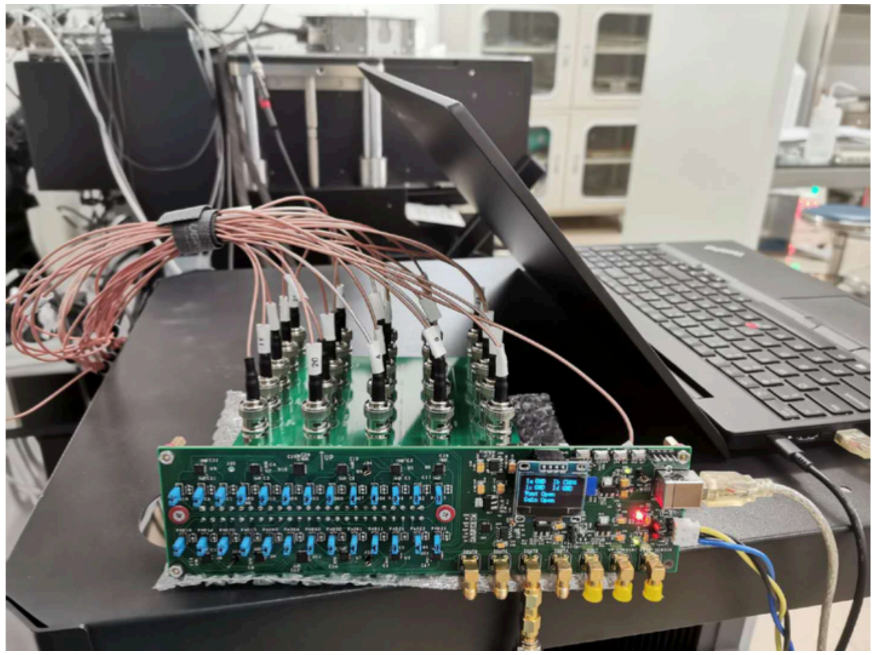


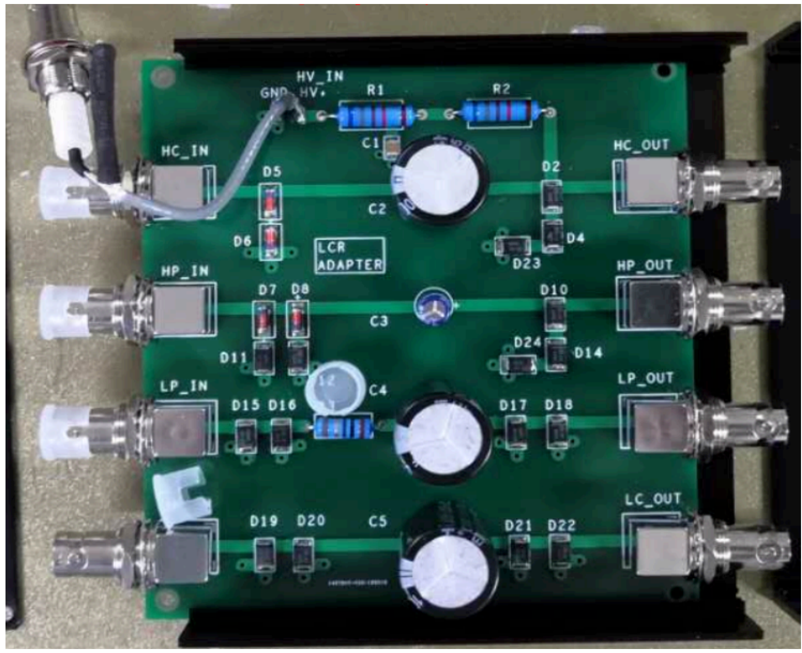
C-V curves of different HPK prototype LGAD

Instruments and Boards

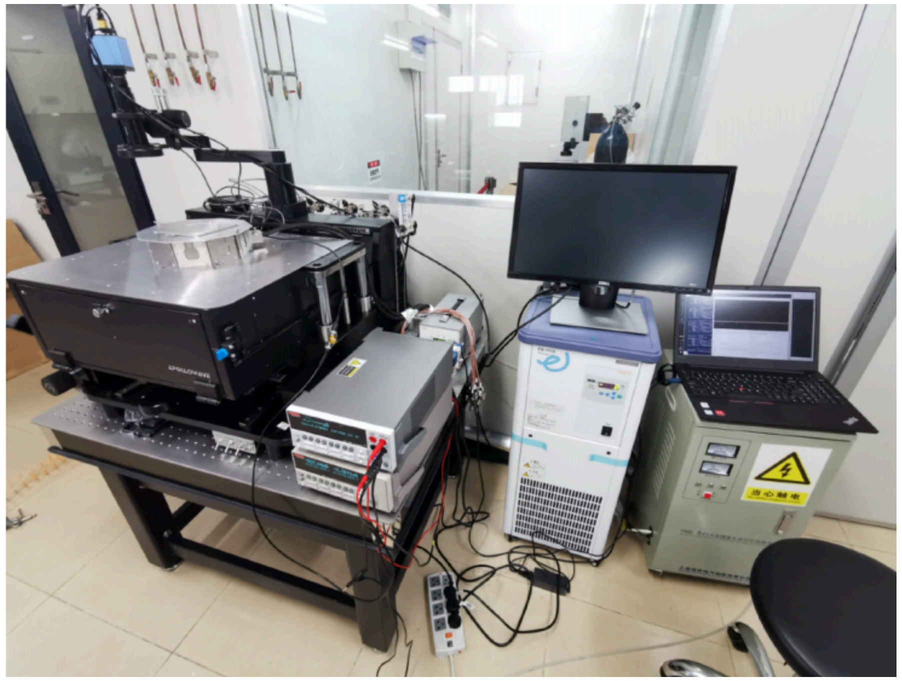


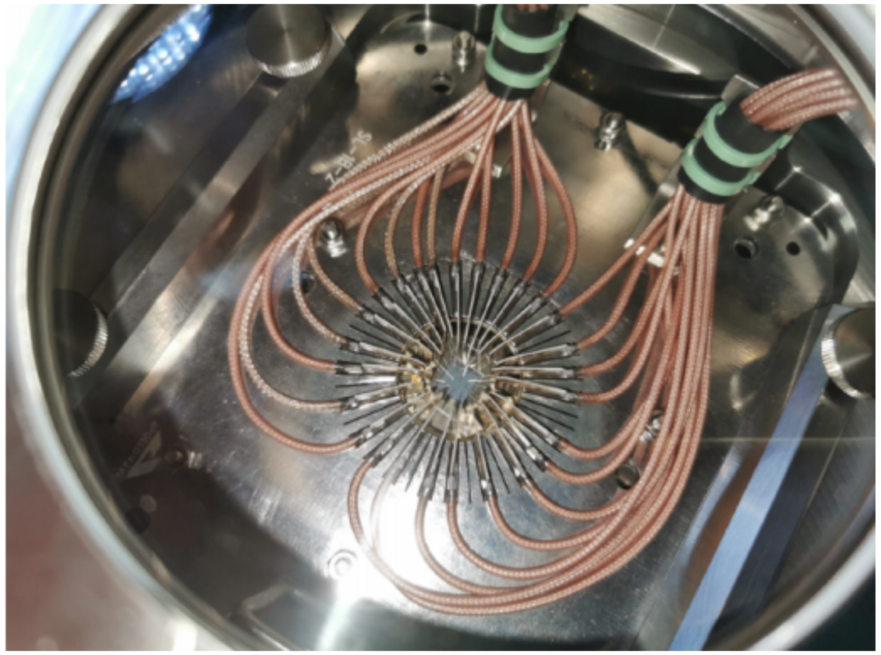
Room T. probe station

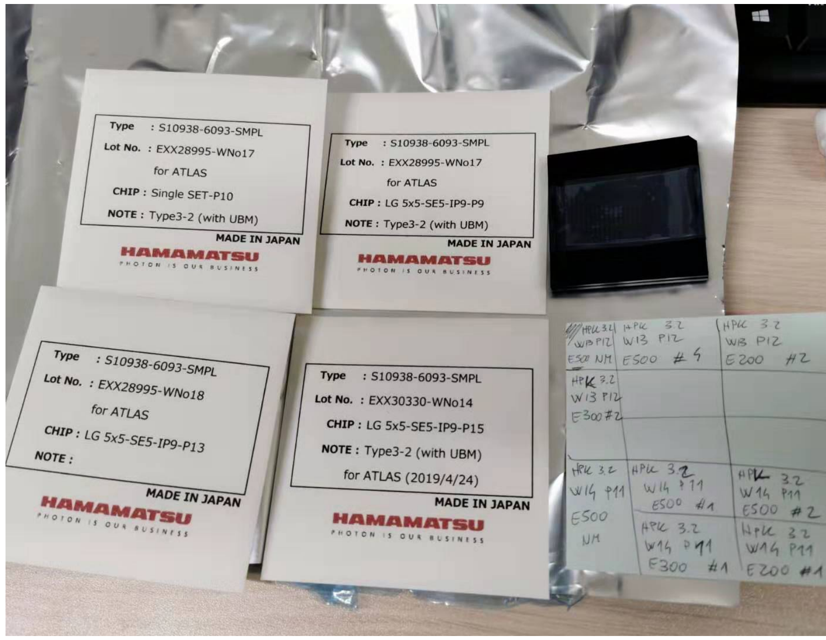

Digital switcher



HV bias module for LCR


New probe system
(cold, dedicated for HGTD)


Customized 5x5 probe card

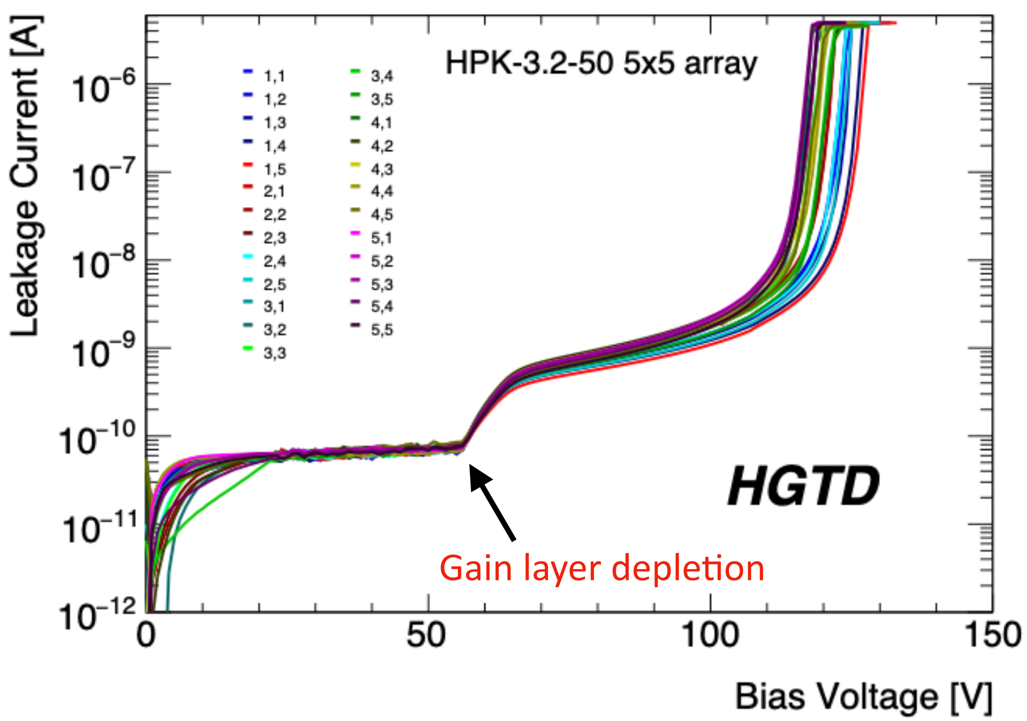


Hamamatsu LGADs with
different structure and size

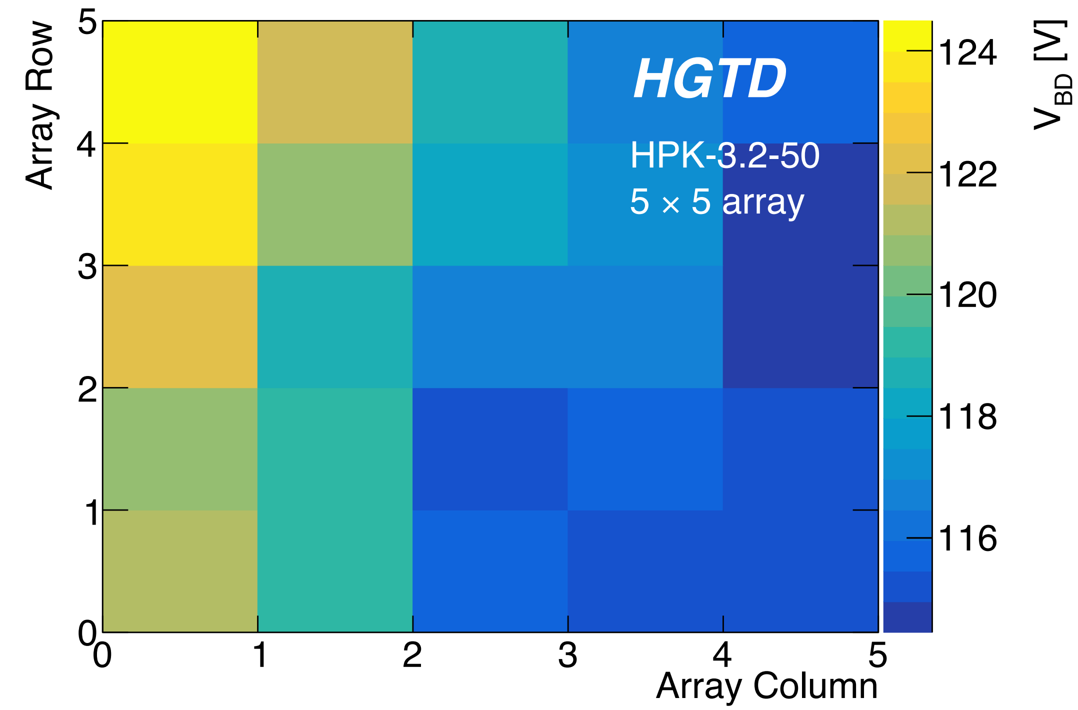
HPK 5x5 LGAD Array Test

I-V curves on the full 5x5 array

I-V →



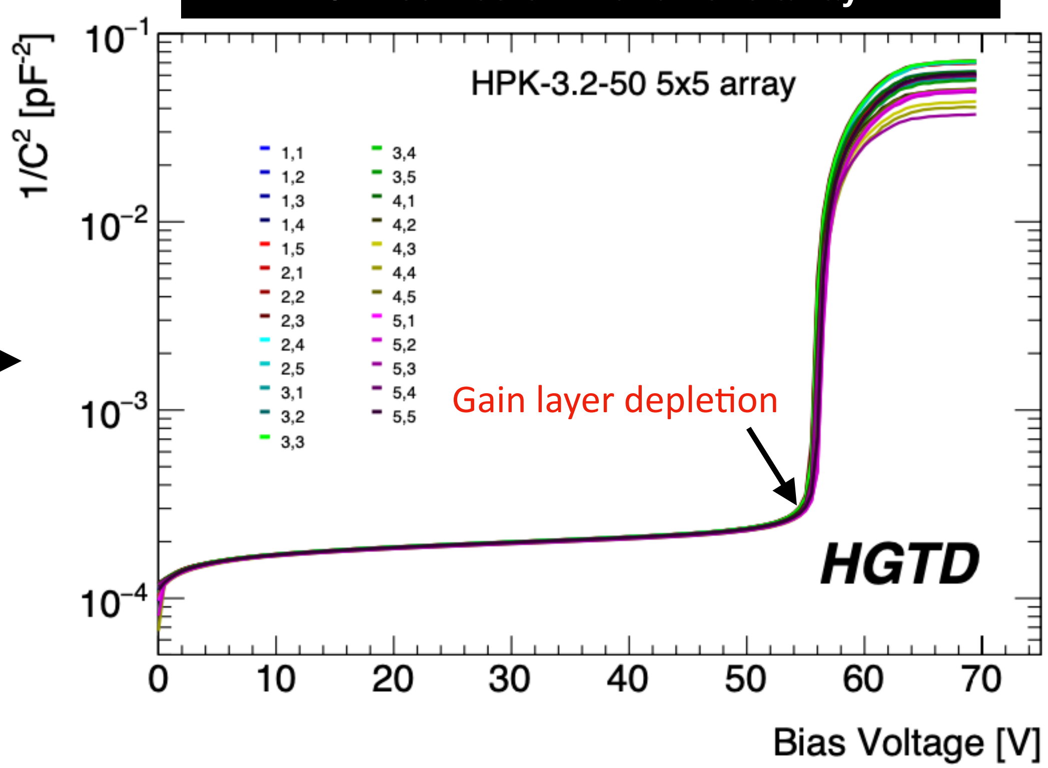
Distribution of the breakdown voltage



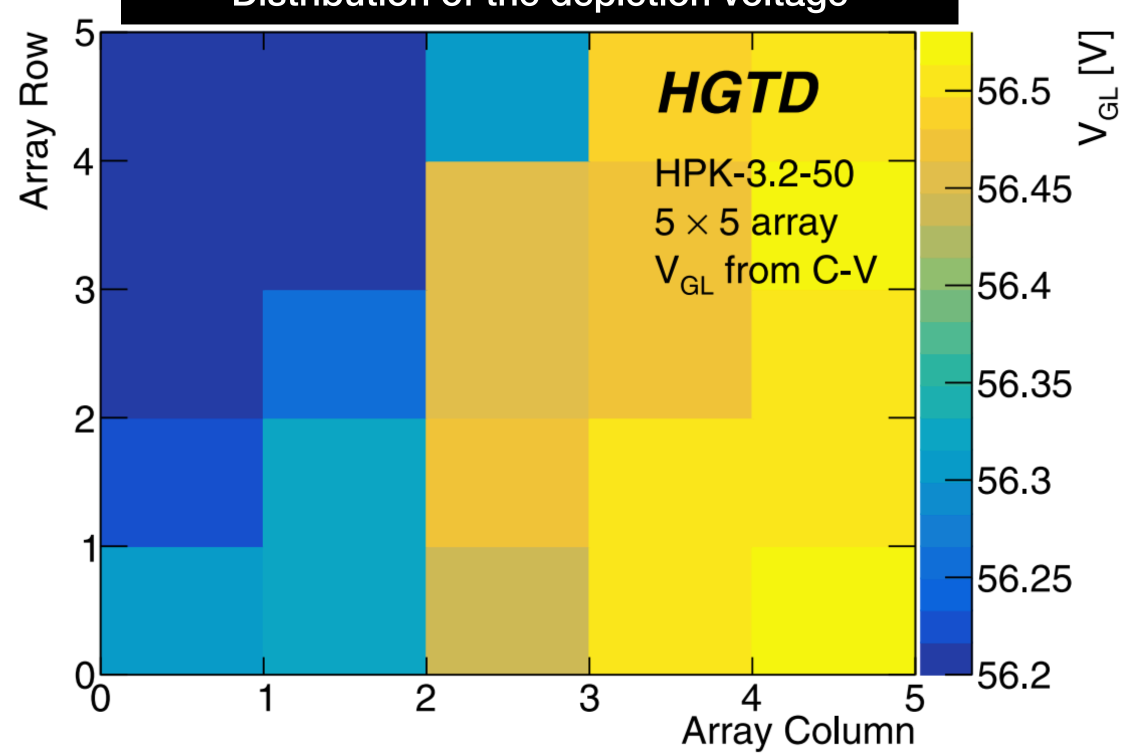
VBD

C-V curves on the full 5x5 array

C-V →

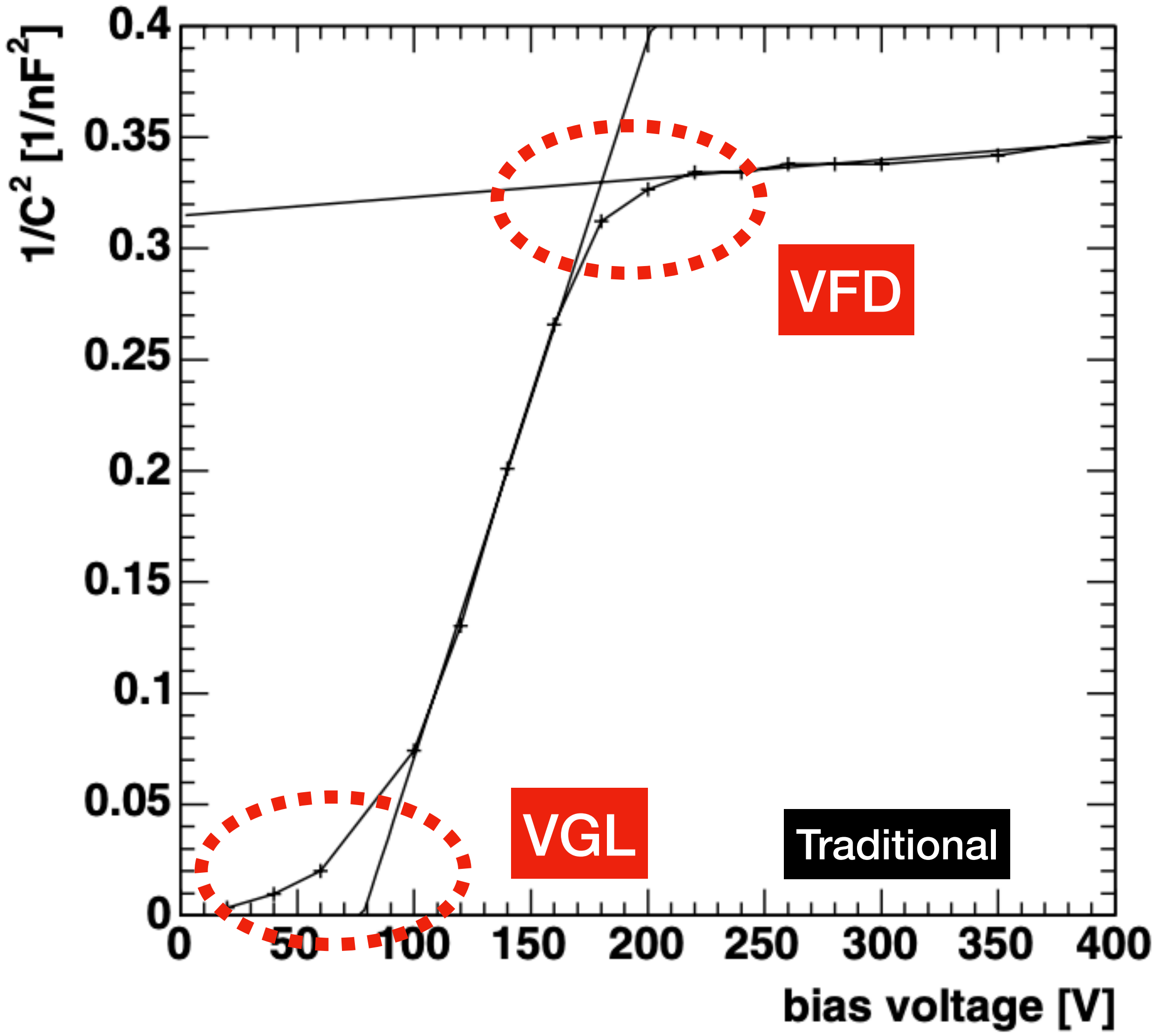


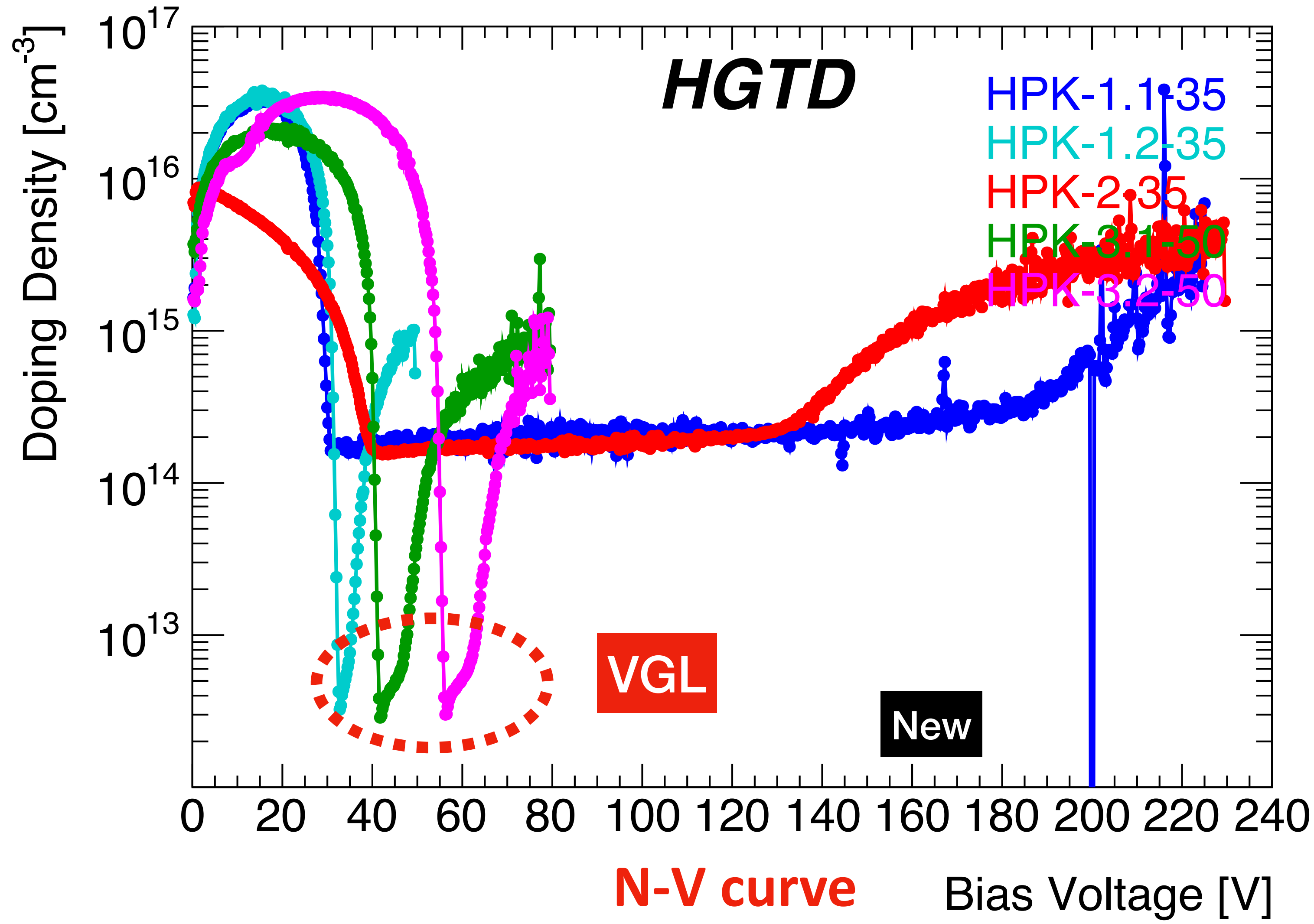
Distribution of the depletion voltage



VGL

VGL Determination Methods





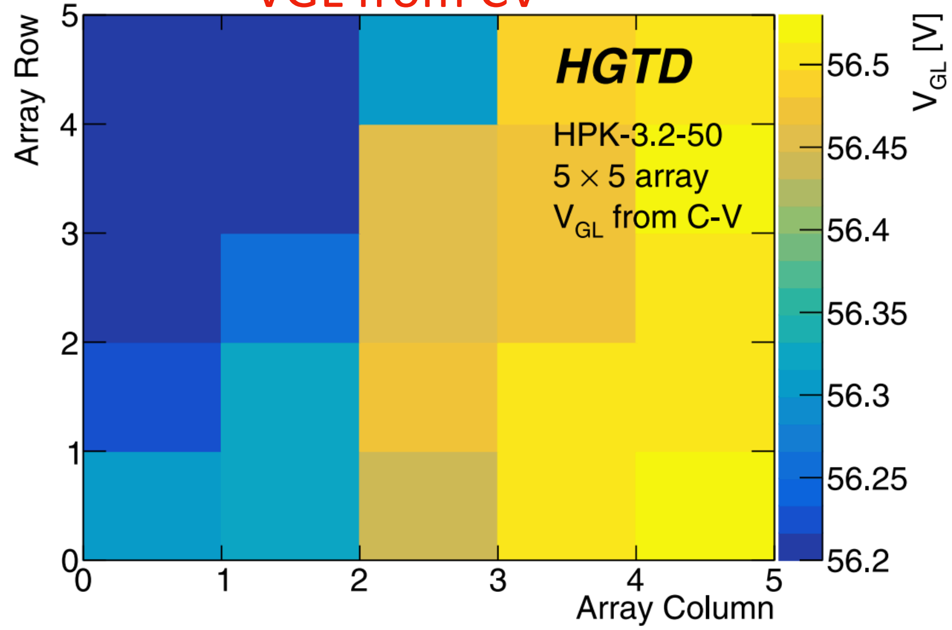
- *Traditional*: The turning points are determined by **extrapolating the adjacent segments** before and after the transition region and finding the intersections of the extrapolations.

- *New*: We use the minimum point on the "Doping density- Bias voltage"(N-V) curve to determine the **VGL** and obtained promising results on HPK-1.2, HPK-3.1 and HPK-3.2

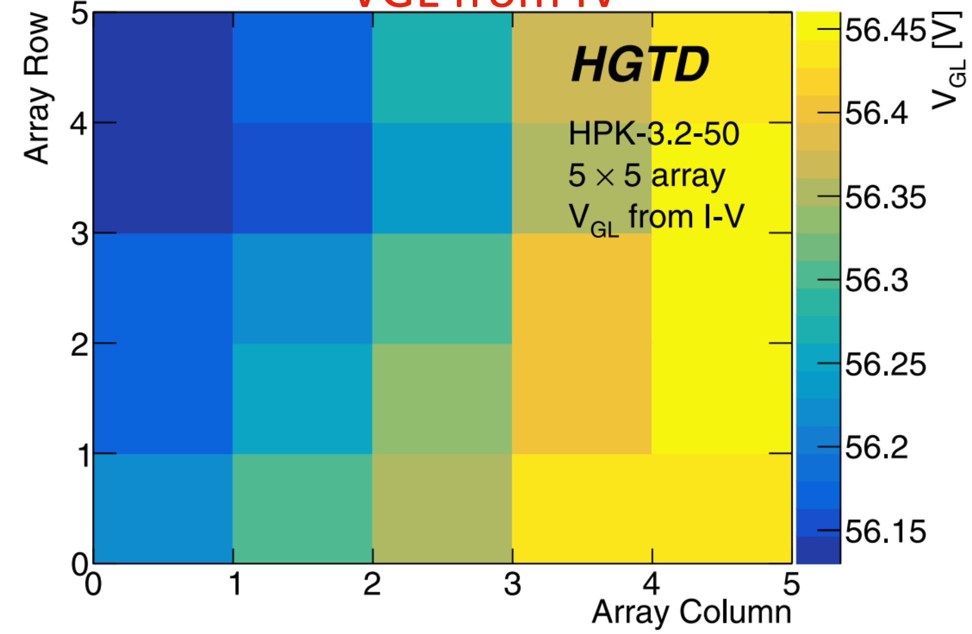
The new method is expected to works better in High-resist. wafer and Epi. wafer

Uniformity of the Gain Layer

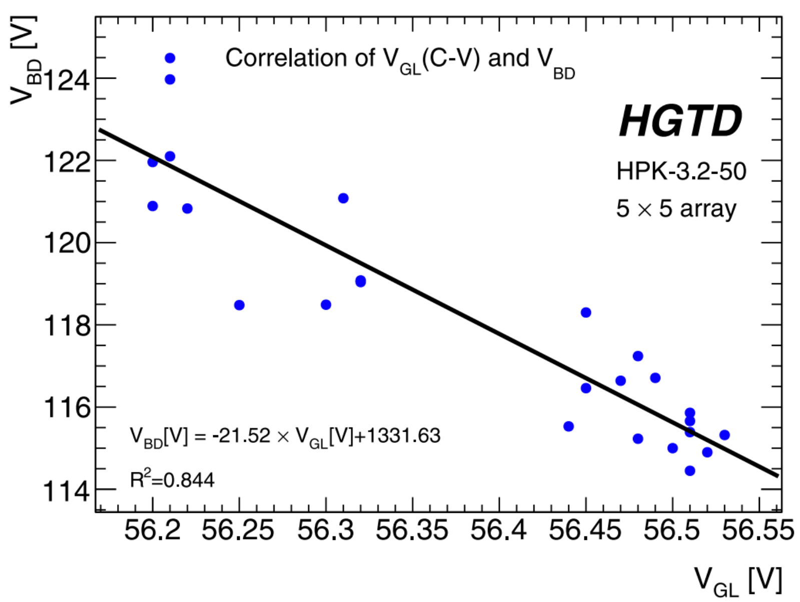
VGL from CV

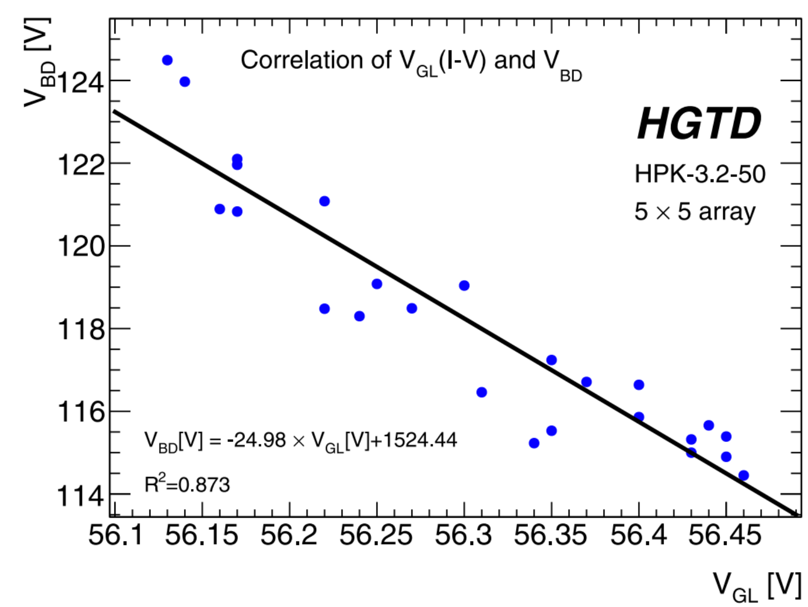


VGL from IV



Correlations between VBD and VGL





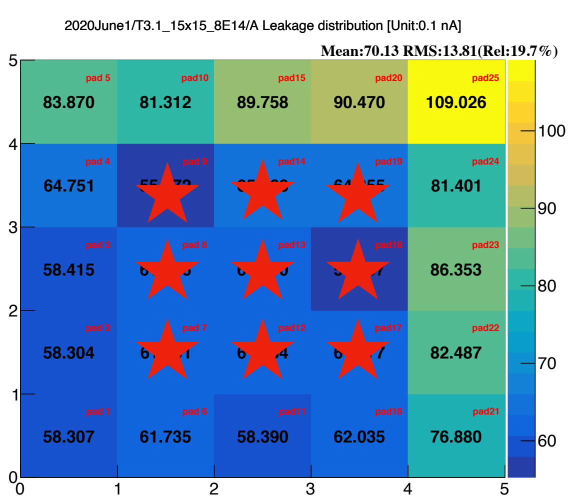
Method	V_{GL} from C-V	V_{GL} from I–V	V_{BD}
Mean value [V]	56.38	56.31	118.12
RMS/Mean ×100%	0.22%	0.19%	2.48%

Finally, a 0.2% variation on the boron implantation dose is observed!

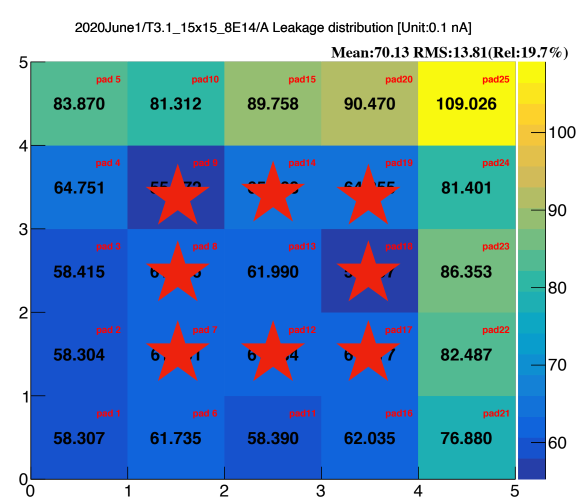
Impact of Floating Pad Study

- ***TDR referees*** have concern about the **floating pads** influences to the whole array during the operation. (punch-through effect)
- We invested it by simulate one disconnected pad and compare the surrounding pads I-V change.
- **Conclusion**: safe, only few extra current is observed. Furthermore, a **picture of the punch-through** with a quantitative model are given.

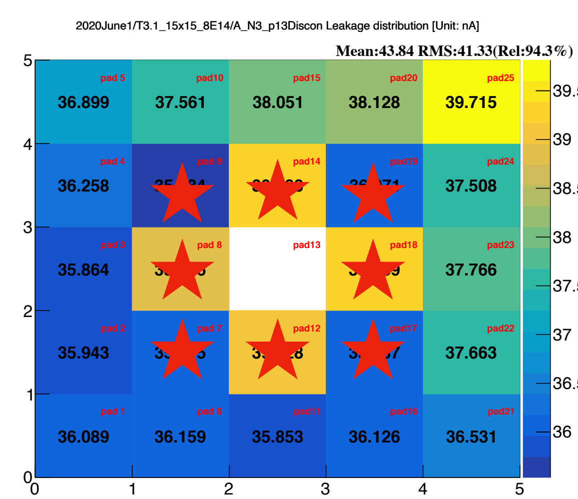
All pads grounded **Central pad floating.**



AllGround sum. 9 pads



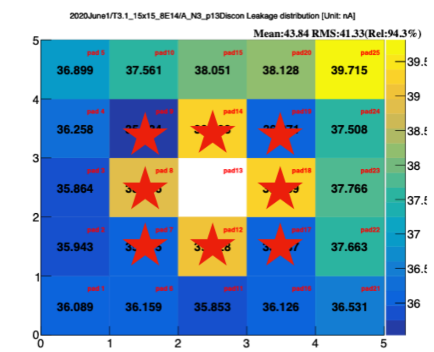
AllGround sum. 8 pads



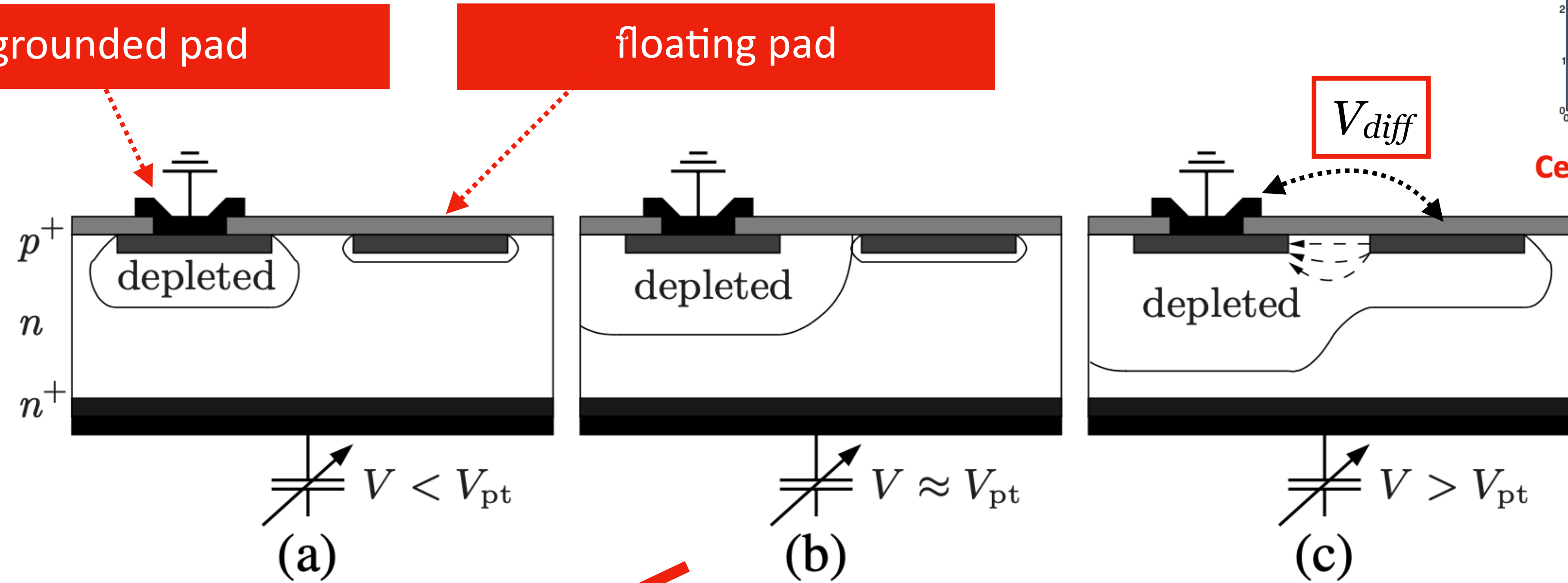
Central DisCon sum. 8 pads

* Tested on a 15x15 array with 5x5 probe card

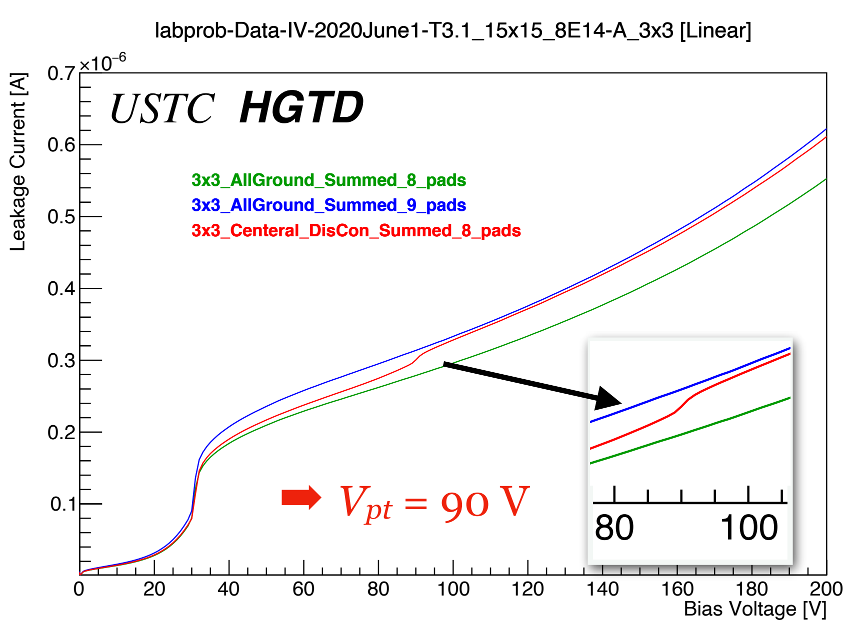
Punch-through Effect

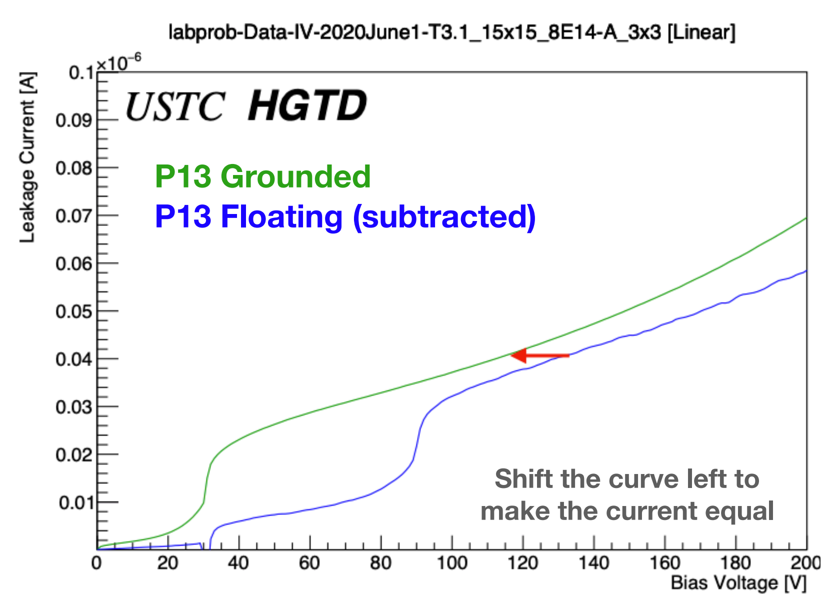


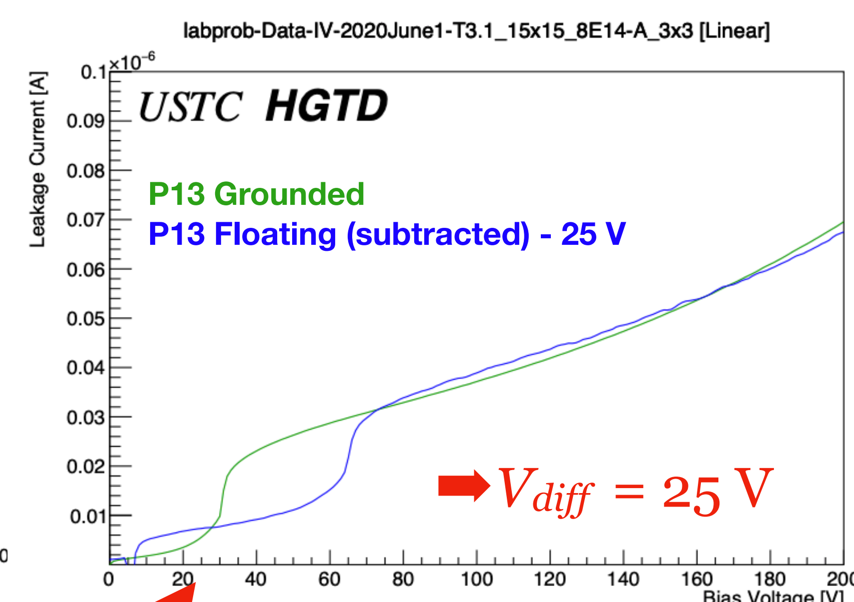
Central DisCon sum. 8 pads



Behaves as an sudden change on the IV curve



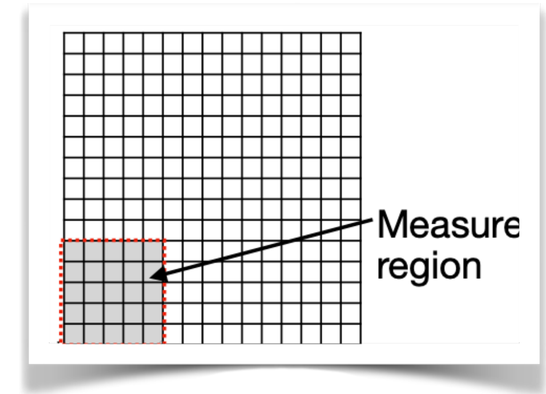




With these curves, we can extract the floating pads' IV by subtraction

Then, we can estimated the real bias on the floating pads by move the curve horizontally and get V_{diff}

Picture of the Punch-through in LGAD



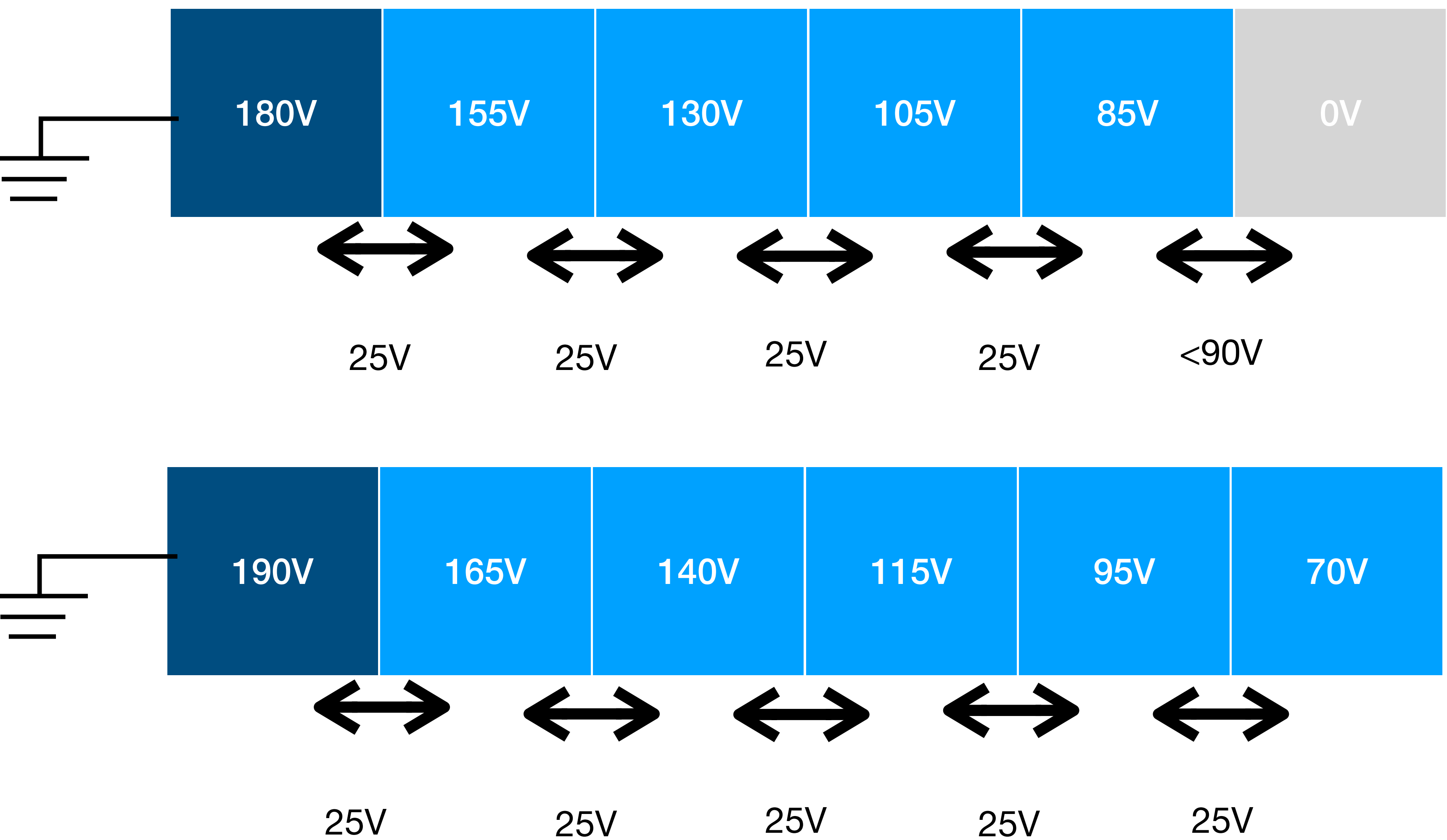
- $V_{pt} = 90\ \mathrm{V}$
- $V_{diff} = 25\ \mathrm{V}$

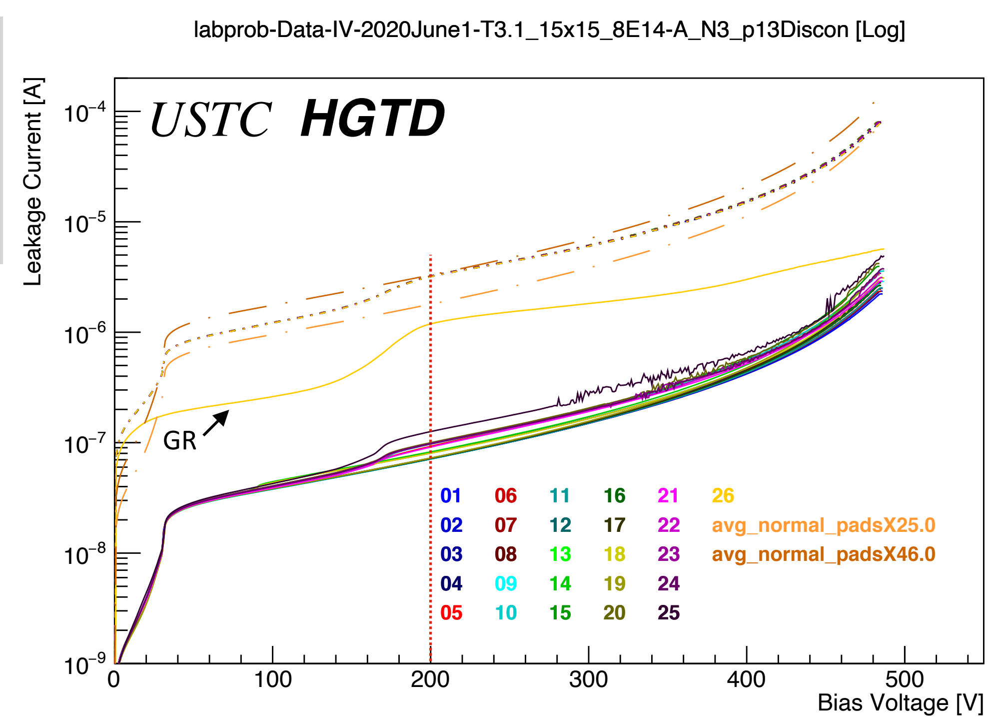
Grounded Pad

Dis.Conn. Pad Biased by Punch-through

Dis.Conn. Pad Not Biased

I-Vs of a 15x15 array corner with 5x5 probe card





The final punch through occurs at ~200V

Prediction:

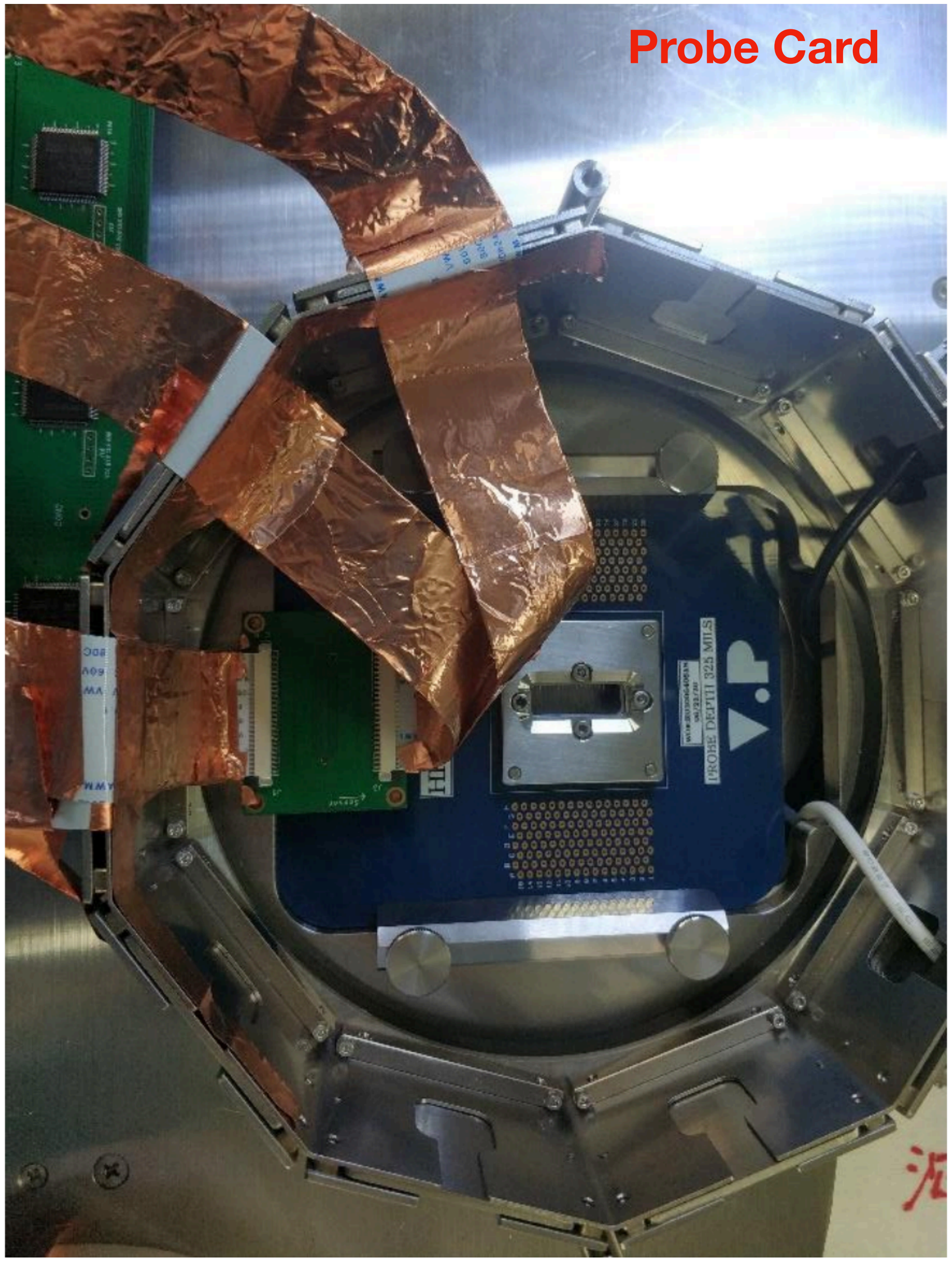
~5 pad distance -> ~215V final punch through

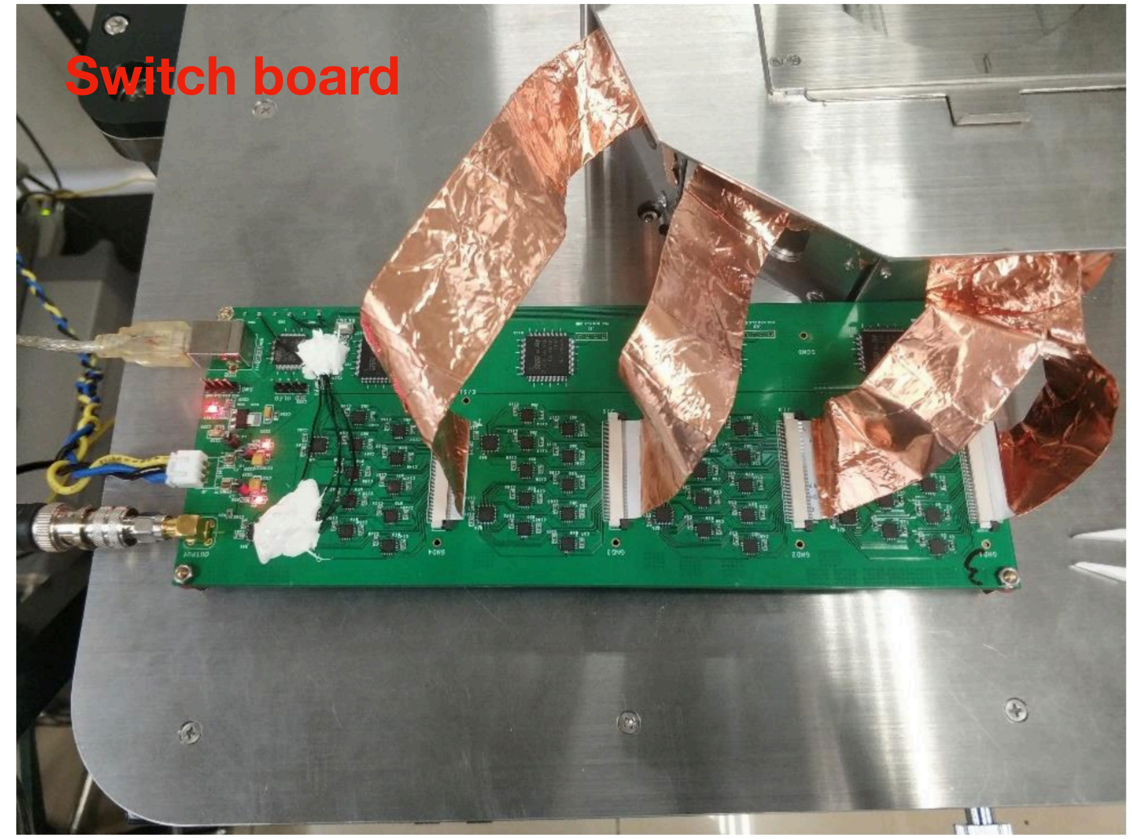
Explained the curves' shape measured form 15x15 array with 5x5 probe card

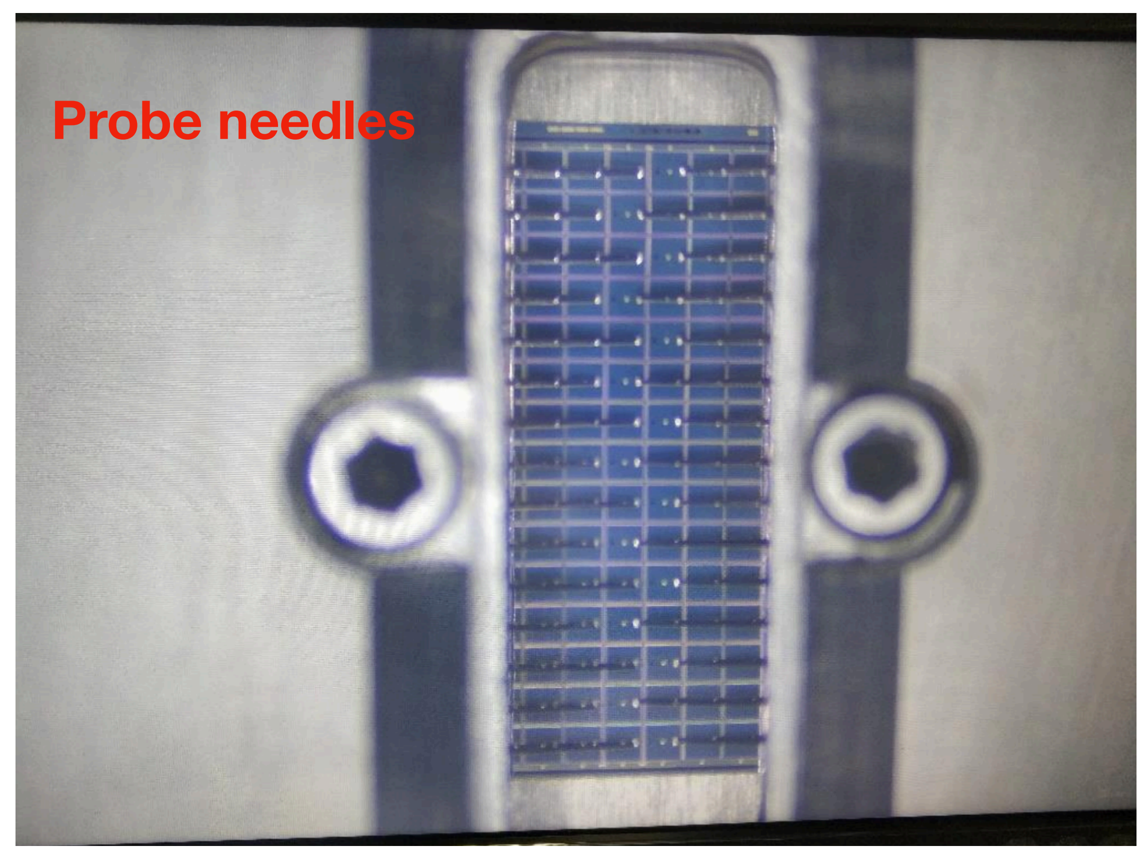
15x15 Array Test System

5x5 array -> 15x15 array

25 pads -> 225 pads!



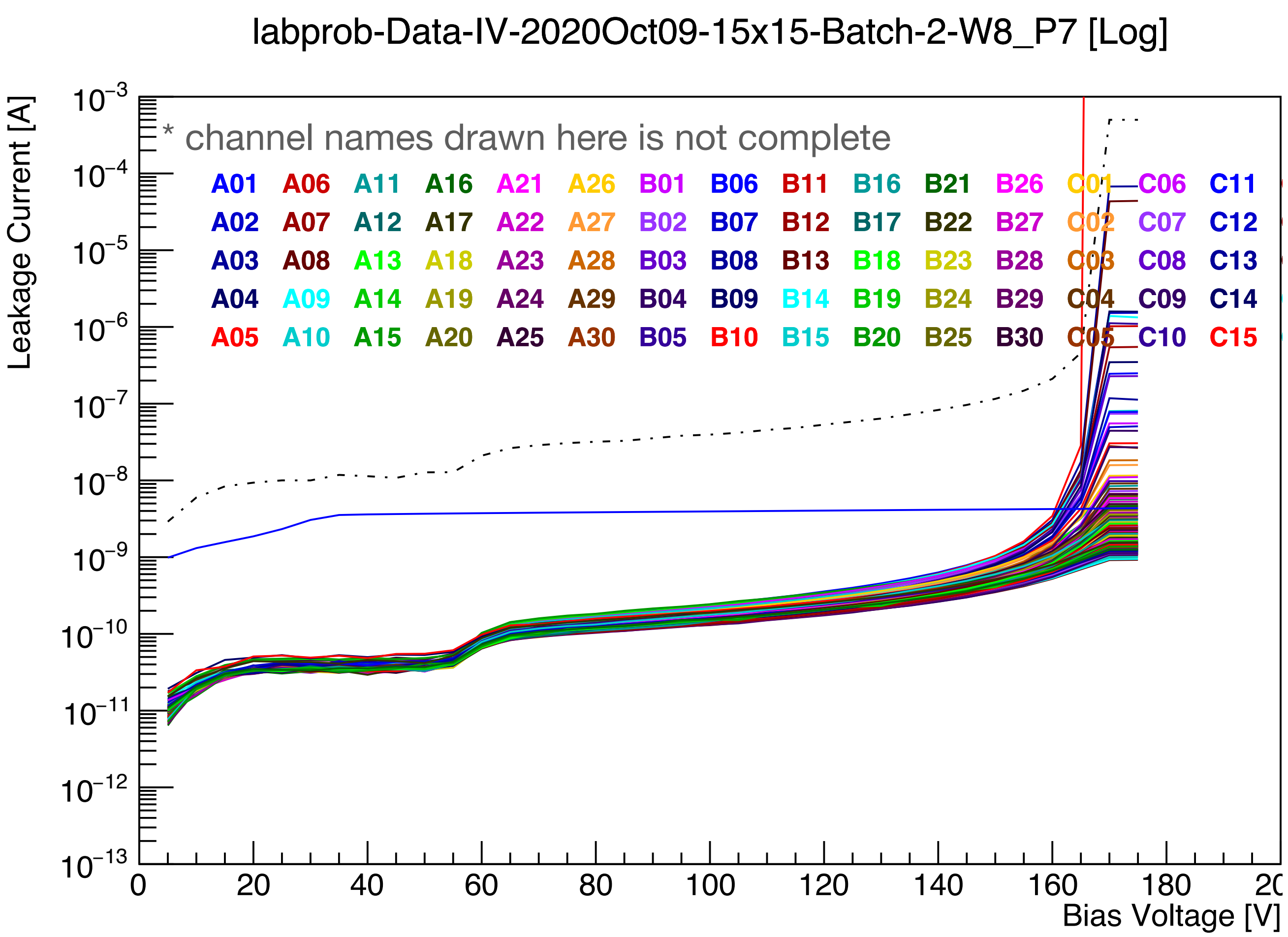




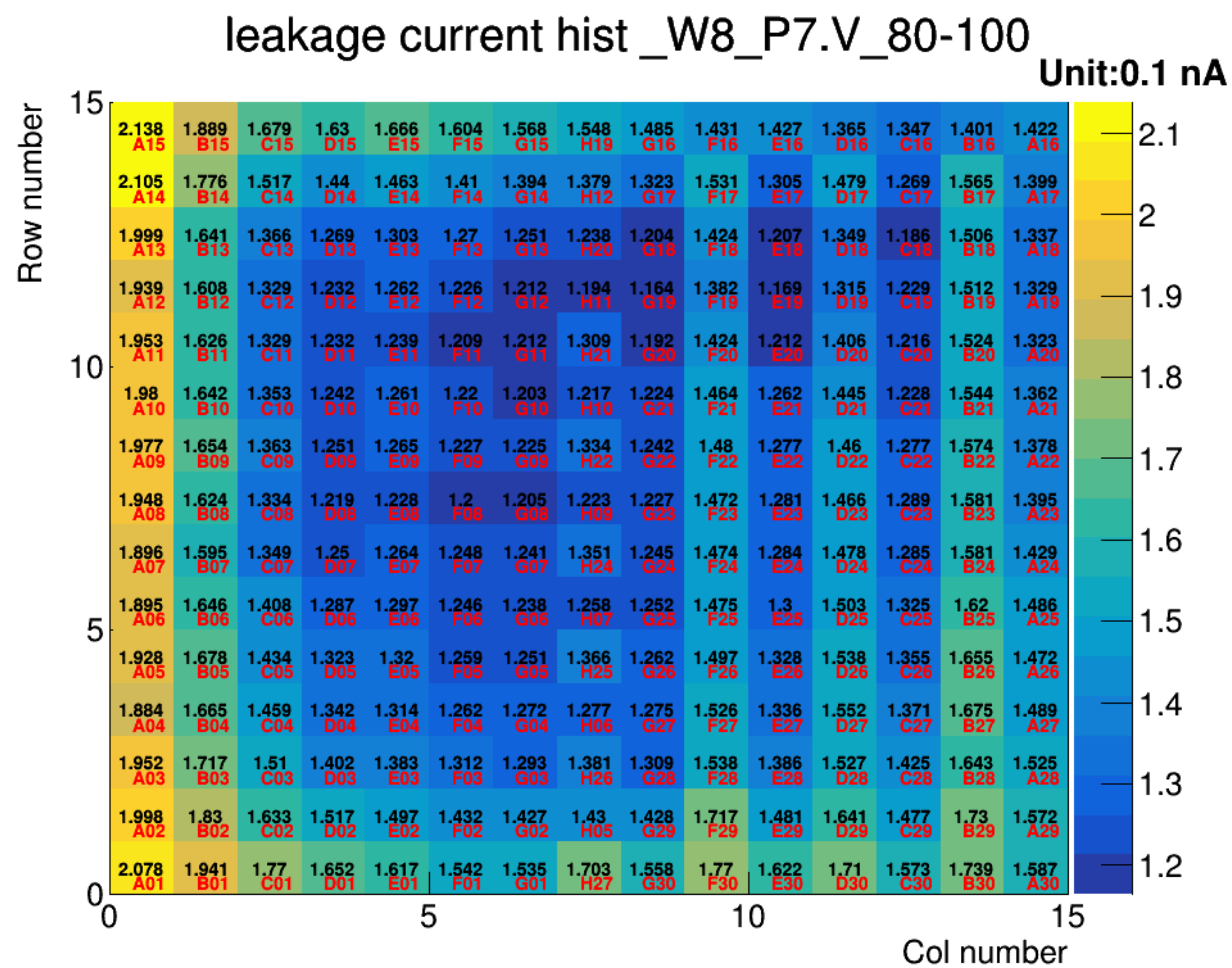
X. Yang, X. Zheng, USTC, The 6th China LHC Physics Workshop

HPK Batch 2 15x15 Array Test

I-V curves



Distribution of the average leakage current



* The variation on column you may find is due to few abnormal chips on the board, it have been identified and fixed later

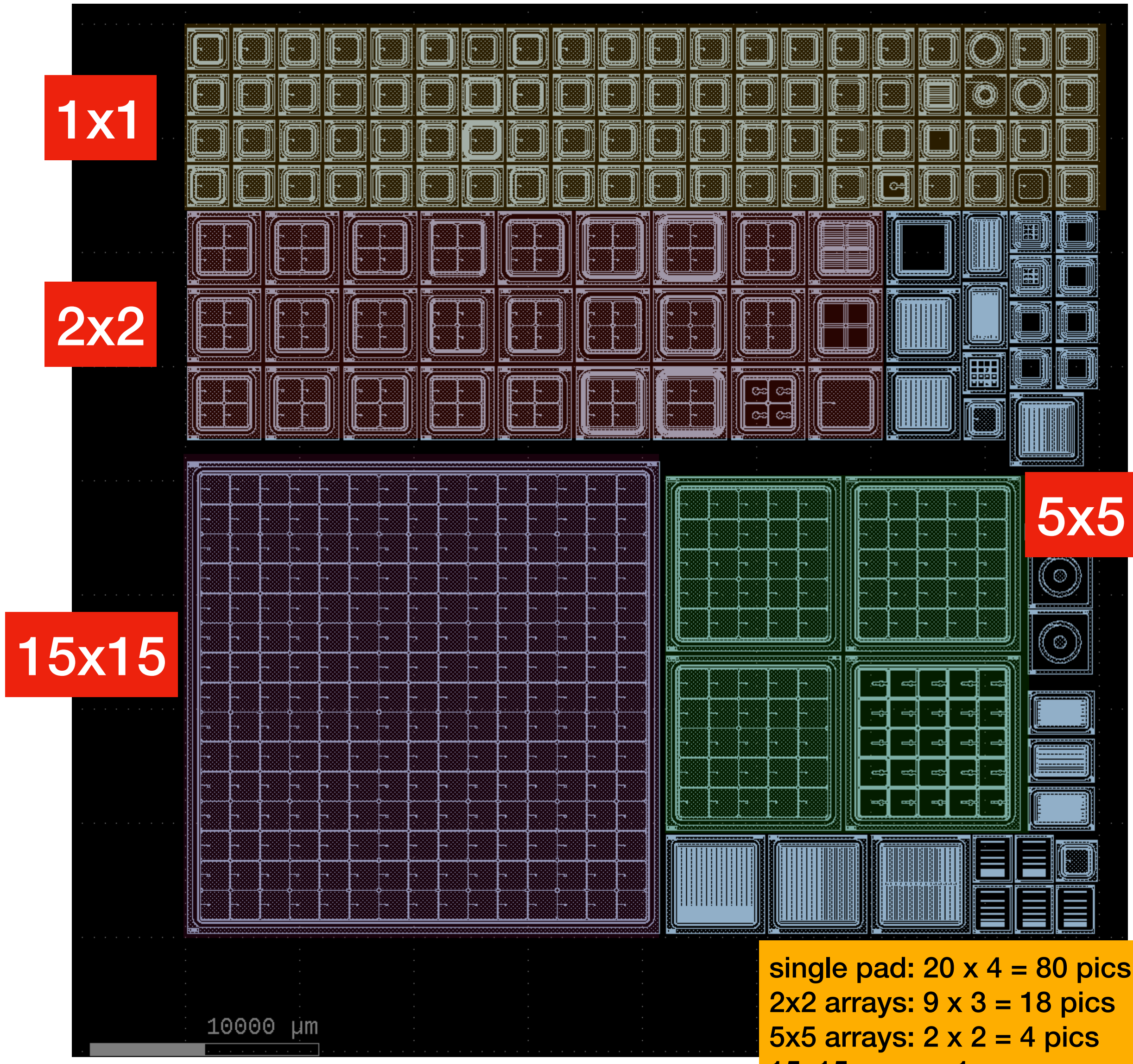
- All channels have good connection and noises are controlled below ~10 pA
- The variation is clearly shown on the leakage current distribution

USTC First Version LGAD Wafers (USTC-1)

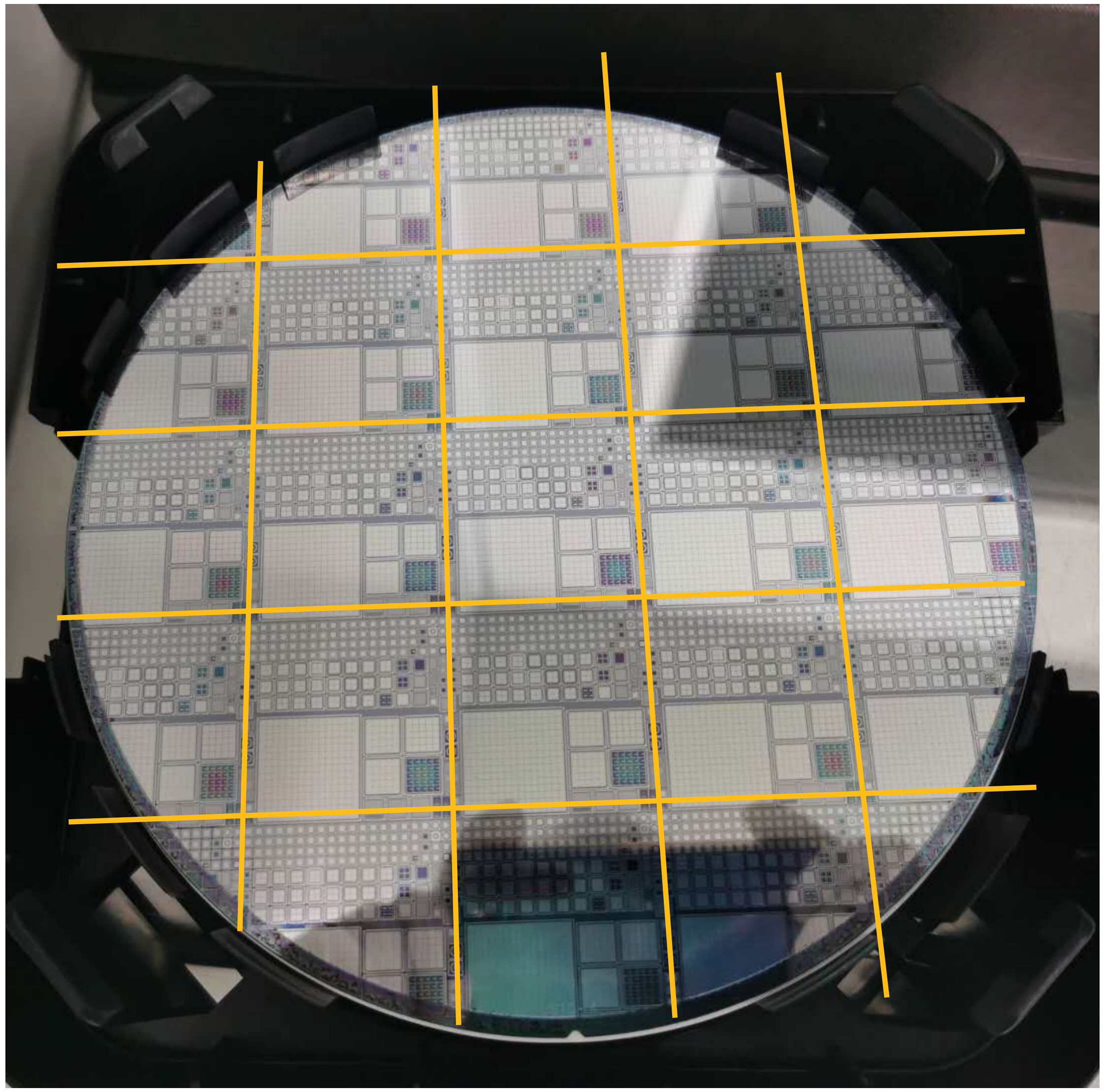
Wafer	Designed VBD [V]	GL.Energy	GL.Dose	Implantation
W1	165	Medium	Medium	B
W2	165	Medium	Medium	B
W3	150	Low	High	B
W4	180	High	Low	B
W5	265	Medium	Low	B
W6	165	Medium	Medium	B+C

- **Designed by: USTC**
  Fabricated by: IME,CAS
- Lot of simulation work are done with TCAD
- Deep gain layer: W3
- Carbon diffusion: W6

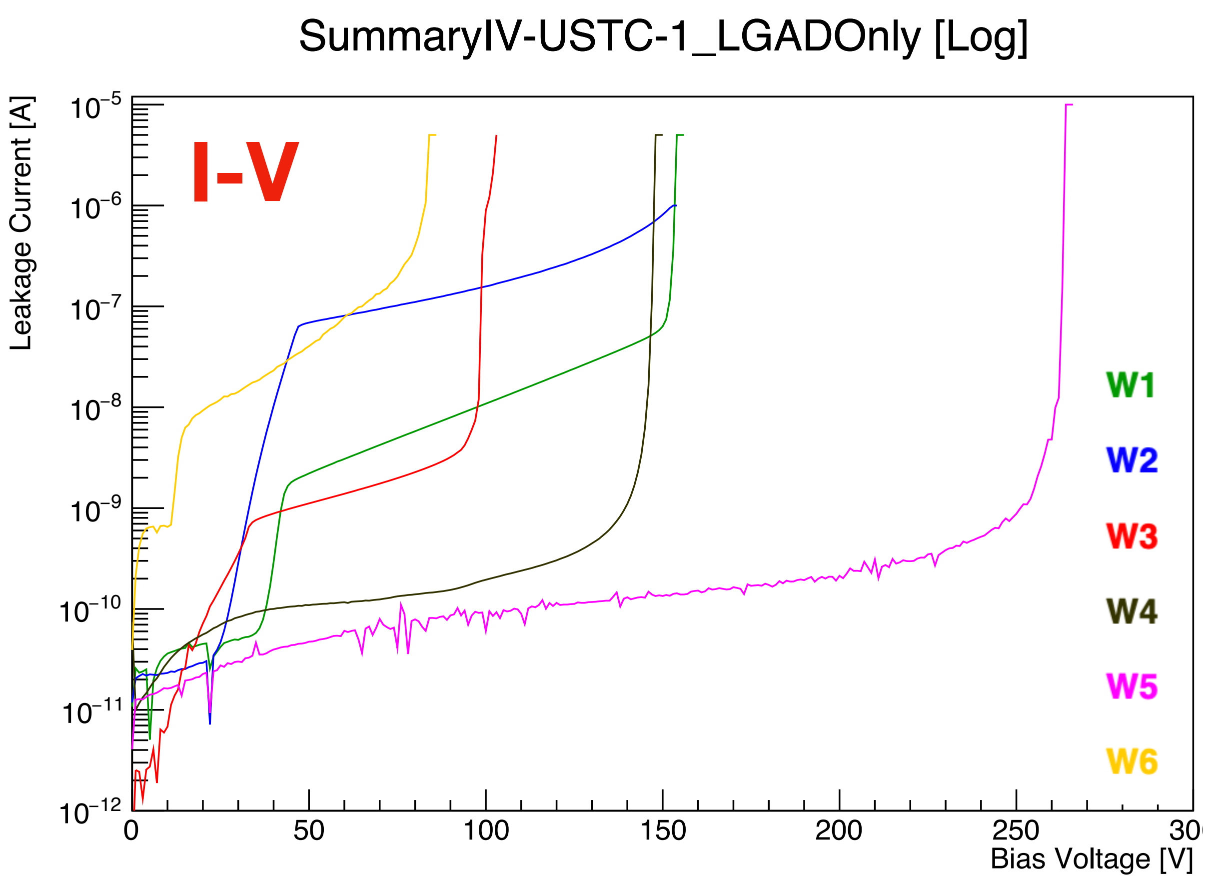
8 inch wafer, with 50 μm Epi. layer.
Stepper size: 40 mm x 40 mm,

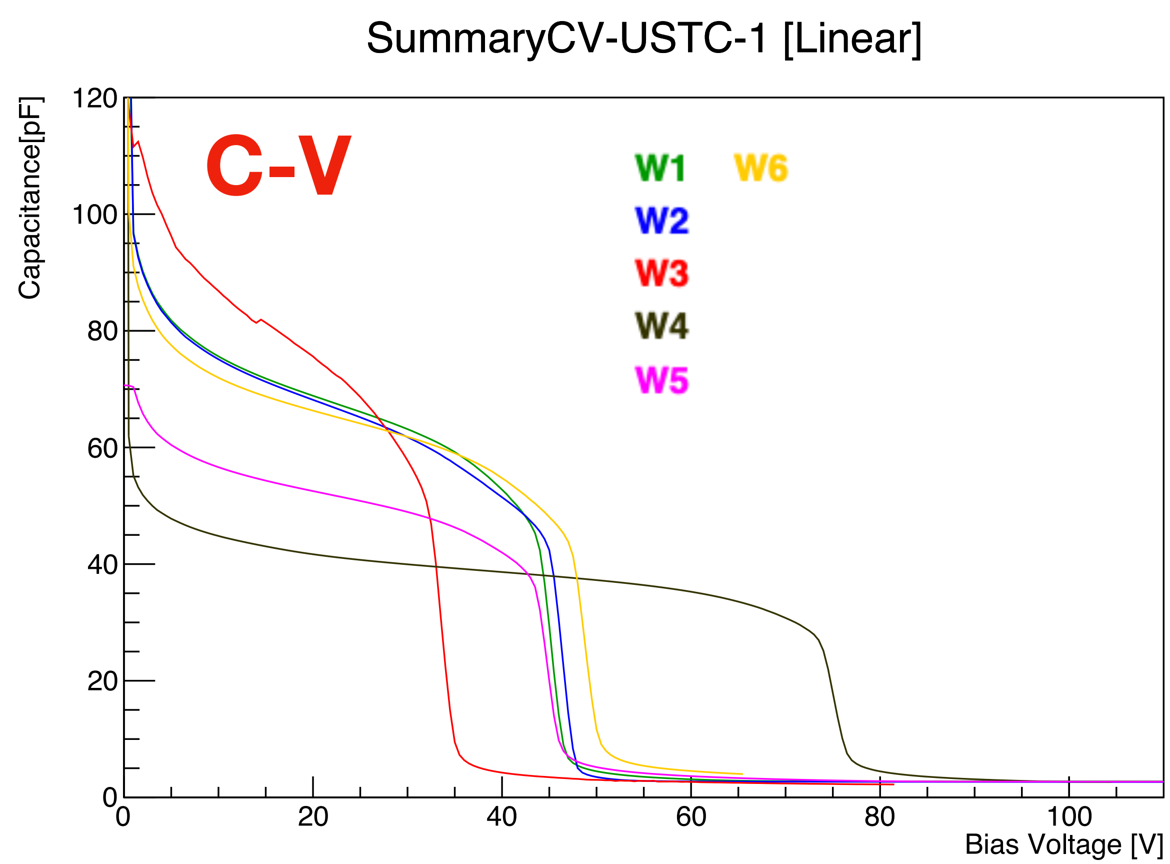


single pad: 20 x 4 = 80 pics
2x2 arrays: 9 x 3 = 18 pics
5x5 arrays: 2 x 2 = 4 pics
15x15 arrays: 1



Summary of the USTC-1 I-V and C-V





Wafe	Designed VBD	GL.Energy	GL.Dose	Implantation	VBD [V]	VGL [V]	VFD [V]
W1	165	Medium	Medium	B	154	45	65
W2	165	Medium	Medium	B	150	46	54
W3	150	Low	High	B	110	34	>70
W4	180	High	Low	B	148	75	100
W5	265	Medium	Low	B	264	45	80
W6	165	Medium	Medium	B+C	84	48	>65

- For the majority of wafers (W1,W2,W4,W5), the measured VBD and VGL agree with the design well.
- The timing performance would be shown in Tao's talk (next)

✳GL.Energy/Dose: Gain layer implantation energy/dose

Summary

I. Characterized the first batch of HPK Prototype with USTC platform, serval results are put in the **TDR** and the **collaboration paper**.

II. Proposed new method for precise **depletion voltage (VGL) determination**

- With the new **N-V method**, we studied gain layer variation on the ~**0.2%** level precision.

III. Built up the **punch-through model** to describe the **floating pad's impact**

IV. Overcome the **large scale connection and readout** challenges to test large arrays (5x5 and 15x15), results are stable and accurate.

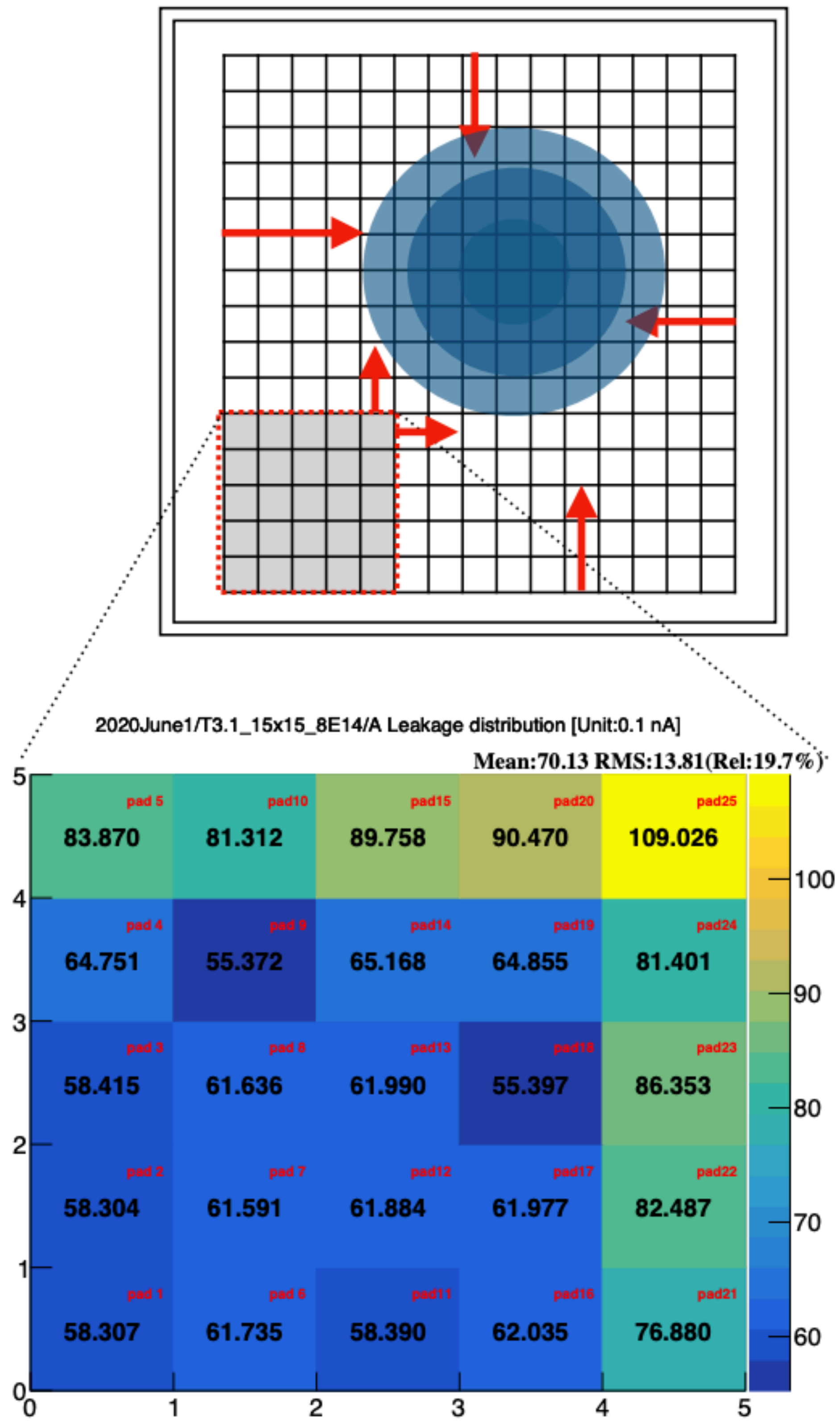
V. Designed and fabricated **USTC-1 LGAD**, the preliminary test result show I-V and C-V of serval wafers meet the expectation.

(i) HGTD TDR: https://cds.cern.ch/record/2719855/files/ATLAS-TDR-031.pdf

(ii) *Layout and performance of HPK prototype LGAD sensors for the High-Granularity Timing Detector*, NIMA, Volume 980, 11 November 2020 https://doi.org/10.1016/j.nima.2020.164379

Backup

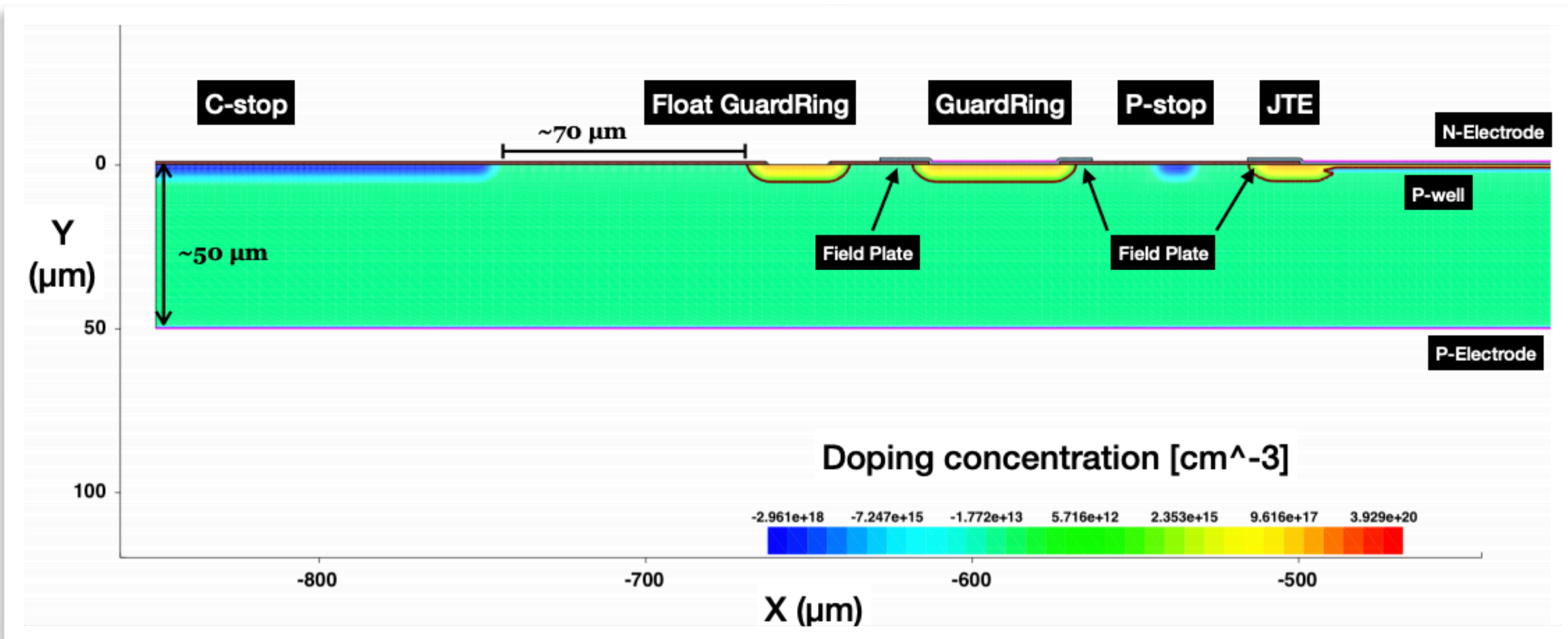
Punch through path

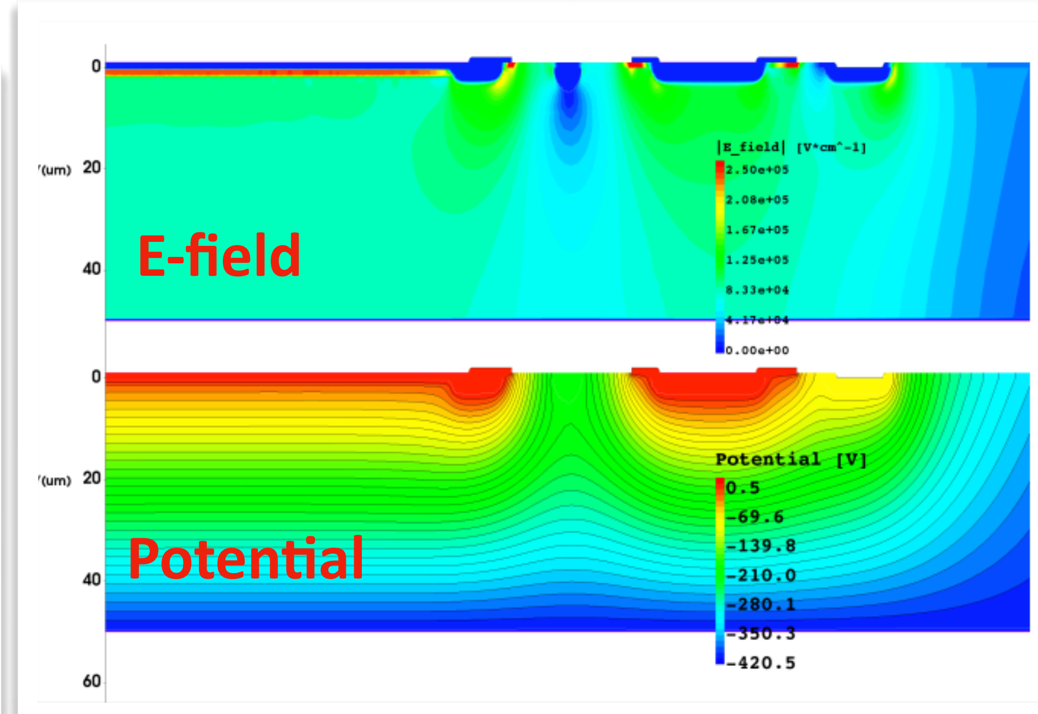


In 15x15 array with 5x5 probe card -> final punch-through needs **5-8 pad distance**

But, the current growth reach maximum at ~5 pads punch through

USTC-LGAD Design with TCAD



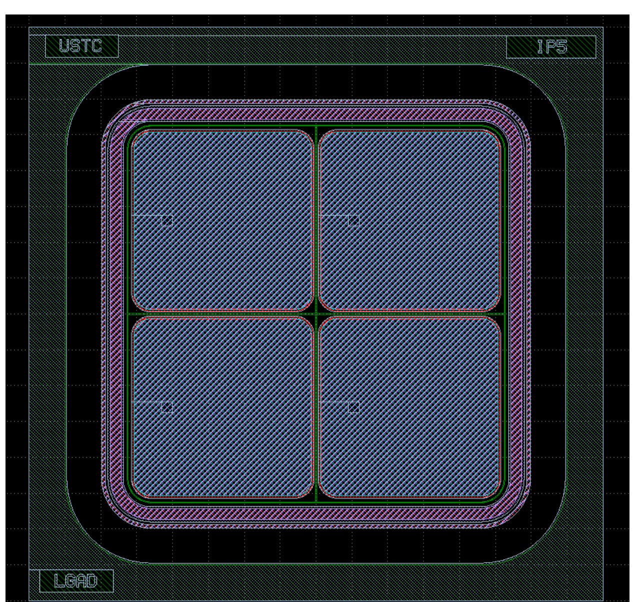


- TCAD structure based on process simulation
- Lots of optimization work done
- Major radiation damage model included

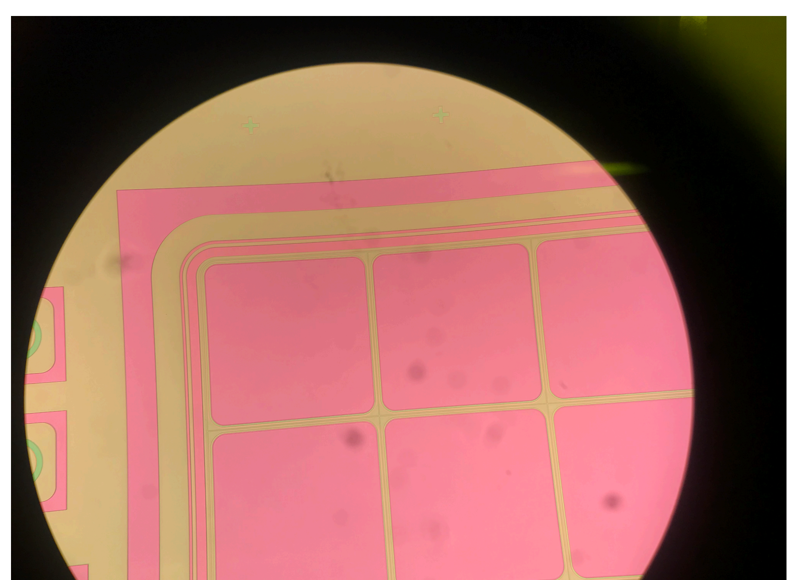
➡**Recommendation:**

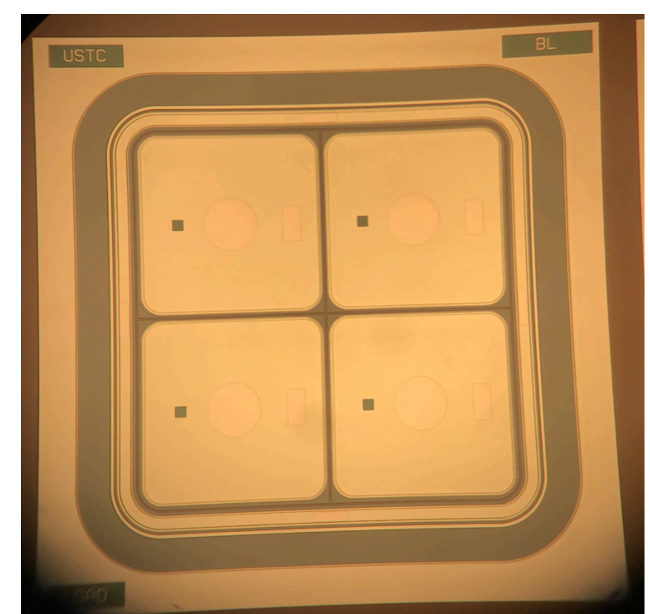
- High resist. substrate: >1kOhm*cm
- High energy boron implantation: at least ~1MeV
- Carbon diffusion on one wafer

Simulation → • **Layout Mask** • **Fab. Process** → **Functional LGAD (USTC-1)**



Designed Mask (2x2 array)





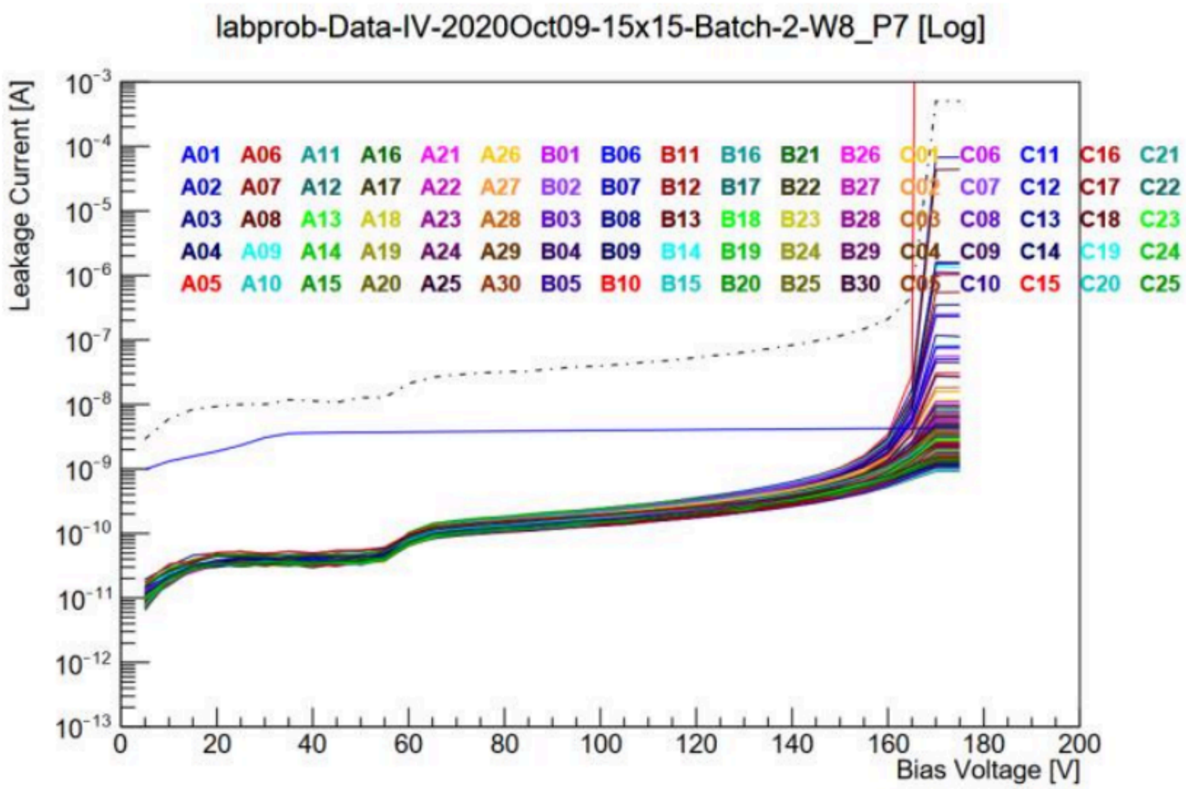
Wafer under fabrication

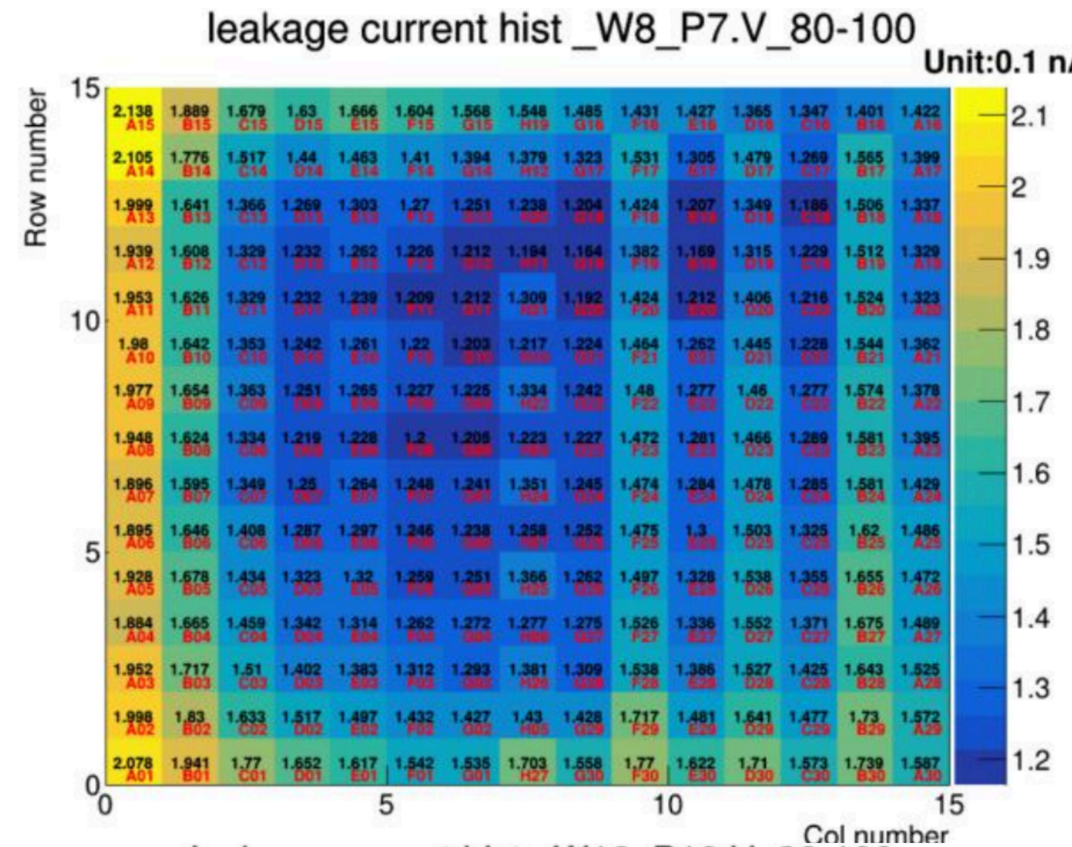
HPK Batch 2 15x15 Array Test

I-V curves

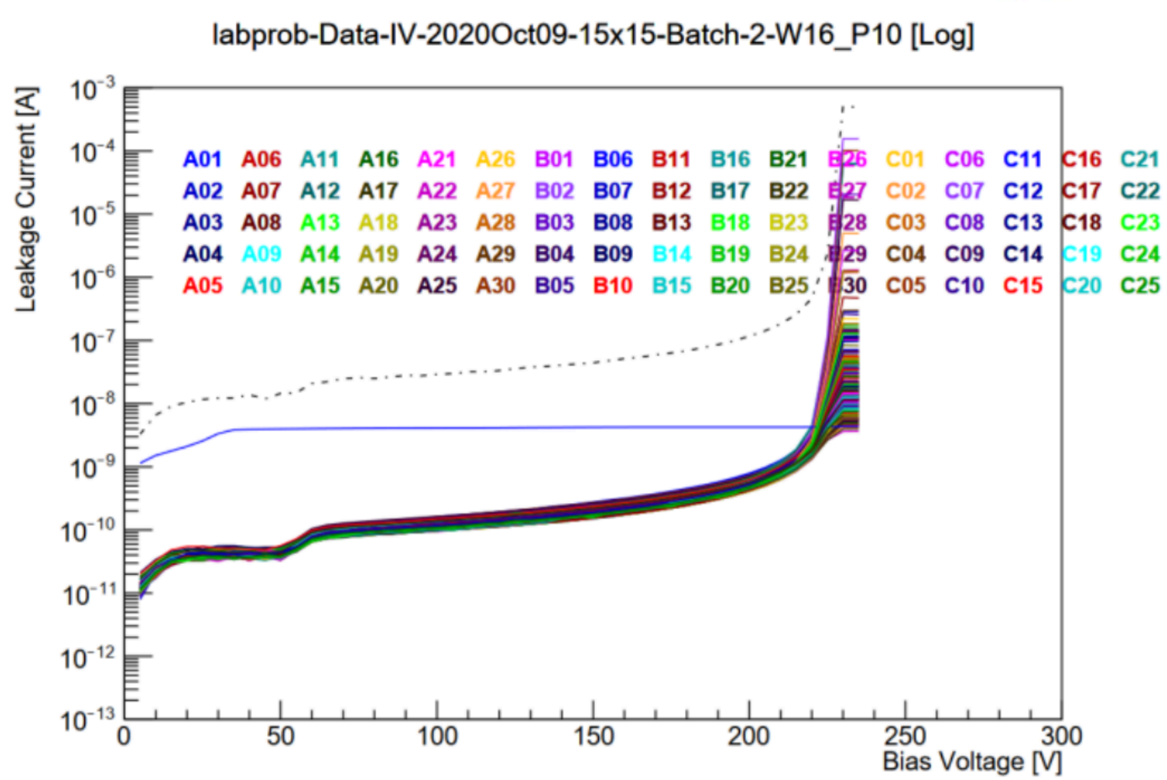
Distribution of the average leakage current

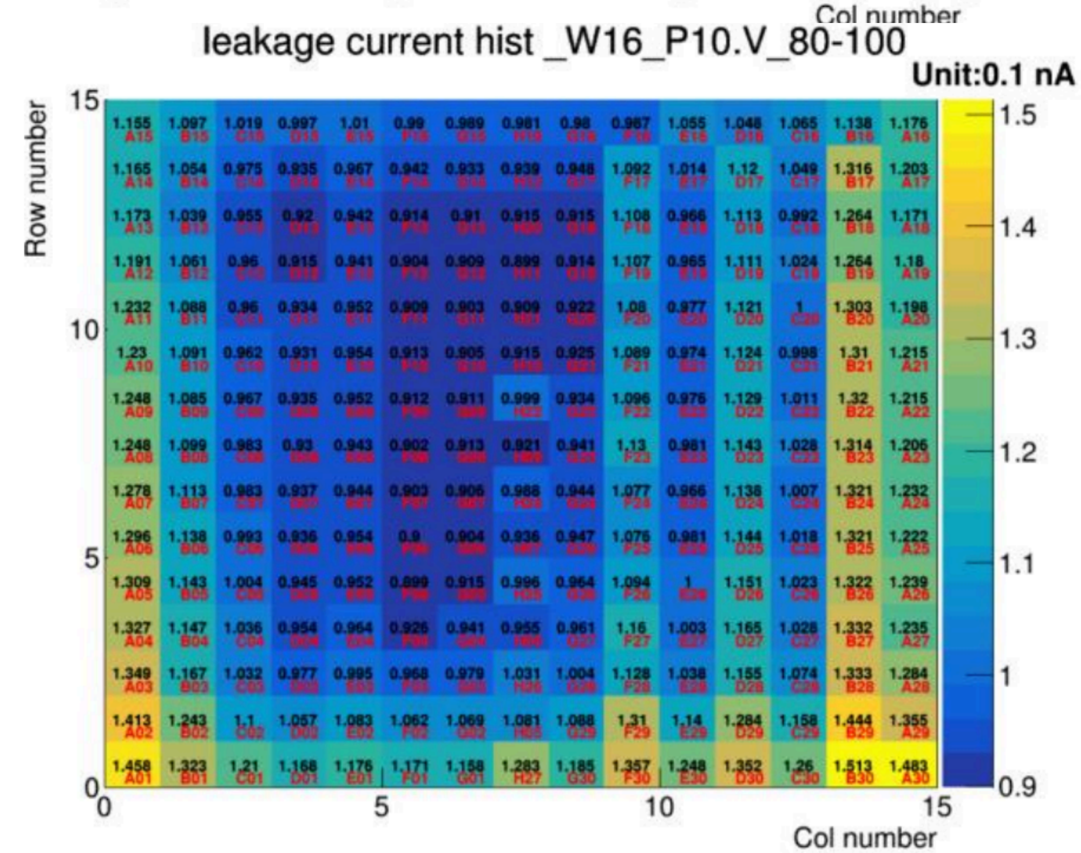
W8



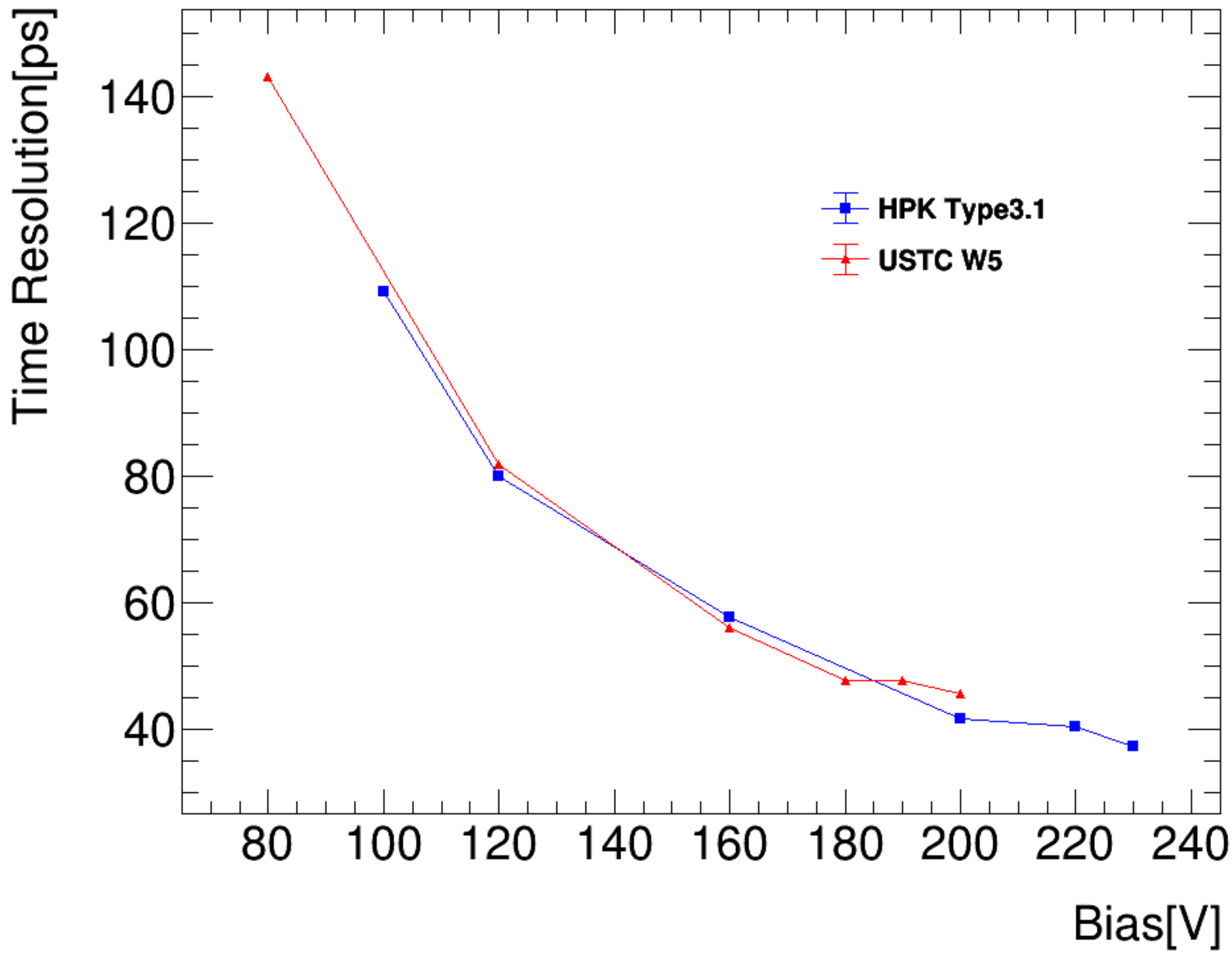


W16

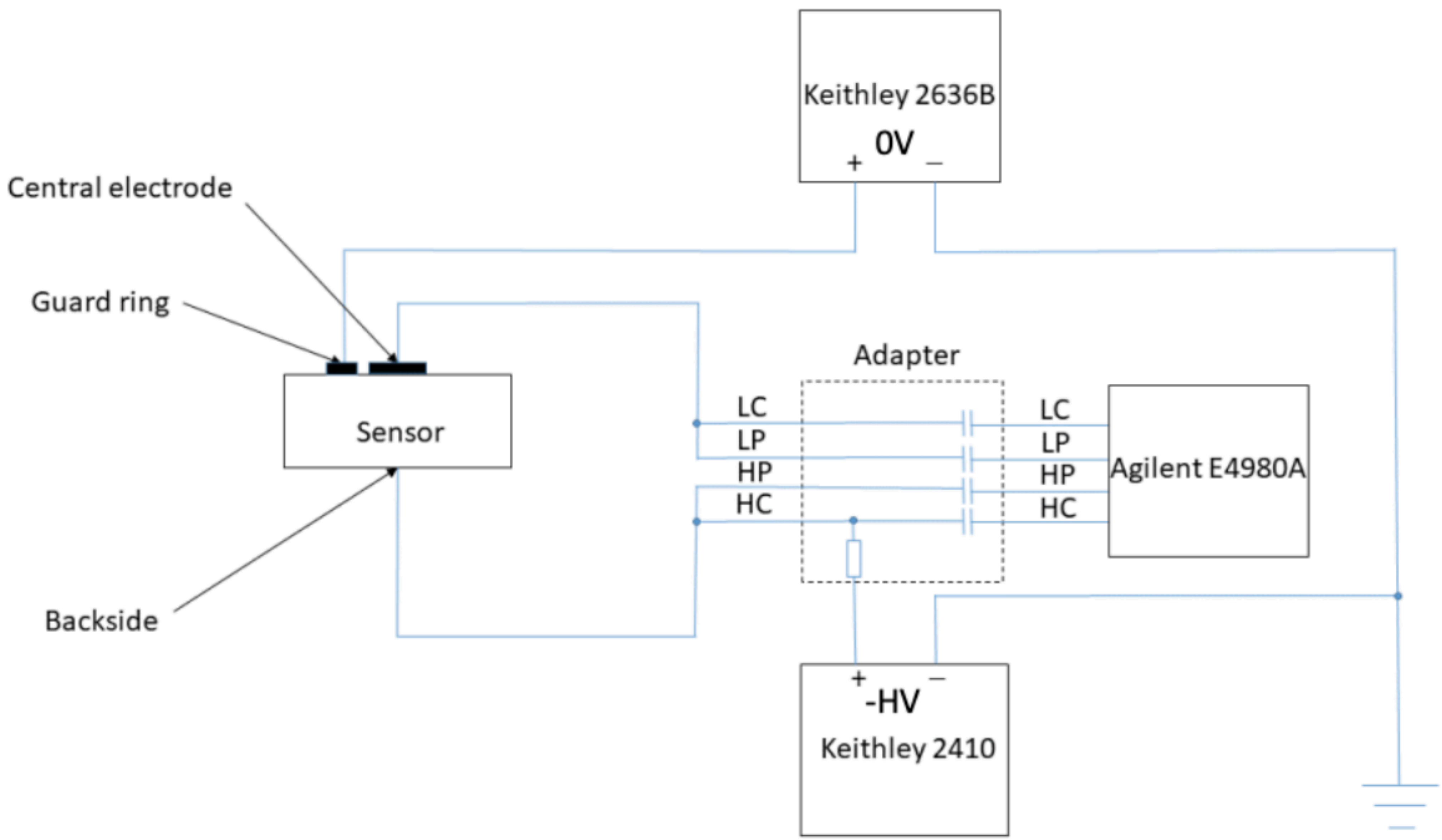




Beta-TCT result

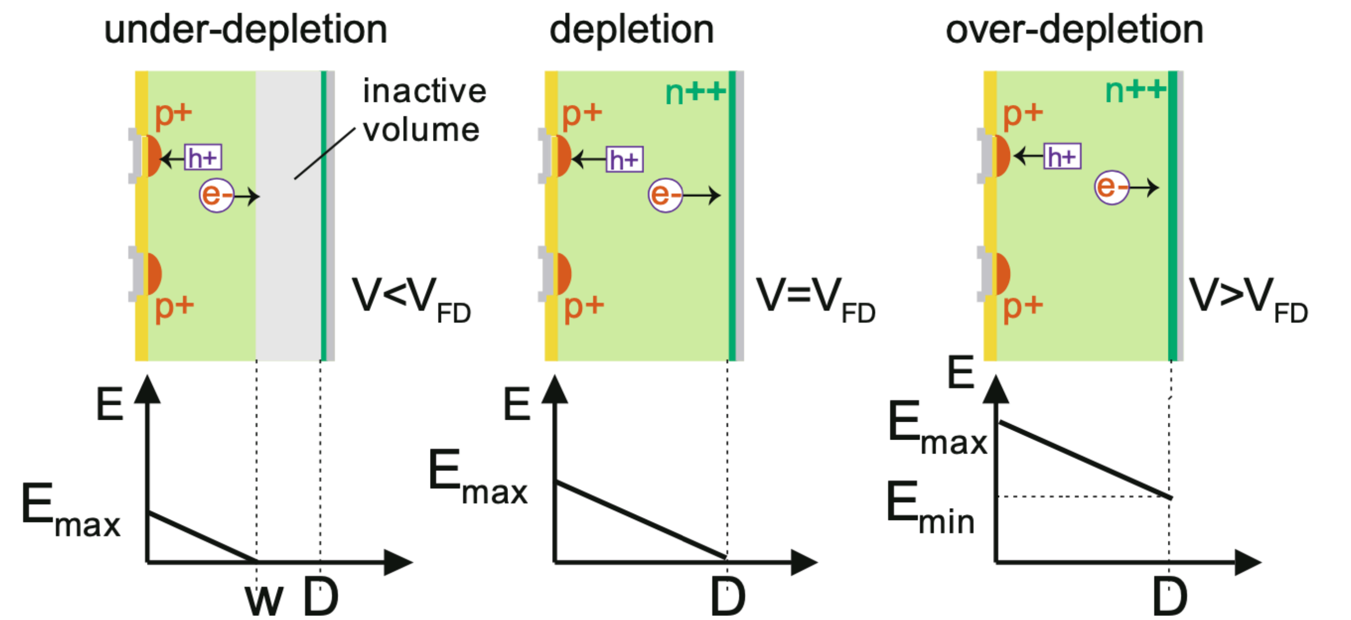


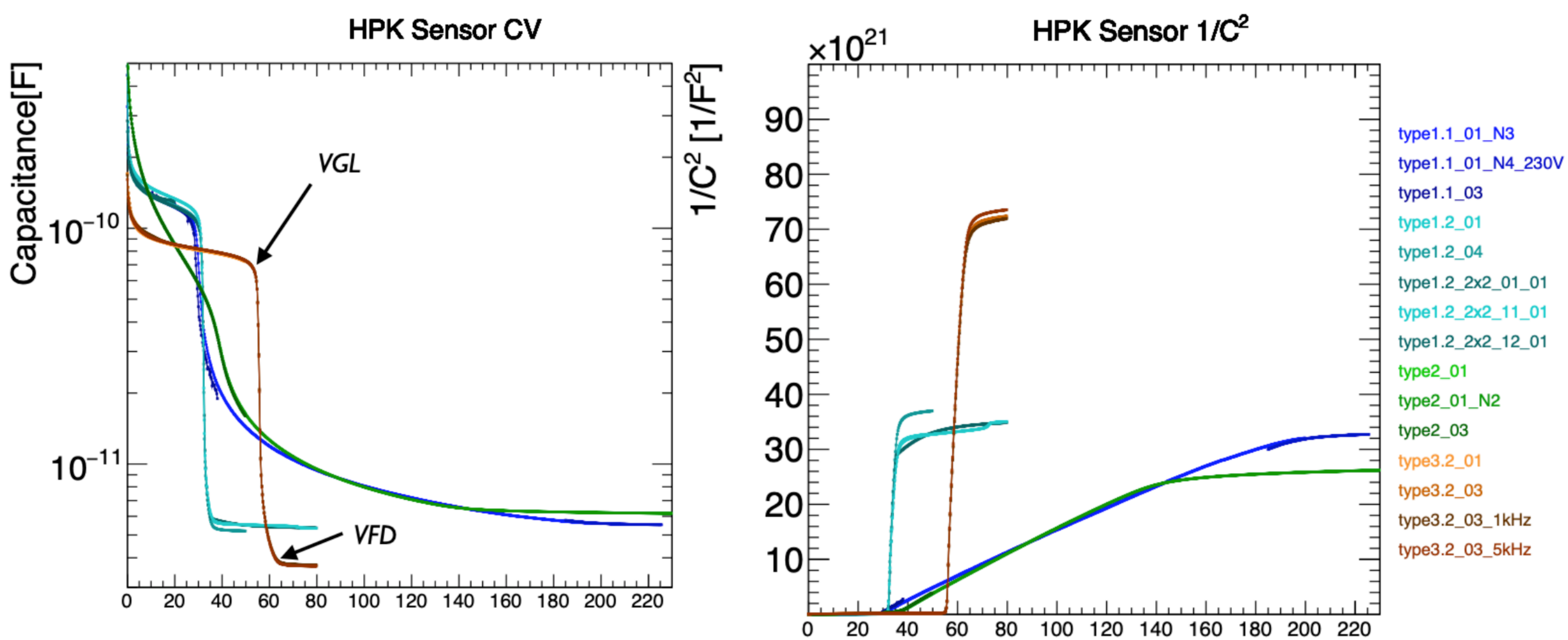
CV circuit


Keithley 2636B
0V
+
–
Central electrode
Guard ring
Sensor
Backside
Adapter
LC
LP
HP
HC
LC
LP
HP
HC
Agilent E4980A
+
-HV
–
Keithley 2410

C-V principle

Depletion process



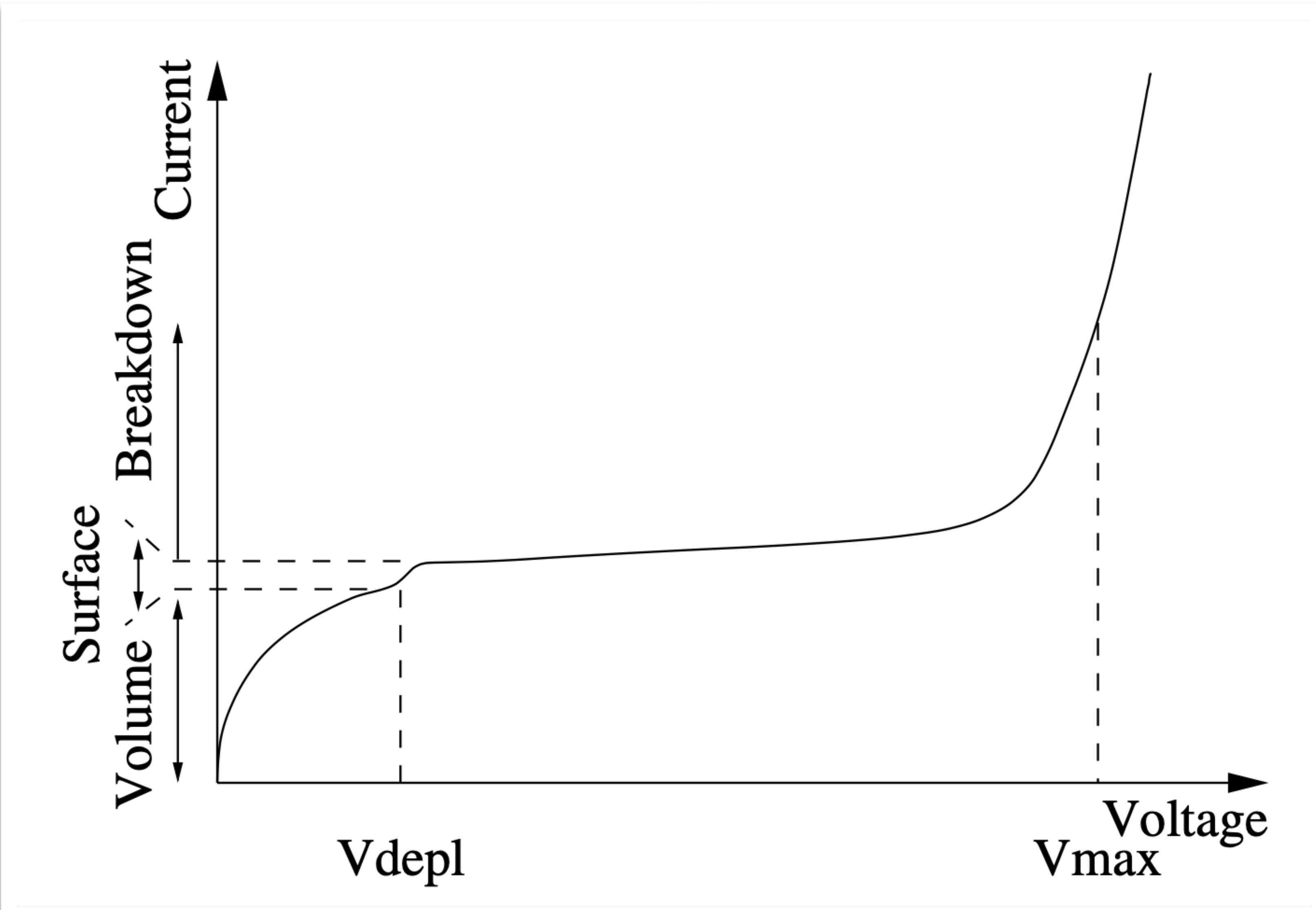


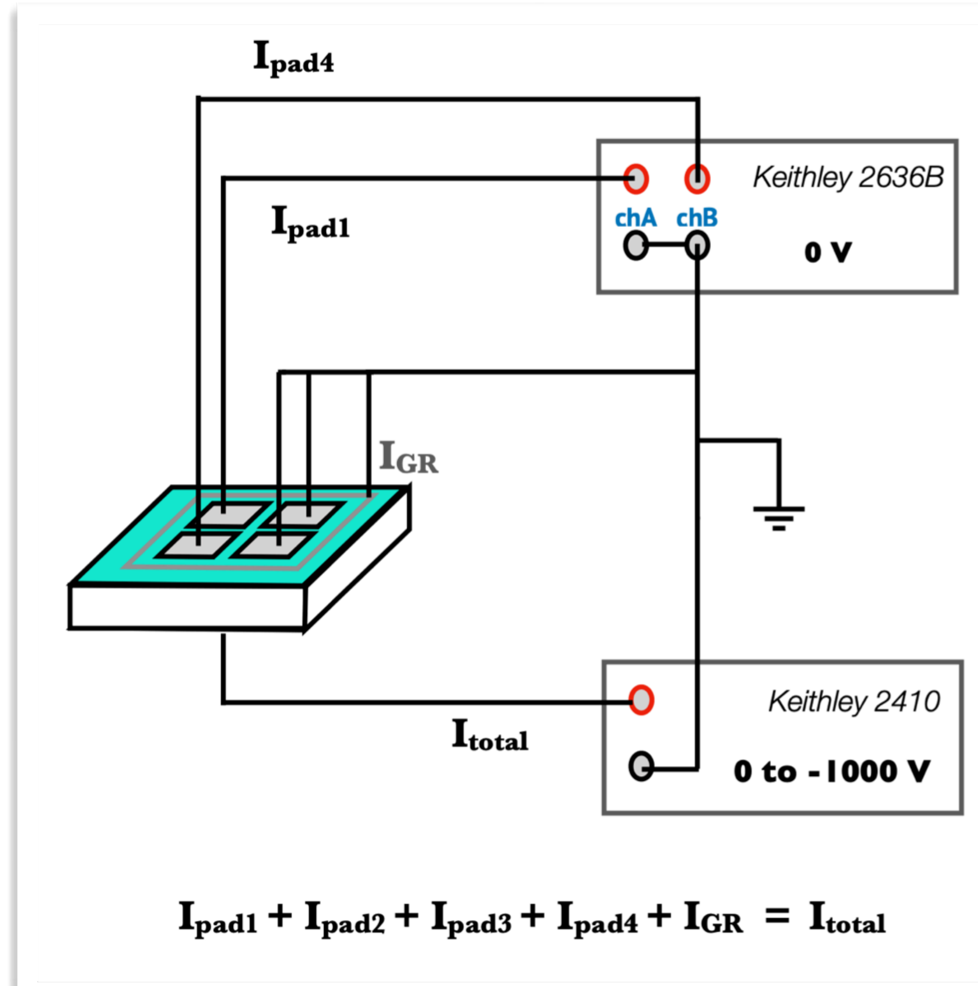
$$N(w) = \frac{2}{e \cdot \epsilon \cdot A^2}\left[\frac{d(C^{-2})}{dV}\right]^{-1}$$

$$w = A \cdot \epsilon \cdot \frac{1}{C}$$

N: doping density
w: depth
A: active aera

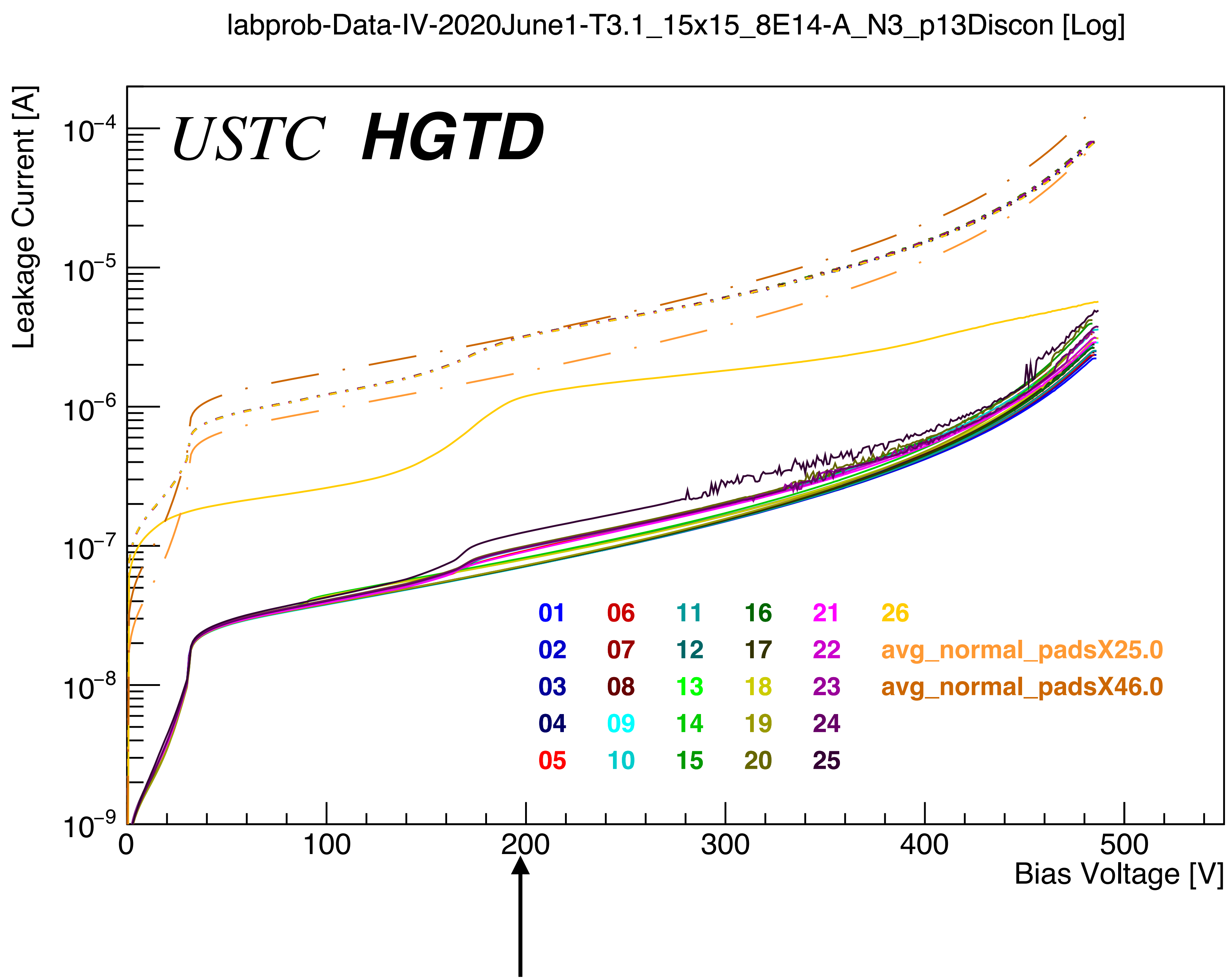
I-V





Setup of I-V measurements

Results from 15x15 sensor with 5x5 probe card



The final punch through occurs at ~180-200V

Single pad PIN

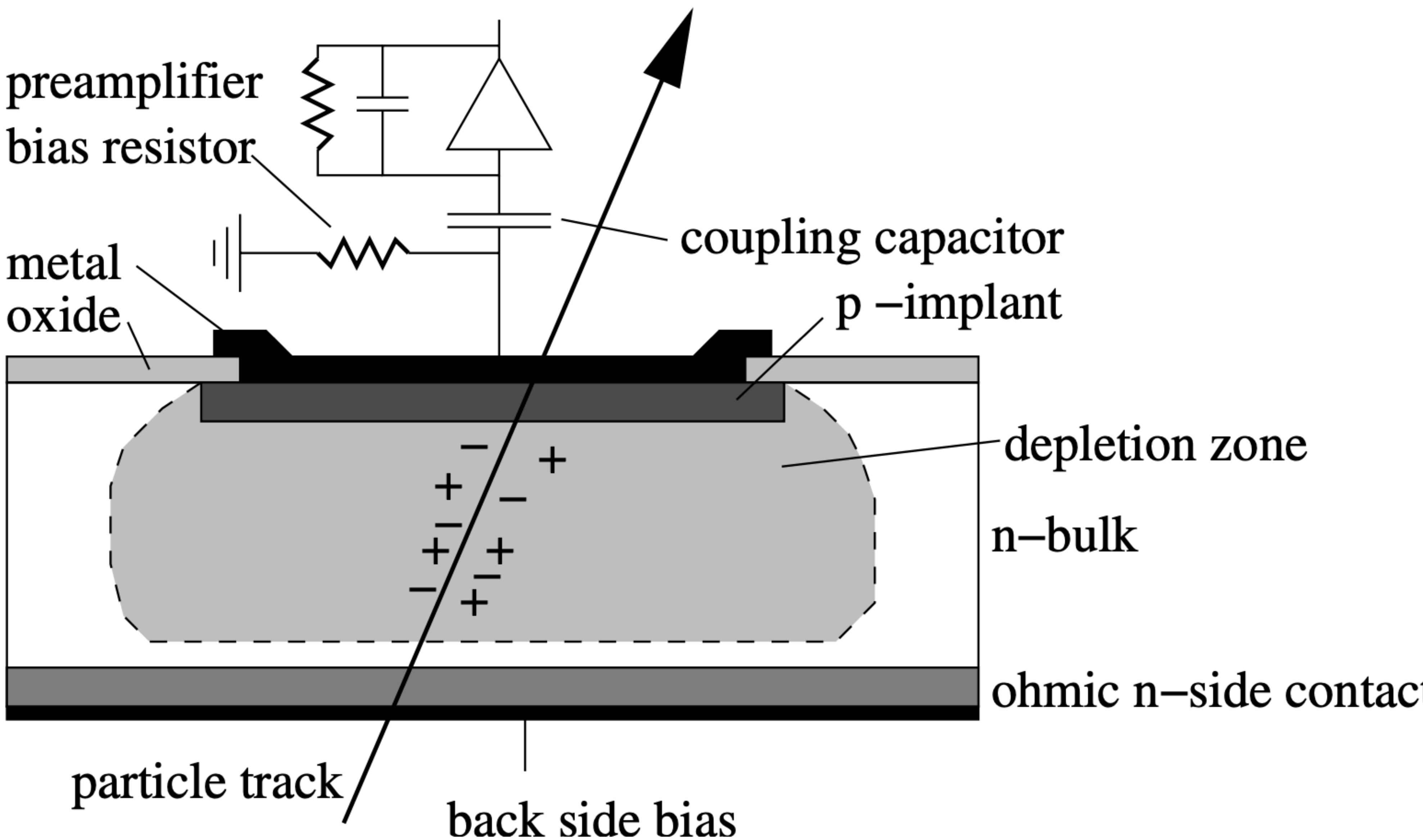


Fig. 2.12. Schematic cross section of a simple silicon pad sensor

LGAD Charge collection and JTE

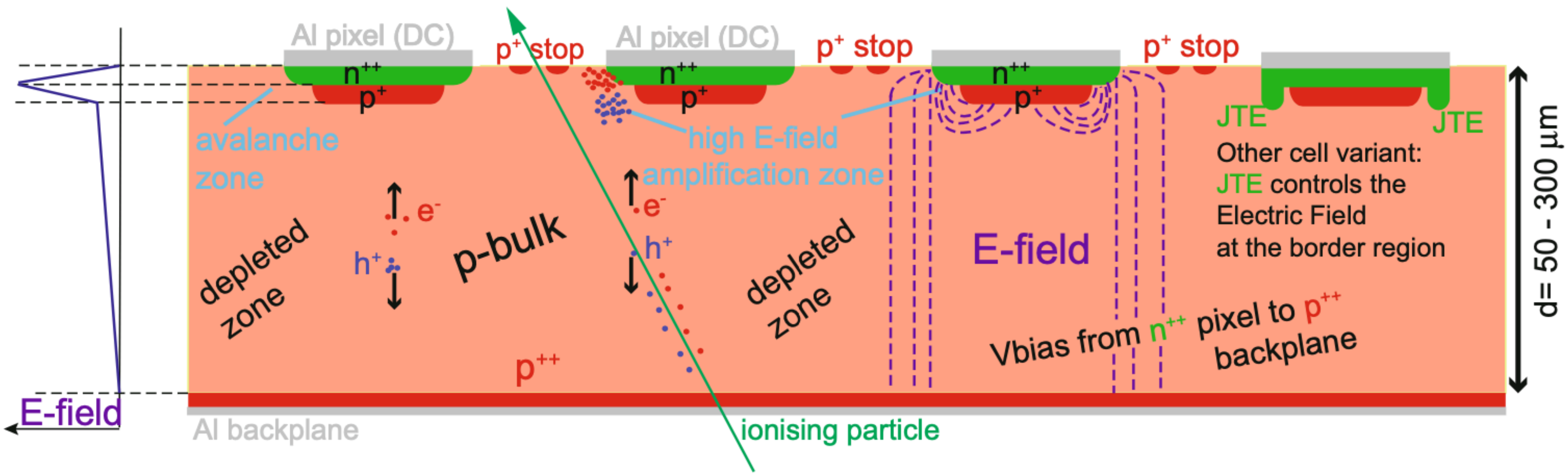
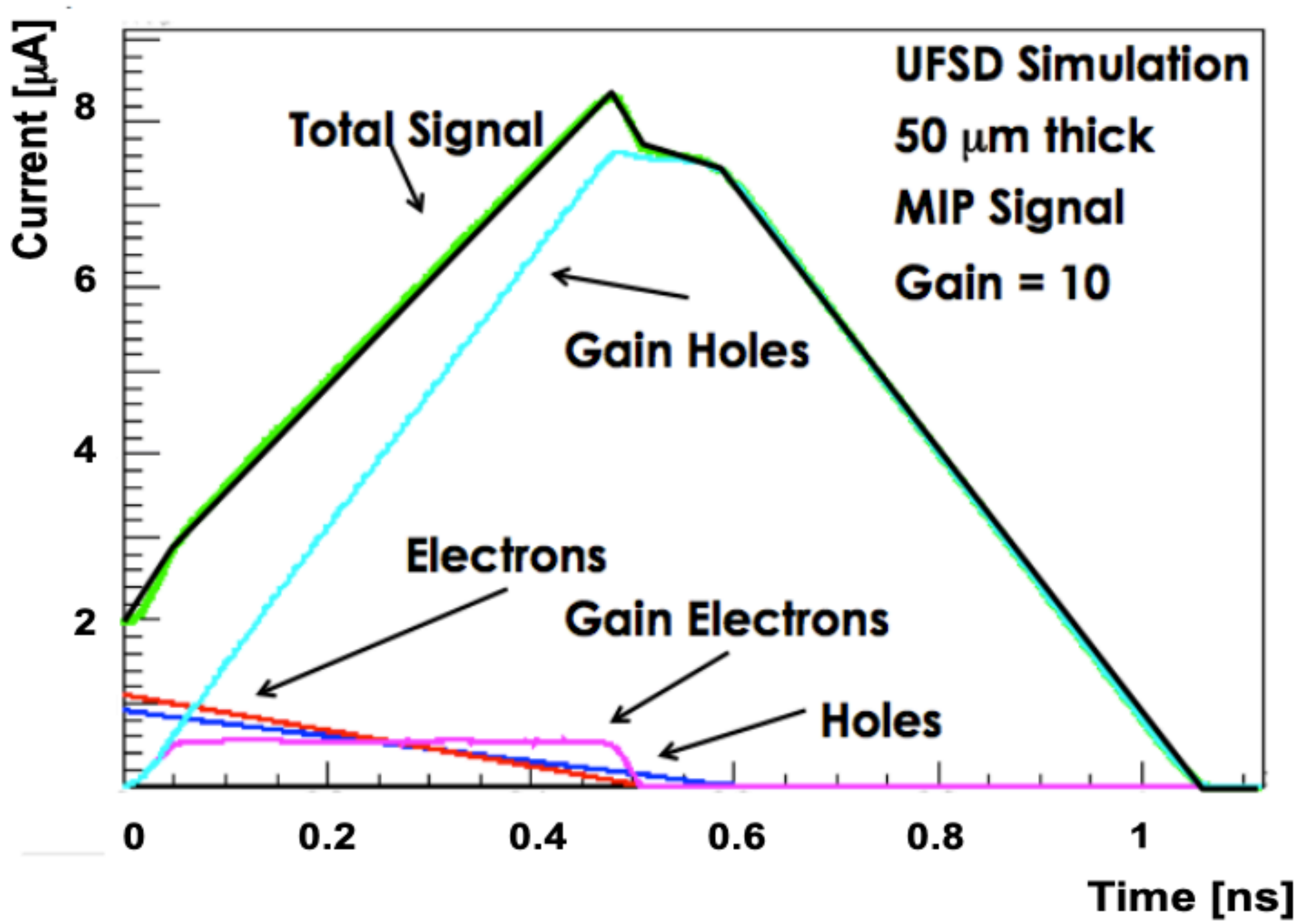
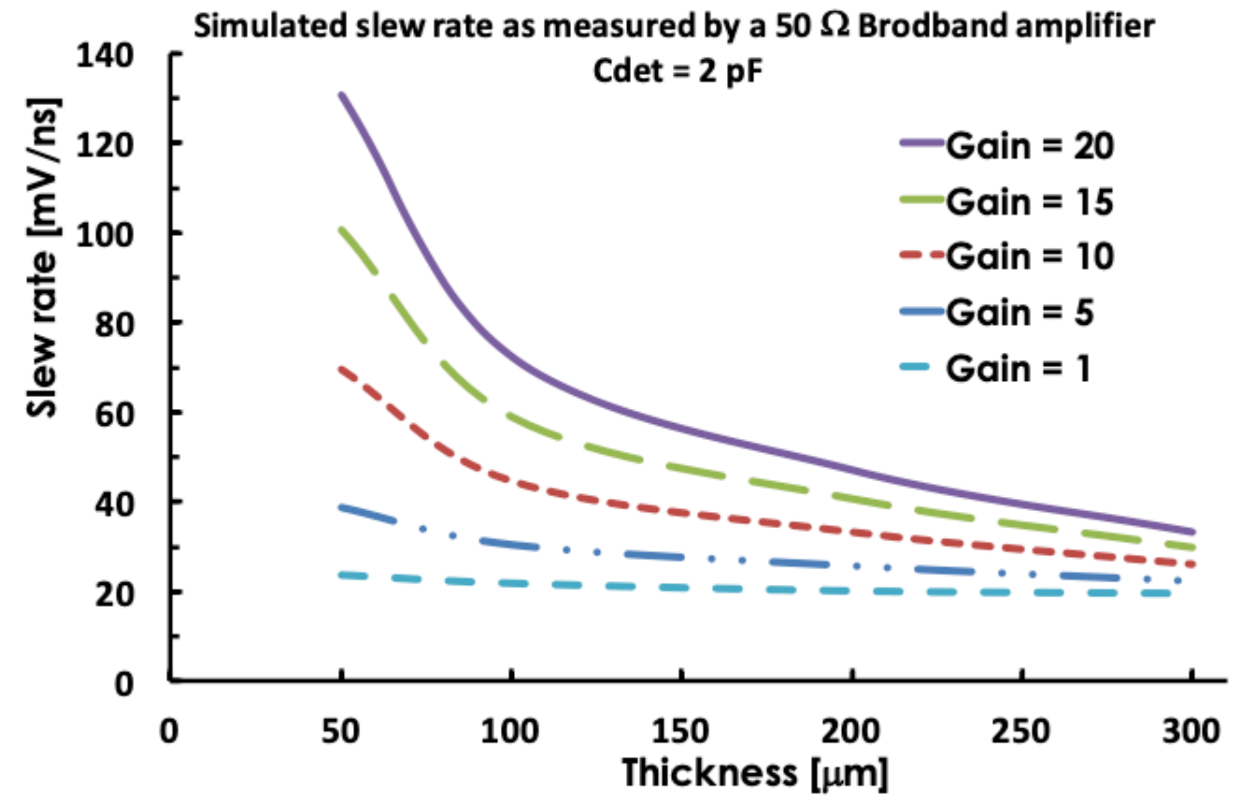


Fig. 1.85 A schematic of a segmented **L**ow **G**ain **A**valanche **D**etector LGAD is shown emphasising several different features – electric field, amplification, cell isolation, cell varieties. Cells can be strip, pads or pixels – mostly millimetre sized pads these days. The bulk is fully depleted. The amplification stage is localised between the deep p^+ implant and the n^{++}-electrode, see field configuration on the right. As for an n^{++}-in-p sensor the cells need to be isolated, here by p^+ stops. On the right another variant with a Junction Termination & Guard Ring is shown – **J**unction **T**ermination **E**xtension JTE. The JTE controls the electric field at the border region. A significant high bias voltage is applied between n^{++} cells (pixels or pads) and p^{++}-backplane

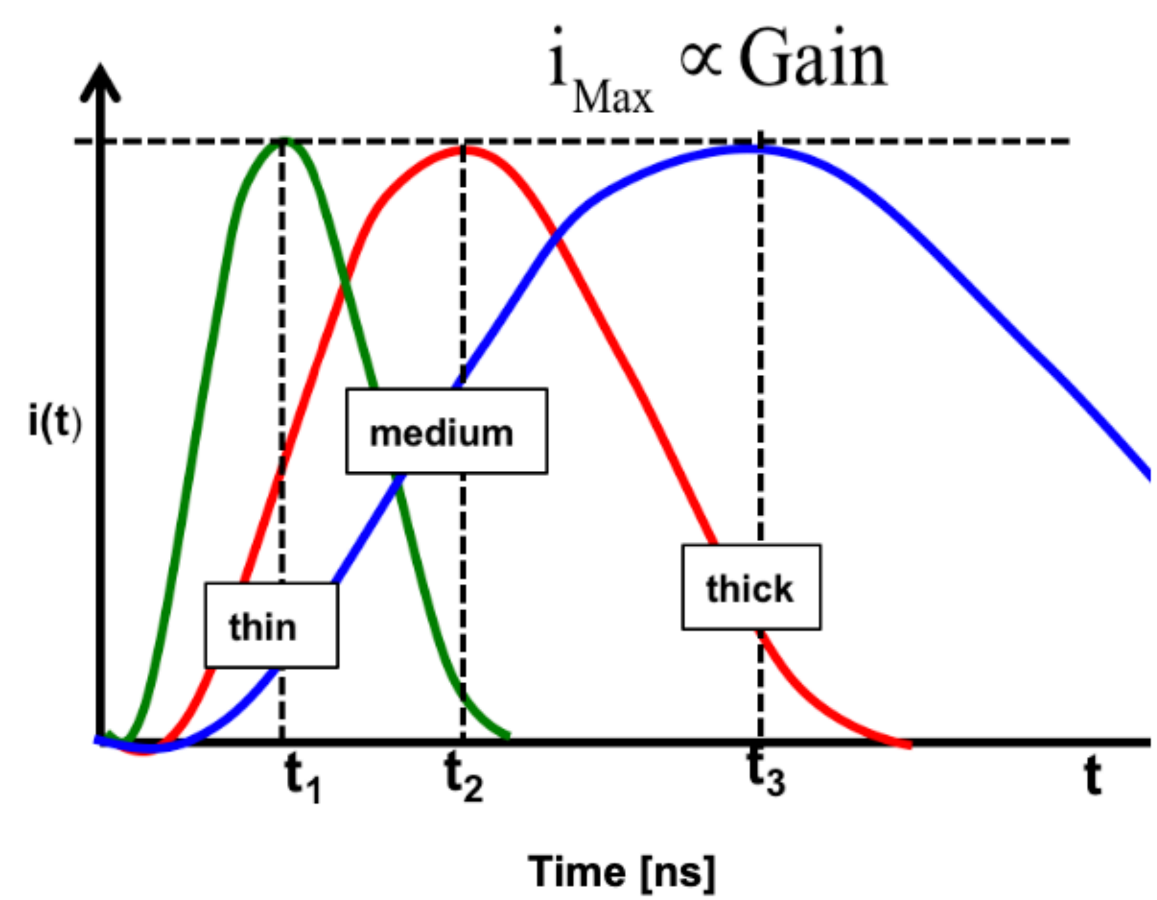
LGAD Signal



Current [μA]
8
6
4
2
0
0.2
0.4
0.6
0.8
1
Time [ns]
UFSD Simulation
50 μm thick
MIP Signal
Gain = 10
Total Signal
Gain Holes
Electrons
Gain Electrons
Holes



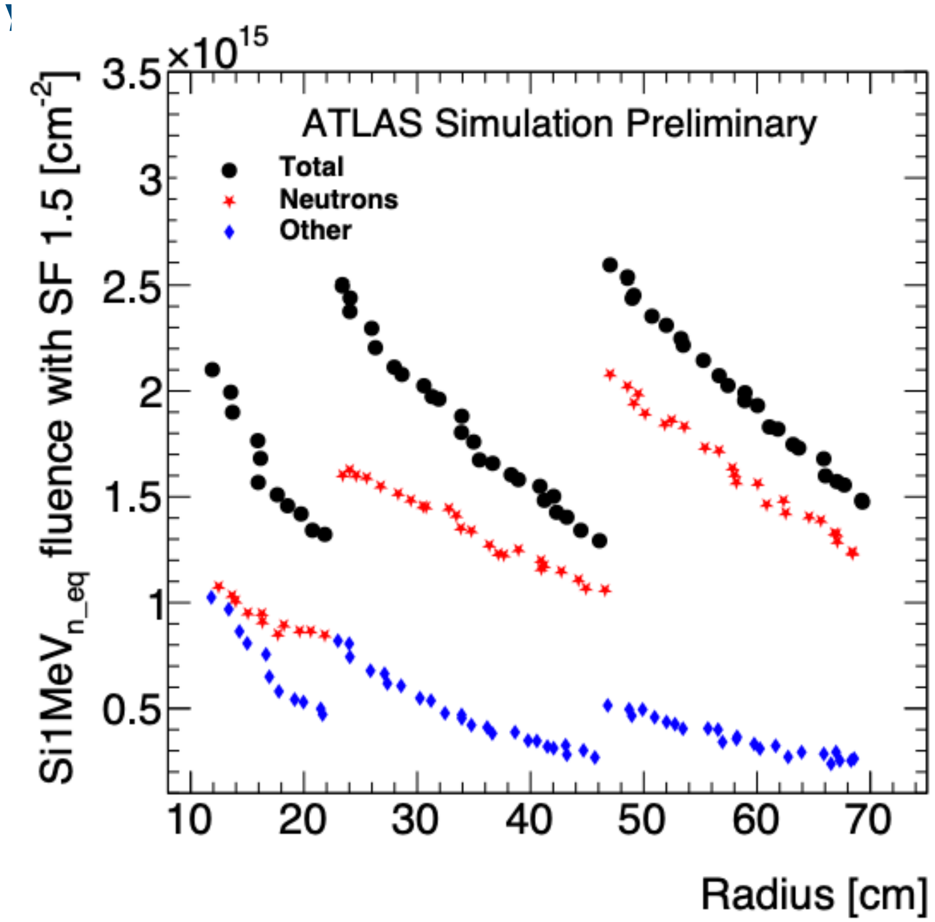
Simulated slew rate as measured by a 50 Ω Brodband amplifier
Cdet = 2 pF
Slew rate [mV/ns]
140
120
100
80
60
40
20
0
50
100
150
200
250
300
Thickness [μm]
Gain = 20
Gain = 15
Gain = 10
Gain = 5
Gain = 1

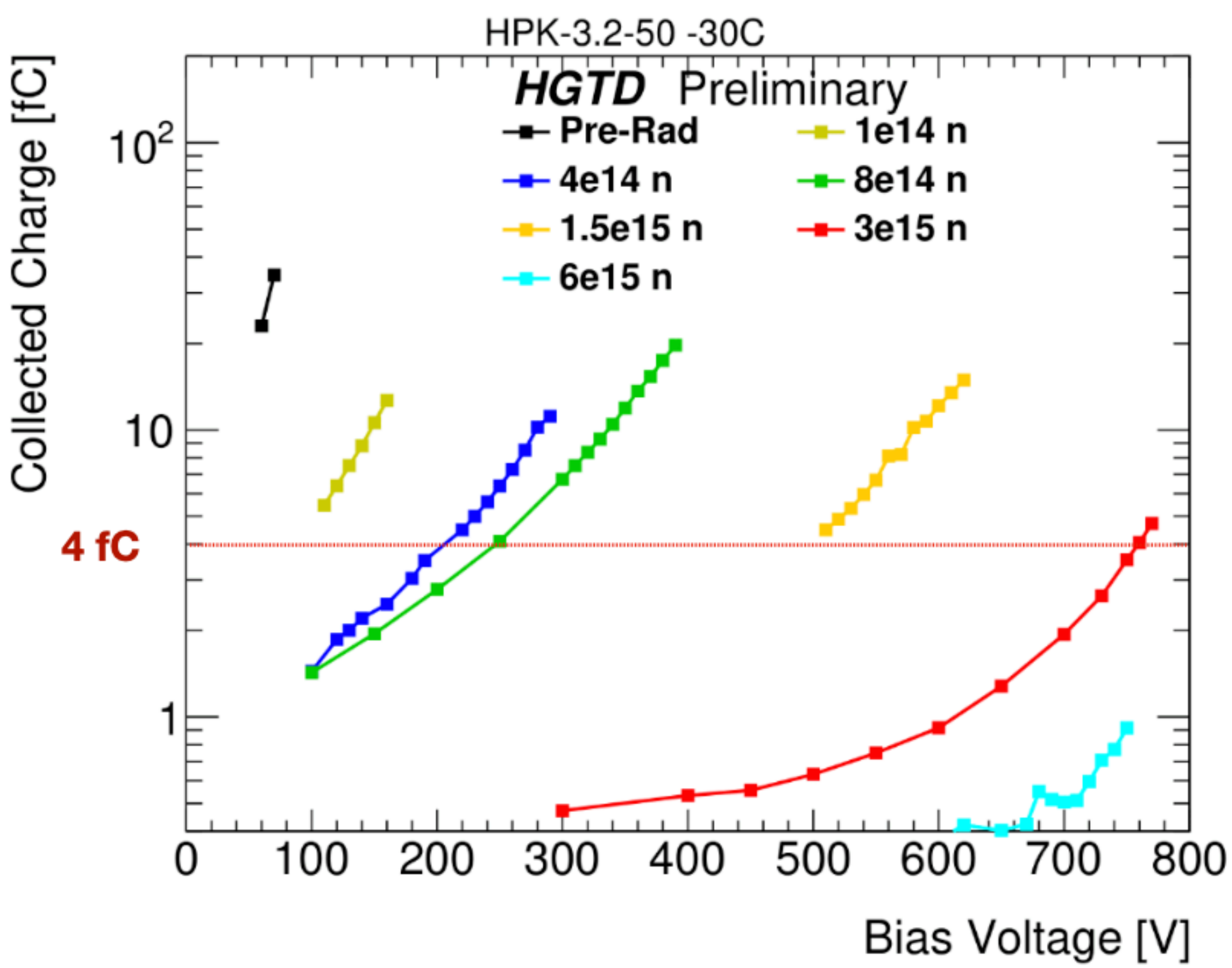


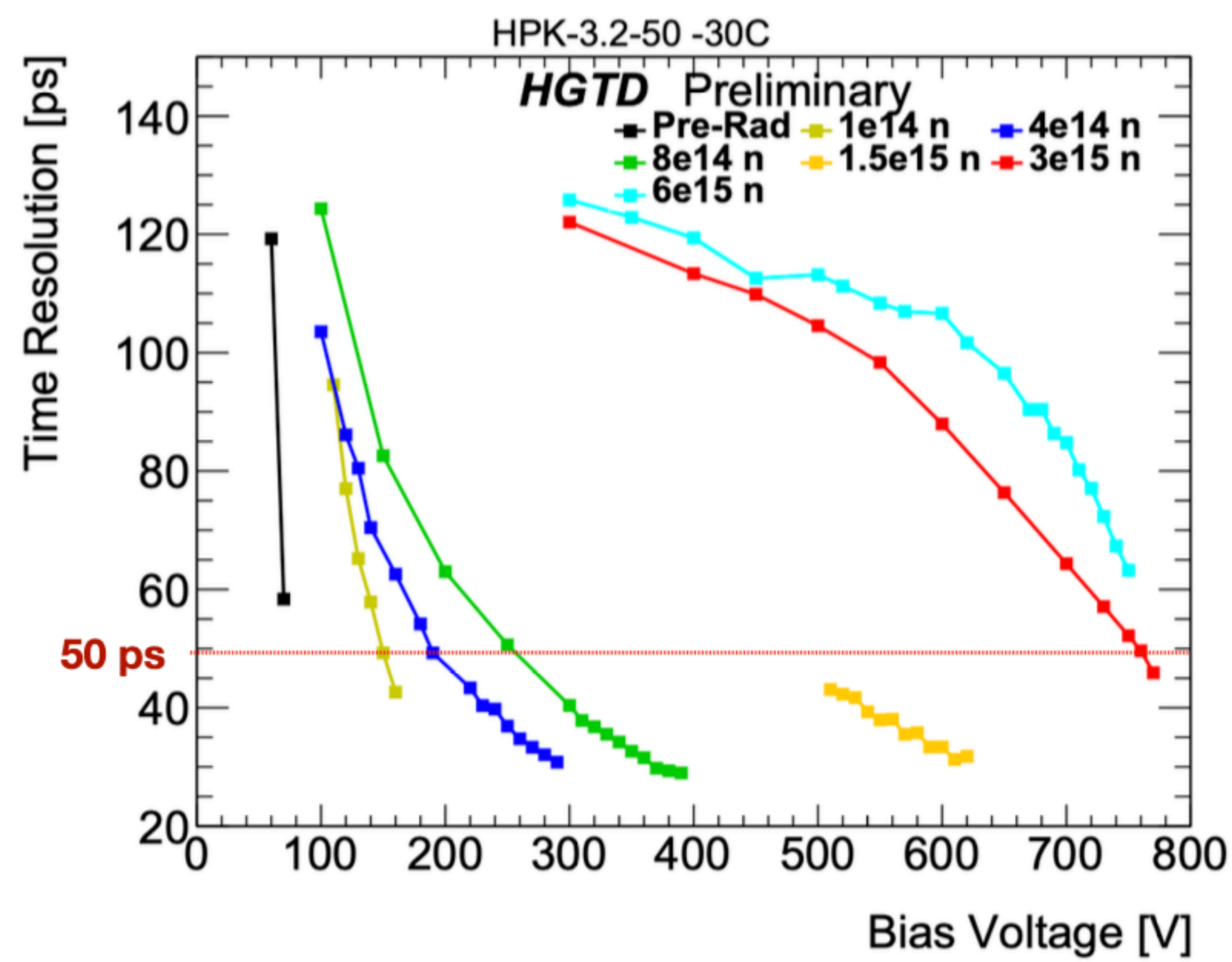
$i_{Max} \propto Gain$
i(t)
thin
medium
thick
t_1
t_2
t_3
t
Time [ns]

LGAD Challenge

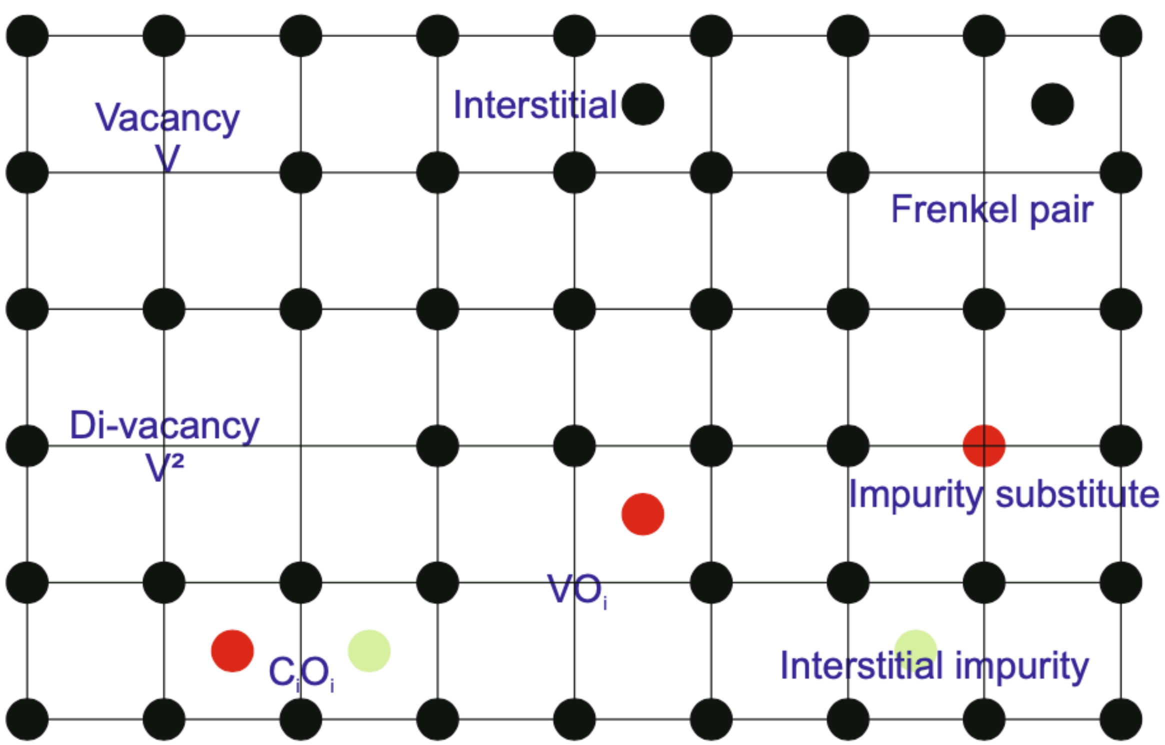
- Radiation damage is a main concern: 2.5E15 n_eq/cm²

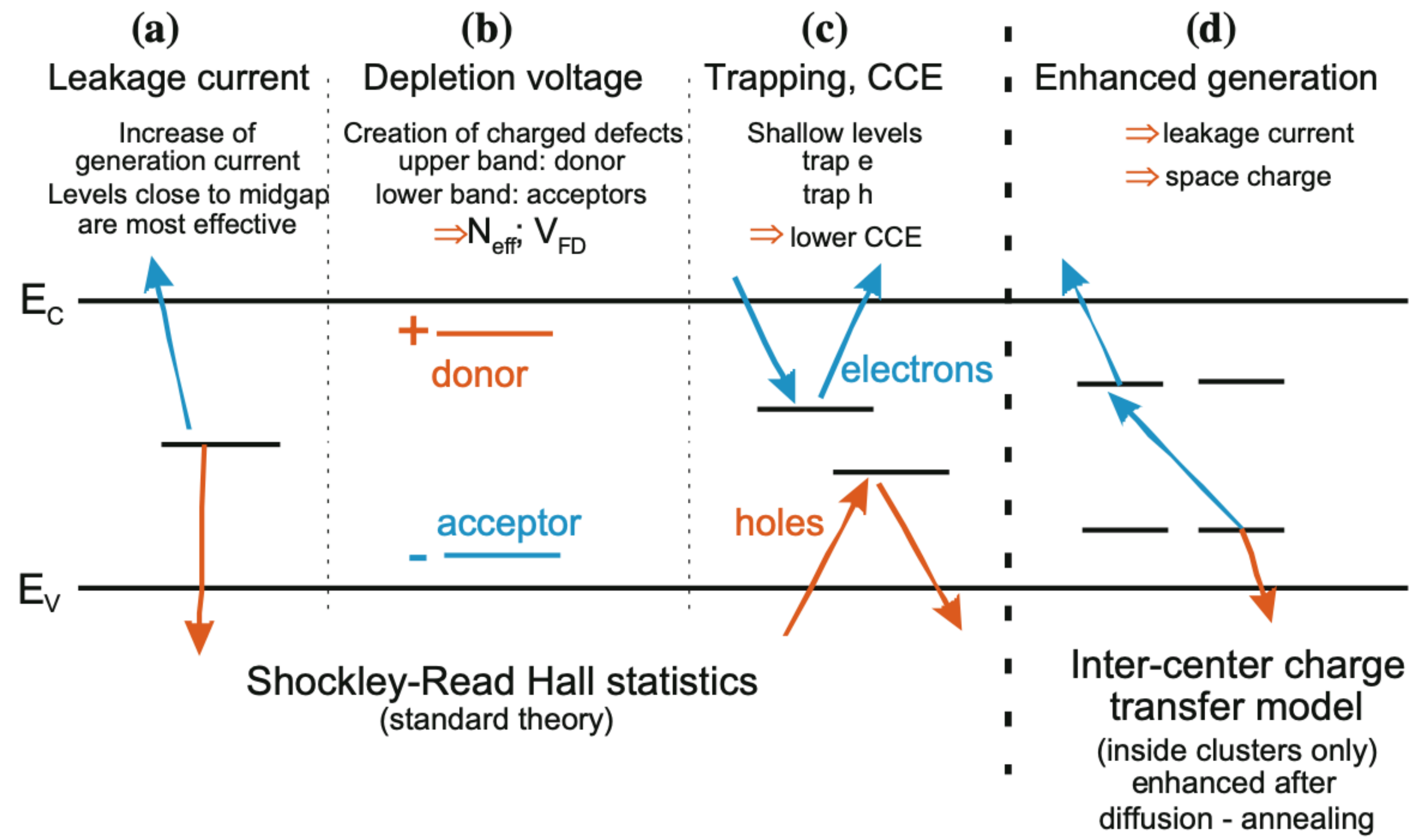






Radiation Damage





$$\Delta N_{eff}(\Phi_{eq}, t, T) = N_{C,0}(\Phi_{eq}) + N_A(\Phi_{eq}, t, T) + N_Y(\Phi_{eq}, t, T)$$

$$N_C(\Phi_{eq}) = N_{C,O}(1 - e^{-c\Phi_{eq}}) + g_c\Phi_{eq}$$

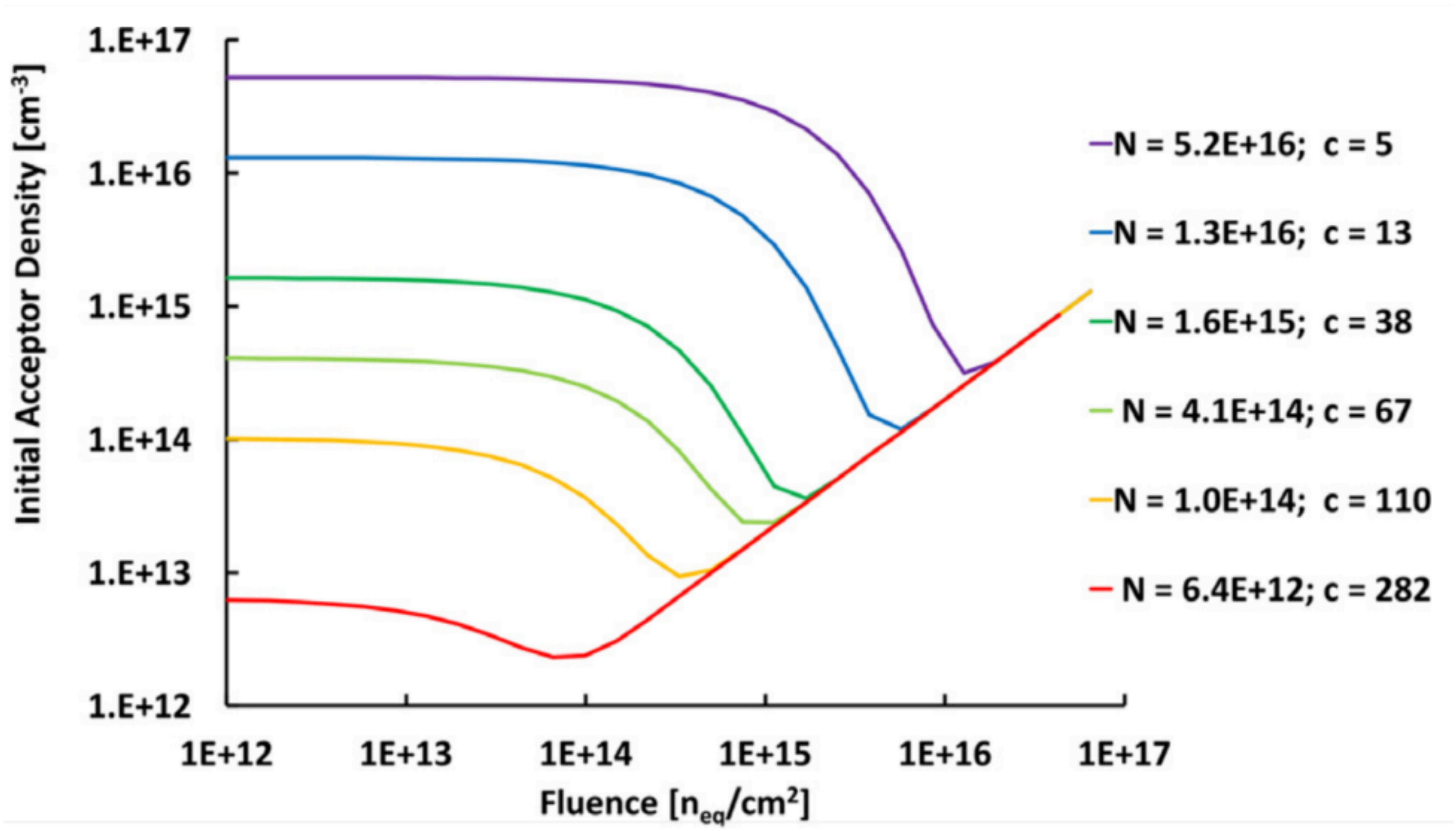
$$N_A(\phi) = g_{eff}\,\phi + N_A(0)\, e^{-c(N_A(0))\phi}$$

$$N_Y = N_{Y,0} \cdot (1 - e^{-t/\tau_Y})$$

Acceptor removal effect

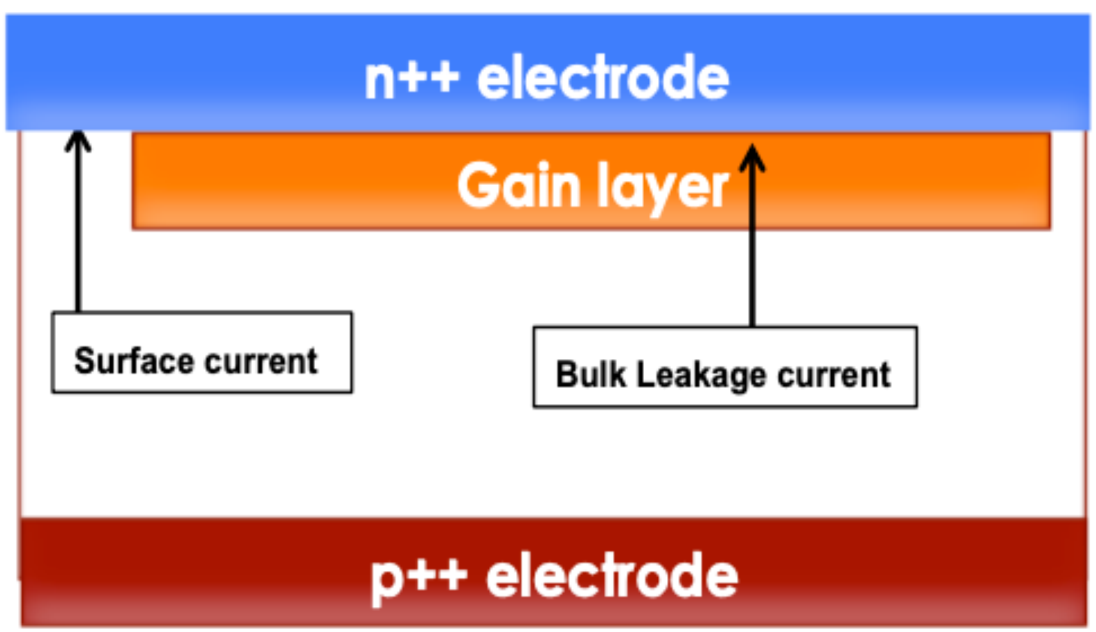
$$\rho_A(\phi) = g_{eff}\phi + \rho_A(0)e^{-c\phi}$$

c: “speed of the removal”

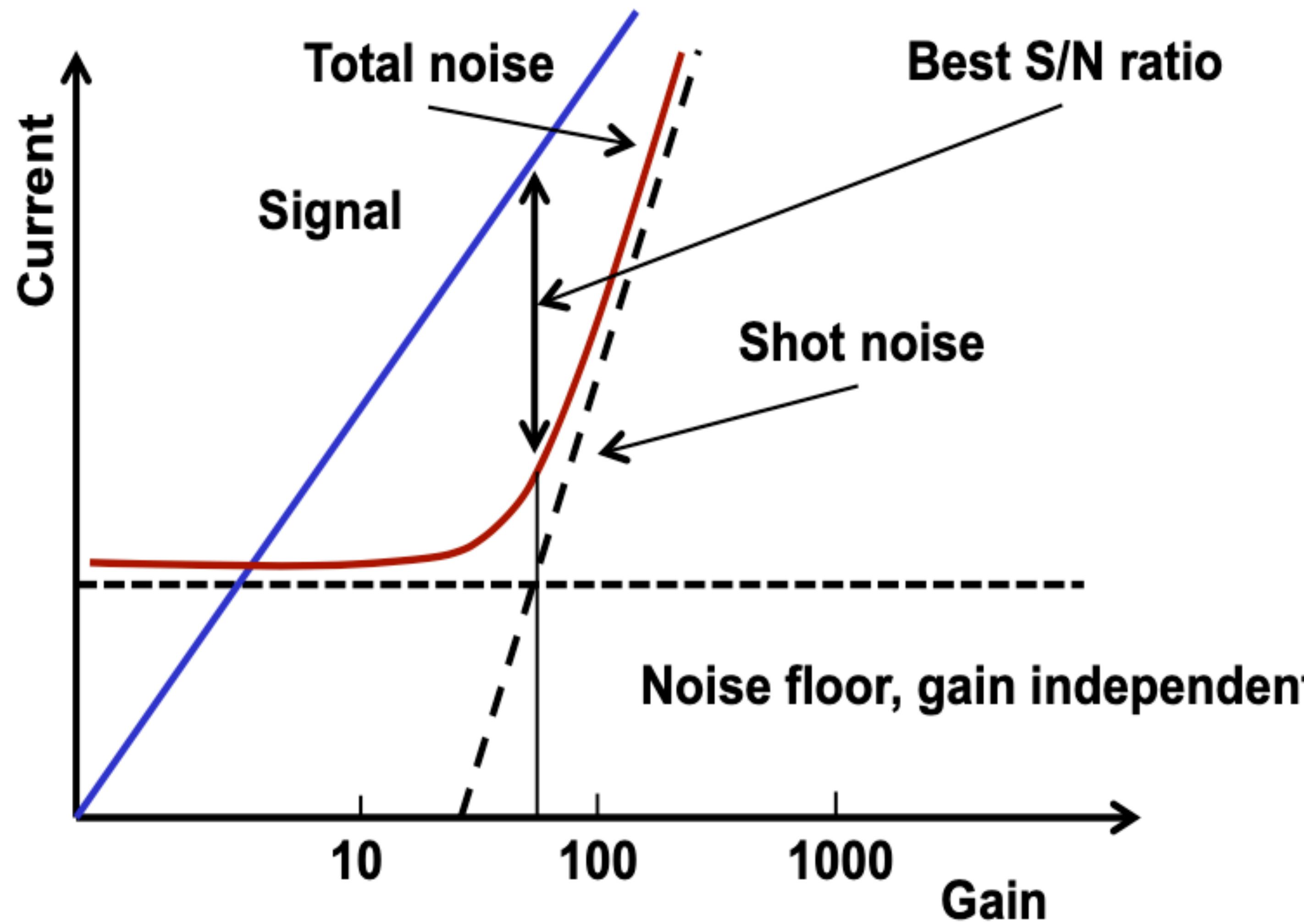


“c” relies on “ρ(0)”

Why Low gain: short noise!



a)



b)

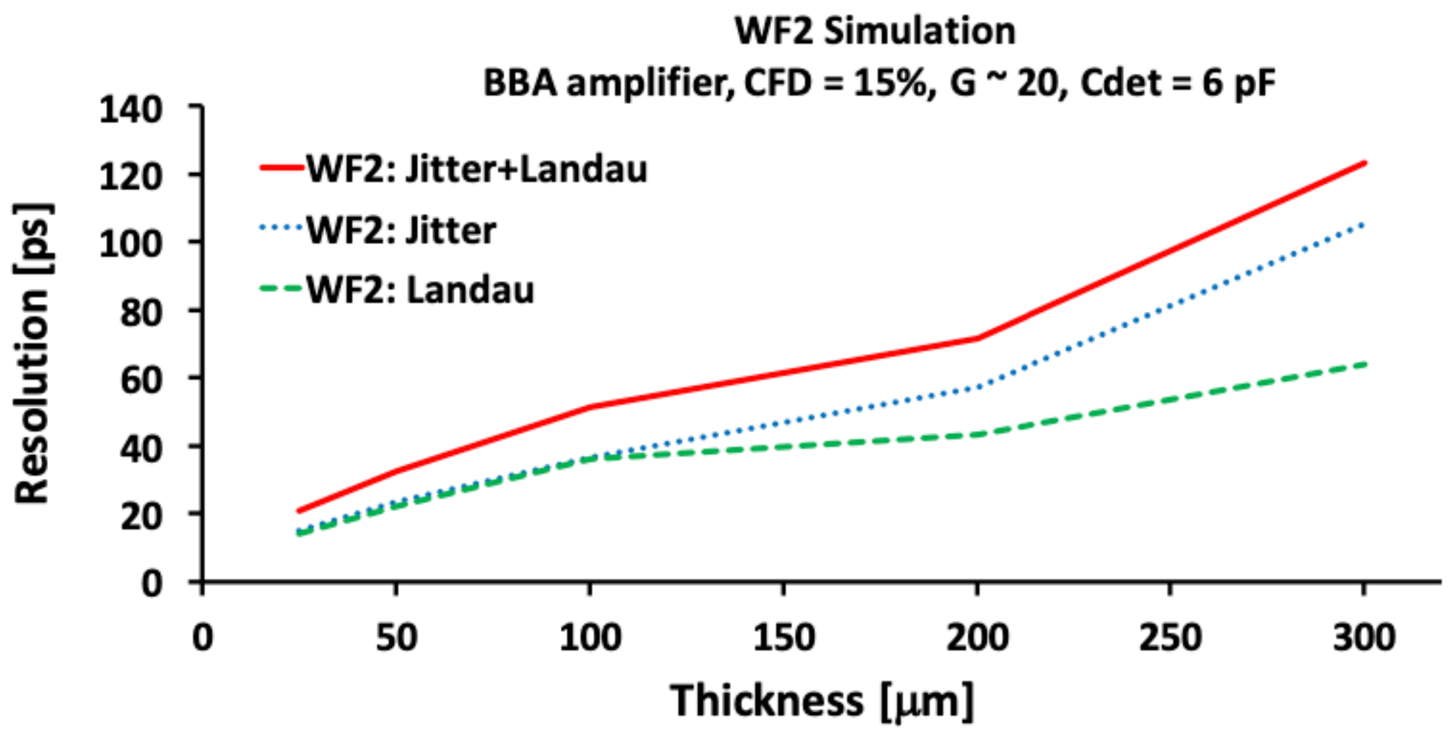
shot noise arises when **charge carriers cross a potential barrier,** as it happens in silicon sensors, and is due to the finite fixed charge of each electron

excess noise factor (ENF).

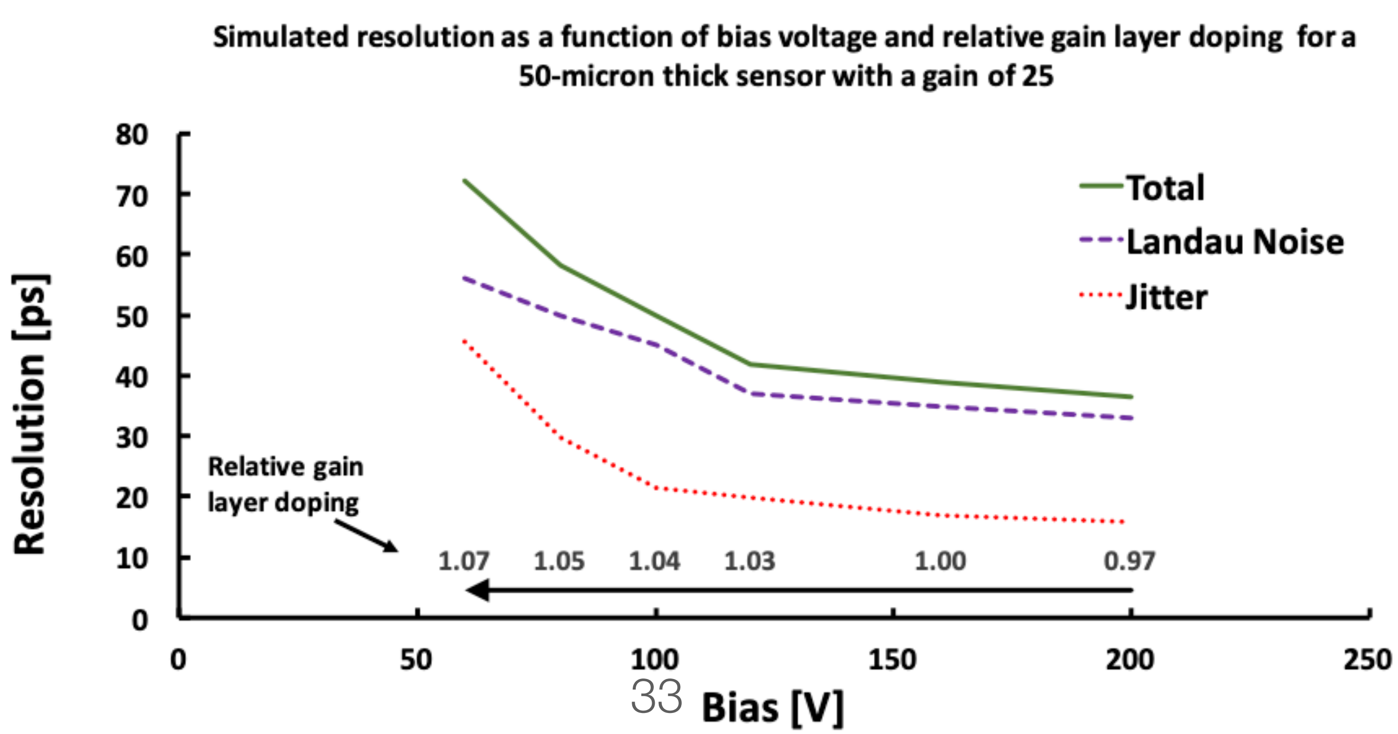
$$i^2_{Shot} = 2qI_{Det} = 2q\left[I_{surface} + \left(I_{Bulk} + I_{Signal}\right)G^2G^x\right],$$

Time Resolutions Rank

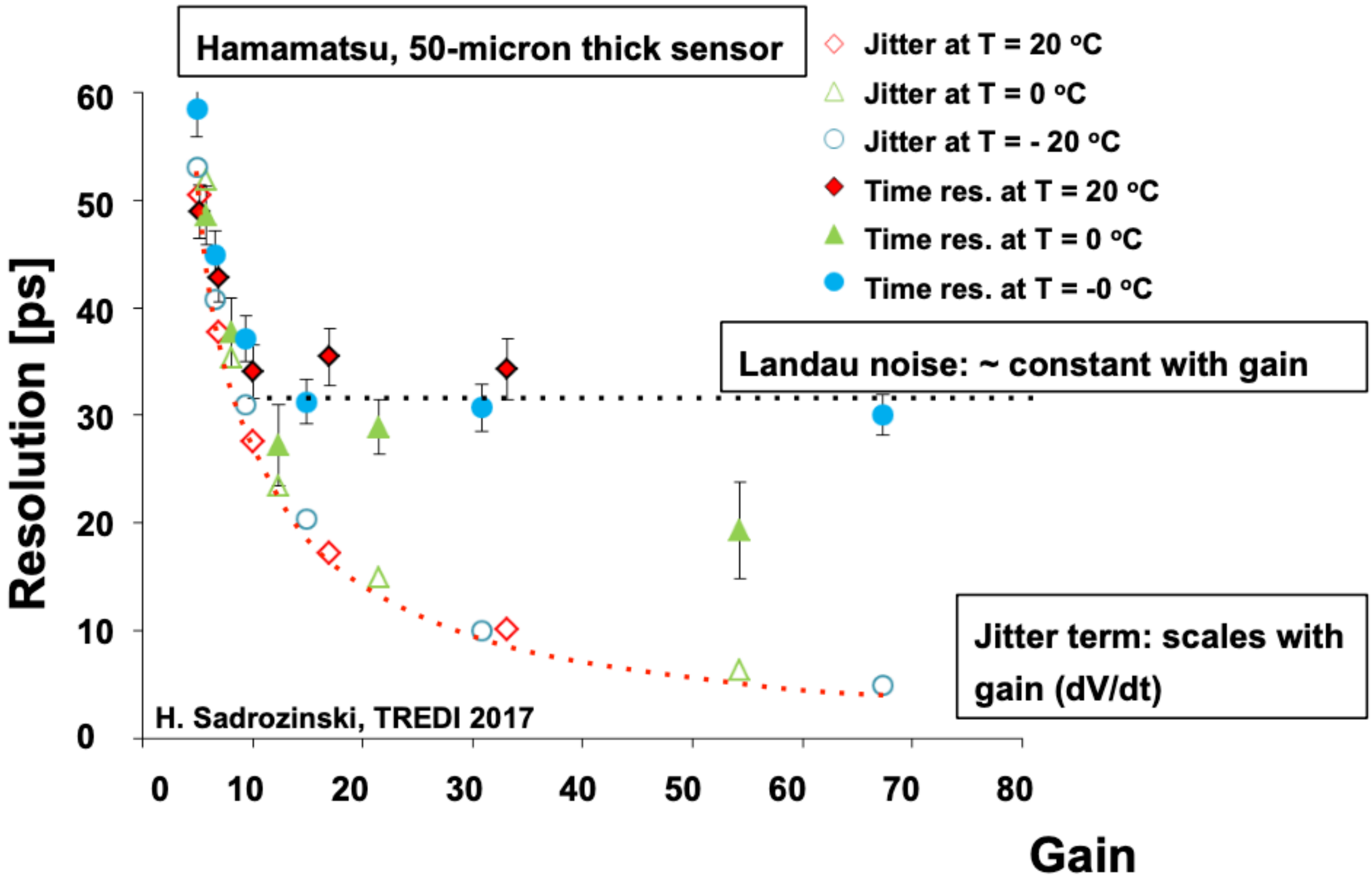
Thickness:



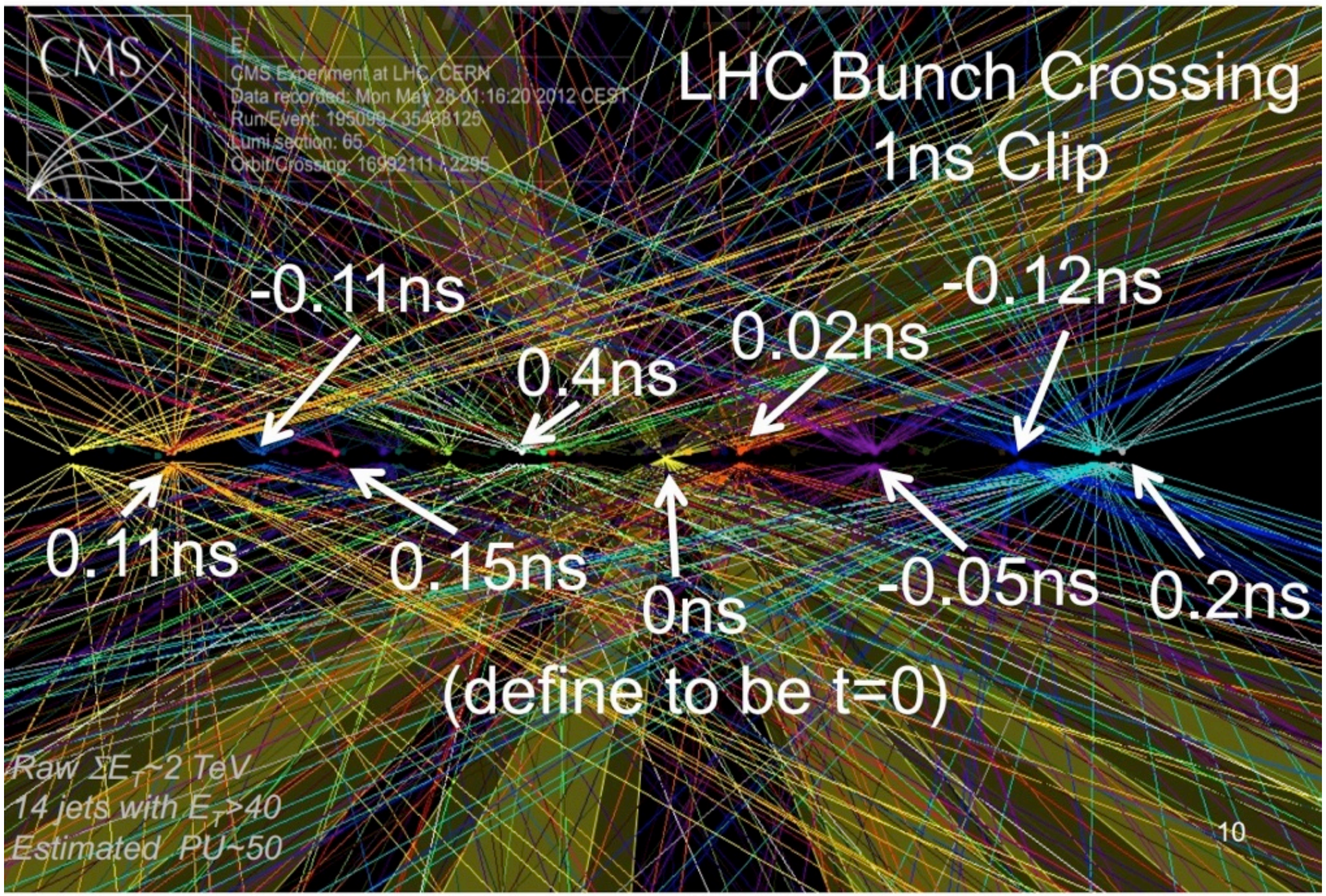
Bias:



Measurement of the Jitter contribution



Track to vertex association with time info. (4-D space)



Sensor Requirements

Technology	Silicon Low Gain Avalanche Detector (LGAD)
Time resolution	$\approx$ 35 ps (start); $\approx$ 70 ps (end of lifetime)
Time resolution uniformity	No requirement
Min. gain	20 (start); 8 (end of lifetime)
Min. charge	4 fC
Min. hit efficiency	95%
Granularity	1.3 mm $\times$ 1.3 mm
Max. inter-pad gap	100 µm
Max. physical thickness	300 µm
Active thickness	50 µm
Active size	39 mm $\times$ 19.5 mm (30 $\times$ 15 pads)
Max. inactive edge	500 µm
Radiation tolerance	$2.5 \times 10^{15}\,\mathrm{n_{eq}\,cm^{-2}}$, 1.5 MGy
Max. operation temperature on-sensor	−30 °C
Max. leakage current per pad	5 µA
Max. bias voltage	800 V
Max. power density	100 $\mathrm{mW/cm^2}$

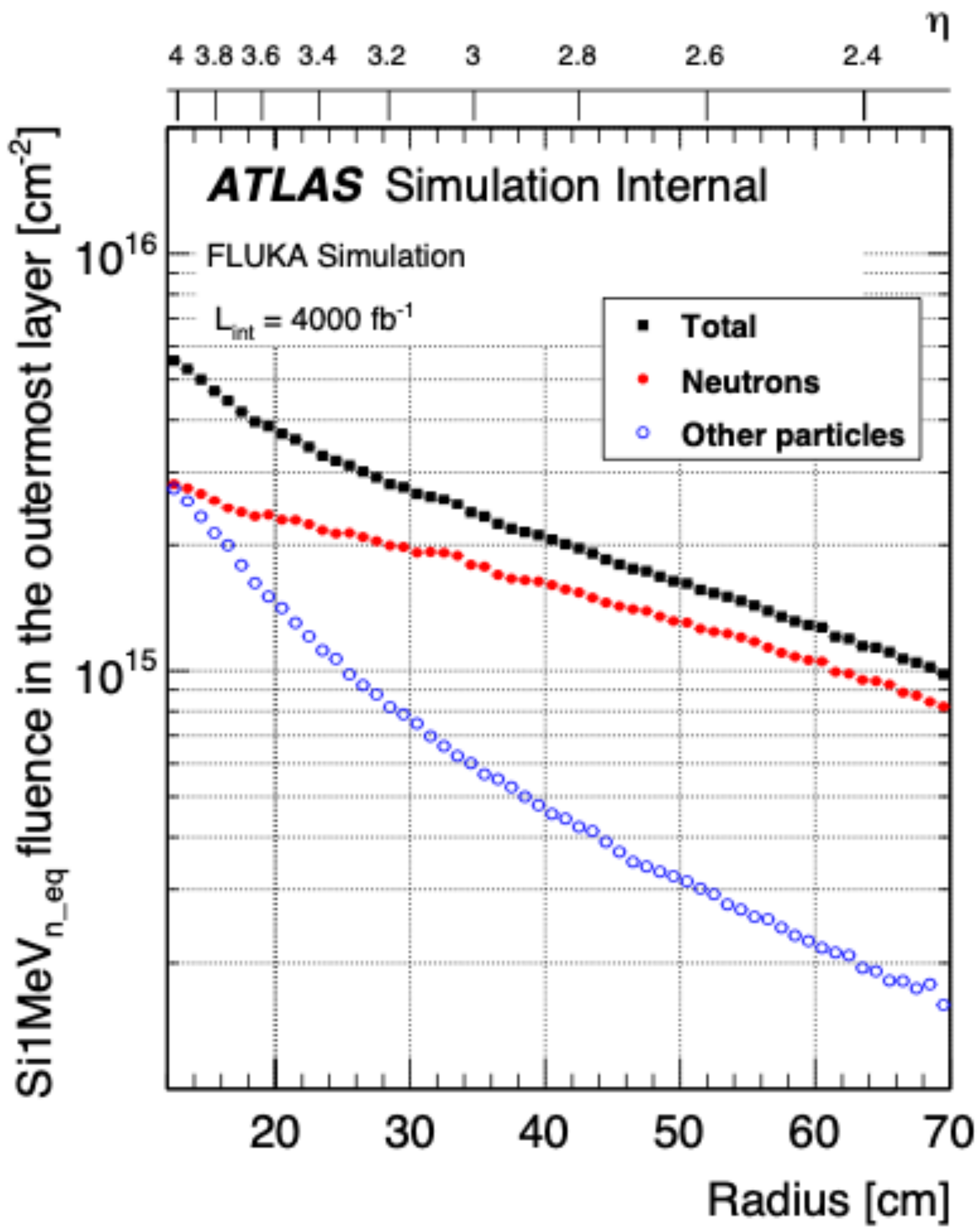
Table 5.1: Sensor parameters and requirements.

HGTD Requirements

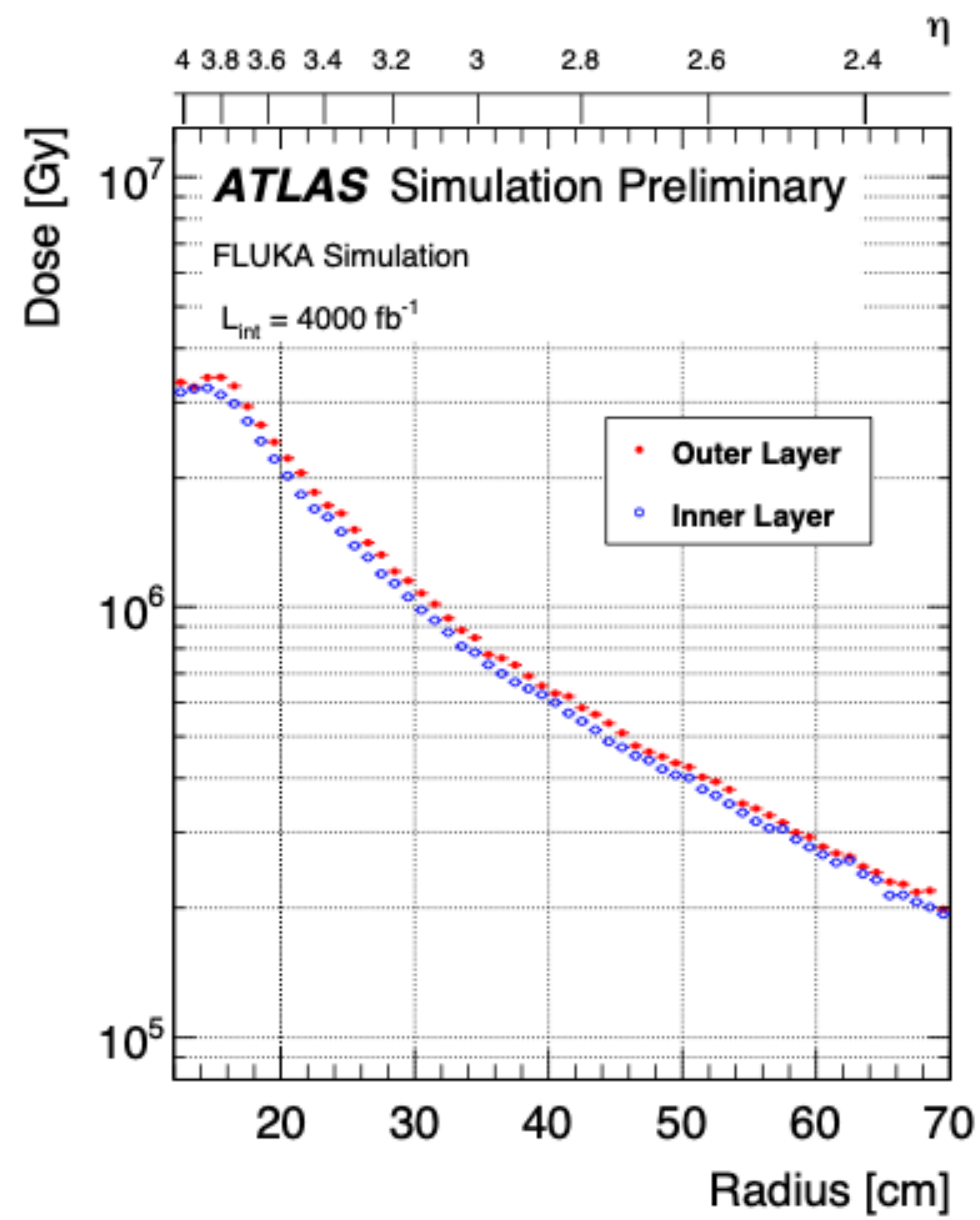
Pseudo-rapidity coverage	$2.4 < \|\eta\| < 4.0$
Thickness in z	75 mm (+50 mm moderator)
Position of active layers in z	± 3.5 m
Weight per end-cap	350 kg
Radial extension:	
Total	$110\,\text{mm} < r < 1000\,\text{mm}$
Active area	$120\,\text{mm} < r < 640\,\text{mm}$
Pad size	$1.3\,\text{mm} \times 1.3\,\text{mm}$
Active sensor thickness	50 µm
Number of channels	3.6 M
Active area	$6.4\,\text{m}^2$
Module size	30 x 15 pads ($4\,\text{cm} \times 2\,\text{cm}$)
Modules	8032
Collected charge per hit	> 4.0 fC
Average number of hits per track	
$2.4 < \|\eta\| < 2.7$ $(640\,\text{mm} > r > 470\,\text{mm})$	≈ 2.0
$2.7 < \|\eta\| < 3.5$ $(470\,\text{mm} > r > 230\,\text{mm})$	≈ 2.4
$3.5 < \|\eta\| < 4.0$ $(230\,\text{mm} > r > 120\,\text{mm})$	≈ 2.6
Average time resolution per hit (start and end of operational lifetime)	
$2.4 < \|\eta\| < 4.0$	≈ 35 ps (start), ≈ 70 ps (end)
Average time resolution per track (start and end of operational lifetime)	≈ 30 ps (start), ≈ 50 ps (end)

Table 2.1: Main parameters of the HGTD.

HGTD Irradiation fluence



(a) Nominal Si1MeV$_{n_{eq}}$ fluence for HL-LHC.



(b) Nominal ionising dose for HL-LHC.