Report on Joint test BEE-iRPC with 2D Detector

Zhen-An Liu, Jingzhou Zhao*, Pengcheng Cao, Hanjun Kou

TriggerLab, IHEP, Beijing

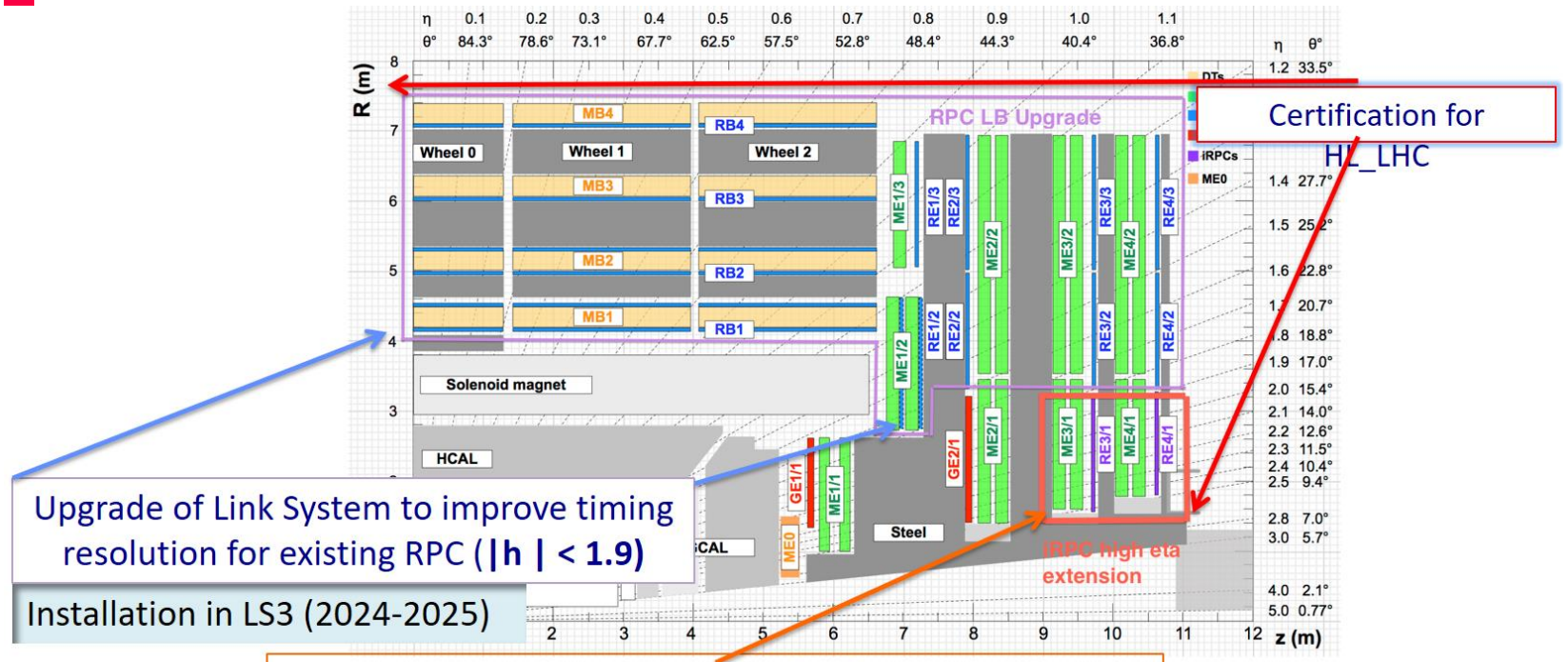
Nov.08 2020

The 6th China LHC Physics Workshop (CLHCP2020)

Outline

- CMS Phase-II RPC Upgrade Project Overview
- BEE prototype overview
- Joint test arrangement and set up
- Performance study of the RPC detector
- Summary

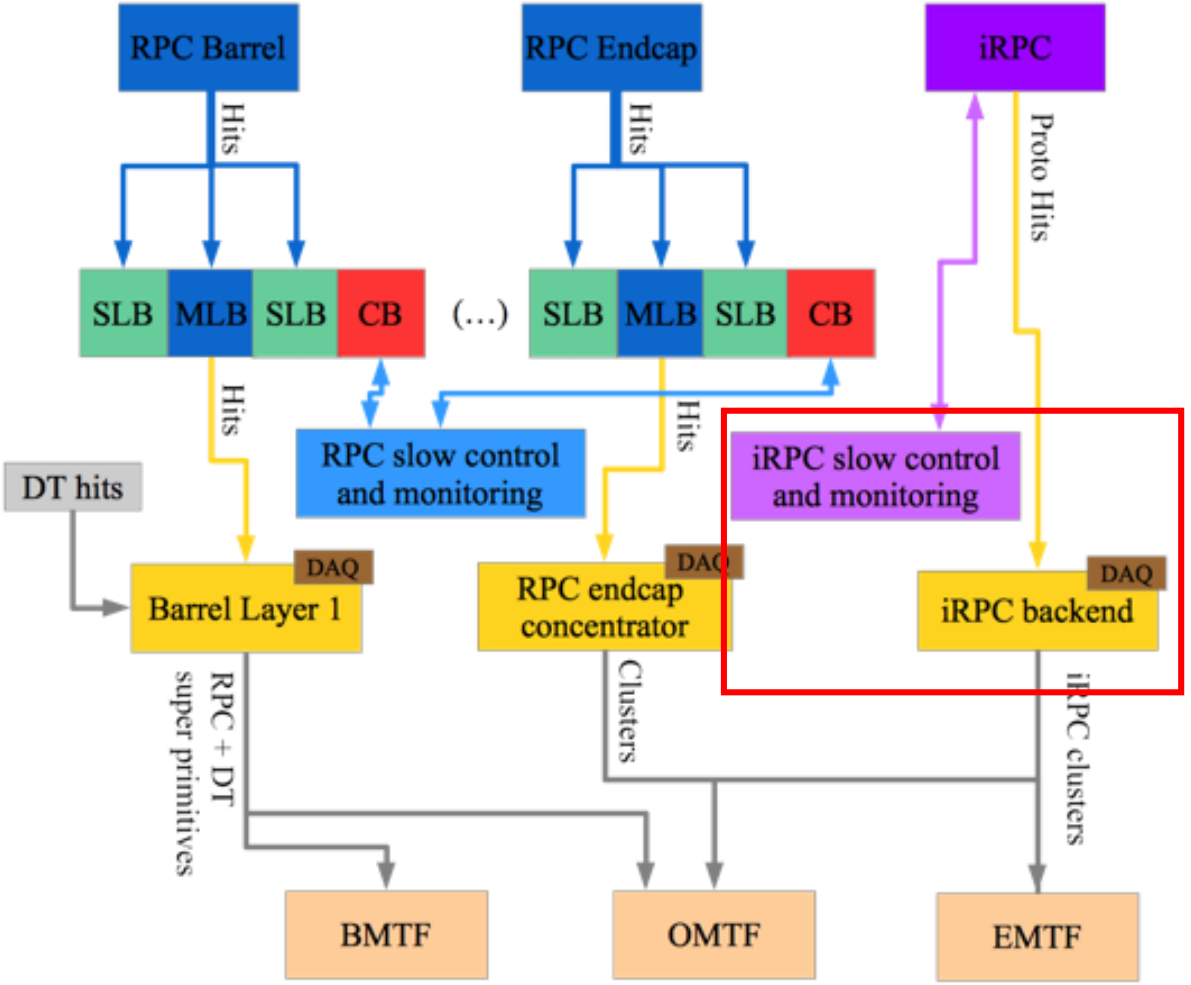
CMS Phase-II Muon RPC Upgrade



- RE3.1/4.1 (iRPC) + new design of FEBs,
- New Link System for present RPC ,
- New RPC Backend Electronic.

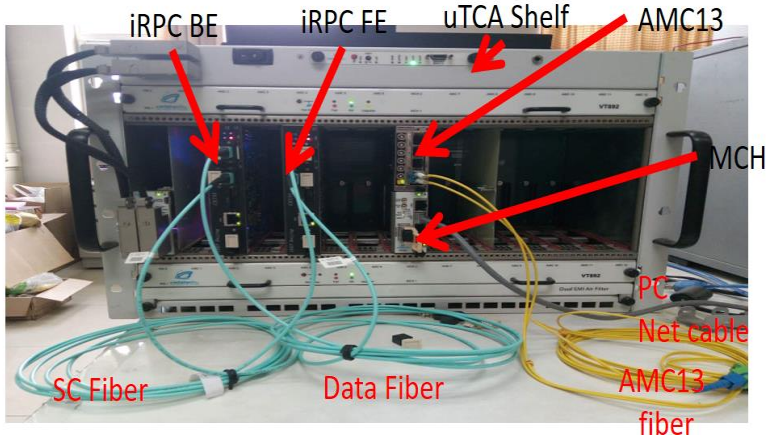
Tasks for iRPC Backend Electronics

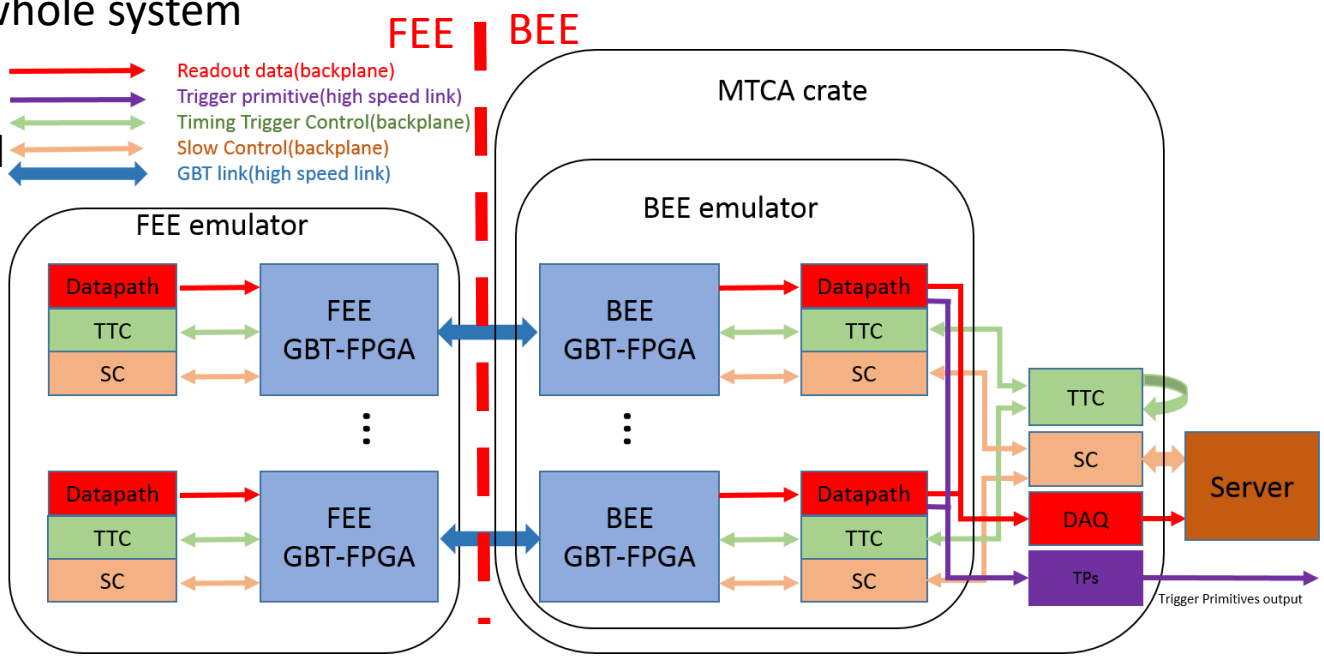
- Providing Fast and Slow Control to FEE via GBT link.
- Processing Data received from GBT link.
- Providing FEE Monitoring function.
- Producing RPC trigger primitives (cluster finding) .



Block Diagram of BEE(iRPC) Prototype

- µTCA compliant BEB,
  -core board
- a µTCA crate,
- an AMC13 card,
  -system clock and fast control
- a µTCA Carrier Hub(MCH),
  -manage the whole system
- a sever PC.
  - slow control and DAQ

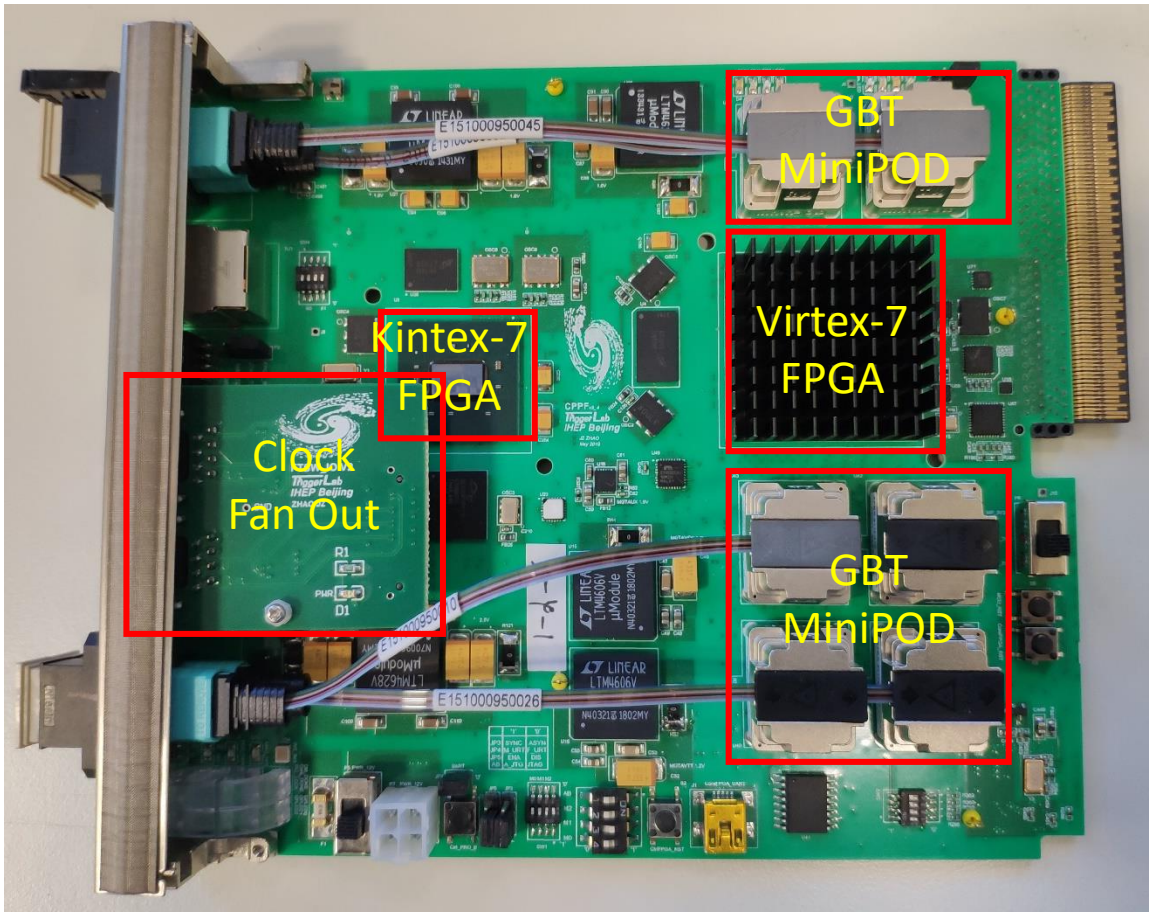




BEE prototype board

Main components:

- Virtex-7 FPGA
  - GBT-FPGA
  - Process
- Kintex-7 FPGA
  - Clock manager for BEE
- Clock module
  - Fan out clock to FEE
- MiniPODs/GTH,36 ch
  - GBT Links
  - DAQ
  - Slow Control/Fast Control

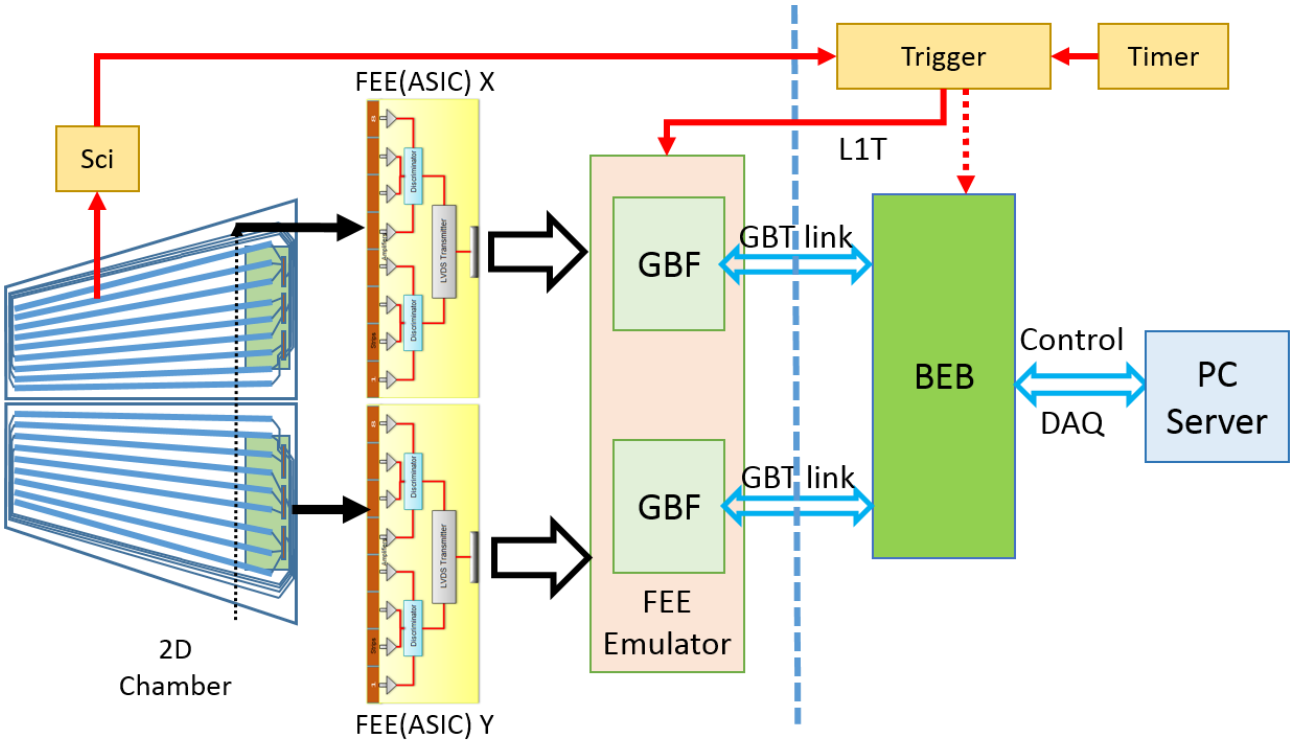


Purpose of this joint testing

- Validating the IHEP BEE-iRPC solution at CERN
  - The requirement for iRPC BEE is not well defined yet
  - The temporary functionalities are based on our IHEP understanding
- Validating the control to the FE side via GBT
- Validating basic PROCESS/FC/SC/DAQ functions of BEE
- Study the Detector Performance IF POSSIBLE

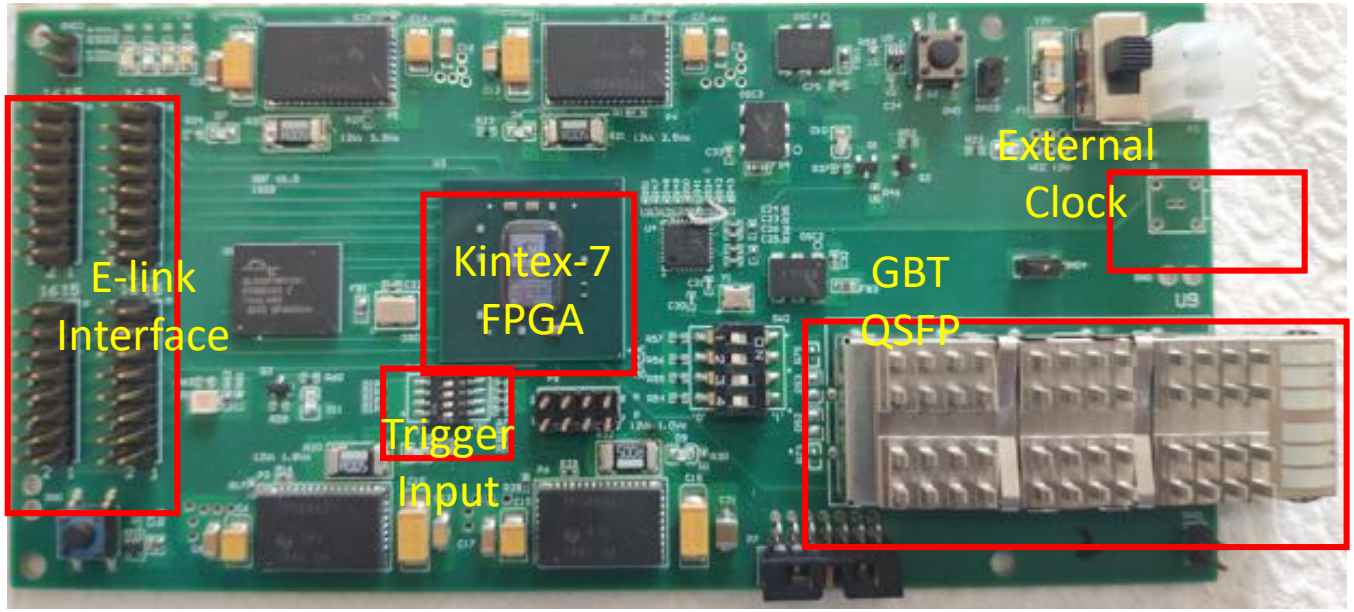
Joint test arrangement

- FEE(ASIC)-X
- FEE(ASIC)-Y
- Trigger
  - Scintillator
  - Timer
- GBF
  - Data-Collector
- BEE
- Control PC



Data Collector board

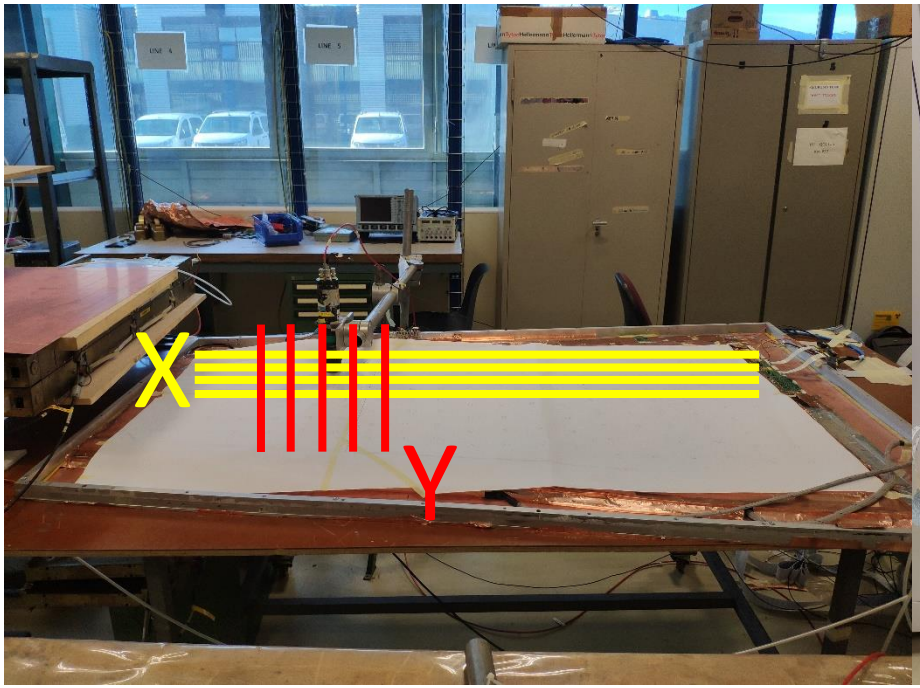
- Data Collector board is designed for join test, not part of BEE for upgrade.
- Main components are:
  - Kintex-7 FPGA: GBT-FPGA, TDC-FPGA, Rising&Falling Edge, 2.5ns
  - E-link Interface: 32 pairs of LVDS input
  - SMA Interface: External clock input from BEE
  - Trigger Interface: Pulse Generator or Scintillator
  - QSFP: 4-channel optical module, GBT link

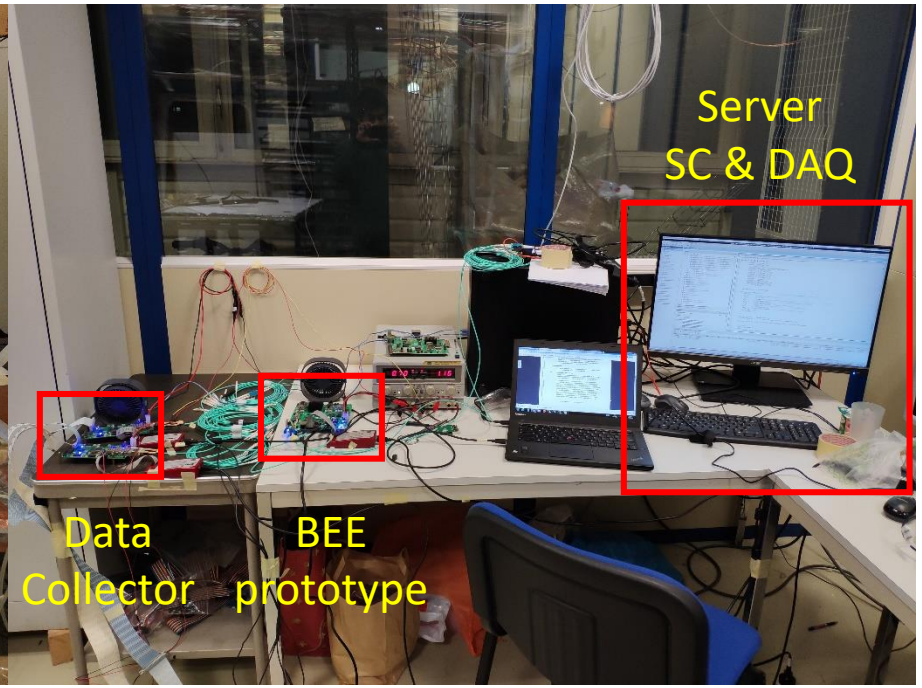


Test system set up at cern 904

- iRPC 2D chamber
  - X 16 strips, 3 dead
  - Y 10 strips, 1 dead
- Trigger: Timer/Scintillator

- one BEE board
- two Data Collector boards
  - 16 inputs each
- One server for SC and DAQ





Commissioning/System adjusting

Step1: System connection

Detector/FEE + Trig + Data Collector + BEE + PC Server

Step2: Firmware upgrade

Step3: GBT Link testing

Step4: Slow Control testing (own requirement)

Step5: Cosmic ray testing (from Scintillator)

Step6: Random trigger testing (from timer)

Step7: Trigger/Signal delay adjusting (delay signals)

Step8: Trigger Window adjusting (100ns is taken)

Step9: Data analysis/Plotting optimization

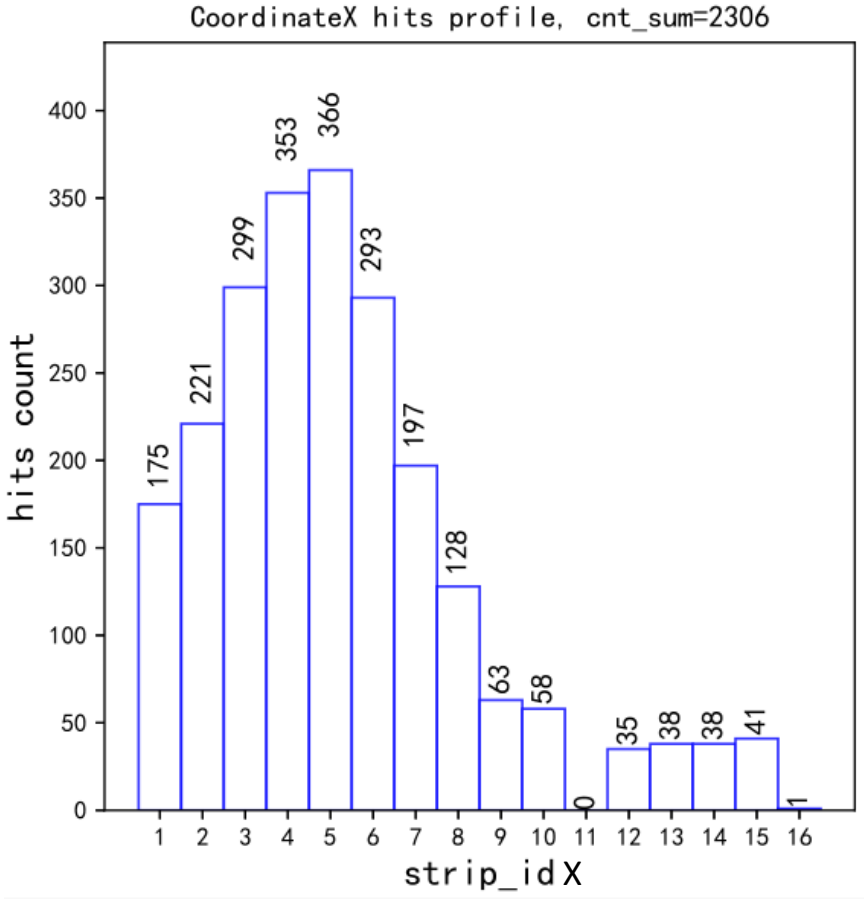
First our own plots, then added Jan's efficiency/cluster plots

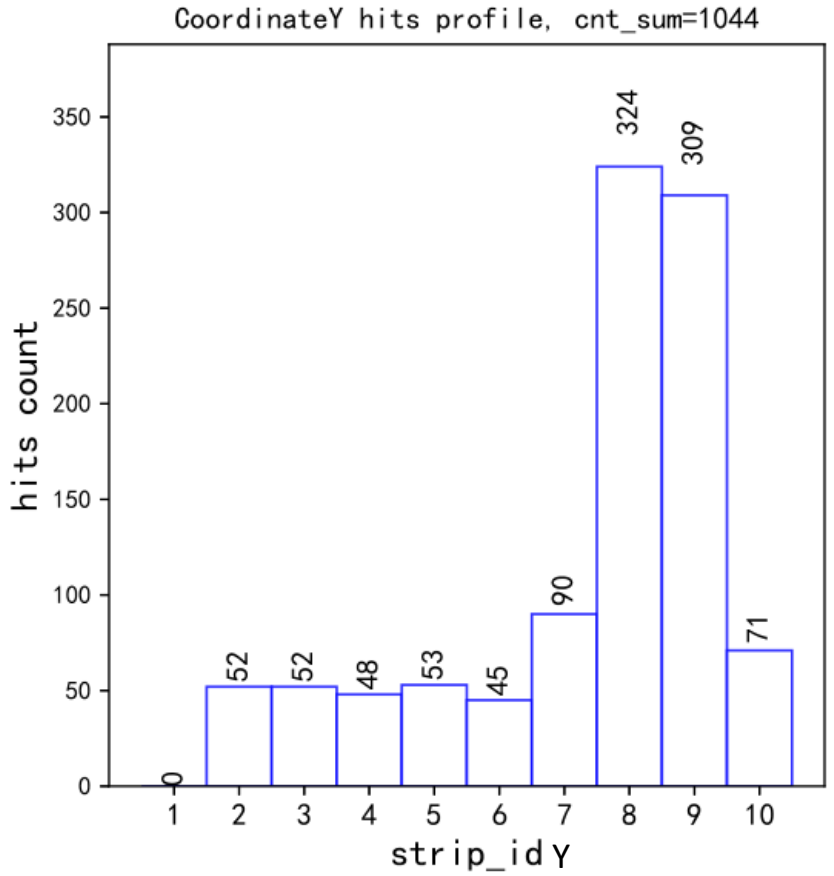
Sample of the studies-Hit profiles (X&Y)

7100HV, 1.5 hours, ~350 triggers. Scintillator located over strip_X4/X5 AND strip_Y8/9

X coordinate: 16 strips in total, 11 and 16 dead Y coordinate: 10 strips in total, 1 dead

Hit profile looks fine after interference removal



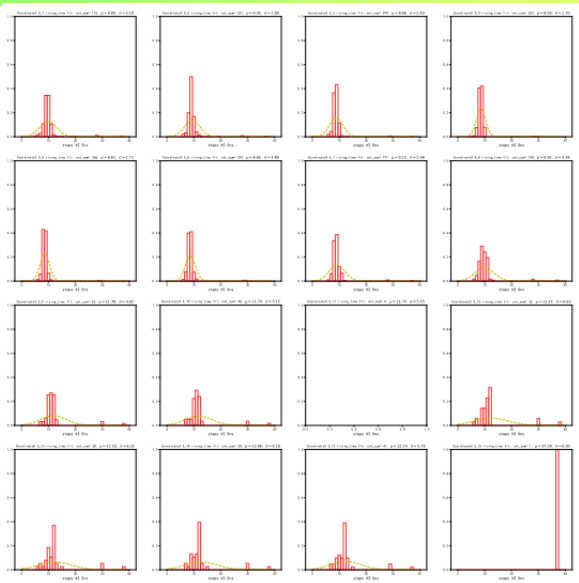


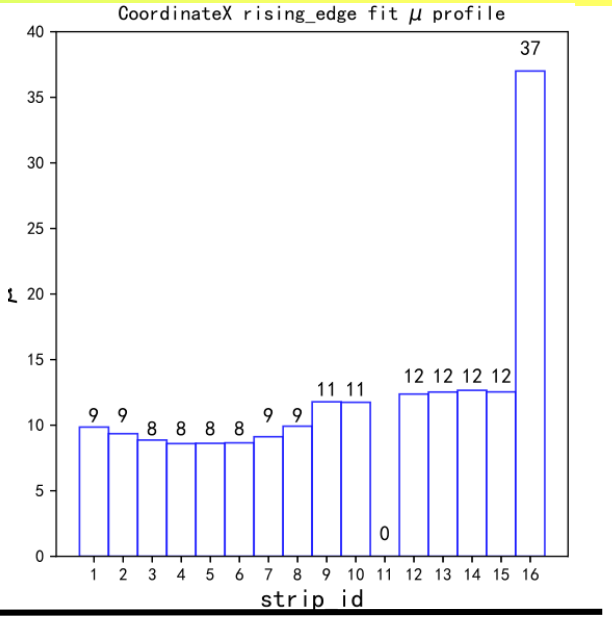
Rising and Falling Edge distribution (X)

7100HV, 1.5 hours, ~350 triggers

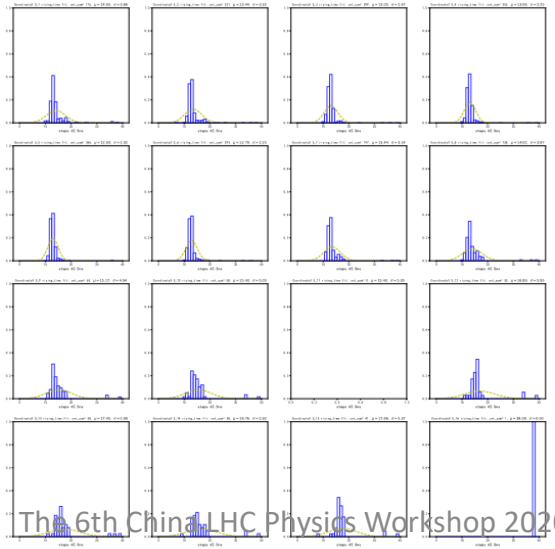
X coordinate: Best shape(X4,X5) in accordance with trigger scintillator position.

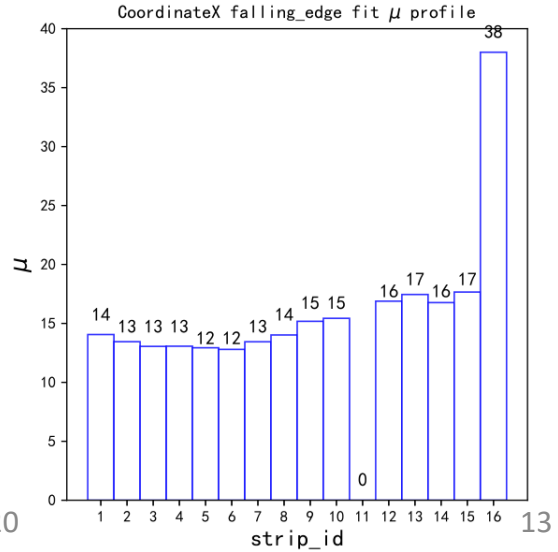
Rising





Falling



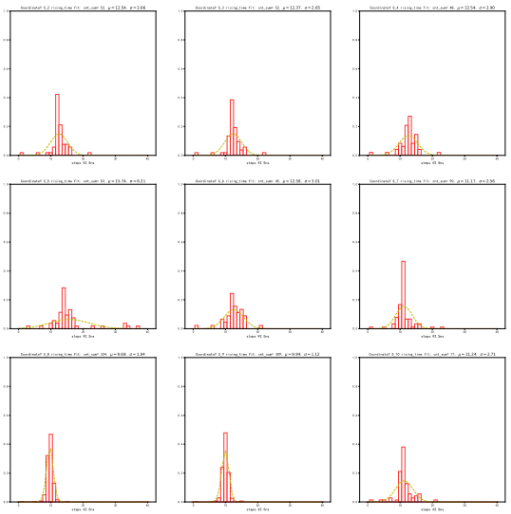


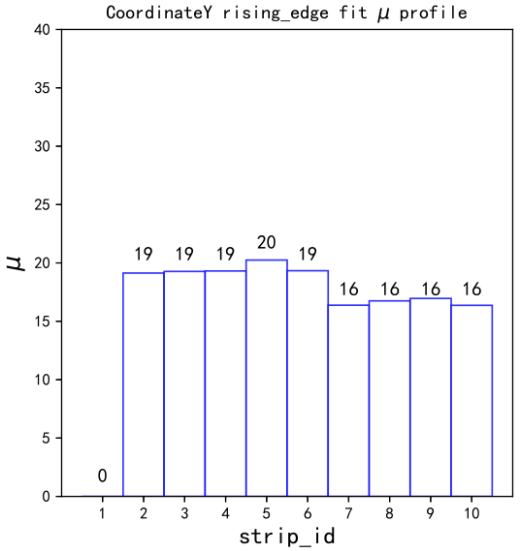
Rising and Falling Edge distribution (Y)

7100HV, 1.5 hours, ~350 triggers

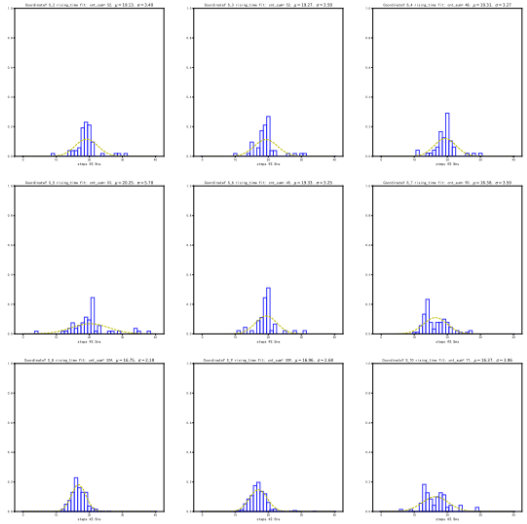
Y coordinate: Best shape(Y8,Y9) in accordance with trigger scintillator position.

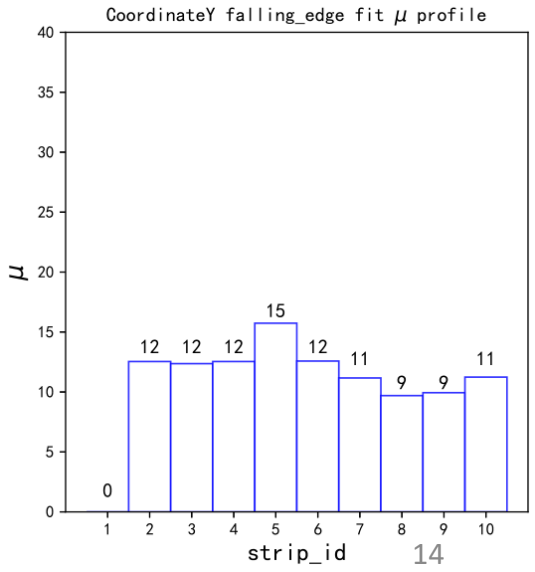
Rising





Falling

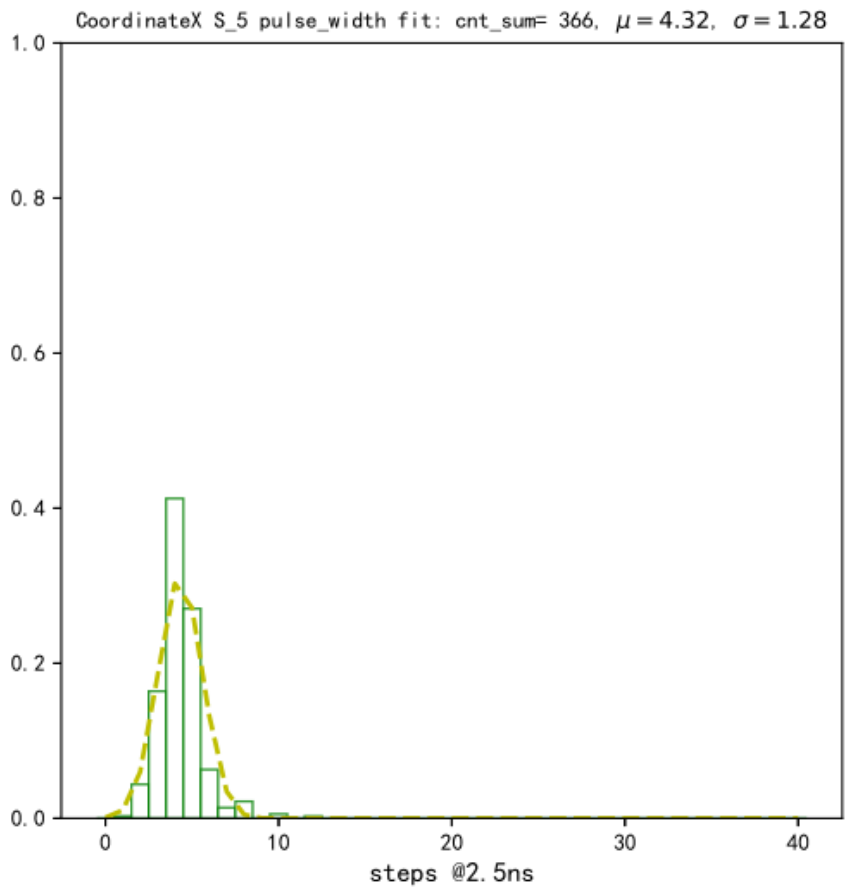


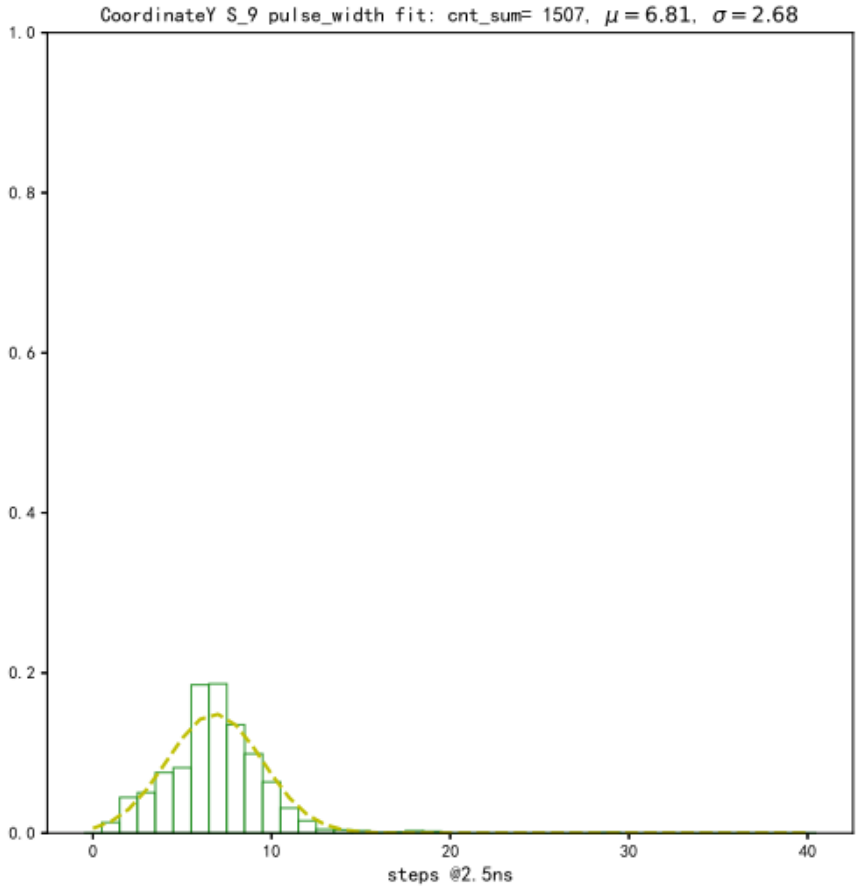


Pulse width (X&Y)

7100HV, 1.5 hours, ~350 triggers

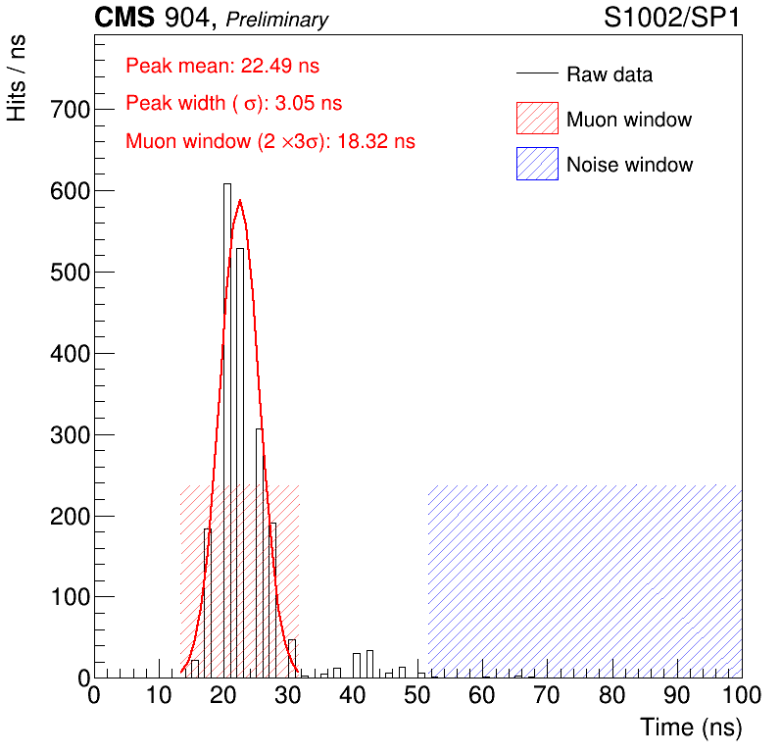
Best shape(X5,Y9) in accordance with trigger scintillator position.



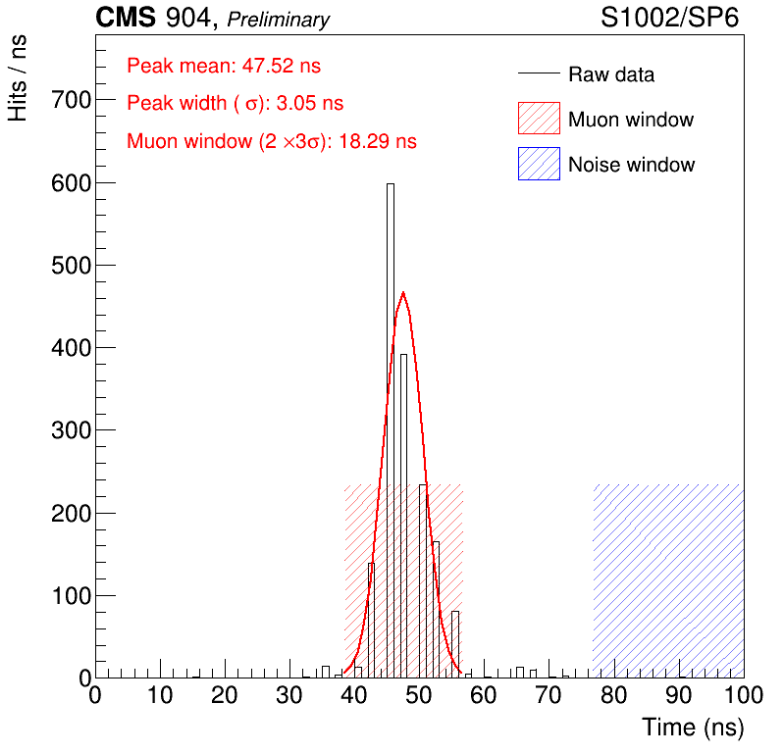


Study – Delay adjustment (7200HV)

- Trigger Window size: 100ns
- ~3 hours, 600 triggers
- Shown timing profile for X
  - Profile is shifting with different delay set by SC.



Delay value set as 22.5ns



Delay value set as 47.5ns

Study – Timing stability in X&Y (7200HV)

To evaluate the stability of the difference between this two readout path.

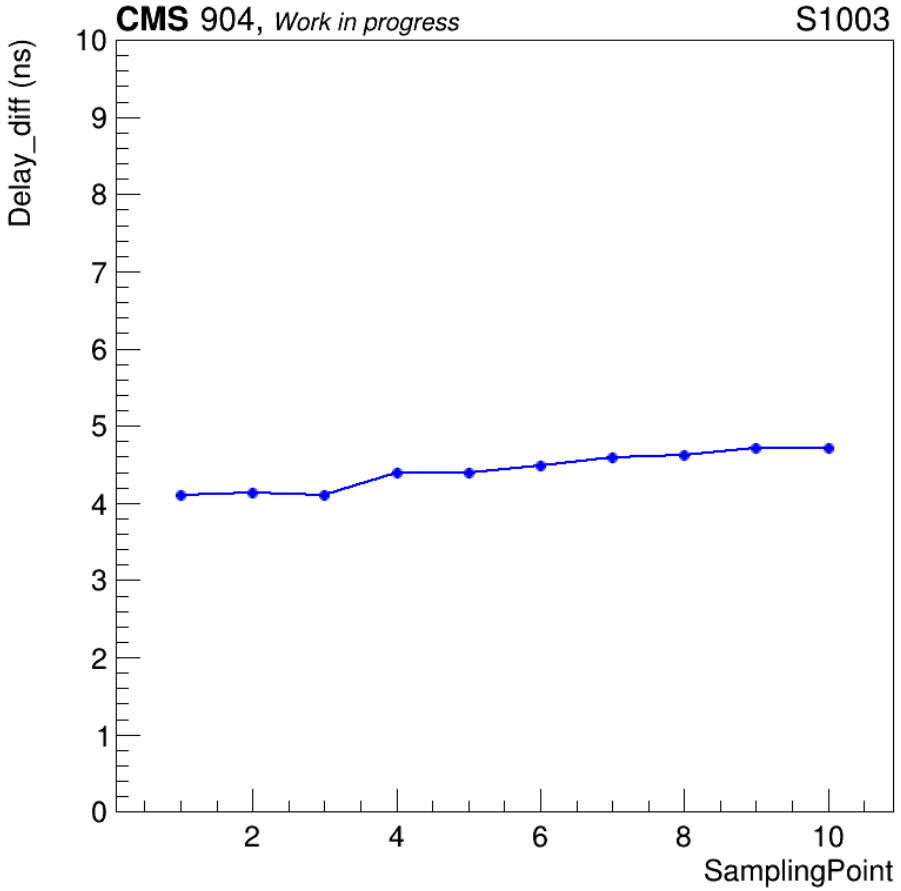
A long term run is taken:

- ~13 hours
- Trigger window 100ns
- 3000 triggers, 10 parts

Shown the delay difference of X and Y

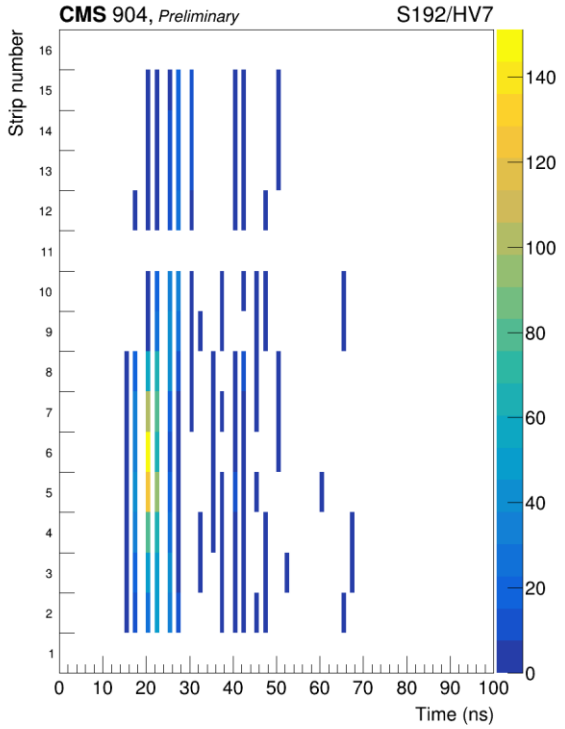
- Change within 4+1ns

This set up is working stably.

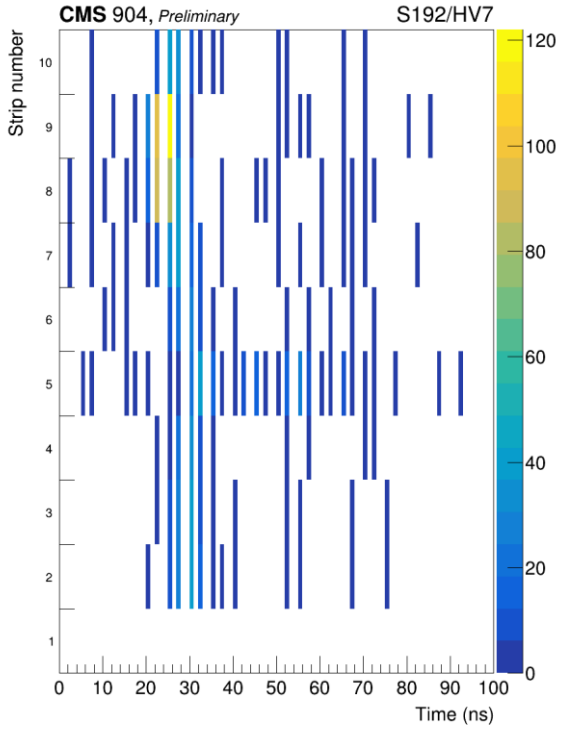


2D Timing profile for (7200HV, 300 triggers, left: X, left: Y)

- X axis: Time with respect to trigger
- X axis: 16 strips , 3 are masked
- Maximum number at strip6 AND 22ns
  - Scintillator located over strip 6
  - Strip signals are Delayed by SC



- Y axis :Time with respect to trigger
- Y axis : 10 strips , 1 is masked
- Maximum number at strip6 AND 26ns
  - Scintillator located over strip 9
  - Strip signals are Delayed by SC



Comparison with previous Run

The performances of same 2D RPC chamber with IHEP readout are studied, as seen on

- ➢New Run: HVSCAN192, BEE DAQ

  http://webdcsinfn1.cern.ch/HVSCAN/BACKEND/results/000192/

Comparison with the previous Run:

- ➢HVSCAN185(Done by Jan, with CAEN TDC):

  http://webdcsinfn1.cern.ch/HVSCAN/000160/

Are made in (next pages)

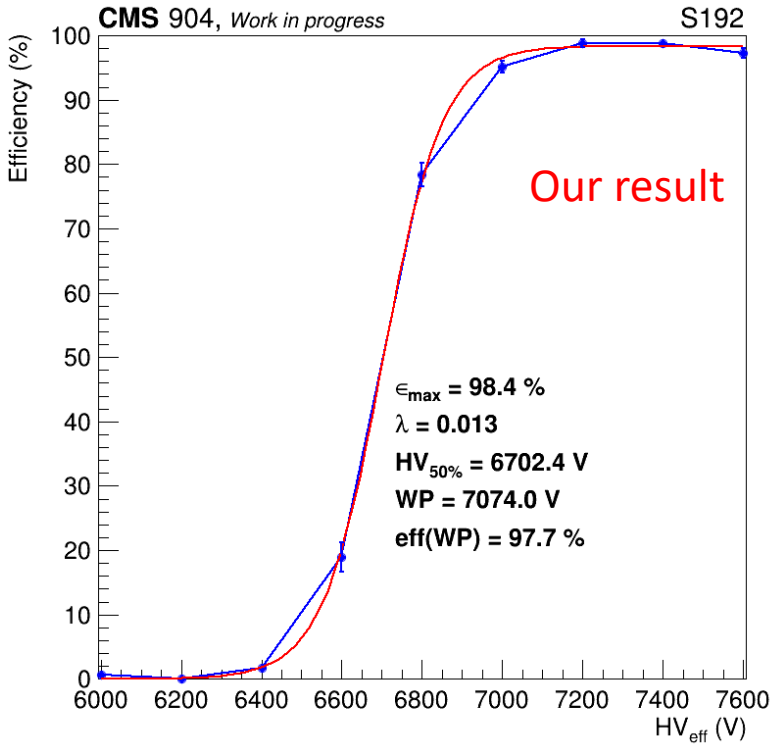
- ✓Muon efficiency

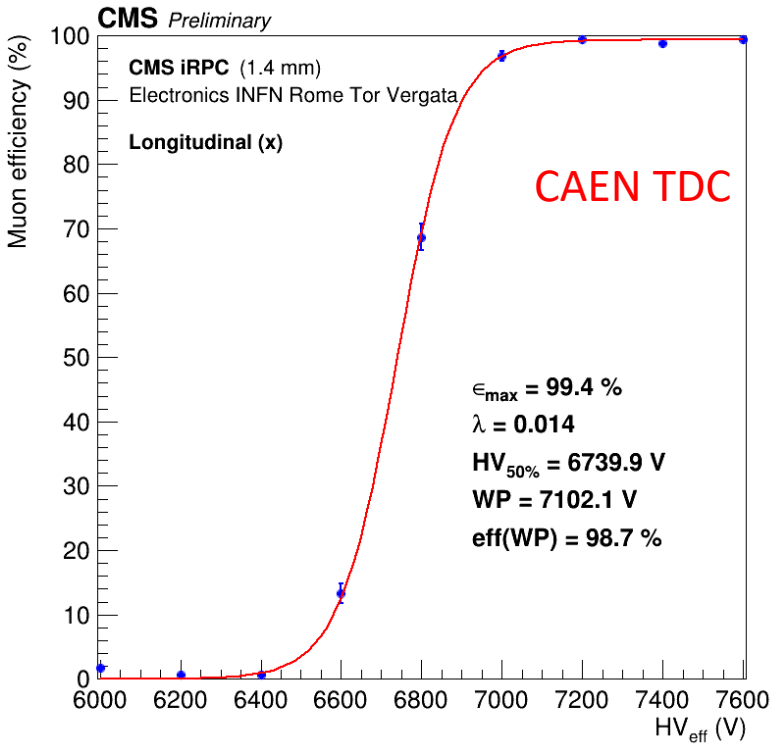
Muon Efficiency (X)

Muon efficiency for the longitudinal strips as function of high voltage.
Working at 7074V is in accordance with CAEN at 7102V with effi of 97.7 % and 98.7%.

$$E = \frac{E_{max}}{1 + e^{-\lambda (HV_{eff} - HV_{50\%})}}$$

WP = ln(19)/λ + HV(50%) + 150 V



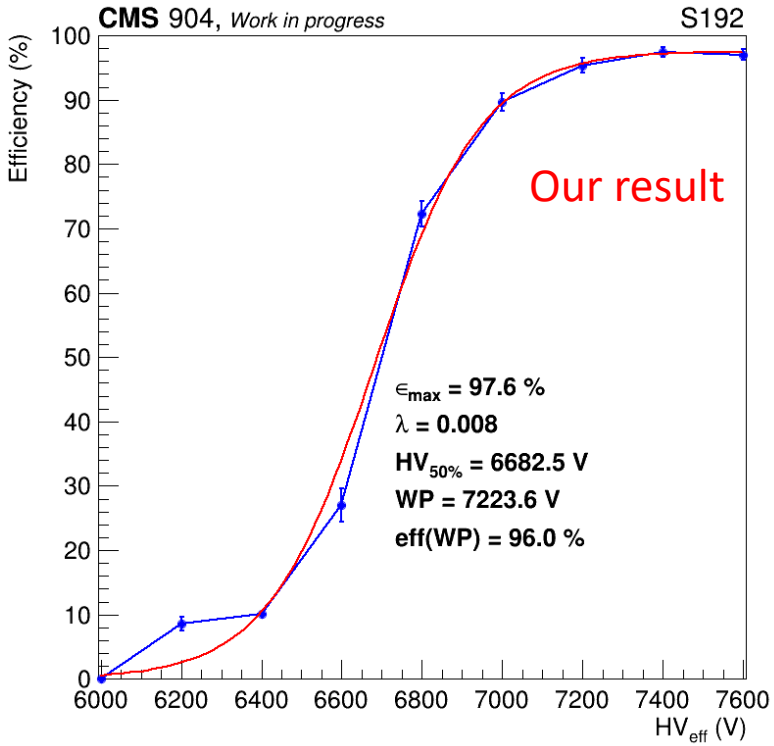


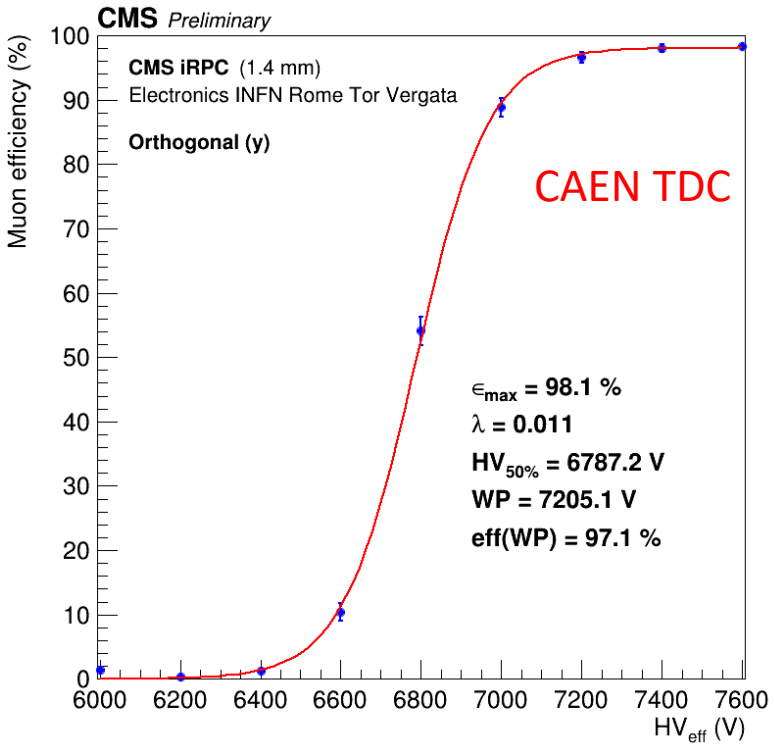
Muon Efficiency (Y)

Muon efficiency for the orthogonal strips as function of high voltage.
Working at 7223V is in accordance with CAEN at 7205V with effi of 96.0 % and 97.1%.

$$E = \frac{E_{max}}{1 + e^{-\lambda (HV_{eff} - HV_{50\%})}}$$

WP = ln(19)/λ + HV(50%) + 150 V





Summary

- BEE prototype works with Fast/Slow Control and Trigger/DAQ with IHEP understanding so far.
- Joint tests with the RPC 2D real size chamber are successful.
  - Two GBT links have been used for this chamber.
  - Both Rising and Falling edges of signals are measured.
  - Delay of the strip signal is configurable via Slow Control.
  - Window of trigger signal is configurable via Slow Control.
  - Readout long term stability is measured (<1ns jitter, 13 hours).
- Chamber performances are studied, in good agreement with the previous Run160 by CAEN TDC system
  - Muon efficiency