ALICE Upgrade

Zhong-Bao Yin

(Central China Normal University)

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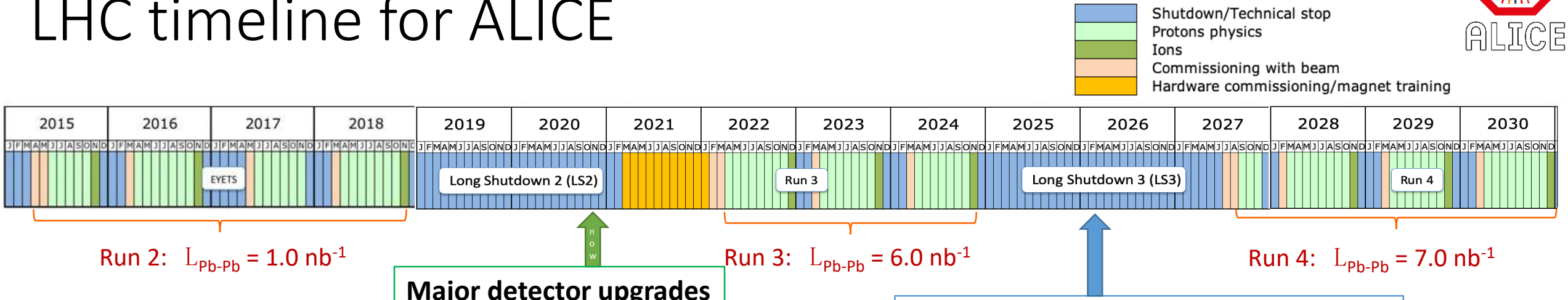
Outline

- Overview on ALICE detector upgrade programs
- Ongoing detector upgrade during LS2
- Further detector upgrade for RUN4
- Summary and outlook

LHC timeline for ALICE



ALICE strategy for Run 3 + Run 4:

- **50 kHz Pb-Pb interaction rate (Run 2 <10 kHz)**
- **Collect L_{Pb-Pb} = 13 nb^{-1}**

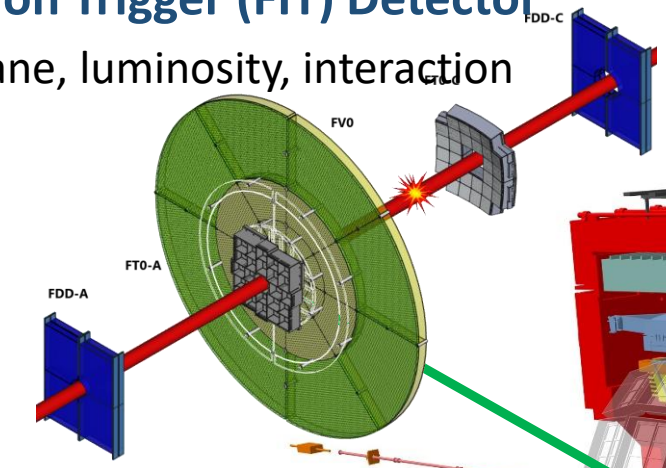
ALICE physics goals driving the upgrade requirements – rare probes and high precision

- **Heavy-flavour hadrons (down to very low p_T) → mechanism of quark-medium interaction**
- **Charmonium states → dissociation/regeneration as tool to study de-confinement and medium temperature**
- **Dileptons from QGP radiation and low-mass vector mesons → χ symmetry restoration, initial temperature and EOS**
- **High-precision measurement of light and hyper-nuclei → production mechanism and degree of collectivity**
- **……**

Ongoing Major detector upgrade

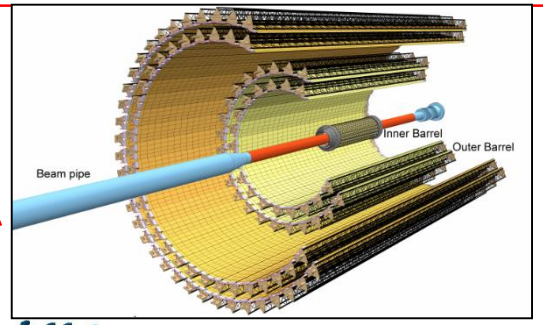
New Fast Interaction Trigger (FIT) Detector

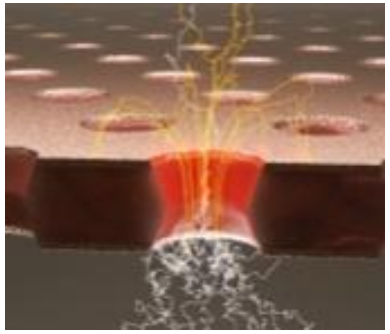
-Centrality, event plane, luminosity, interaction time



New Inner Tracking System (ITS)

-CMOS pixel, MAPS technology
-Improved resolution, less material, faster readout





New TPC Readout Chambers (ROCs)

-Gas Electron Multiplier (GEM) technology
-New electronics (SAMPA), continuous readout

with our contribution

Readout upgrade

-TOF, TRD, MUON, ZDC, Calorimeters

Integrated Online-Offline system (O^2)

-Record MB Pb-Pb data at 50 kHz

New Muon Forward Tracker (MFT)

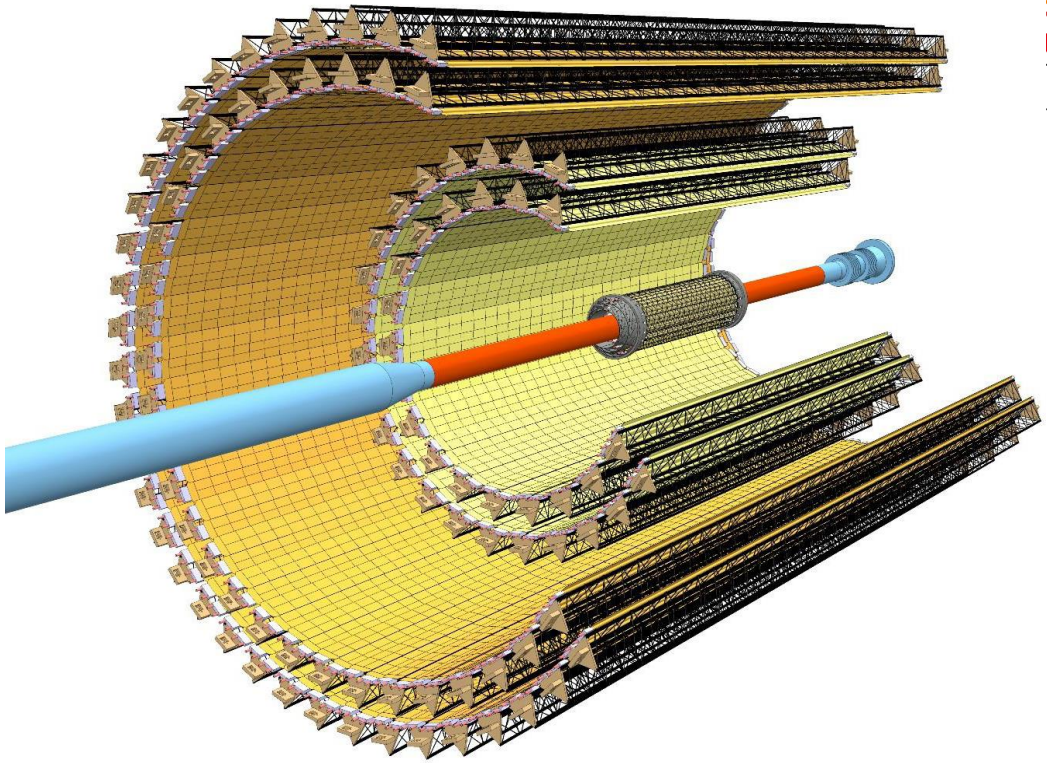
-CMOS Pixels, MAPS technology
-Vertex tracker at forward rapidity

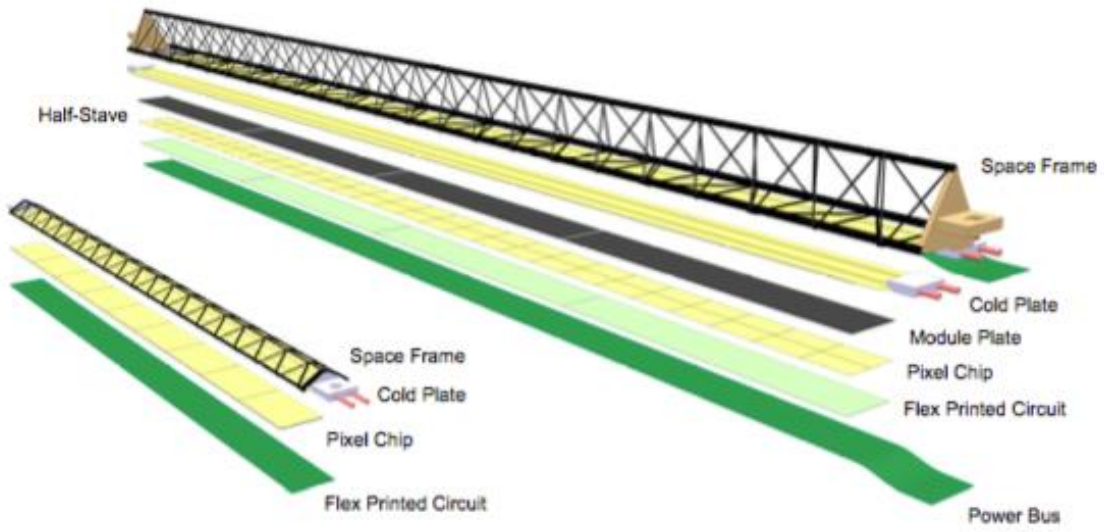
ITS upgrade during LS2 (ITS2)

Improving tracking performance at low p_T

- 7-layer barrel fully equipped with dedicated Monolithic Active Pixel Sensors (**MAPS**): **ALice PIxel DEtector (ALPIDE)**
  - Inner Barrel
    - 3 Inner Layers (48x 9-chip Staves)
    - Material per layer: **~0.35% X_0**
  - Outer Barrel
    - 2 Middle Layers (54x 8-module Staves)
    - 2 Outer Layers (90x 14-module Staves)
    - Material per layer: ~ 0.8% X_0

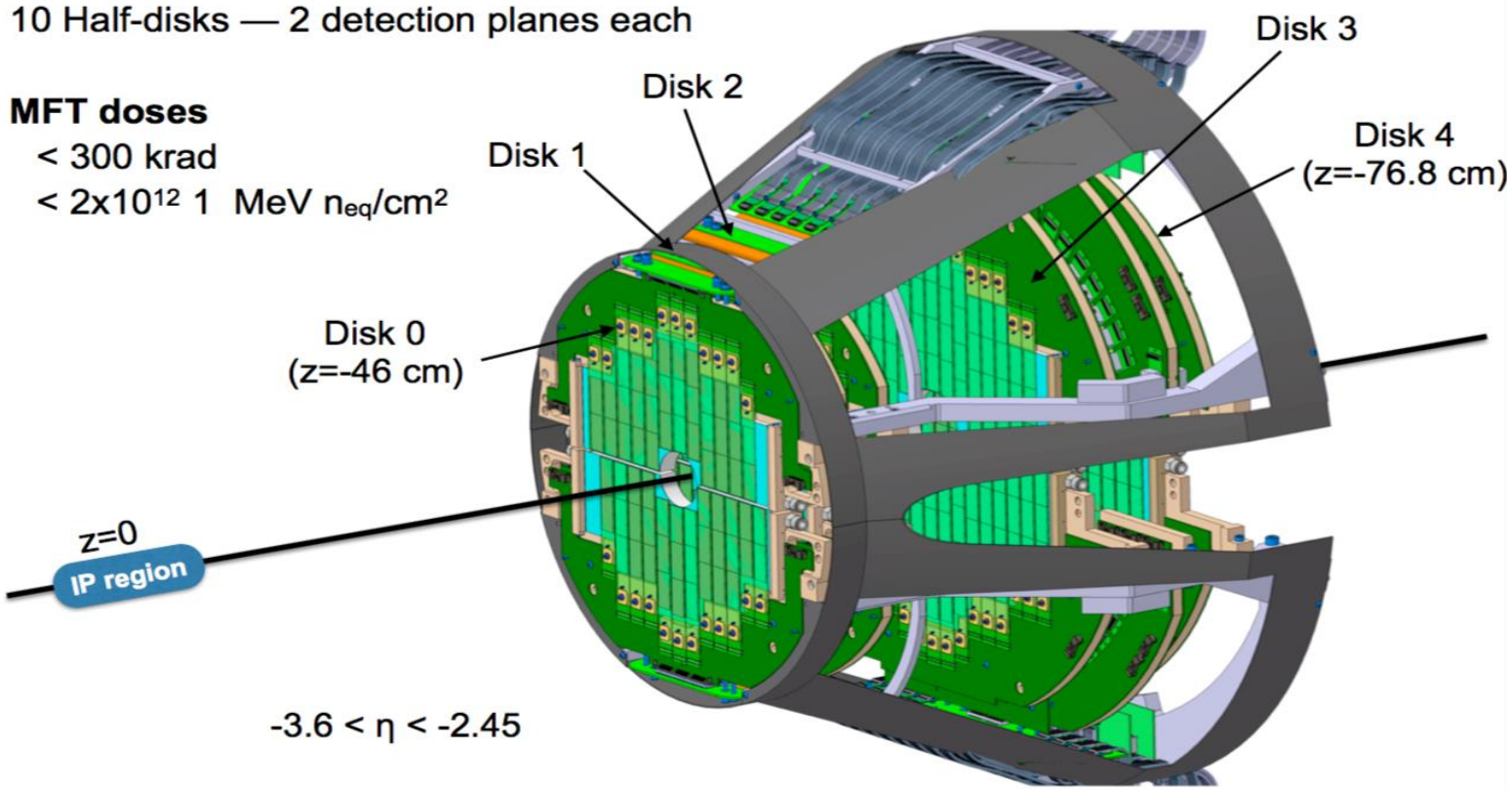
- Radial coverage: 23 – 400 mm
- η coverage: $|\eta| \leq 1.3$
- Total active area about 10 m^2
- 24,000 pixel chips (12.5G pixels)
- Spatial resolution: 5 μm

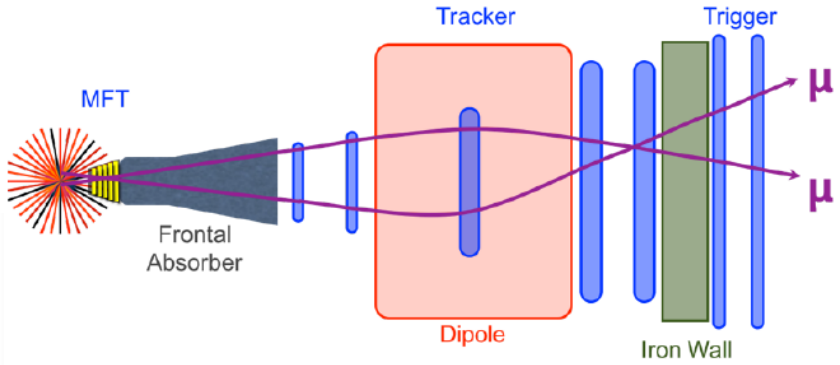




Muon Forward Tracker (MFT)

Add precise vertexing capabilities to muon tracking at forward rapidity





- **Based on same MAPS as ITS upgrade**
- 2212 chips in total
- 5 disks with 2 planes on each disk
- Enables better matching to vertex

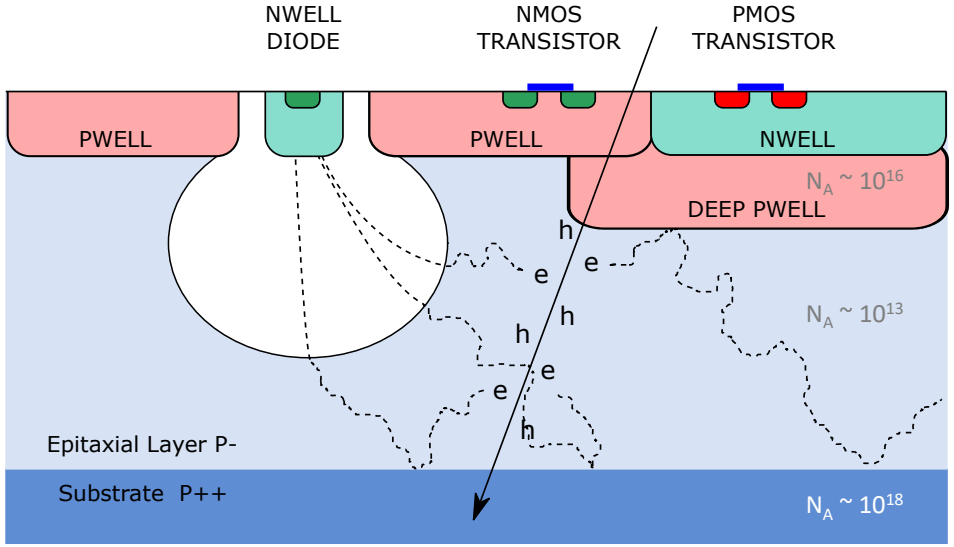
- **Charm/beauty separation possible**
- **Improved mass resolution**

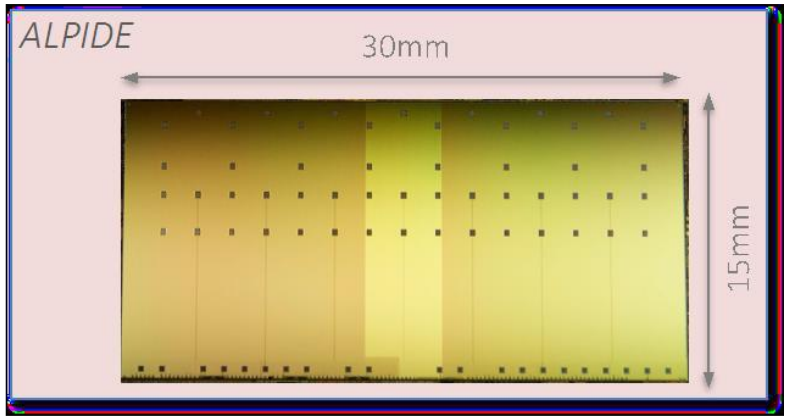
The ALPIDE sensor

the core of the new ITS and MFT

IB&MFT: 50 μm thick
OB: 100 μm thick

Pixel Sensor produced using 0.18μm CMOS Imaging Process



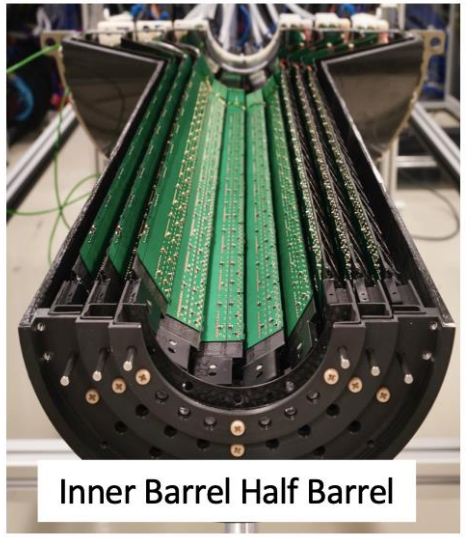


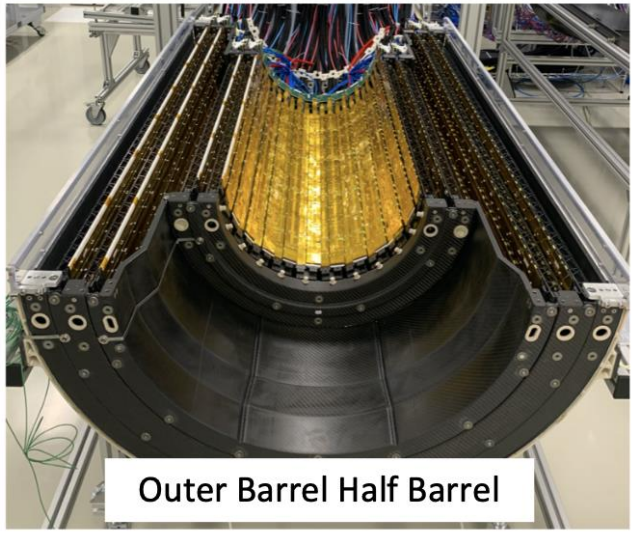
High speed serial data output (HSO)
- OB: 400 Mbit/s
- IB: 600 Mbit/s or 1.2 Gbit/s

- **High-resistivity (> 1 kΩ cm) p-type epitaxial layer (25 μm) on p-type substrate**
- **Small n-well diode (2 μm diameter), ~100 times smaller than pixel => low capacitance (~fF) and low noise**
- **Reverse-bias voltage (-6 V < V_{BB} < 0 V) to substrate (contact from the top) to increase depletion zone around n-well collection diode**
- **Deep p-well shields n-well of PMOS transistors**

- Pixel Matrix: 1024 cols x 512 rows
- Pixel pitch: 29 μm x 27 μm
- Ultra-low power: ~40 mW/cm^2
- Event-time resolution: < 4 μs
- Detection efficiency > 99%
- Fake hit rate << 10^{-6}/pixel/event
- Space resolution: 5 μm
- Max particle rate: 100 MHz/cm^2
- Trigger rate: 100 kHz Pb-Pb, 1 MHz pp
- Continuous or triggered readout
- Radiation tolerant: > 270 krad TID, >1.7x10^{12} 1 MeV n_{eq}/cm^2 NIEL

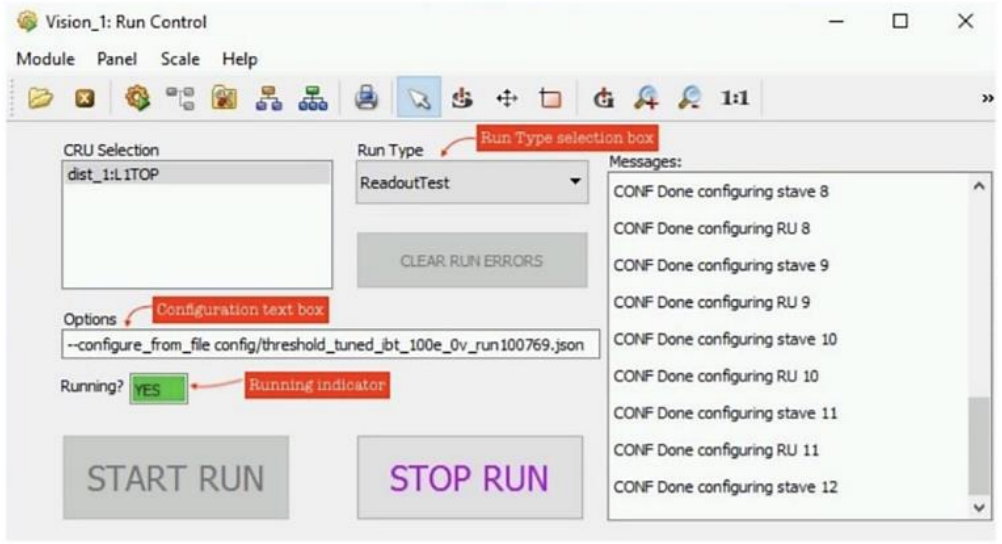
ITS upgrade status


Inner Barrel Half Barrel

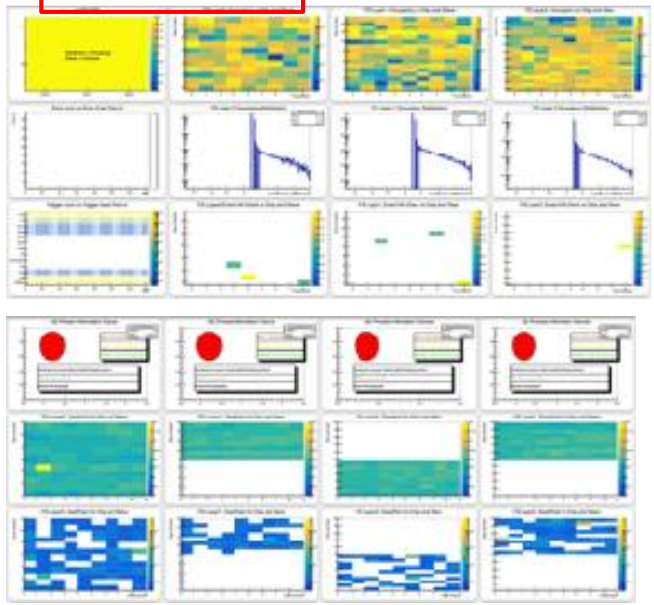

Outer Barrel Half Barrel

Inner and outer barrels fully assembled and under test on surface

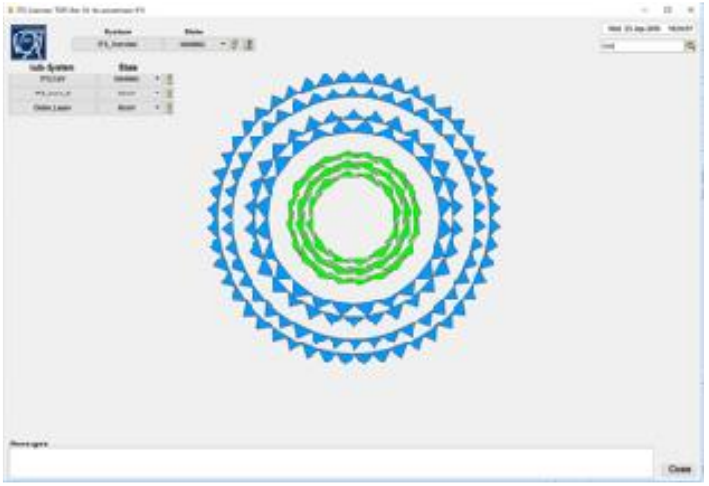
DAQ station



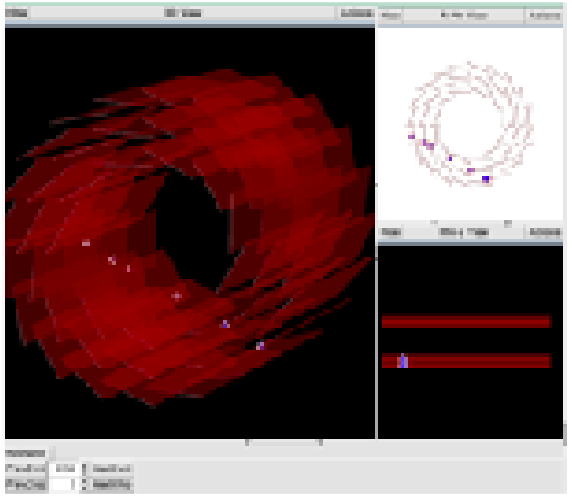
QC analysis



DCS

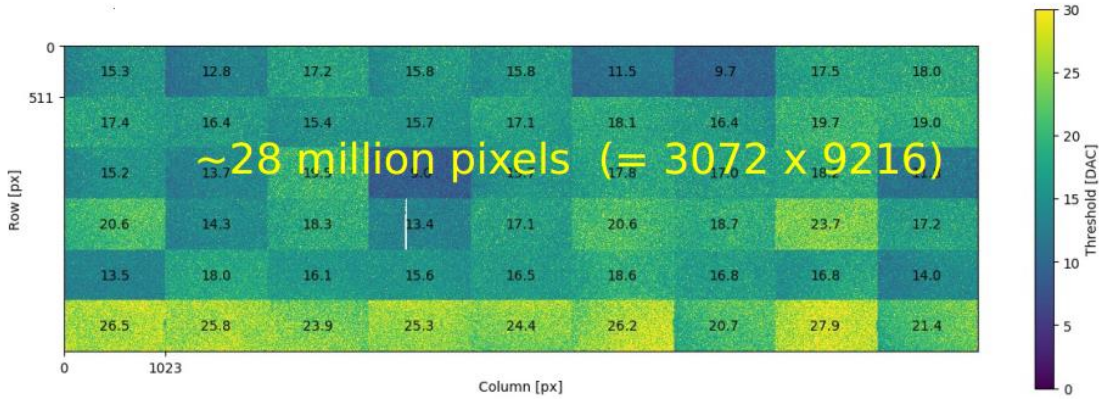


Track reconstruction software



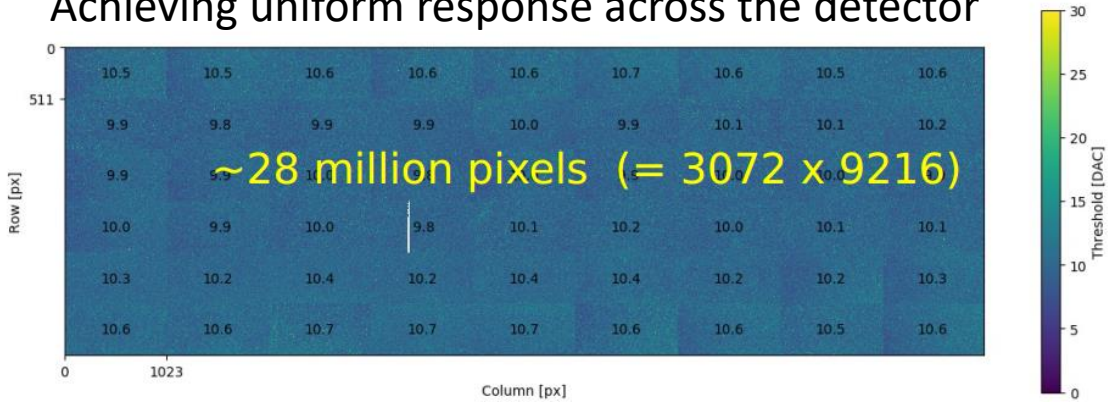
ITS upgrade commissioning - IB

Tuning threshold by adjusting frontend parameters

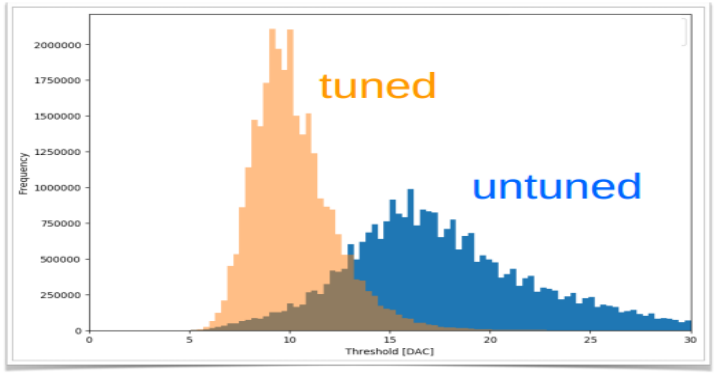


before

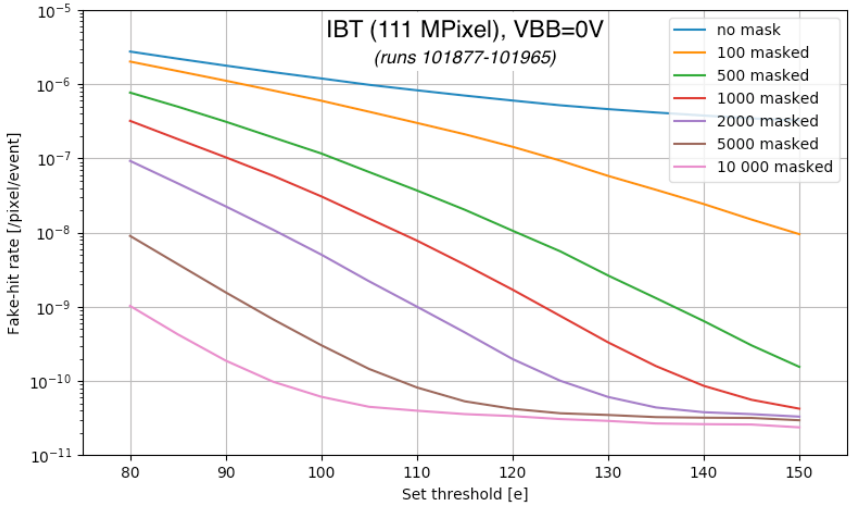
Achieving uniform response across the detector



after



Fake hit rate vs threshold



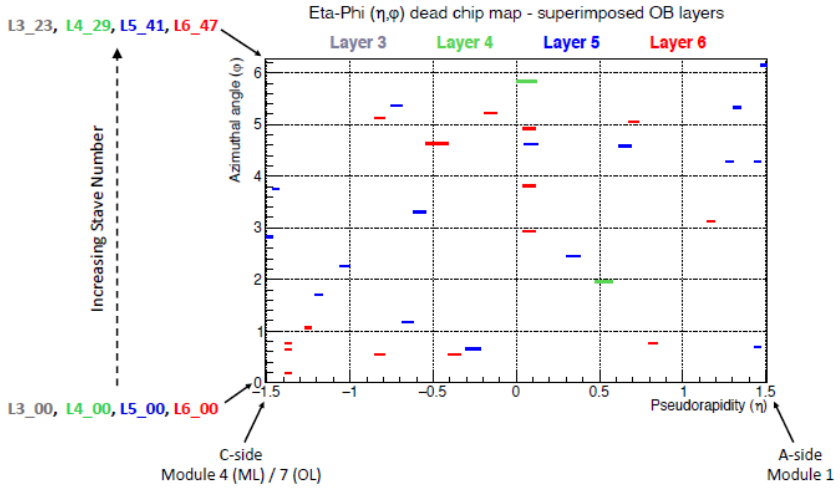
Achieved <10^{-10} /pixel/event by masking a small fraction of pixels

Study cluster and track parameters and alignment via cosmic rays

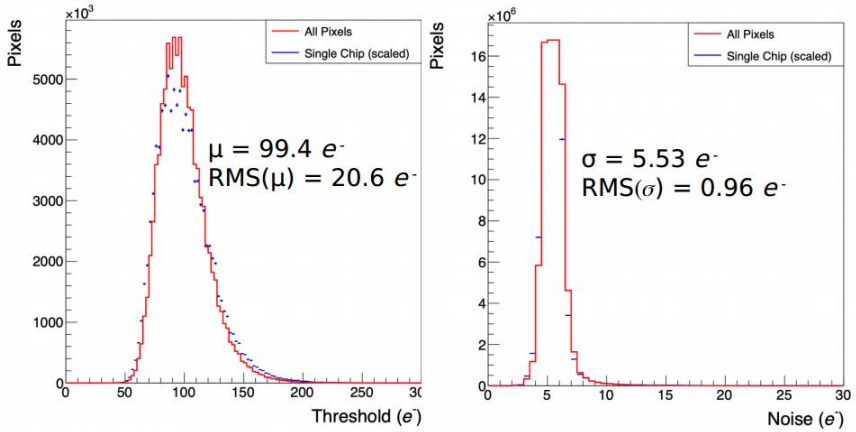
1 week of shift operation (1400 cosmics)

Cosmic tracks in one half layer of the Inner Barrel

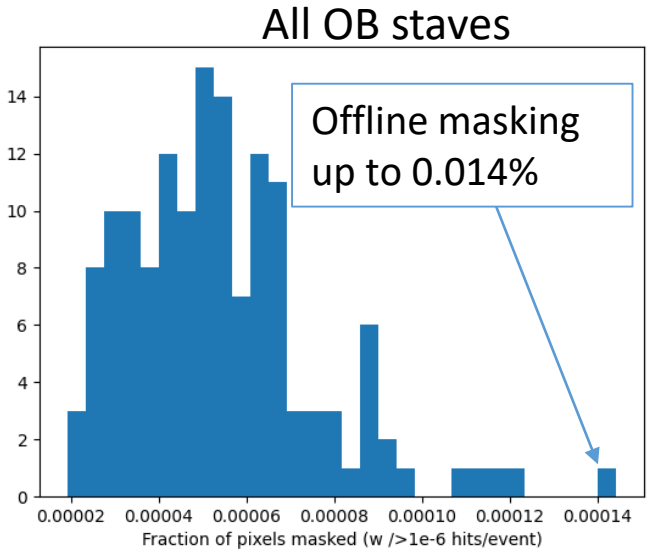
ITS upgrade commissioning - OB

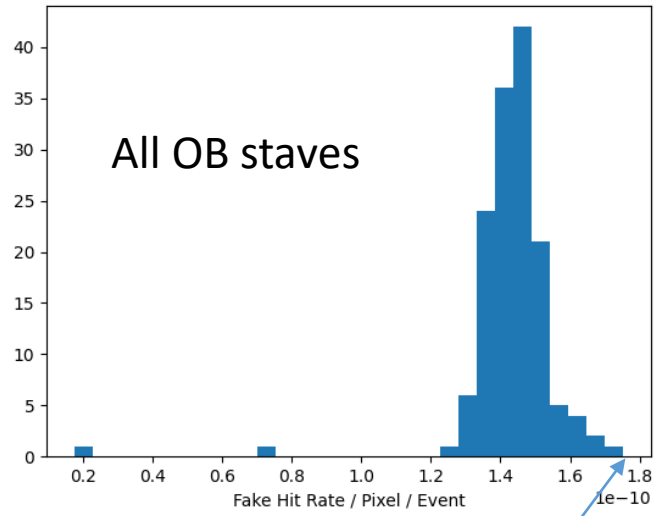


- Dead chips: 32 (over 23688) → Percentage: 0.14%
- No overlap in polar direction

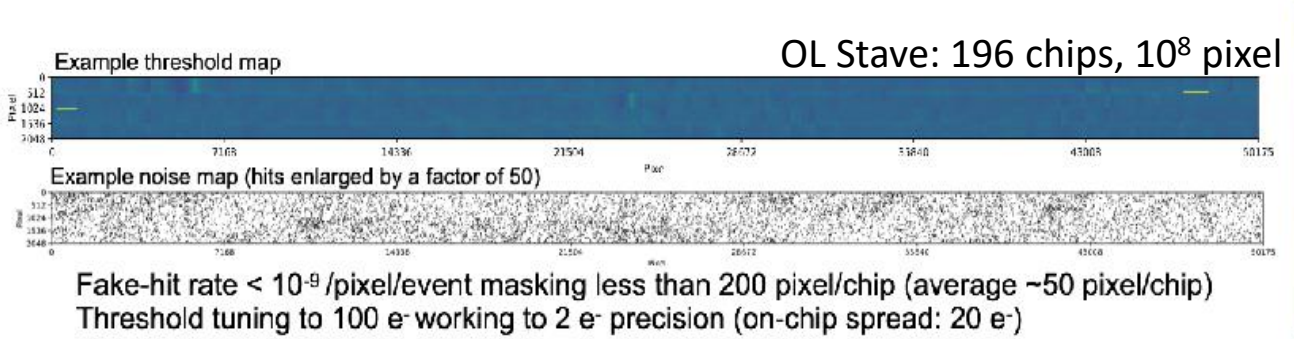


Threshold and noise after tuning an OL stave (~100 M pixels) compared to test data from a single chip





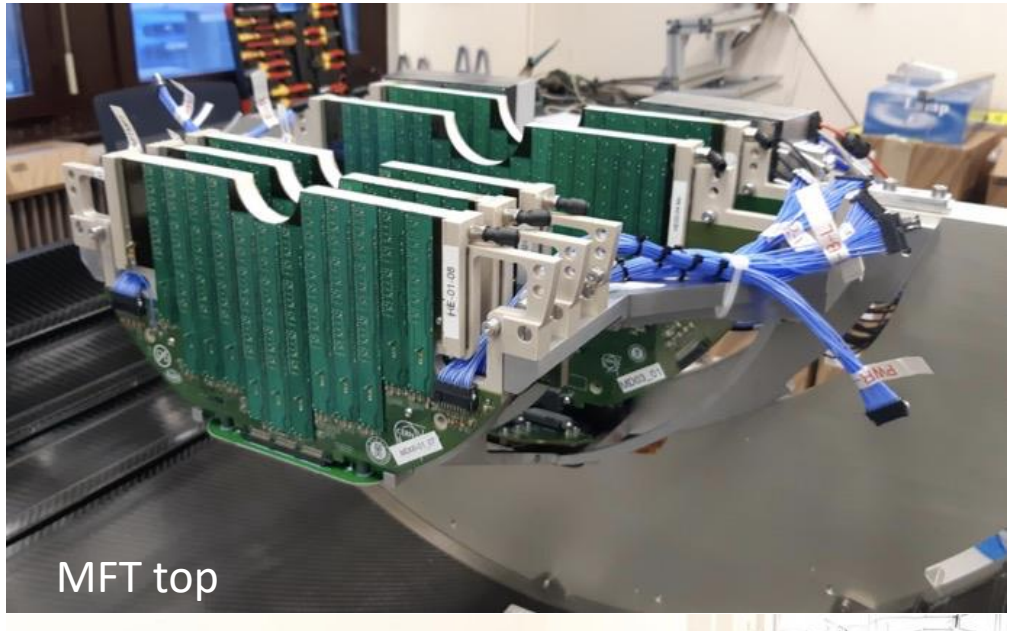
Resulting noise performance: FHR < 2×10^{-10}/pixel/event
→ Well below requested FHR 10^{-6} /pixel/event

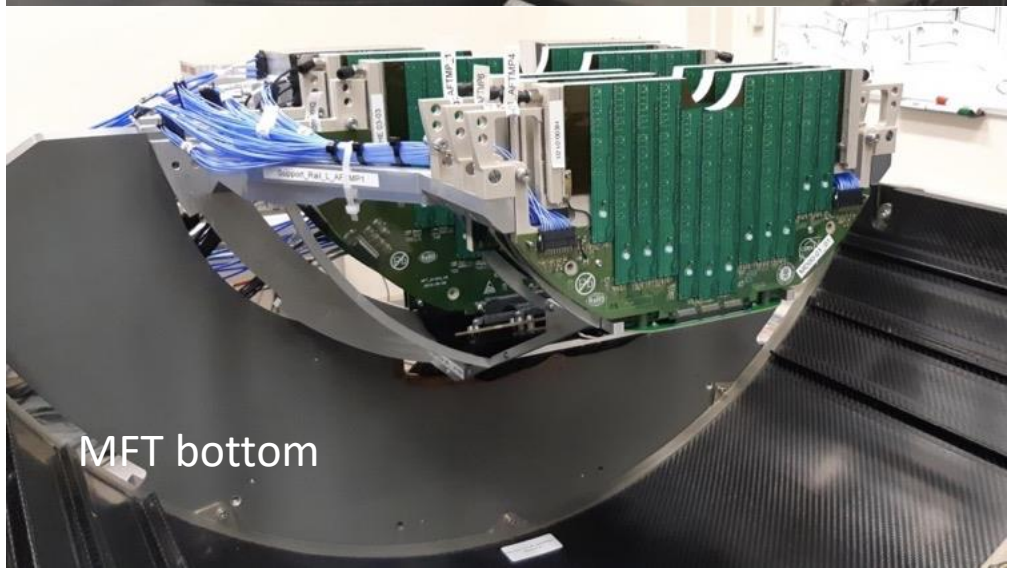


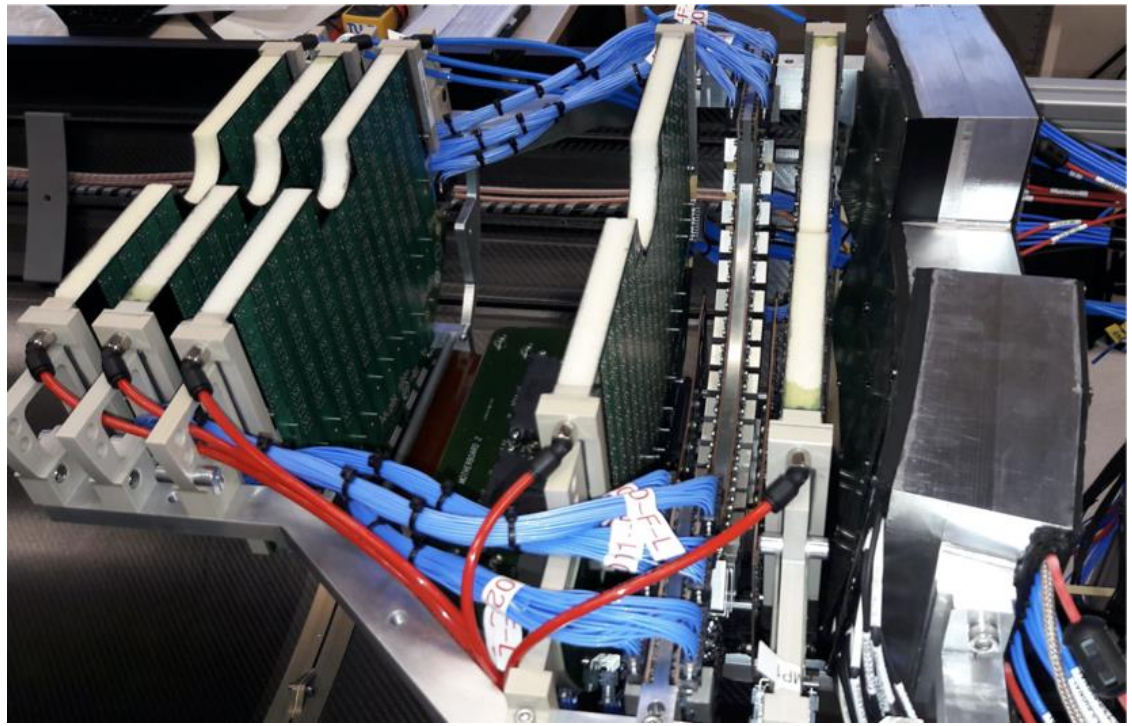
Fake-hit rate < 10^{-9} /pixel/event masking less than 200 pixel/chip (average ~50 pixel/chip)
Threshold tuning to 100 e⁻ working to 2 e⁻ precision (on-chip spread: 20 e⁻)

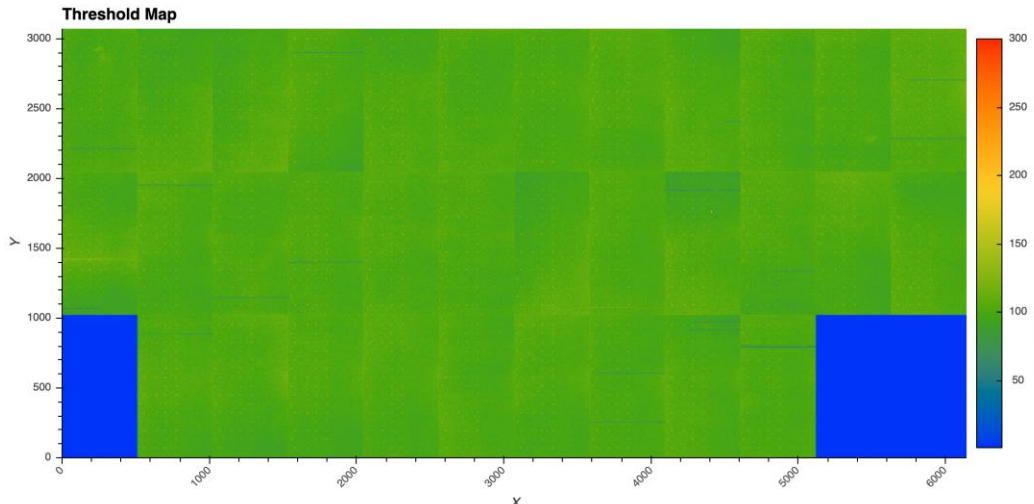
MFT status

MFT is fully assembled and integrated with FIT, ready for installation


MFT top


MFT bottom

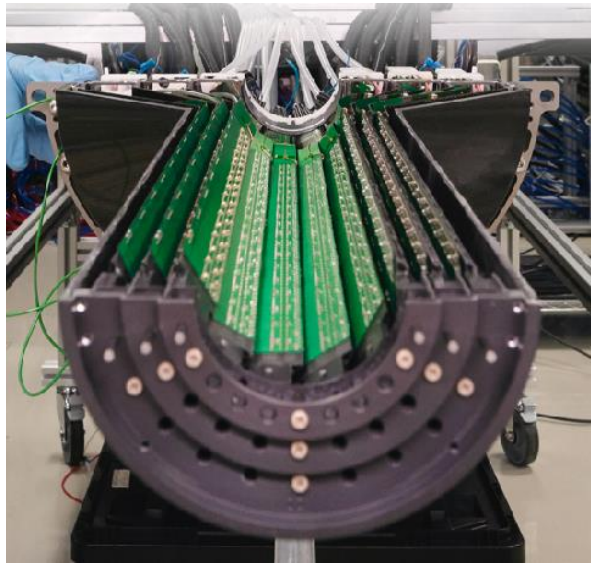


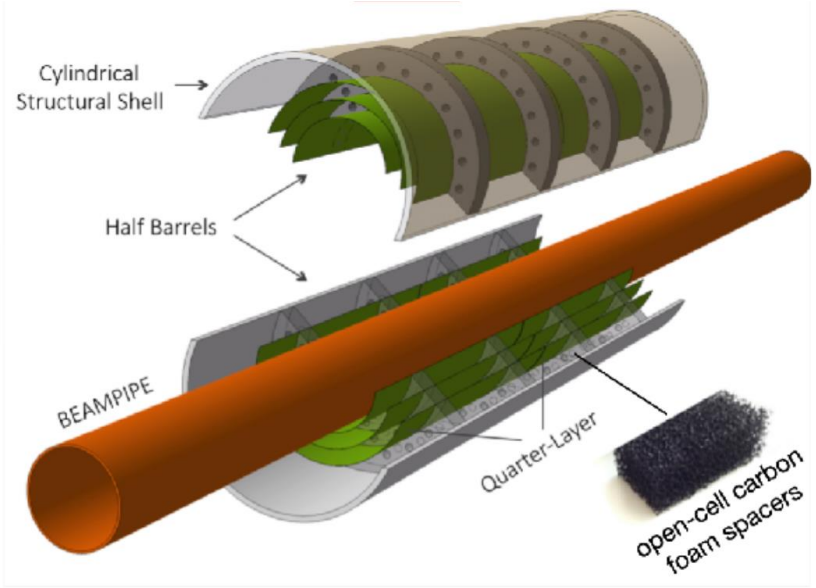


Homogeneous threshold and low noise

ALICE detector upgrade for LS3

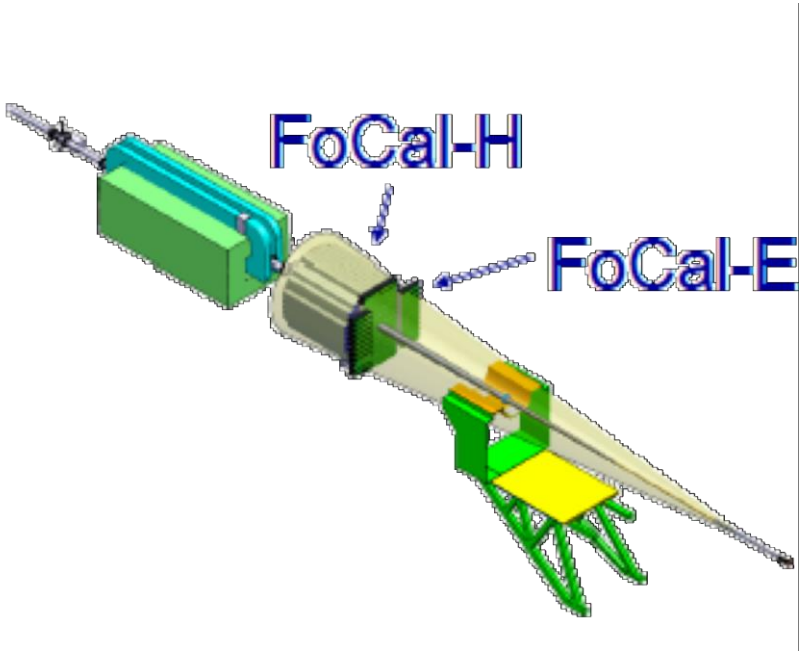
ITS3





- **ITS3**: Replace the 3 inner layers with three truly cylindrical layers based on **curved** ultra-thin sensors
- Closer to beam pipe: 23→18 mm
- Less material: 0.35 % → ~ 0.03 % X_0
- Resolution improved further by factor of 2

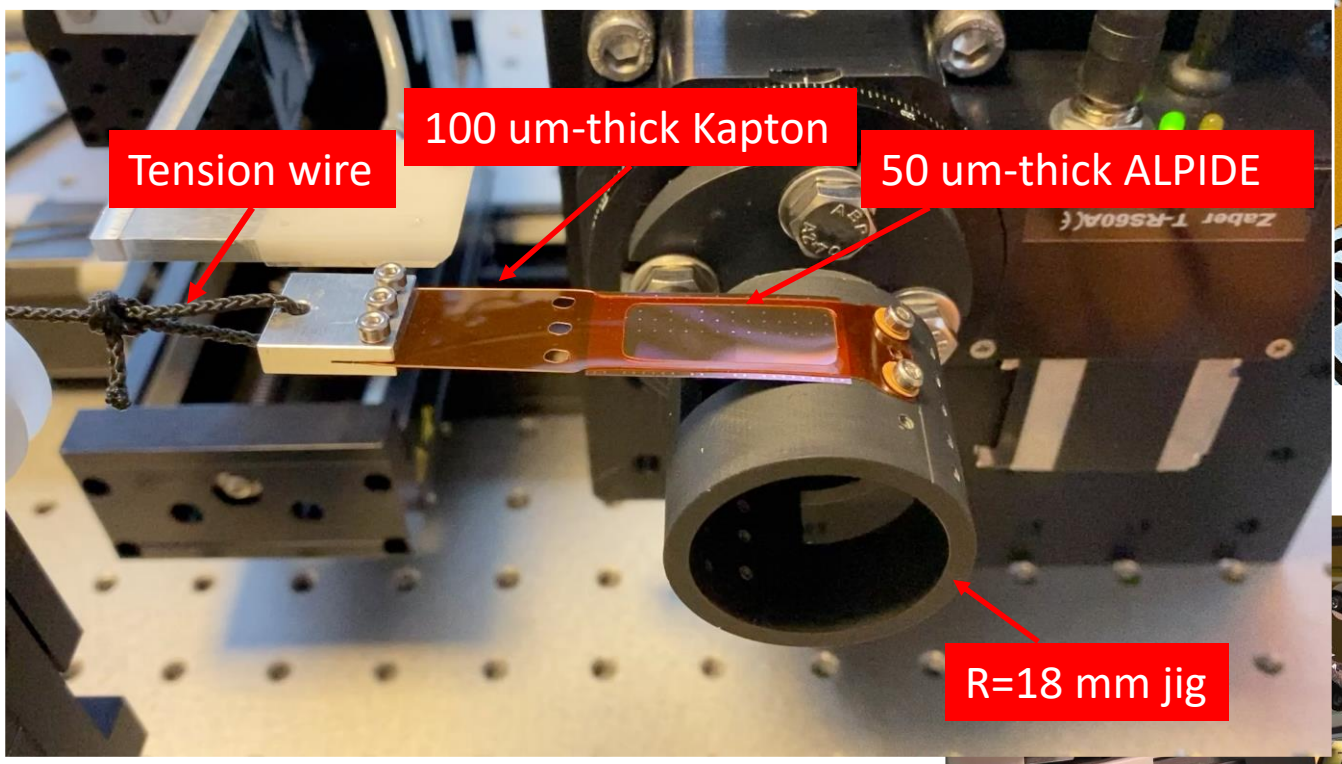
FoCal



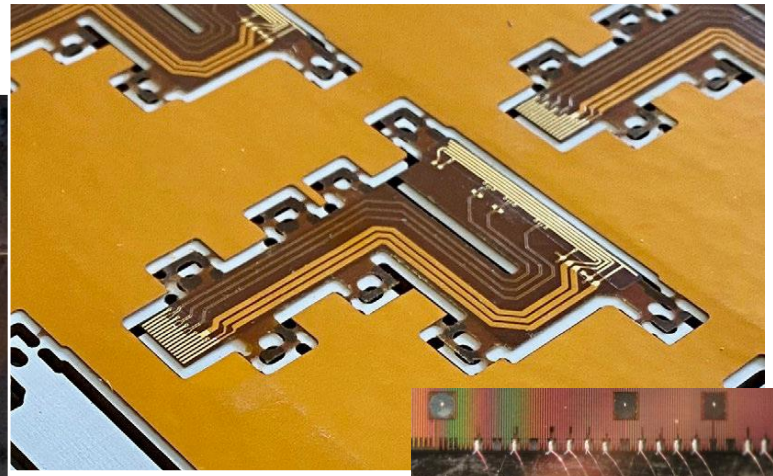
- Add a forward calorimeter (**FoCal**)
- Constrain the gluon nPDF at small Bjorken *x* via measurement of direct photon at forward rapidity

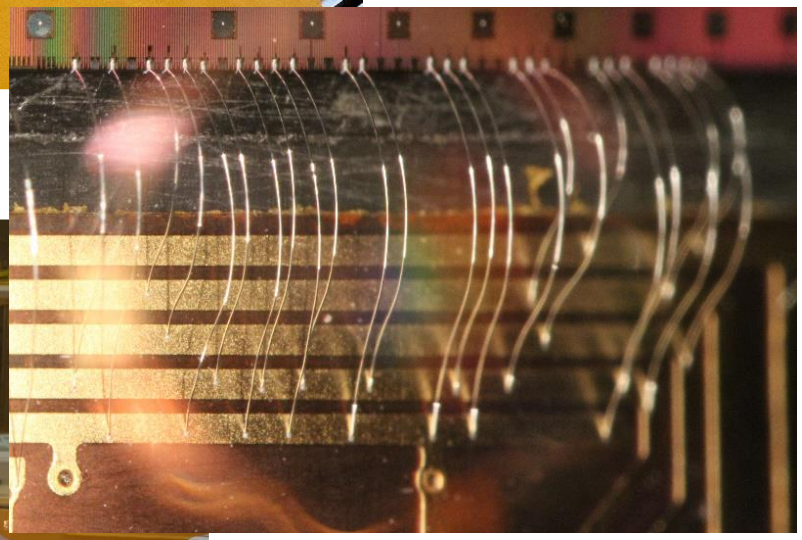
R&D activities for ITS3

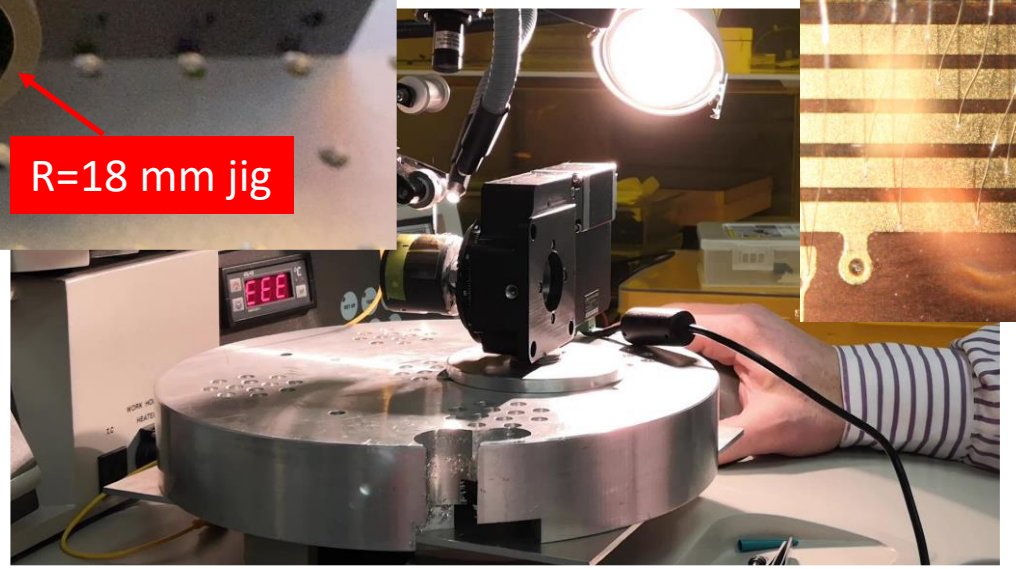
Bending ALPIDE



Bendable FPC

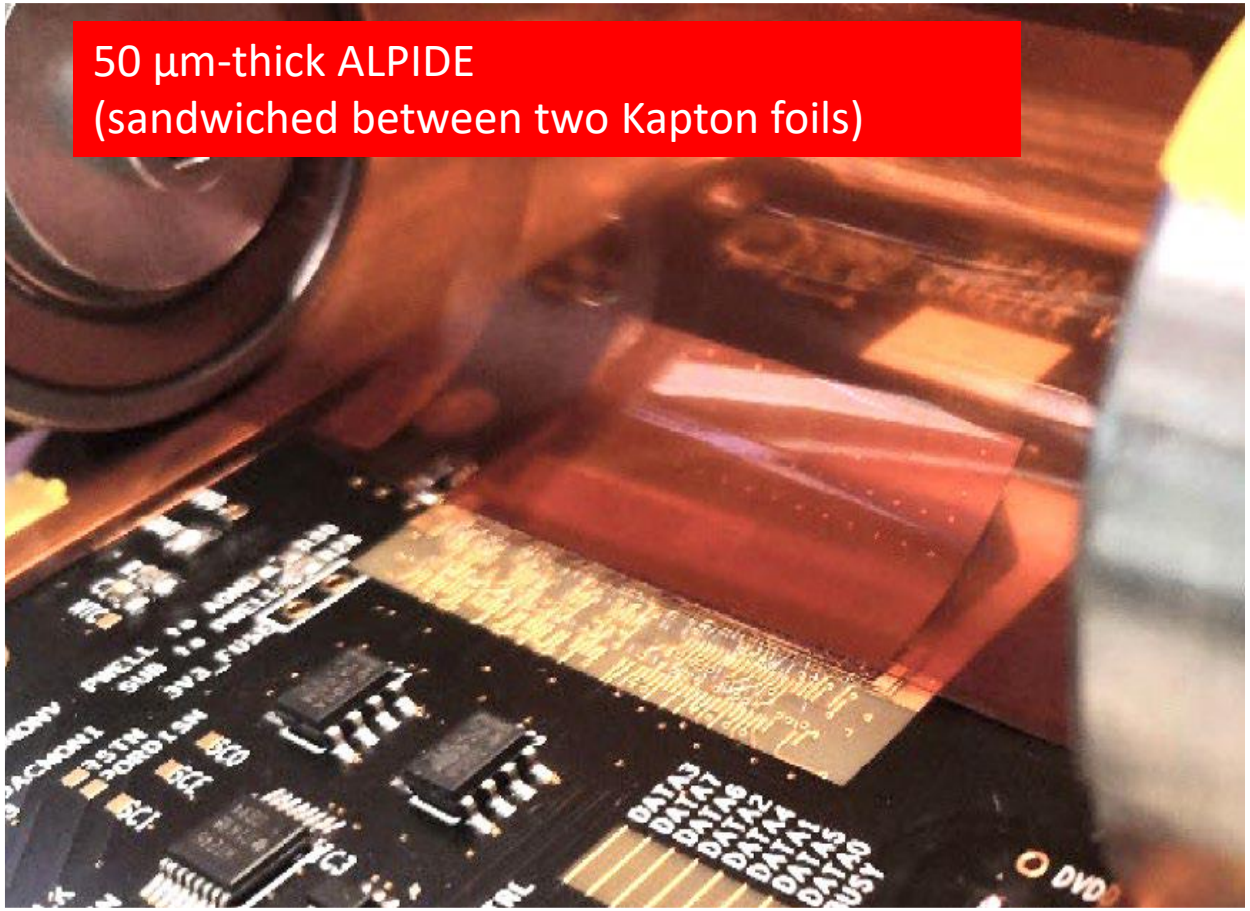


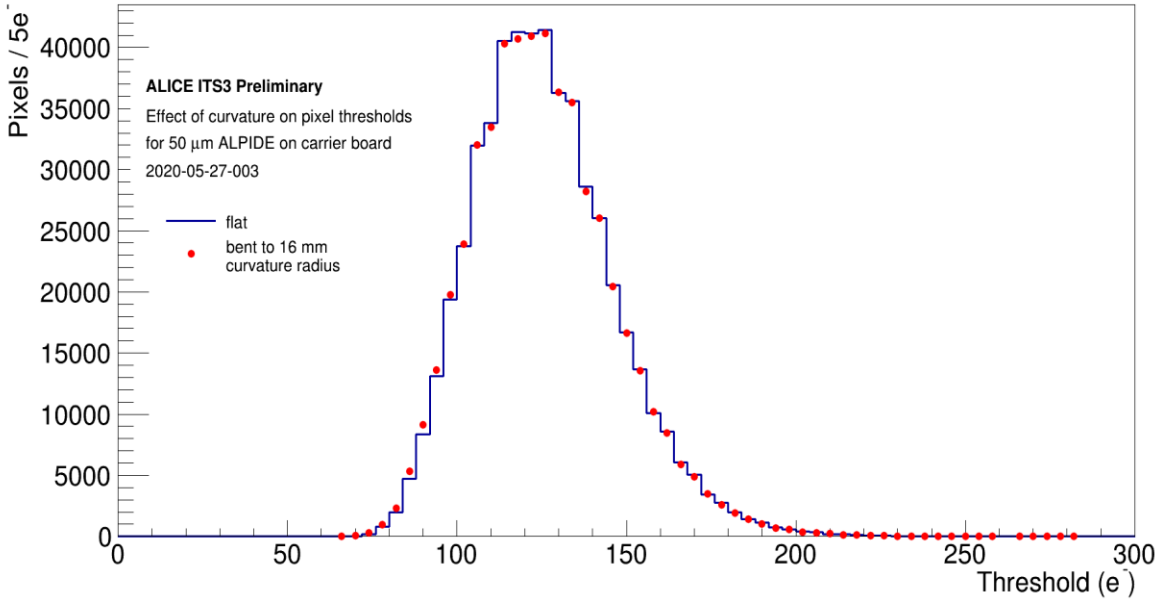




Wire-bonding after bending

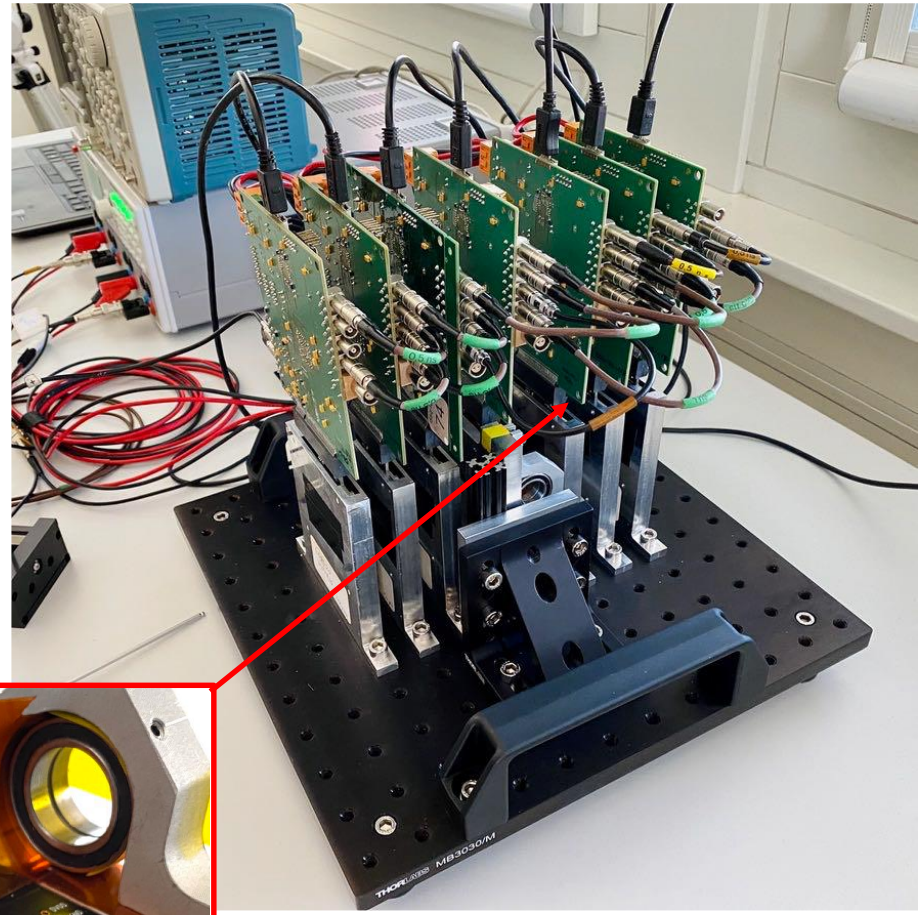
Bent chip electrical test

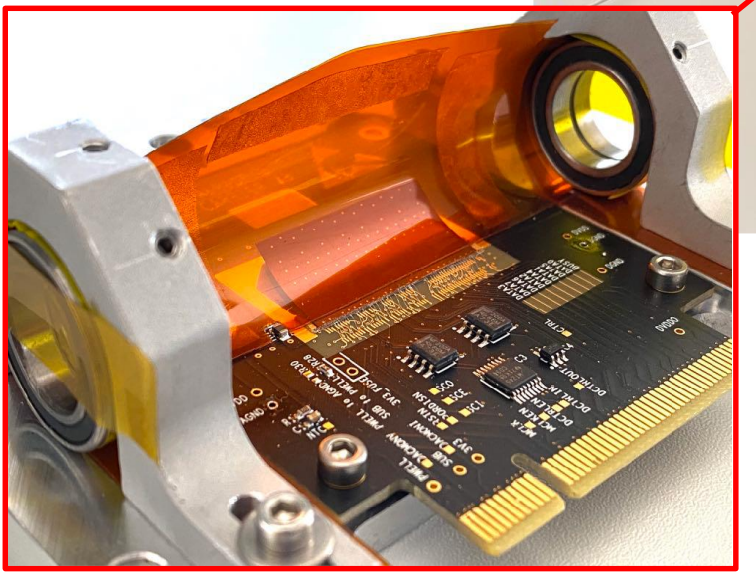




- The curvature effect is not noticeable on:
  - pixel thresholds, FHR, pixel responsiveness
  - tested down to below nominal bending radius

Beam test





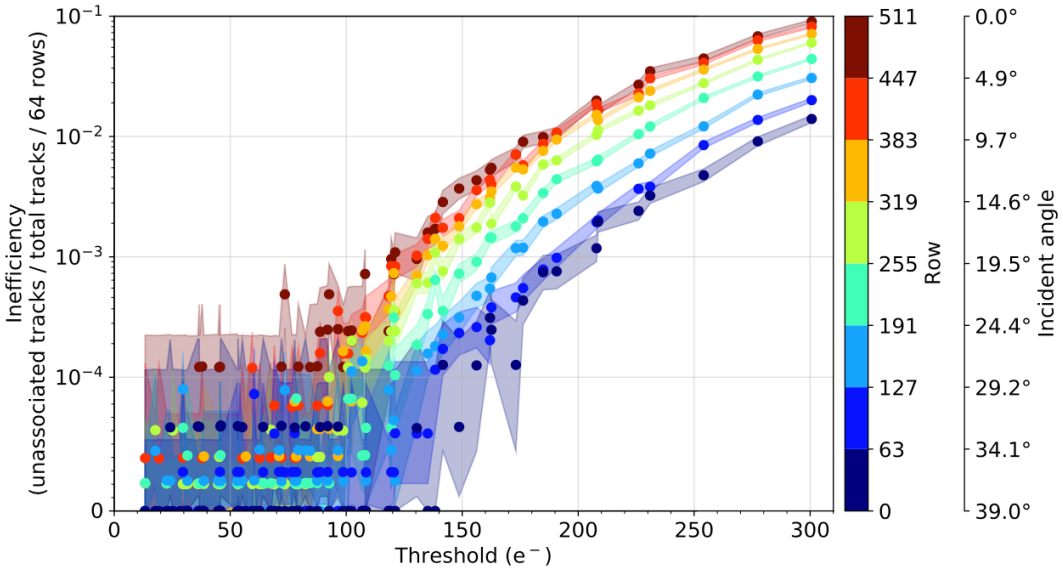
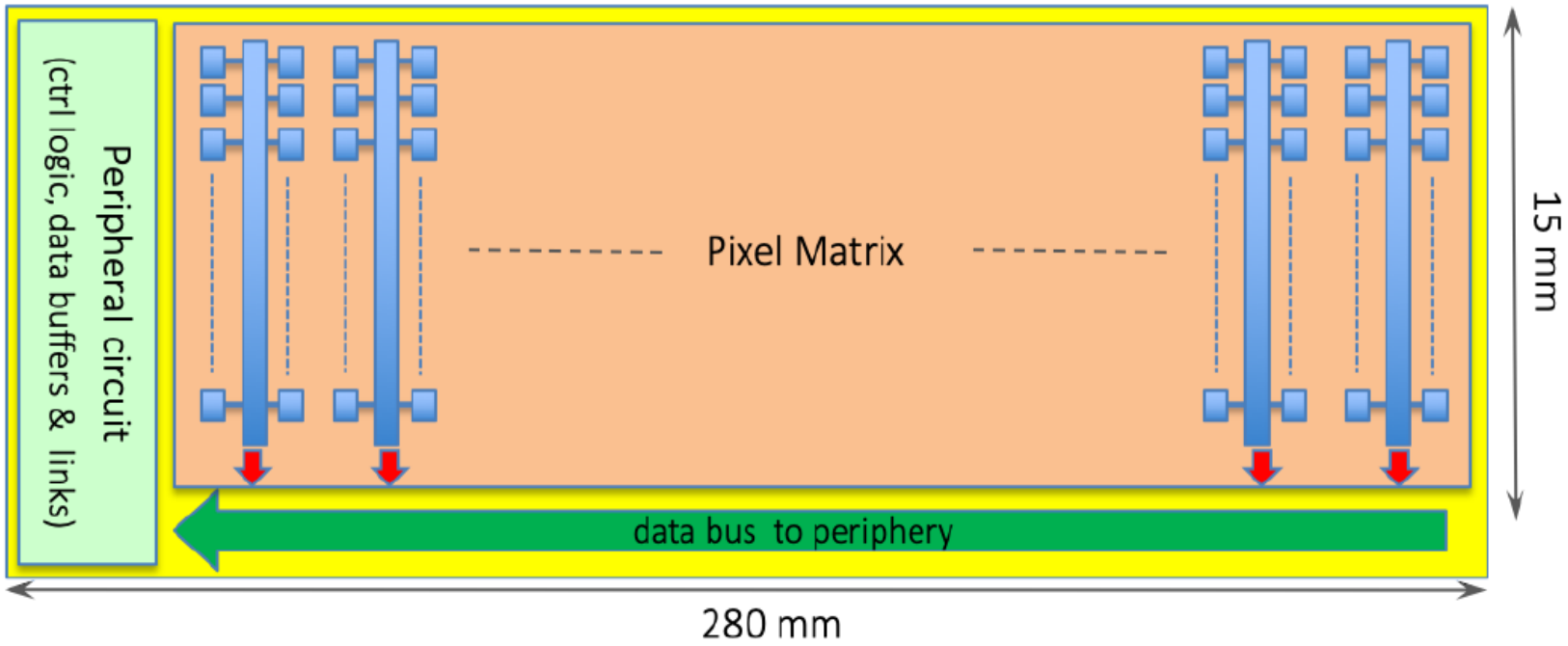


Fig. 10: Inefficiency as a function of threshold for different rows and incident angles with partially logarithmic scale (10^{-1} to 10^{-5}) to show fully efficient rows. Each data point corresponds to at least 8k tracks.

- The chips just continue to work
- The efficiency shows >99.9% at nominal 100 e^- threshold

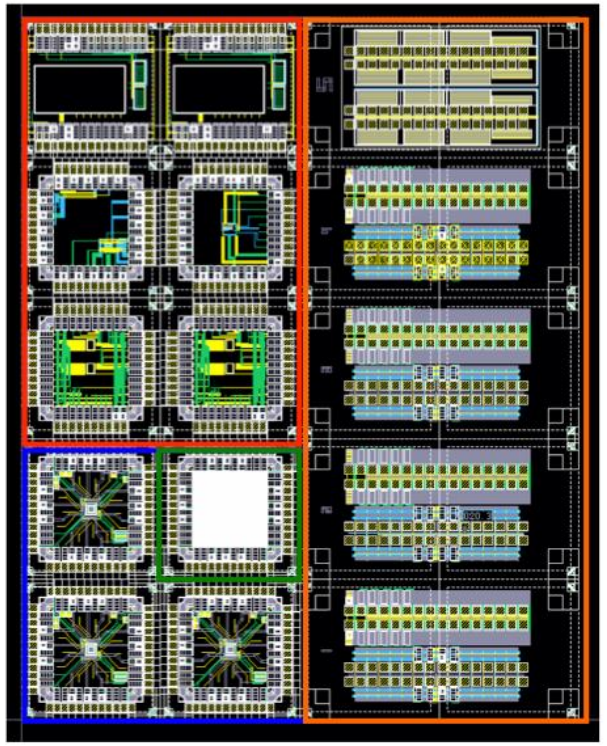
Wafer-scale sensor R&D



- Starting from ALPIDE architecture
- Porting to 65 nm technology node
  - smaller pixels (10 um x 10 um)
  - larger wafers (300 mm instead of 200 mm)

- Basic building block of 15 mm height
  - to be repeated n times in vertical direction to obtain the sizes needed per layer

First 65 nm prototype submission imminent



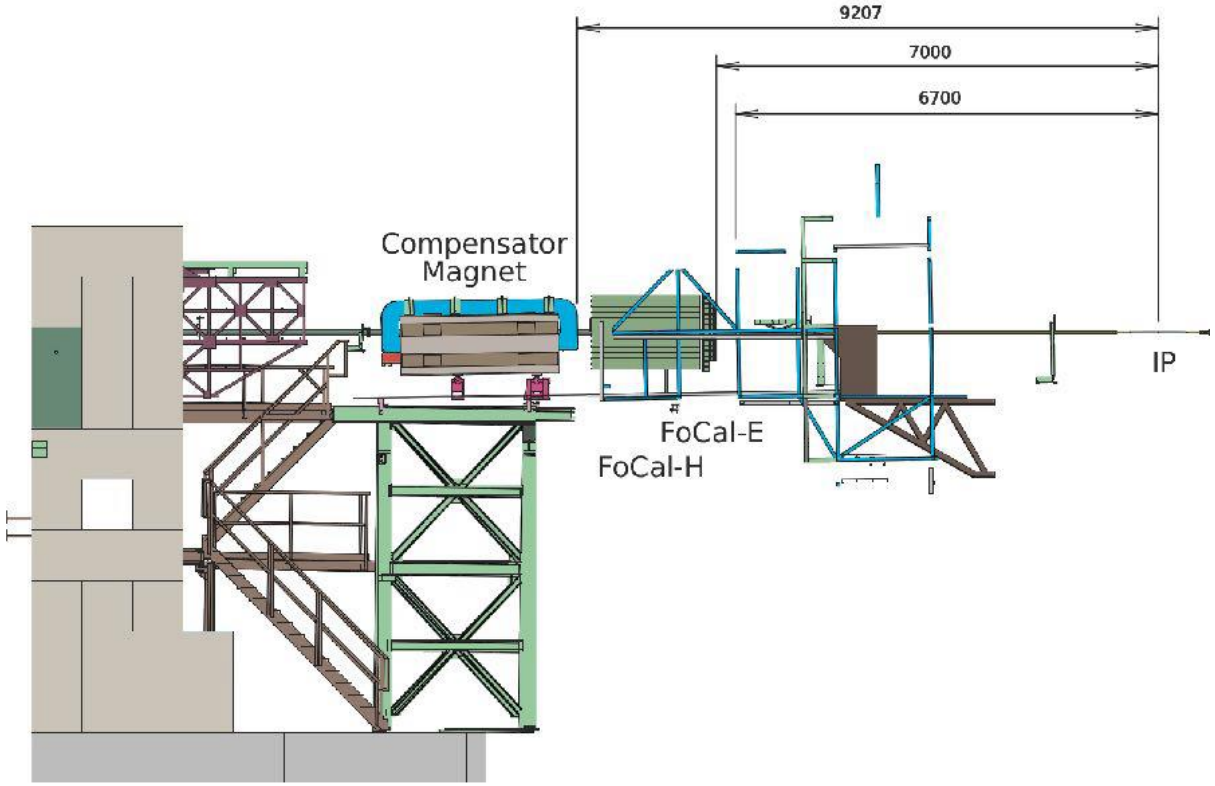
- Content:

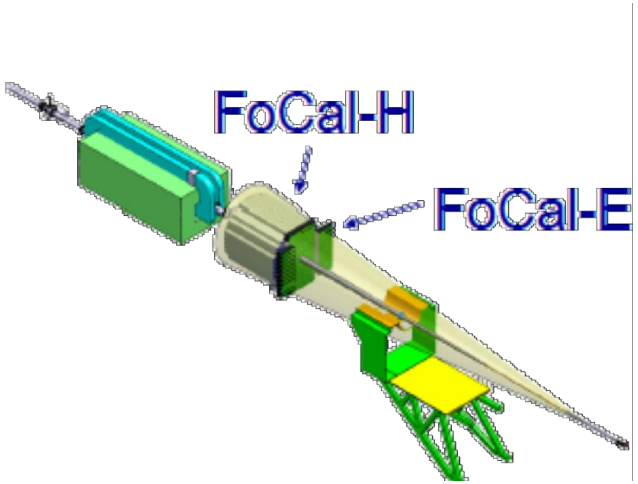
- Transistor Test structures
- Analog Pixel test chips
- Rolling shutter matrix
- smaller building blocks

- Goal: verification technology for:

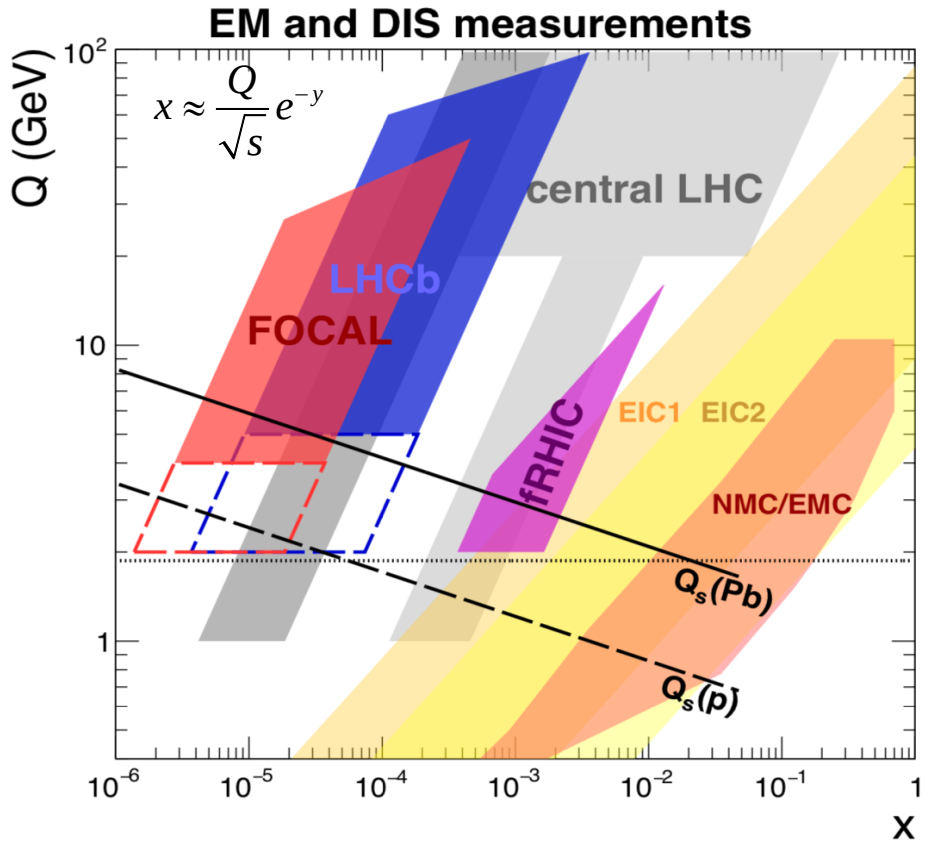
- radiation hardness
- charge-collection properties

FoCal for LS3



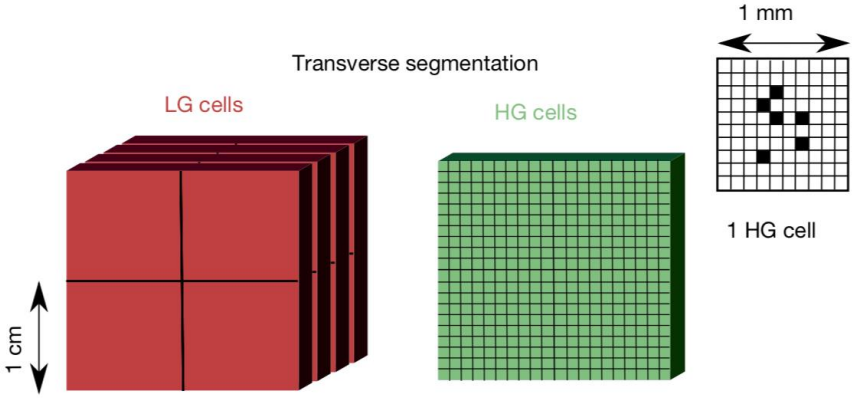


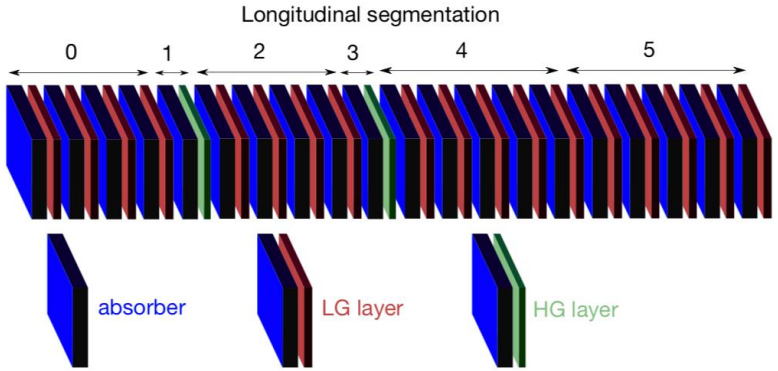
- 7 m away from the nominal IP
- Pseudo-rapidity coverage of 3.2 - 5.8
- To explore small *x* physics



FoCal-E design

high granularity electromagnetic calorimeter for γ and π^0 measurements





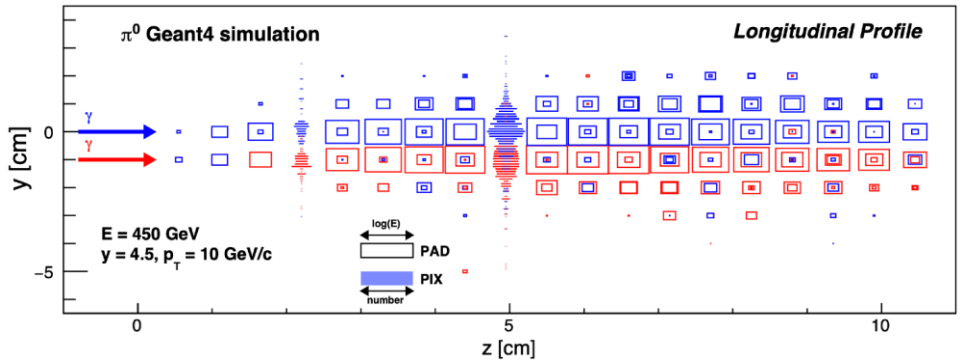
- **Studied in simulations 20 layers:**

W(3.5 mm ≈ 1X0) + silicon sensors

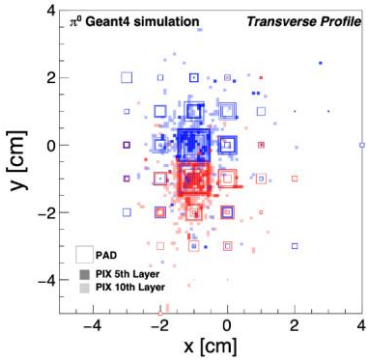
- **Two types: Pads (LG) and Pixels (HG)**
  - **Pad layers provide shower profile**
  - **Pixel layers provide position resolution to resolve shower overlaps**

- Main challenge: Separate γ/π^0 at high energy
  - Two photon separation from π^0 decay (p_T = 10 GeV/*c*, η=4.5) ~2 mm
  - Needs small Molière radius and high granularity readout
  - Si-W calorimeter with effective granularity ≈ 1mm^2

Longitudinal profile (2γ showers)



Trans. profile

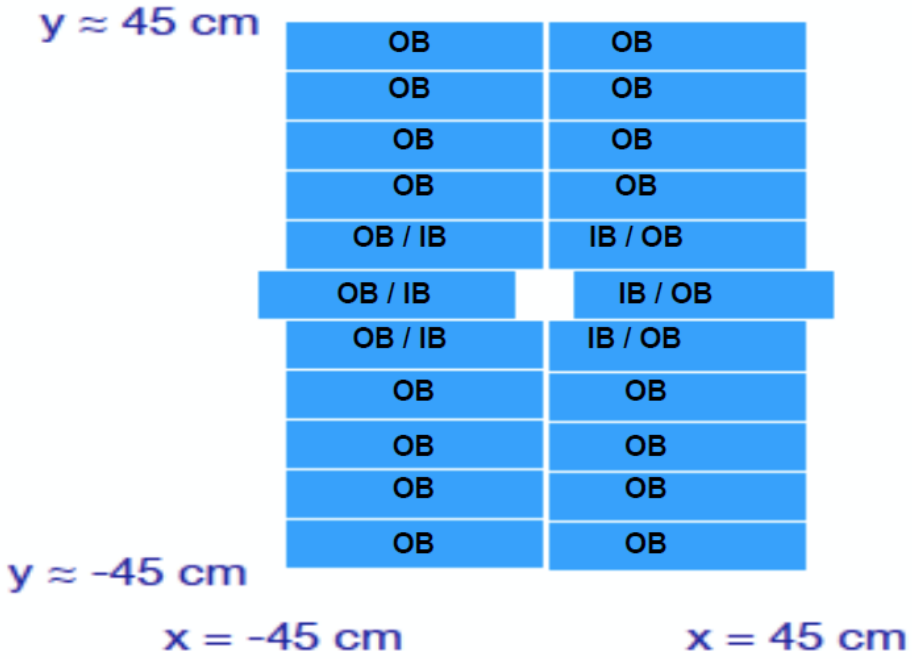


Further optimization left for TDR:

- Location of pixel layers
- Number of pad layers
- Sensitive area at front for CPV/eID

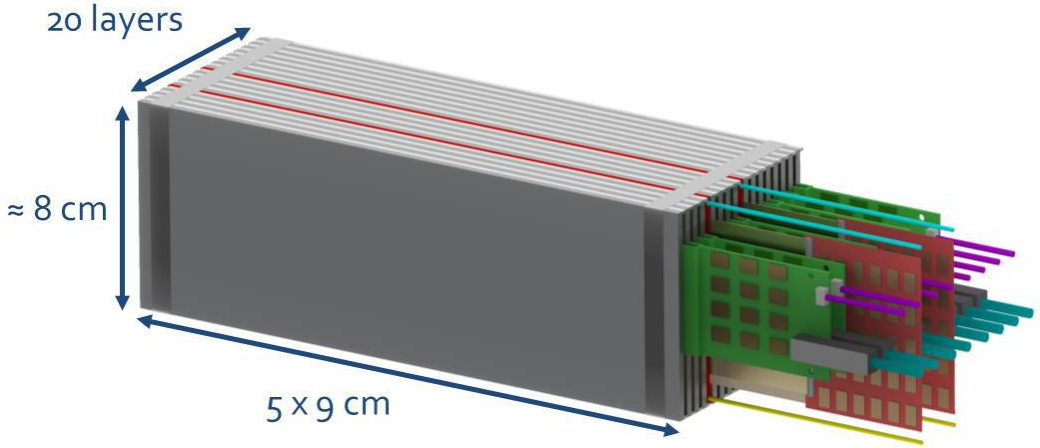
FoCal-E detector Integration

FoCal module layout



Design of detector module

45cm x 8cm



- module of ≈ 18 pad layer and 2 pixel layers
- sensitive area: 45 cm x 8 cm
- use edge of detector for services
- designed to be stacked vertically for full detector setup

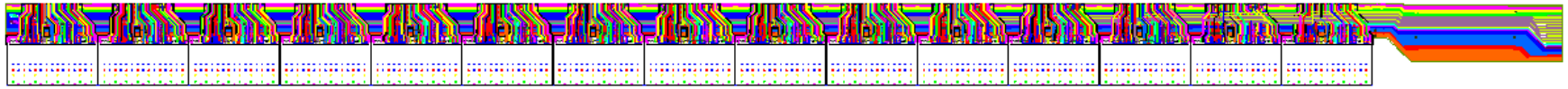
Design of single pixel layer

- single metal layer with cooling pipes
- full area coverage with 2 x 3 chains of 15 ALPIDE sensors

Pixel layer R&D

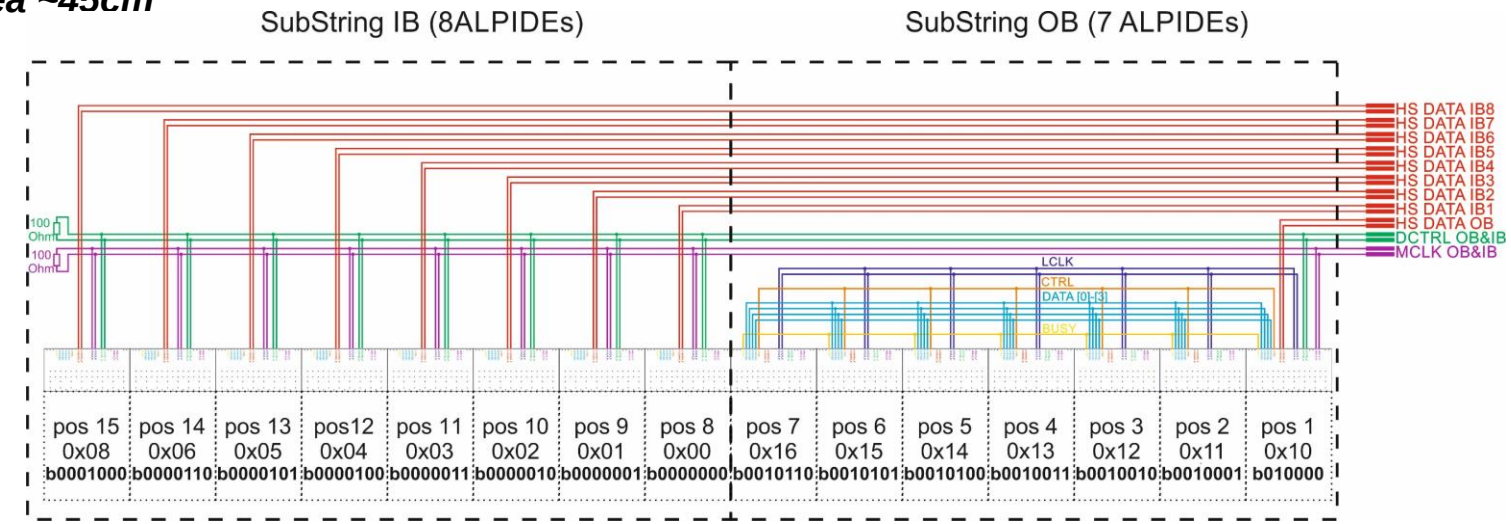
Sketch

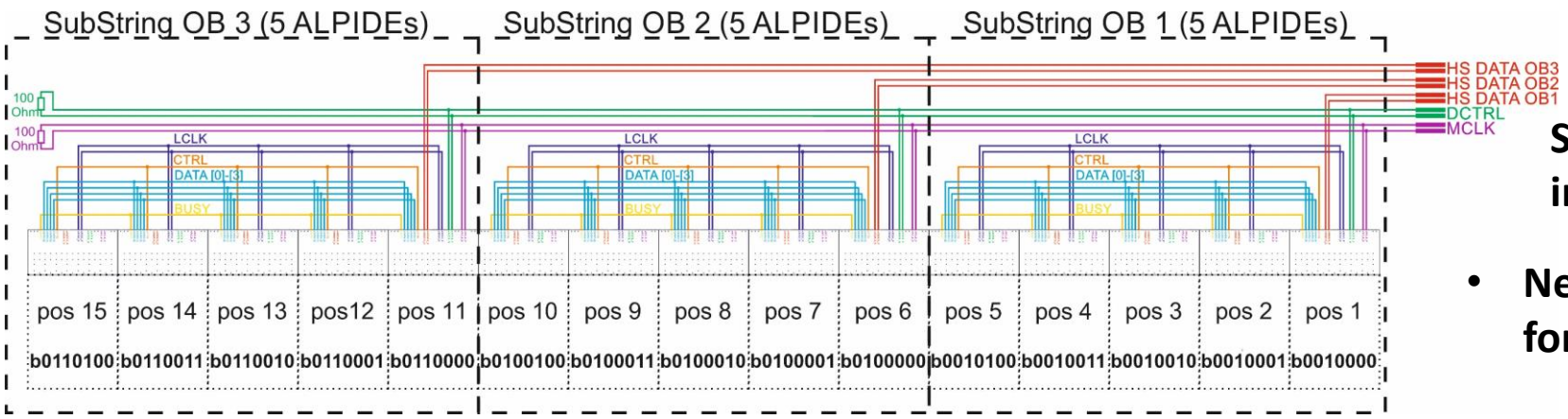
Total length of string ~50cm



Length of active area ~45cm

Schematic diagram of the electrical interconnections for IB/OB combination



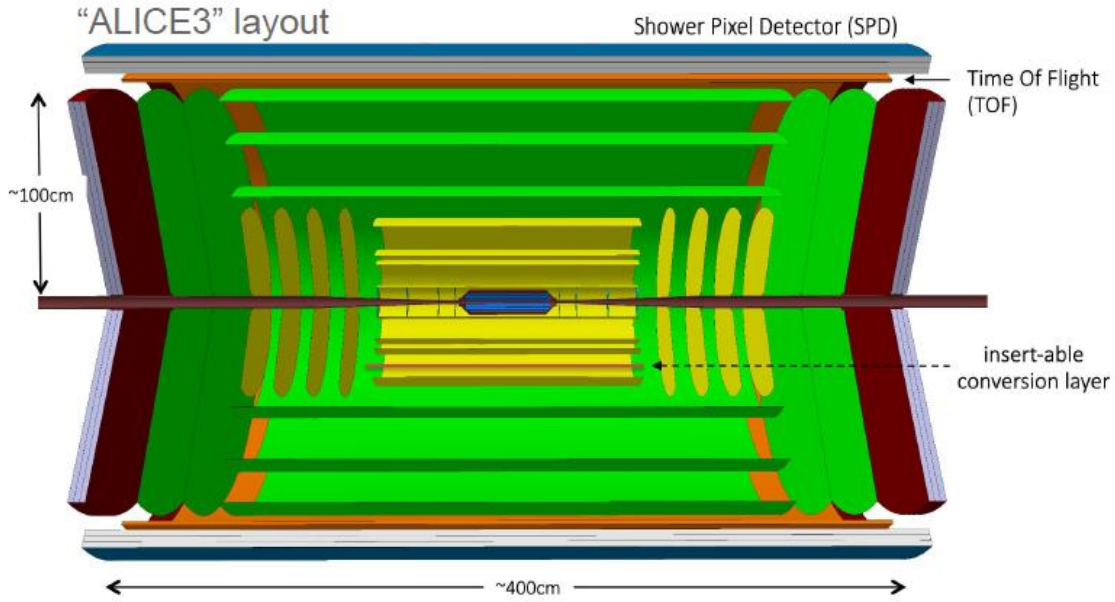


Schematic diagram of the electrical interconnections for OBs only

- **Next important step: get prototype ready for testbeam(s) in 2021/22**

Summary and outlook

- Major upgrade of ALICE detector undergoing to take advantage of the luminosity increase in Run 3 & 4.
  - We are involved in ITS2 and MFT
    - ALPIDE chip R&D
    - OB HIC production completed
    - Commissioning of ITS2 is ongoing
    - MFT PCB production completed
- Active R&D on ITS3 and FoCal for detector upgrade for RUN4 to enhance its physics capabilities.
  - We are involved in R&D of wafer-scale sensor for ITS3
    - first prototype submission is imminent
  - Pixel layers to FoCal-E under R&D
- Outlook: A nearly pure silicon detector for RUN5 (beyond 2030)



Increase rate capabilities (factor 50 wrt to ALICE RUN4)

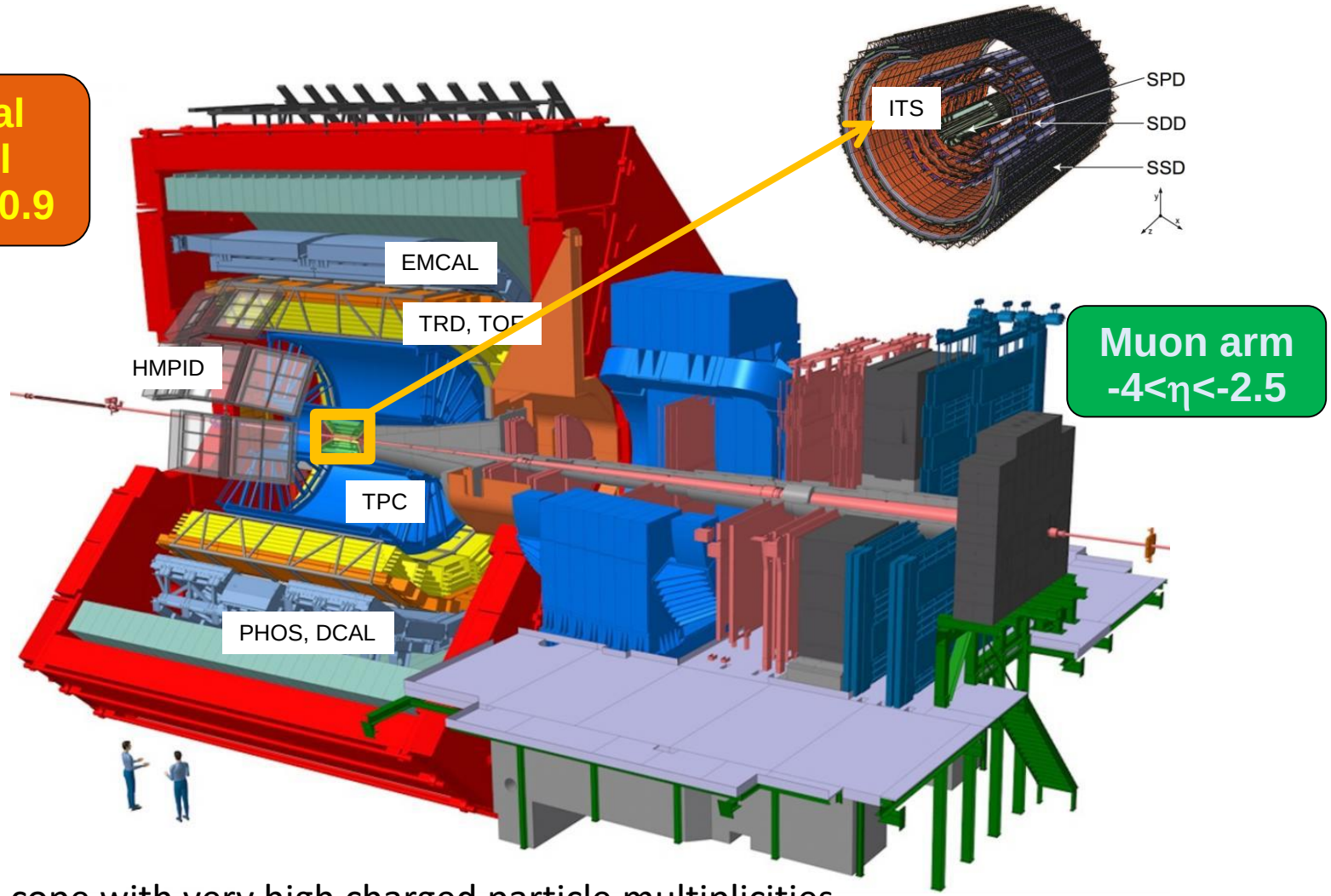
– large acceptance, fast tracker based on wafer-scale MAPS
– 0.05% X_0/layer
– PID by TOF in Si layers
– electron and photons: pre-shower detector, converter

- Access doubly and triply heavy-quark hadrons
- Precise dielectron measurements
- Soft and ultra-soft photons

ALICE

Thank you very much
for your attention !

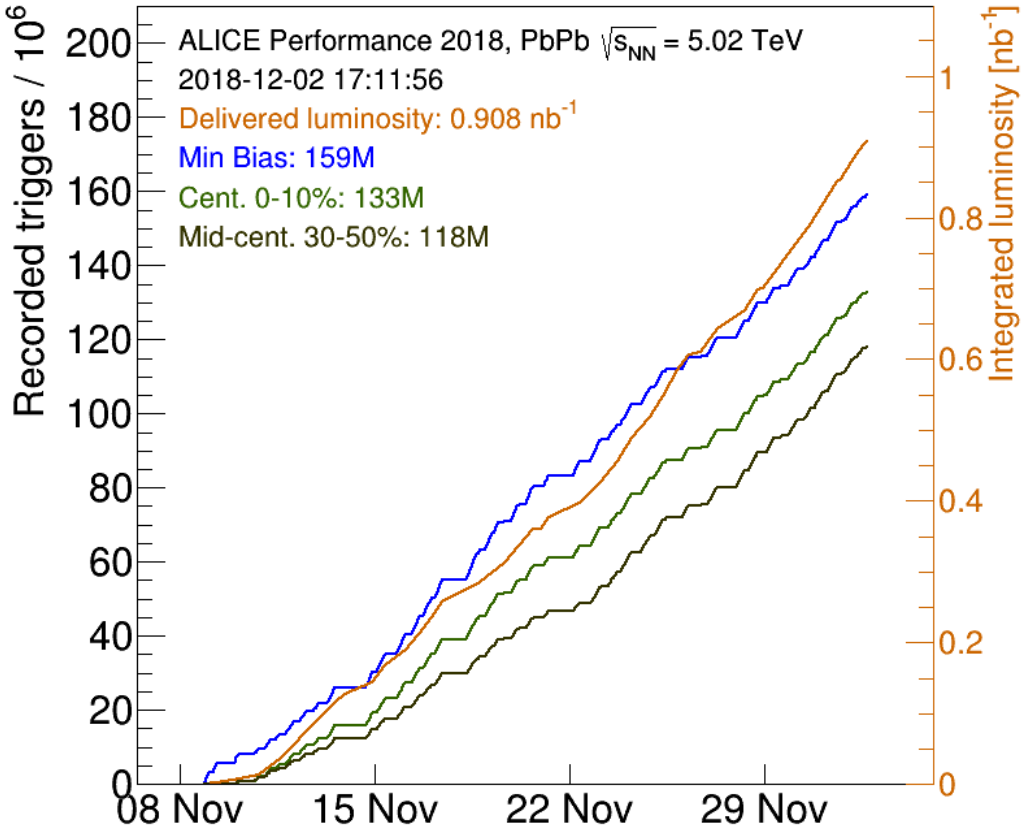
ALICE detector in RUN 1 & 2



- Designed to cope with very high charged particle multiplicities
- Excellent tracking and particle identification of charged particles over wide p_T range

ALICE running status

Colliding System	Year	$\sqrt{s_{NN}}$ (TeV)	Integrated Luminosity
Pb-Pb	2010,2011	2.76	~75 μb^{-1}
	2015	5.02	~250 μb^{-1}
	2018	5.02	~1 nb^{-1}
Xe-Xe	2017	5.44	~0.3 μb^{-1}
p-Pb	2013	5.02	~15 nb^{-1}
	2016	5.02 8.16	~25 nb^{-1} ~3 nb^{-1}
pp	2009-2013	0.9 2.76	~200 μb^{-1}, ~ 100 nb^{-1}
		7 8	~1.5 pb^{-1}, ~2.5 pb^{-1}
	2015,2017	5.02	~1.3 pb^{-1}
	2015-2018	13	~45 pb^{-1}



Pb-Pb 2018 run

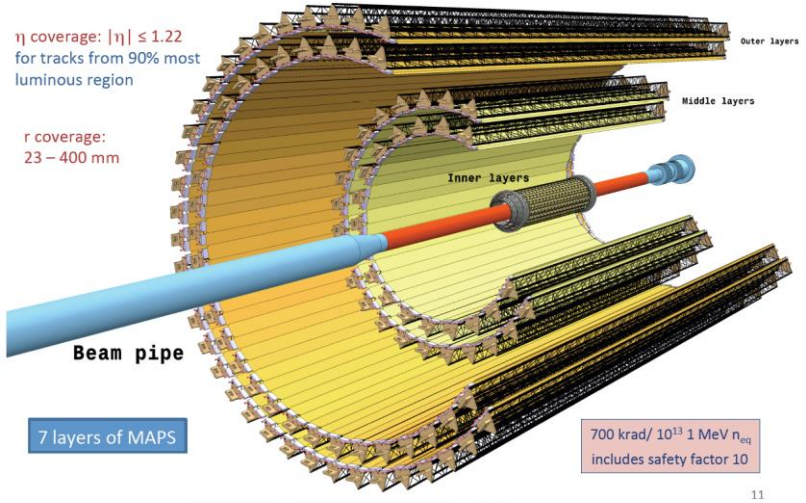
– 0-10%: ~ 9 x 2015

– 30-50%: ~ 4 x 2015

– Minimum Bias: ~ 2015

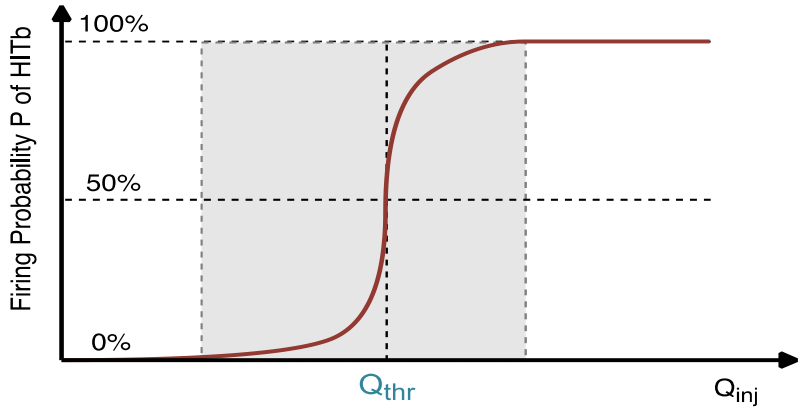
– delivered lumi. ~ 2 x 2015

参与ALICE升级探测器研制的状况

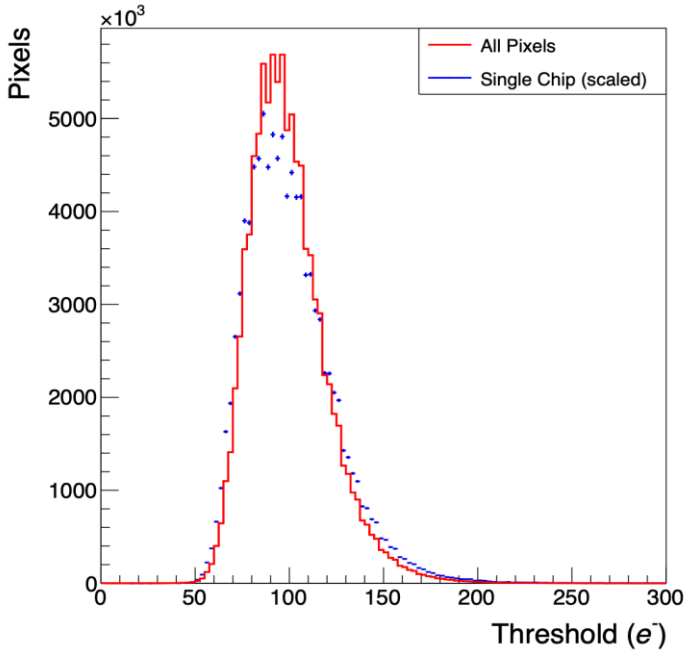


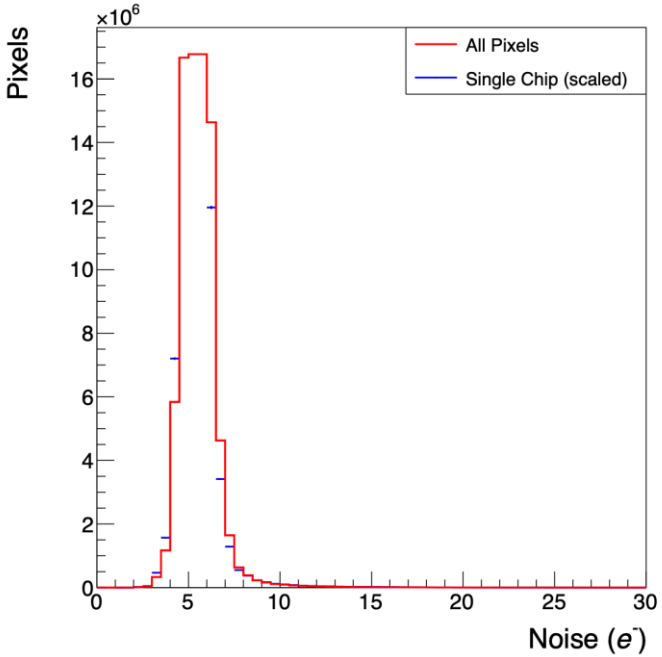
- 参与ITS硅像素芯片设计:
  - (1) 芯片读出结构;
  - (2) 像素模拟前端电子学改进
- ITS探测器模块建造与测试
  - ✓2017年9月份启动预生产
  - ✓2018年4月份启动正式生产，于2019年8月完成（生产率为2模块/天，共建造500个模块）

Noise and threshold performance



$$P(q) = \frac{1}{2} \cdot \mathrm{Erf}\left[\frac{q - Q_{thr}}{\sqrt{2} \cdot \sigma}\right]$$

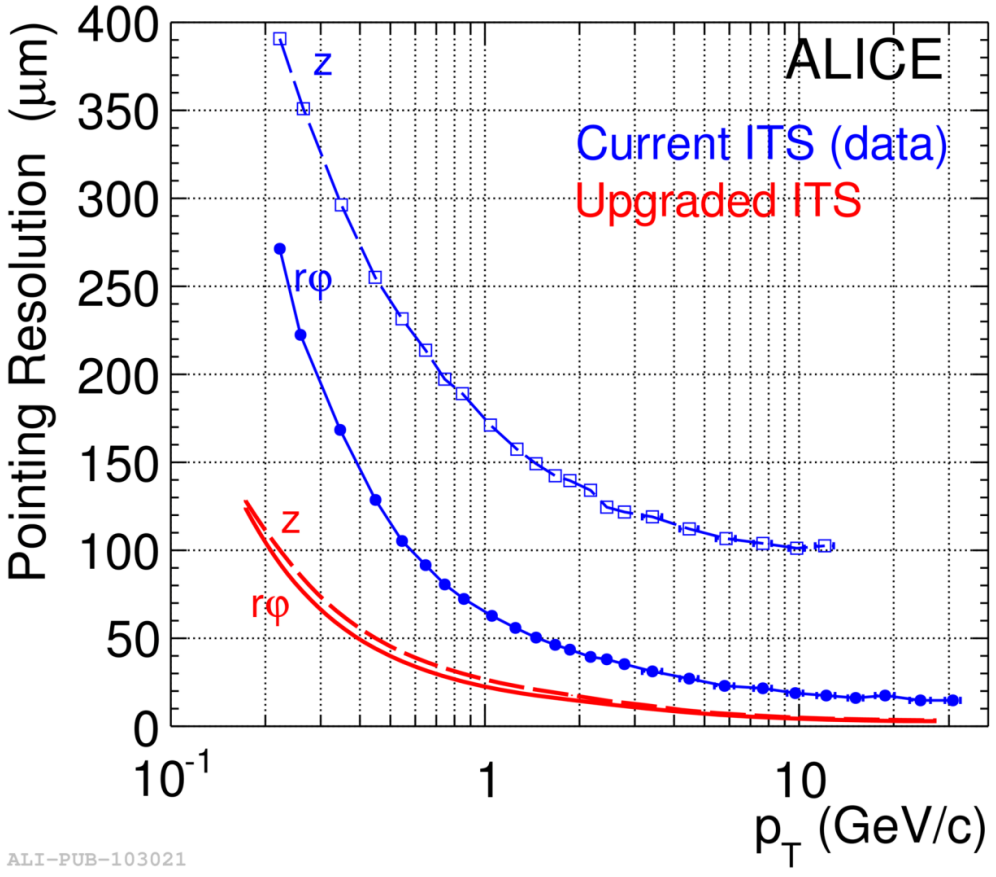




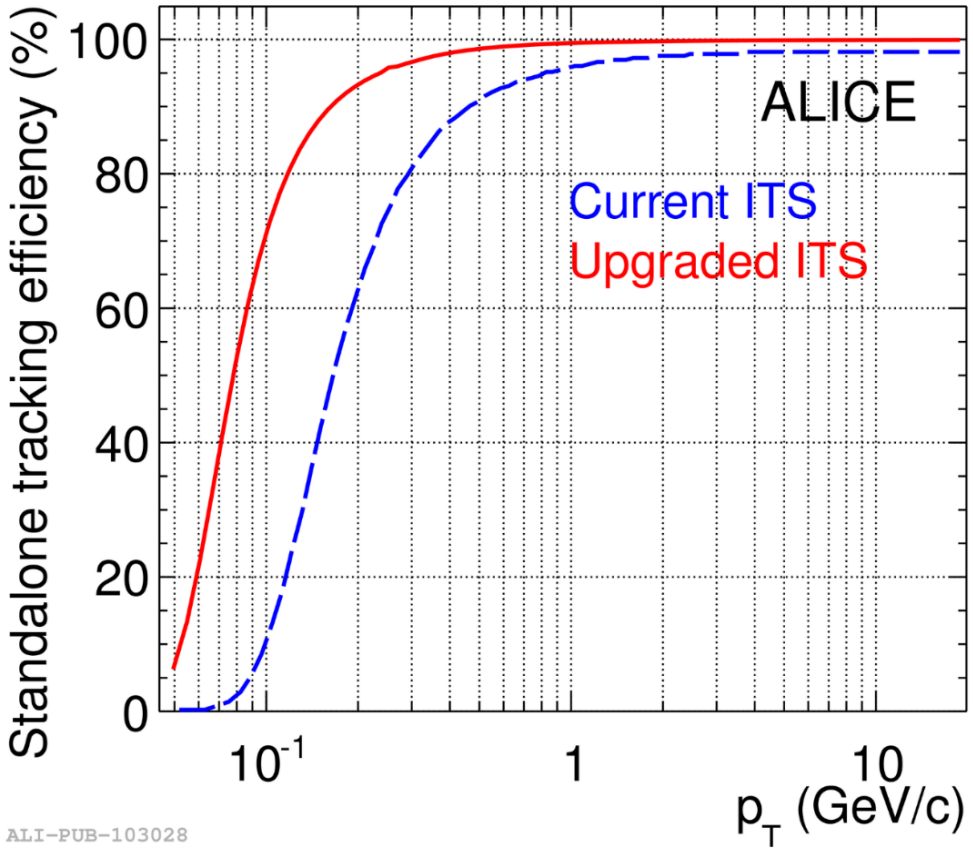
Threshold and noise after tuning for an OL Stave (~100M pixels) compared with a single chip test data

Simulated ITS2 performance

- Pointing resolution improved by a factor of 3 and 5 in rϕ and z direction for 0.5 GeV/*c* π



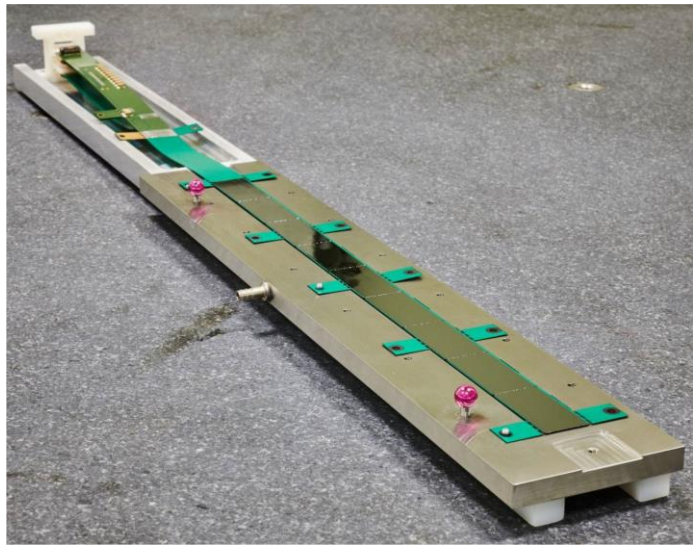
- Standalone tracking efficiency improved significantly at low p_T

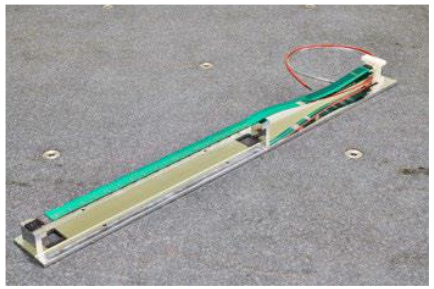


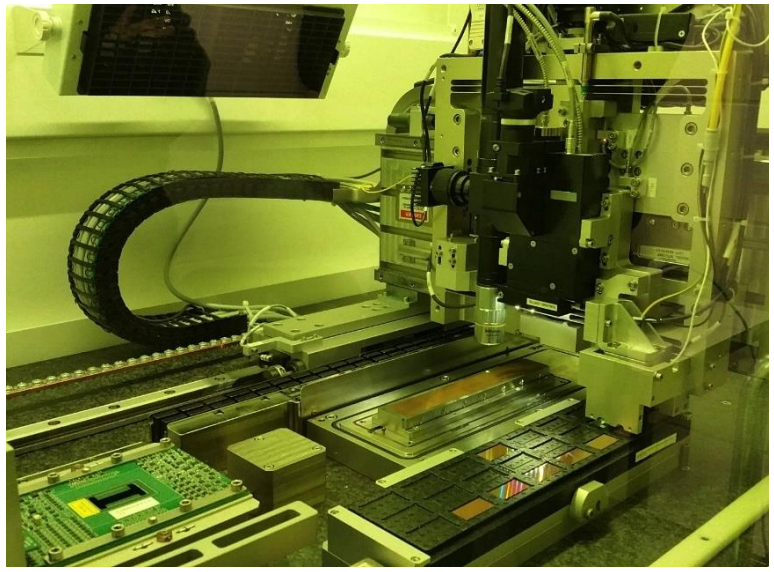
- Physics goal: improve heavy-flavor physics studies through low momentum track reconstruction

From chips to staves: IB

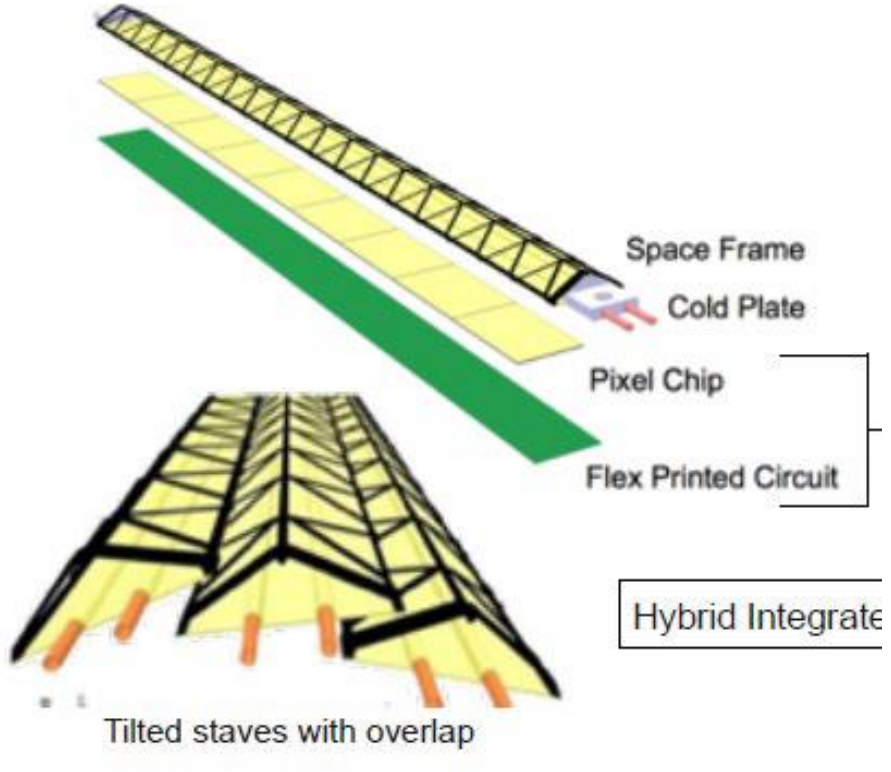
Inner Barrel HIC: 9x 50μm-thick ALPIDE chips wire-bonded to FPC







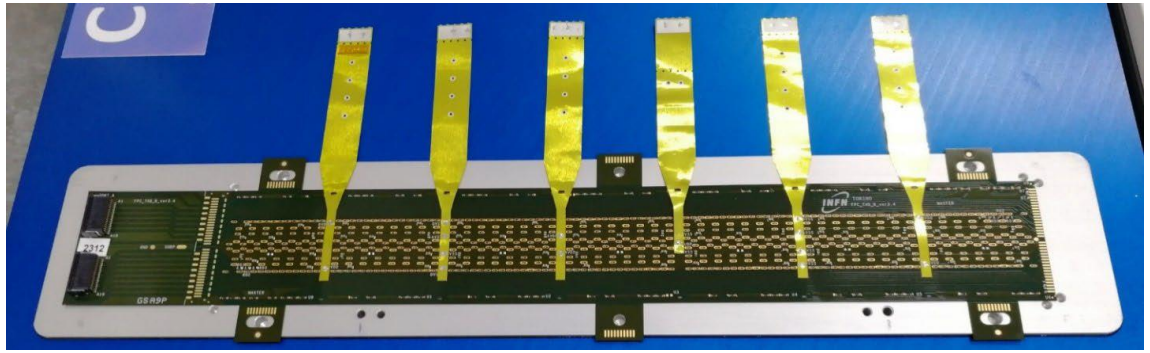
- Chips read out separately
- Clock, control, data, power lines wire-bonded to aluminum FPC
- Produced at CERN with 73% yield
- 27 cm length stave



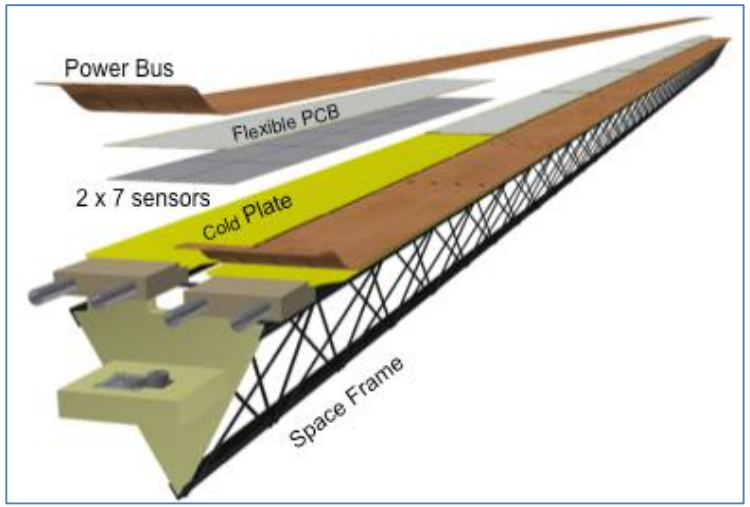
- <radius> (mm): 23, 31, 39
- Nr. staves: 12, 16, 20
- Nr. chips: 432
- Readout speed: 1.2 Gbps

From chips to staves: OB

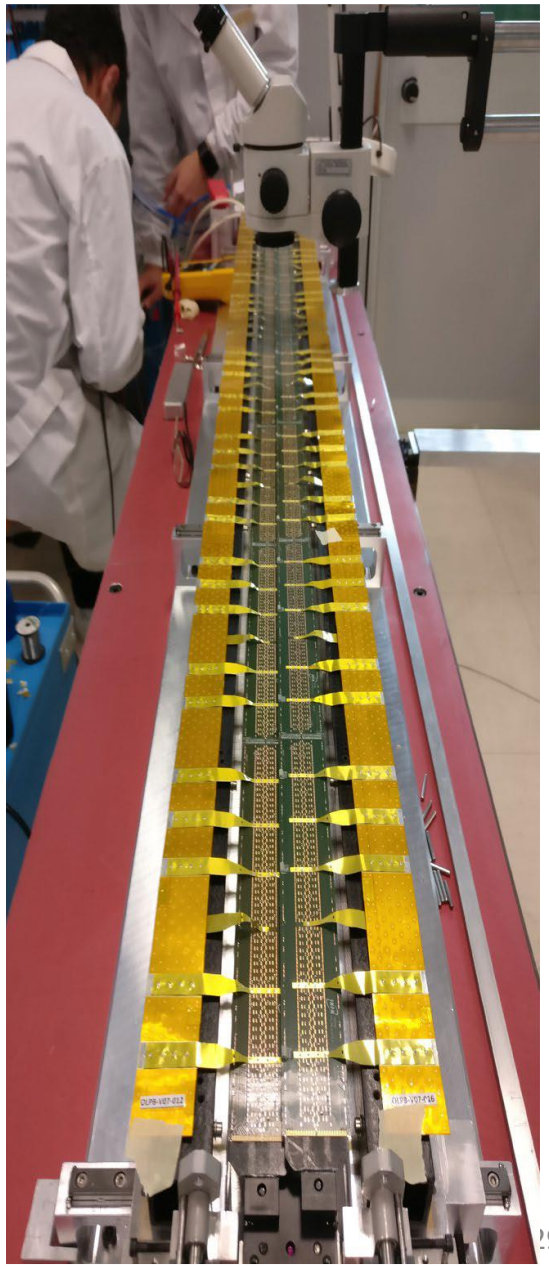
Outer Barrel HIC: 14x 100μm-thick ALPIDE chips (2 rows)



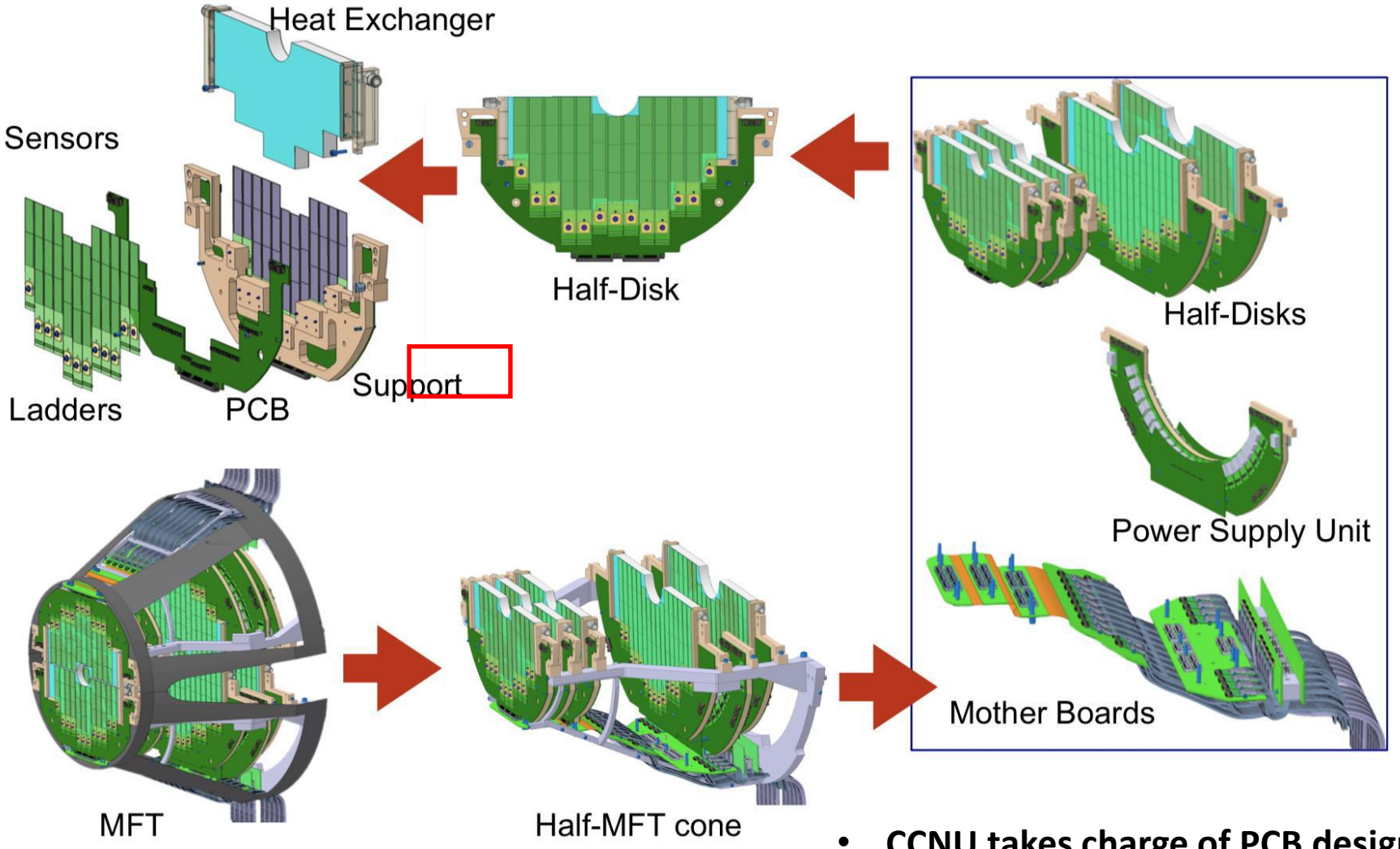
- Data and control transferred through 1 master chip per row
- Chips wire-bonded to copper FPC
- Power delivered via 6 cross-cables soldered to FPC
- Produced at Bari, Liverpool, Pusan/Inha, Strasbourg and **Wuhan**



- HIC alignment on cold plate
- HIC-to-HIC (4 for ML and 7 for OL) interconnection soldering
- Two half staves on space frame
- Power bus installation
- Readout speed for OB: 400 MB/s

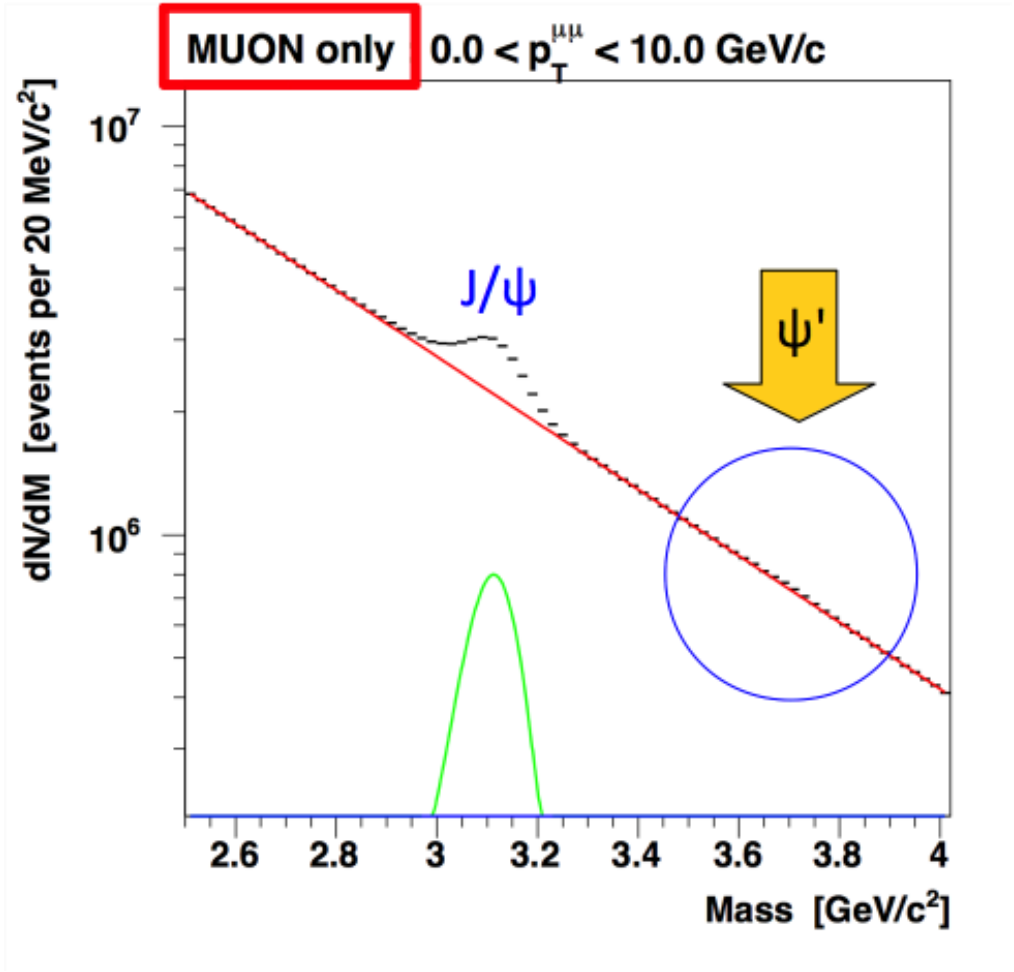


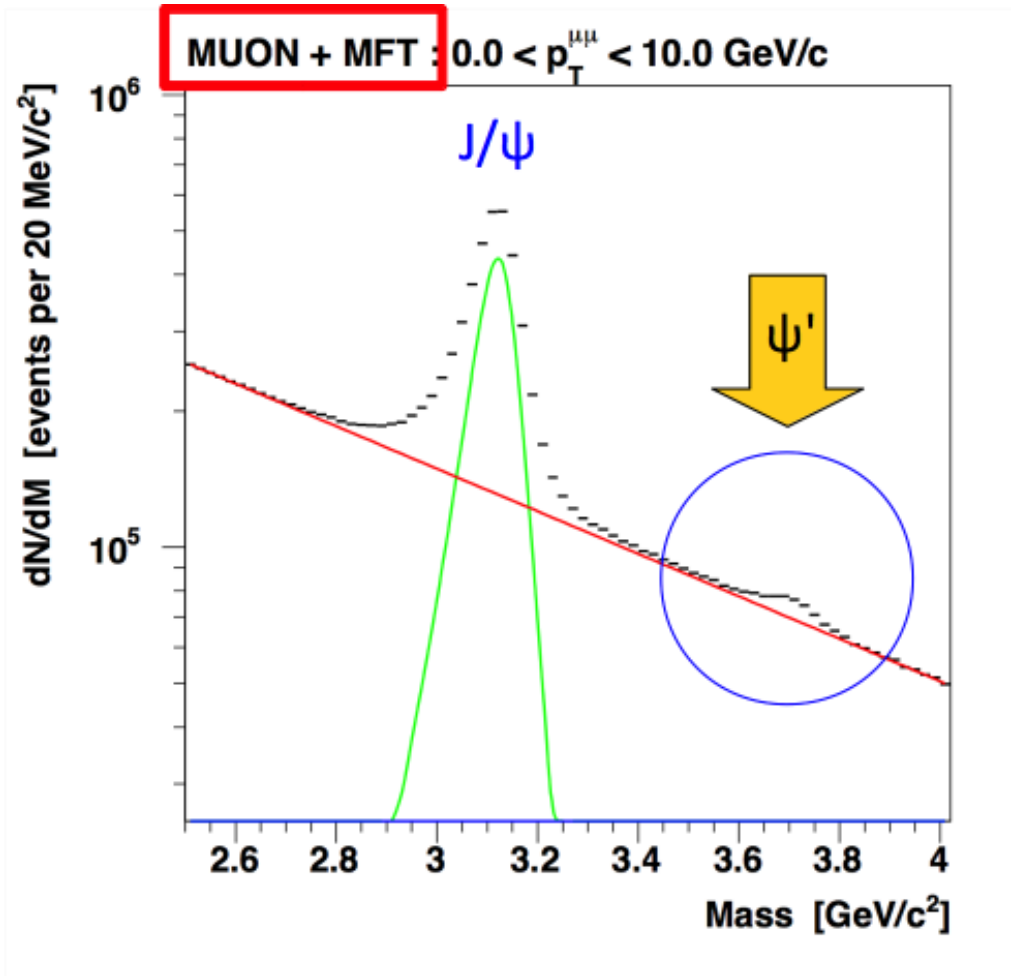
Breakdown of MFT structure



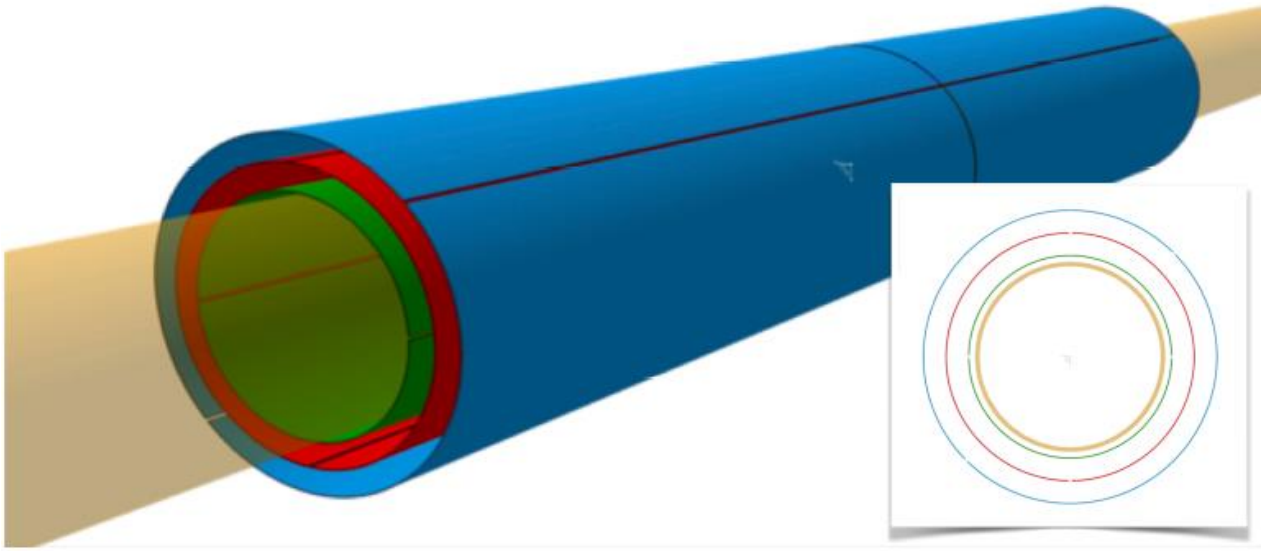
- **CCNU takes charge of PCB design, layout and production.**
- Status: **Completed in 2019**

Simulated MFT performance for charmonium measurement





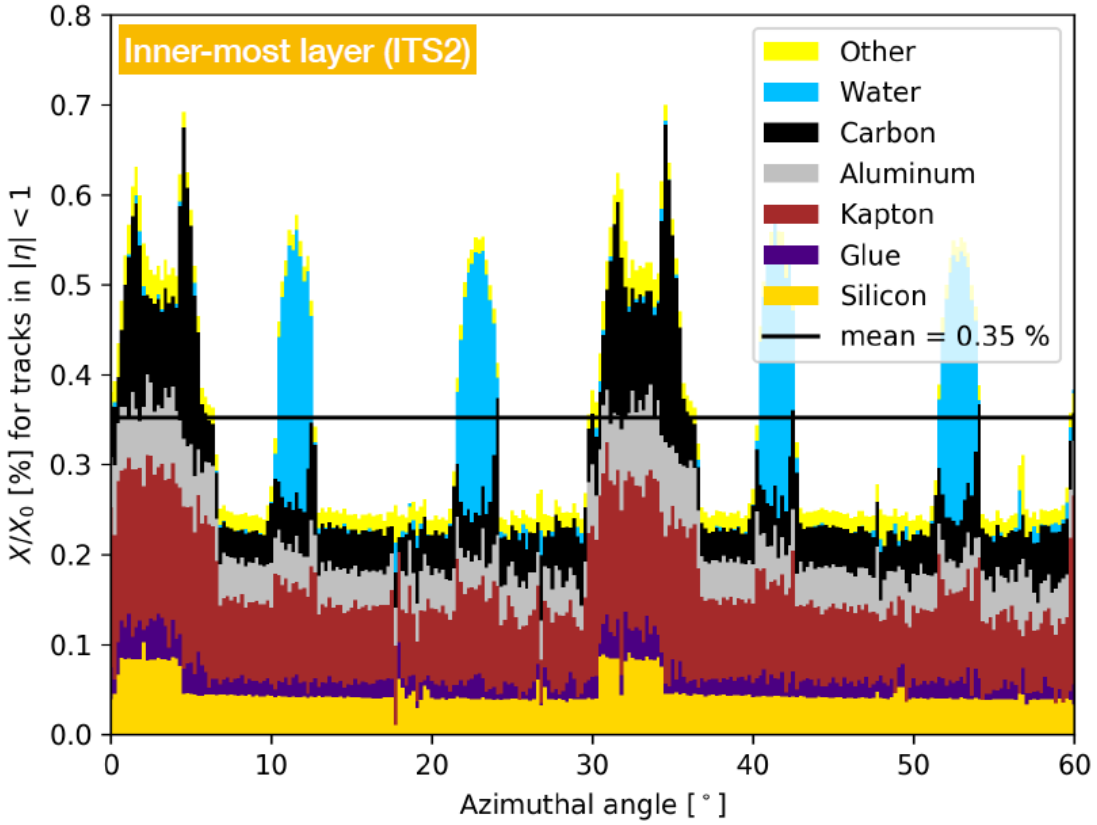
ITS3 layout



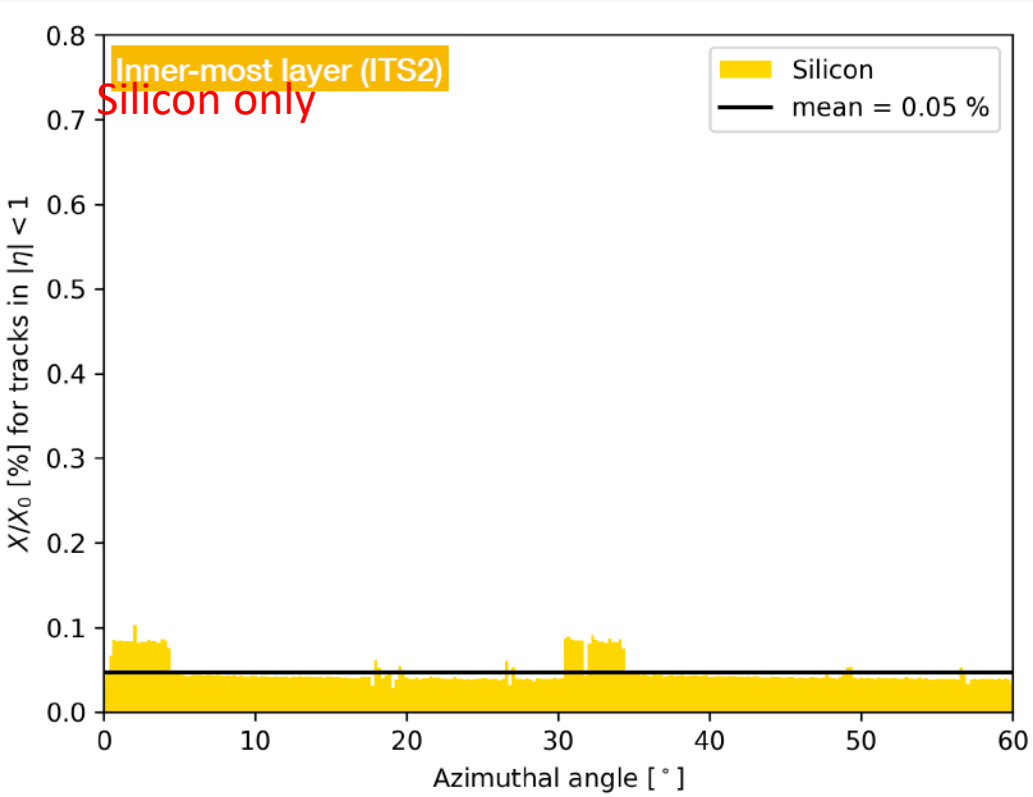
Beam pipe Inner/Outer Radius (mm)	16.0/16.5		
IB Layer Parameters	Layer 0	Layer 1	Layer 2
Radial position (mm)	18.0	24.0	30.0
Length (sensitive area) (mm)	300		
Pseudo-rapidity coverage	±2.5	±2.3	±2.0
Active area (cm^2)	610	816	1016
Pixel sensor dimensions (mm^2)	280 x 56.5	280 x 75.5	280 x 94
Number of sensors per layer	2		
Pixel size (μm^2)	O (10 x 10)		

- New beam pipe:
  - "old" radius/thickness: 18.2/0.8 mm
  - new radius/thickness: 16.0/0.5 mm
- Extremely low material budget:
  - Beam pipe thickness: 500 μm (0.14% X0)
  - Sensor thickness: 20-40 μm (0.02-0.04% X0)
- Material homogeneously distributed:
  - essentially zero systematic error from material distribution

Material budget



- Observations:
  - Silicon makes only about **15%** of total material
  - I**rregularities** due to support/cooling and overlap



- Removal of water cooling
  - **possible** if power consumption stays below 20 mW/cm^2

- Removal circuit board (power+data)
  - **possible** if integrated on chip
- Removal of mechanical support
  - **benefit** from increased stiffness by rolling Si wafers

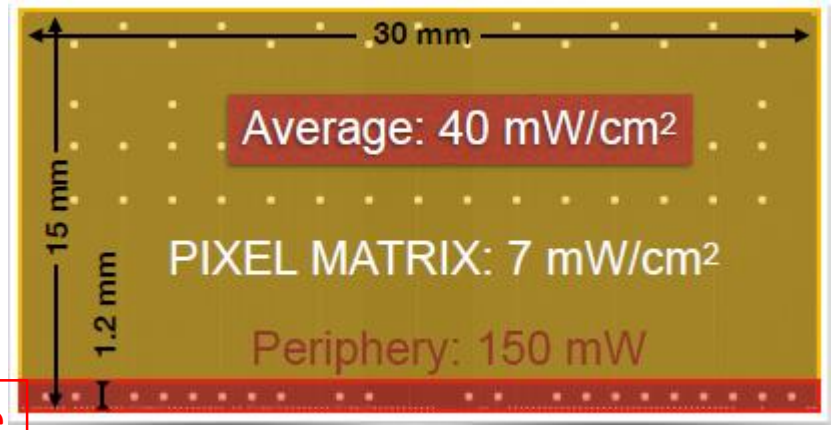
Implementation

- **Air cooling**
  – Possible below 20 mW/cm^2
  – Studied in the context of ITS2
  – Achievable *if* periphery outside the fiducial volume

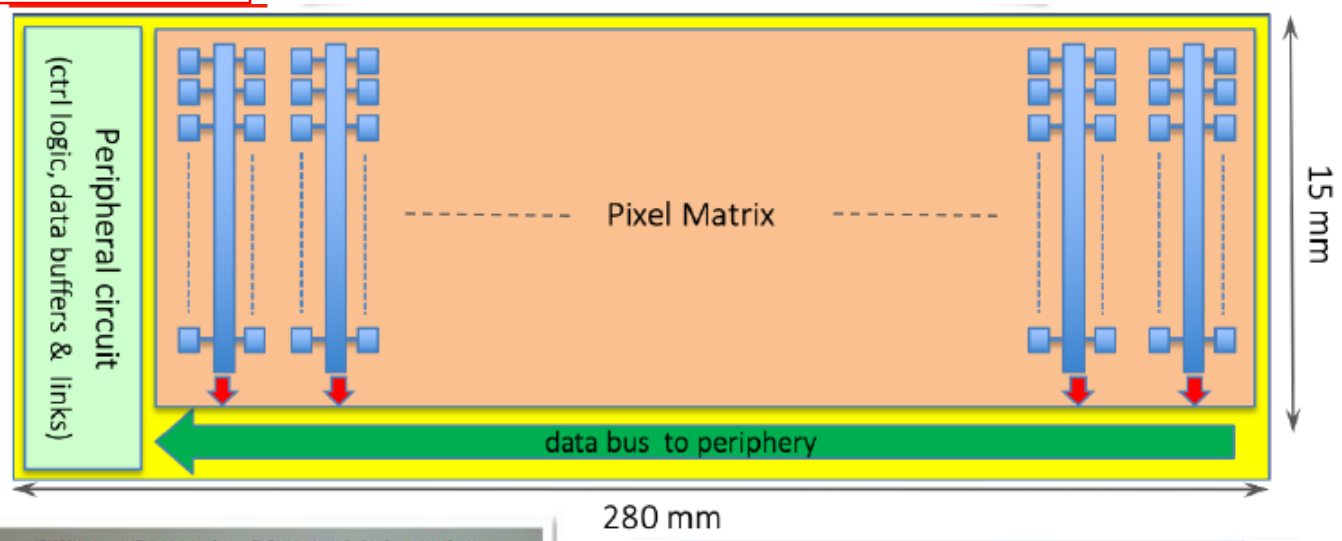
- **Wafer-scale chip**
  – Stitching to overcome reticle size limit
  – Chip spanning half or full stave length
  – Neither support structure nor electrical substrate necessary

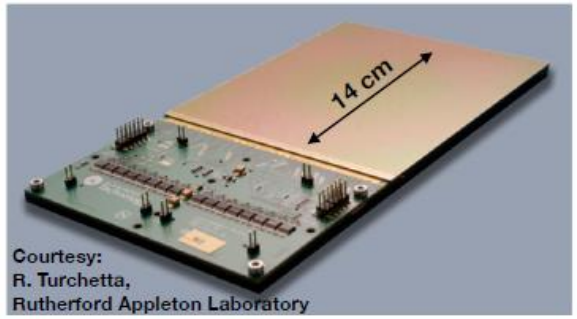
- **Thinning and bending**
  – Currently 50 µm (25 µm active volume)
  – Below 50 µm, Si wafers become flexible, “paper-like”

ALPIDE

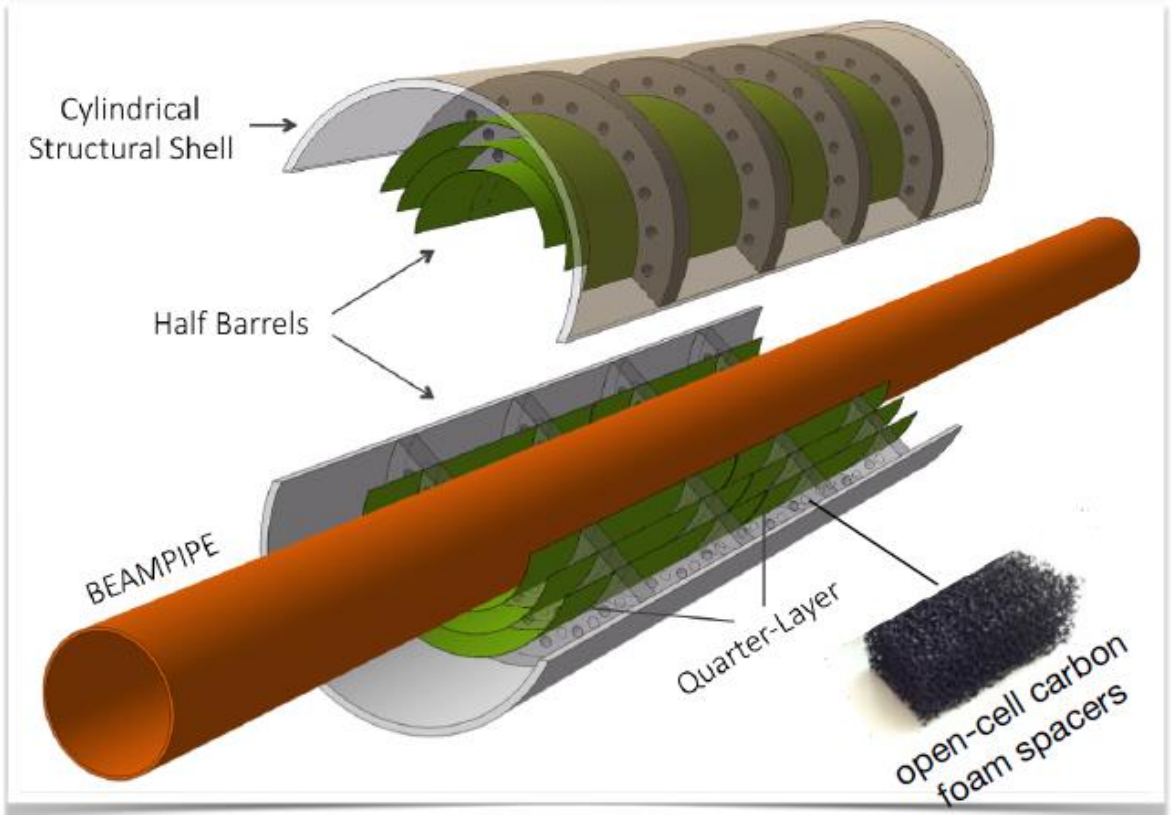


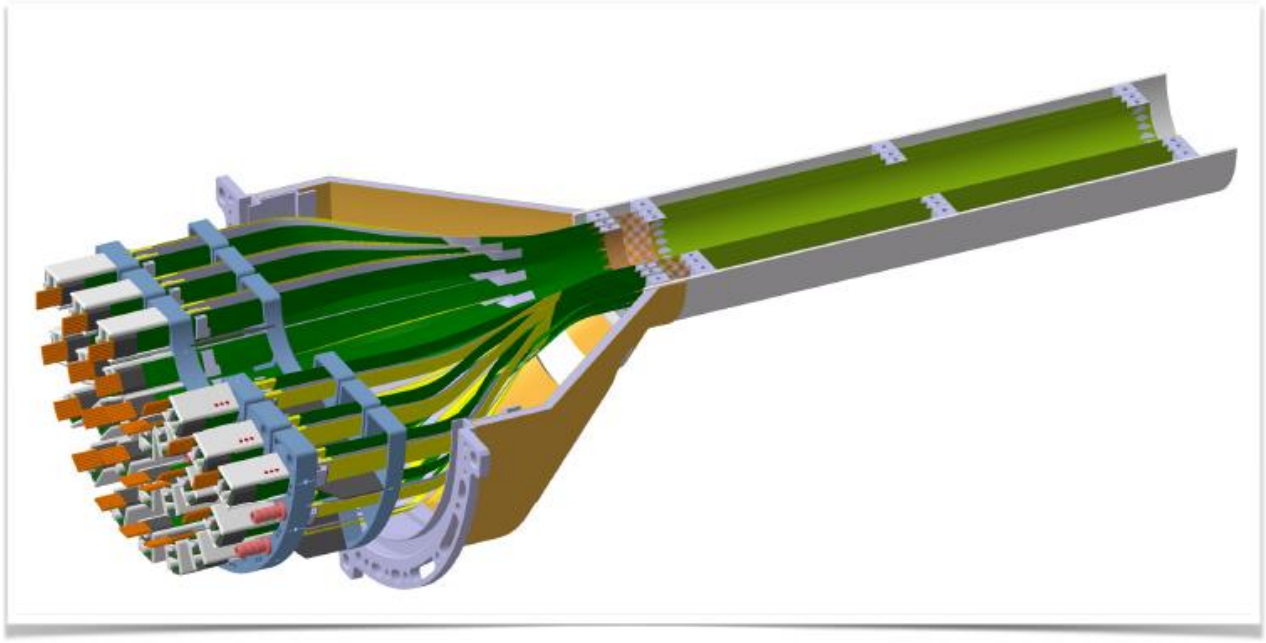
Wafer-Scale





Mechanics layout

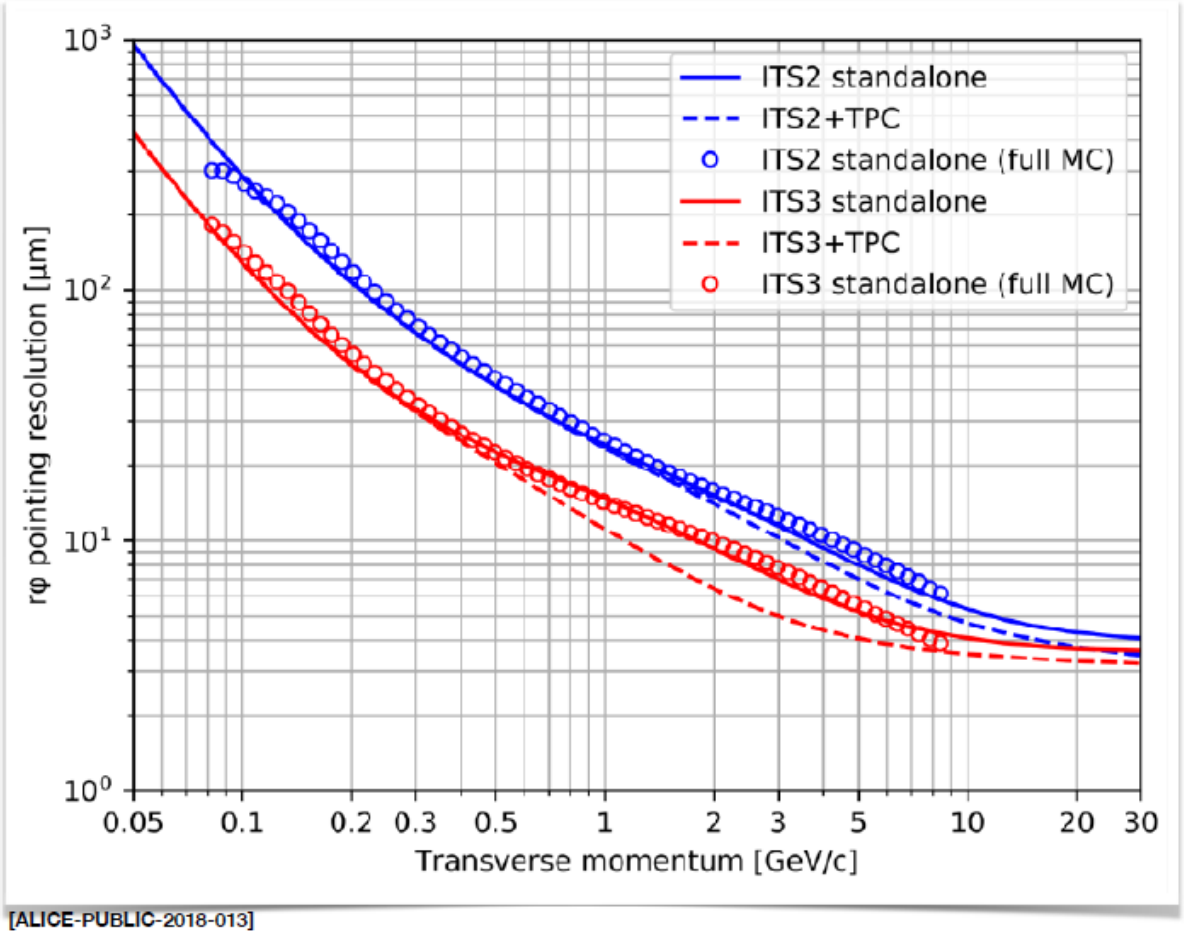




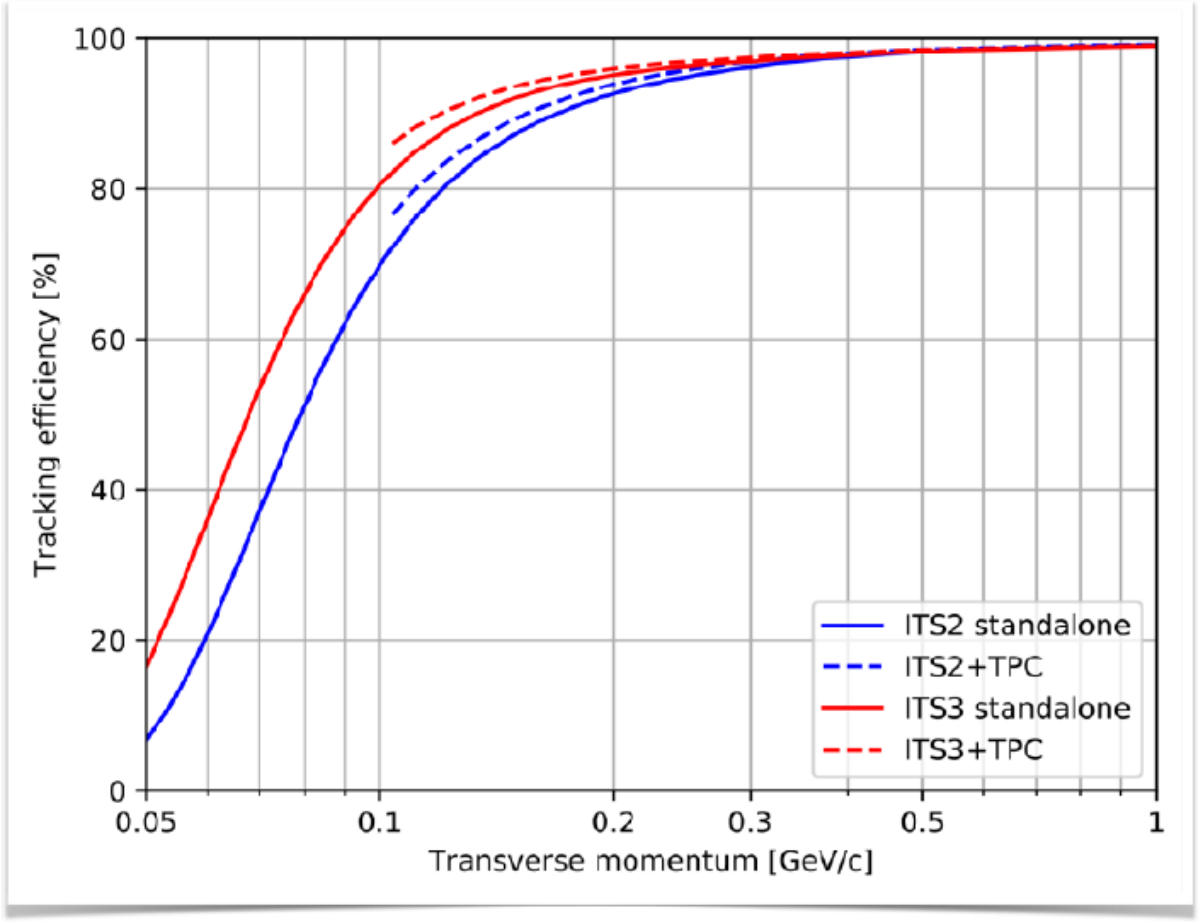
- Possible layout based on air-cooling
- Sensors hold in place with low-density carbon foam

- Fixation into the experiment by surrounding support structure, as well as at both ends
- Cooling at the extremities (chip peripheries)

Simulated ITS3 performance

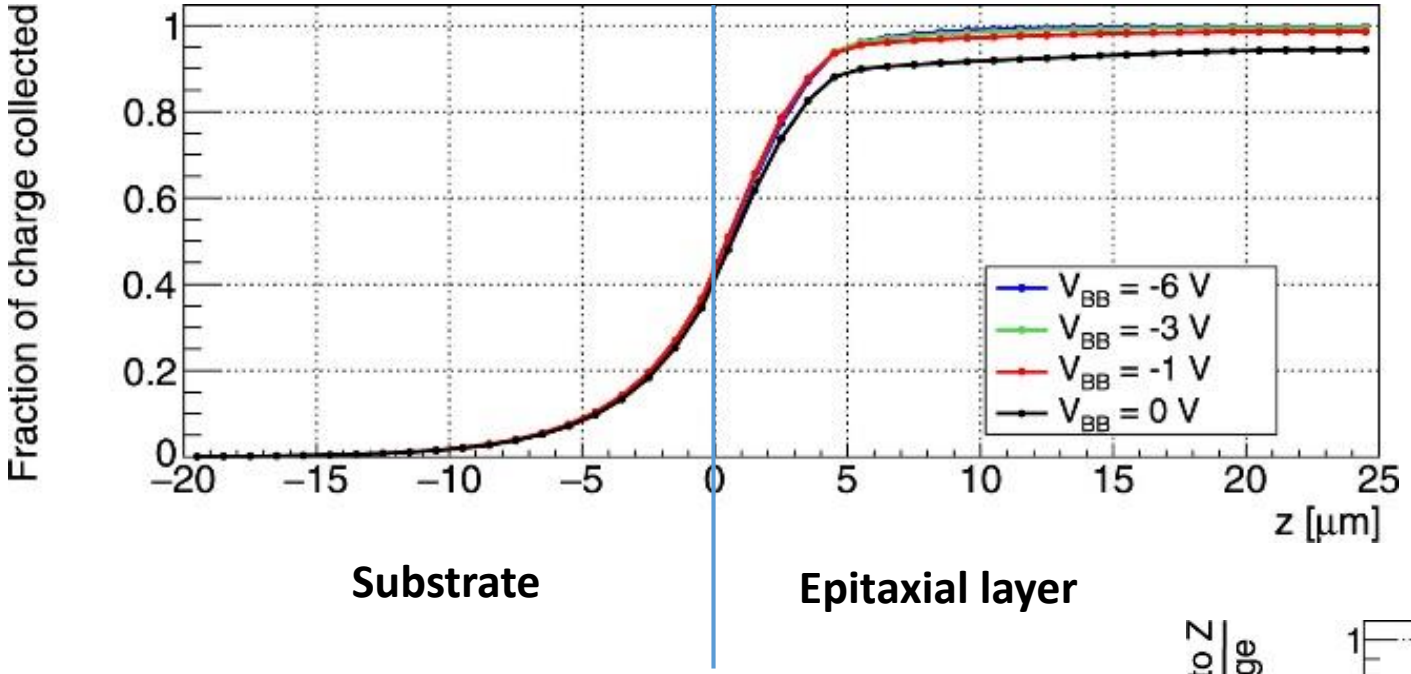


Improvement of a factor of 2 over all momenta

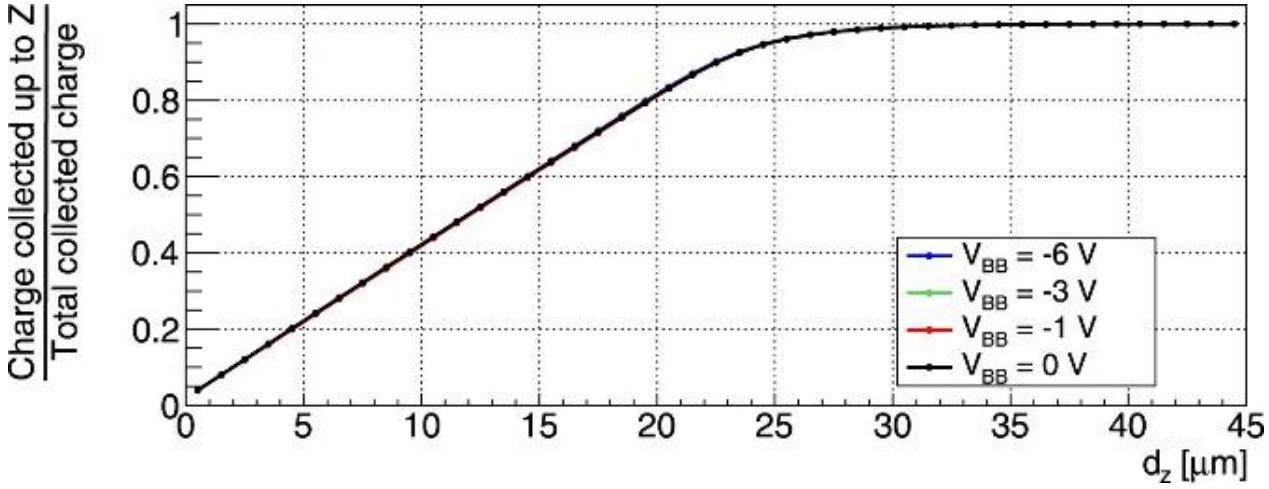


Large improvement at low transverse momenta

How much can the substrate be thinned?

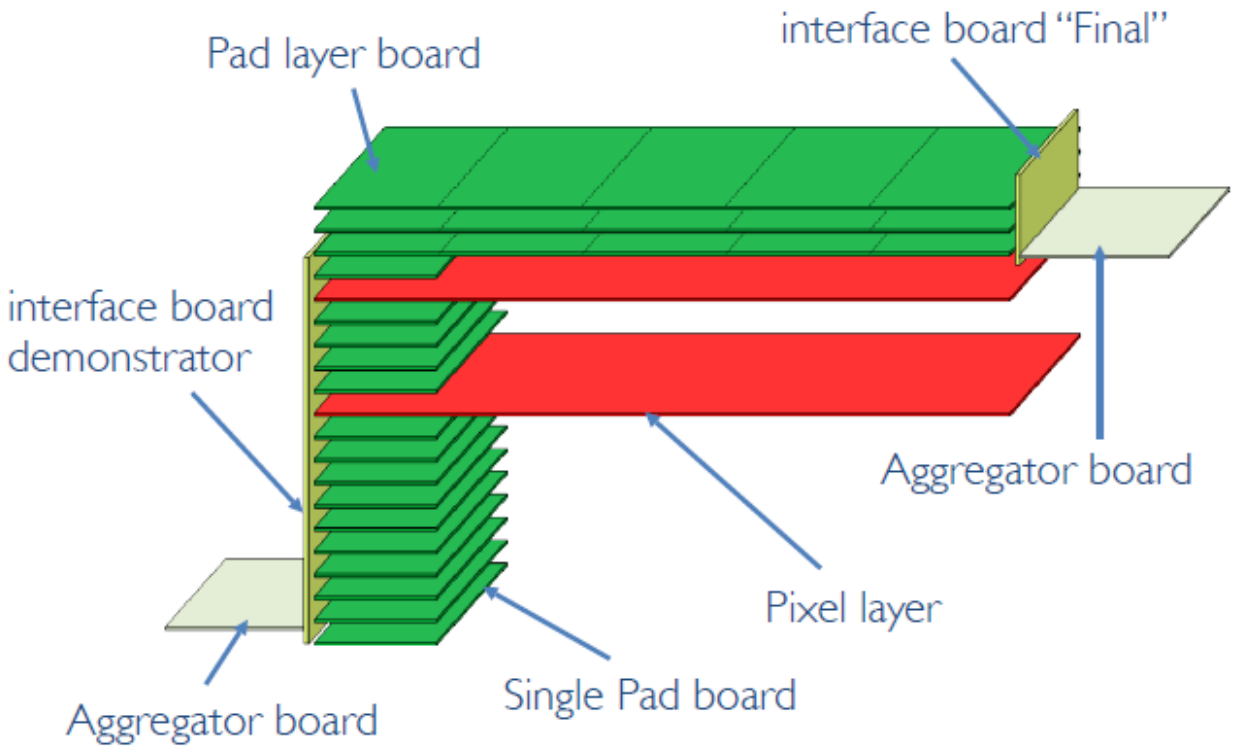


NIM A 950 (2020) 162882



Toward TRD: test module close to final design

FoCal-E test module concept



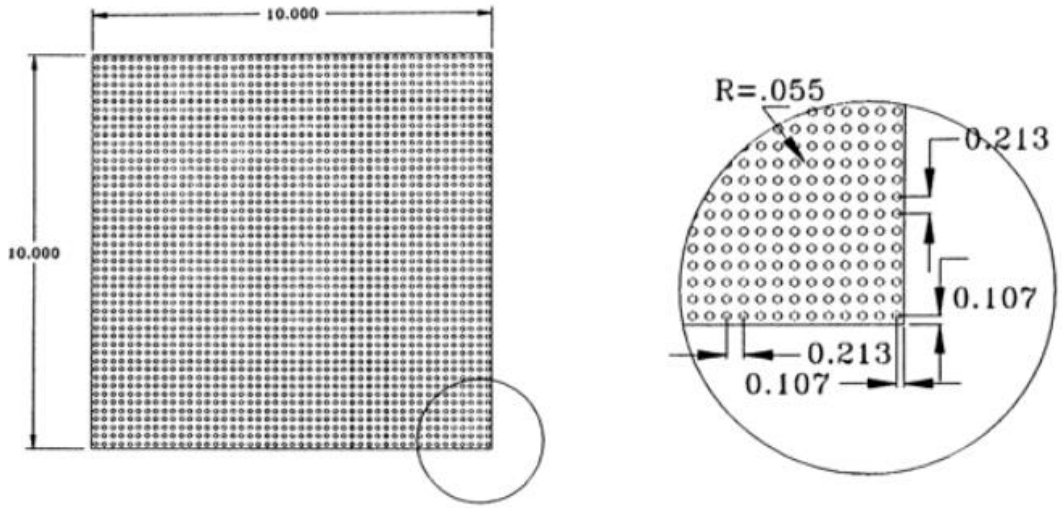
- Use final electronics configuration
- HGCROC + sensor modules + readout
- Pixel modules + readout
- Develop cooling solution
- HCAL module

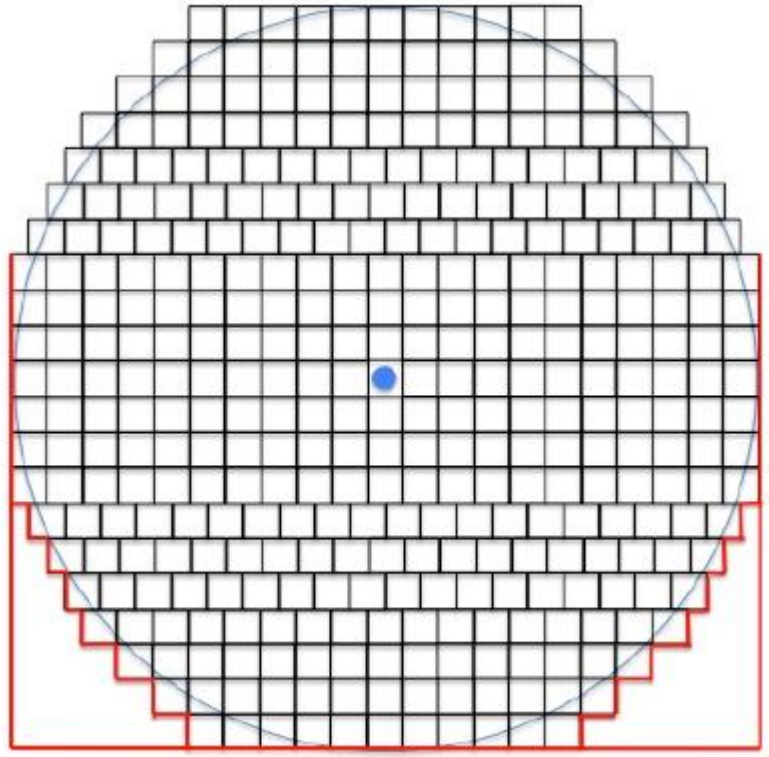
Goals:

- Test/verify performance
- Gain experience with production/assembly
- Optimize processes

FoCal-H design

Allows to isolate photons in FoCal-E and jet measurements





- Pb/scintillating fiber spaghetti calorimeter module as used in E864
- a lead to fiber ratio of 4.55 : 1 by volume to provide good calorimetric compensation and resolution
- a mass of about 100 kg and an active depth of approximately 8 λ_{had}
- Cu as the passive material is also under consideration to reduce the length and weight

- A nearly circular geometry approximately 1 m in radius
- 372 modules
- 1488 towers of 5cm x 5 cm

FoCal timeline

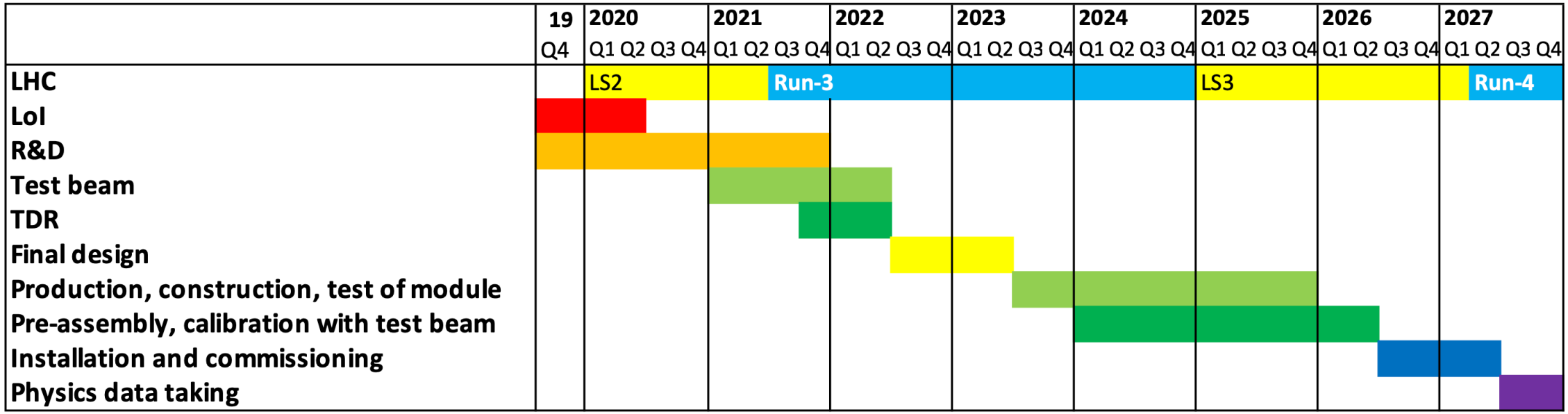


Table 6: Project timeline

Year	Activity
2016–2021	**R&D**
2020	Letter of Intent
2020–2022	**final design**
	Technical Design Report
	design/technical qualifications
2023–2027	**Construction and Installation**
2023–2025	production, construction and test of detector modules
2024–2025	pre-assembly
	calibration with test beam
2026	installation and commissioning
06/2027	Start of Run 4

- Next important step: Entering the engineering phase towards testbeam(s) 2021/22 and TDR
- Production estimated to fit well into 24 months
  Plus half a year of "learning curve"

(not adjusted for Covid-19 changes)