Status of LHCb Upstream Tracker

Ina Carli (IHEP CAS Beijing)

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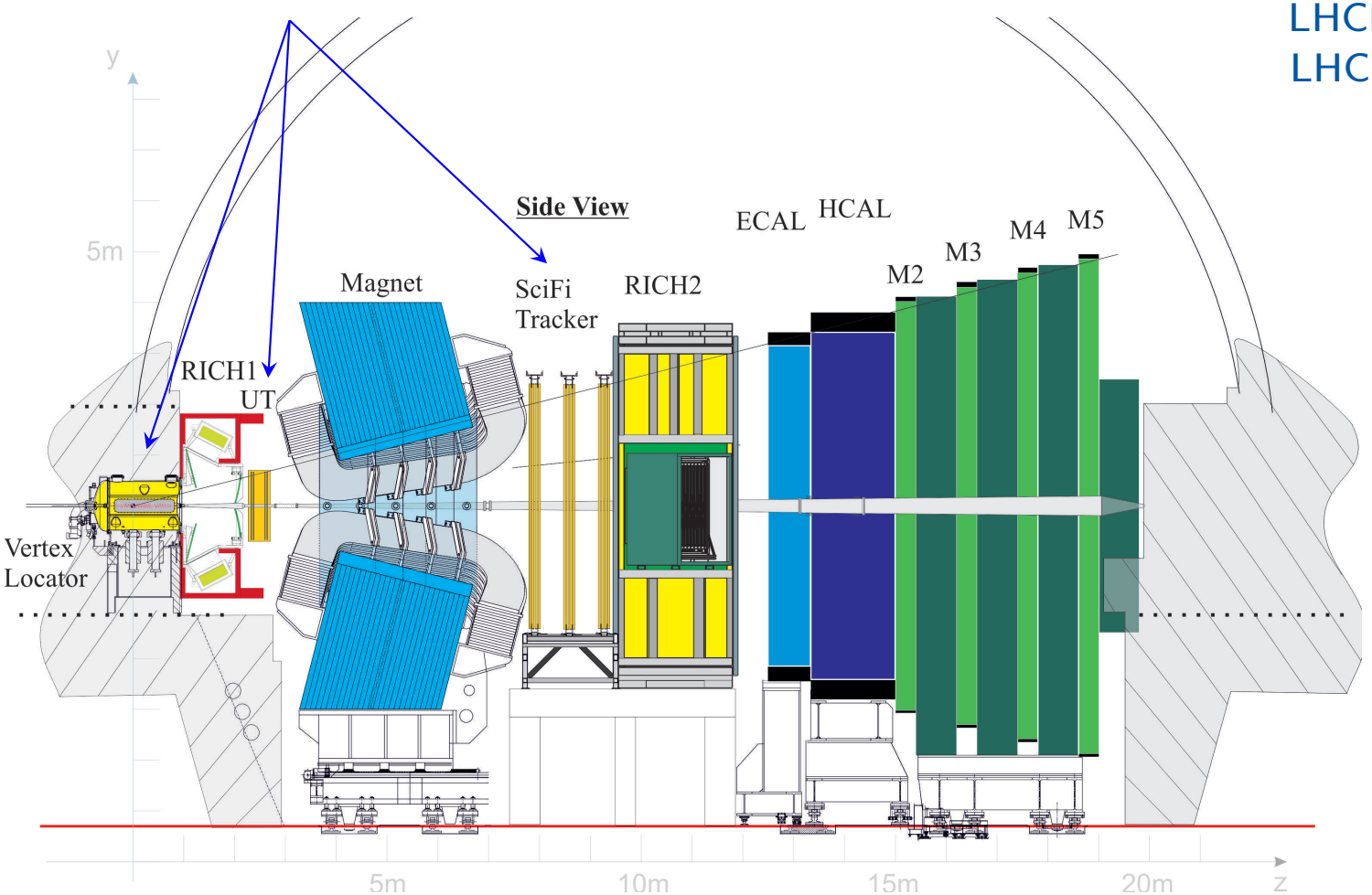
中國科學院高能物理研究所

Institute of High Energy Physics Chinese Academy of Sciences

LHCb upgrade I during LHC LS2

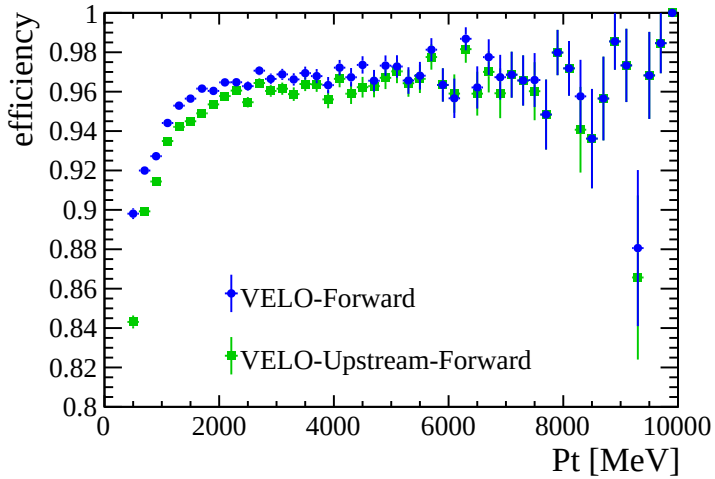
- 5-times higher instantaneous luminosity for Run 3 and 4 ($2 \times 10^{33}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$), expected integrated luminosity $50\,\mathrm{fb}^{-1}$
- new electronics with 40 MHz readout, software-only trigger
- replace tracking detectors, new optics and PMTs of RICH1&2

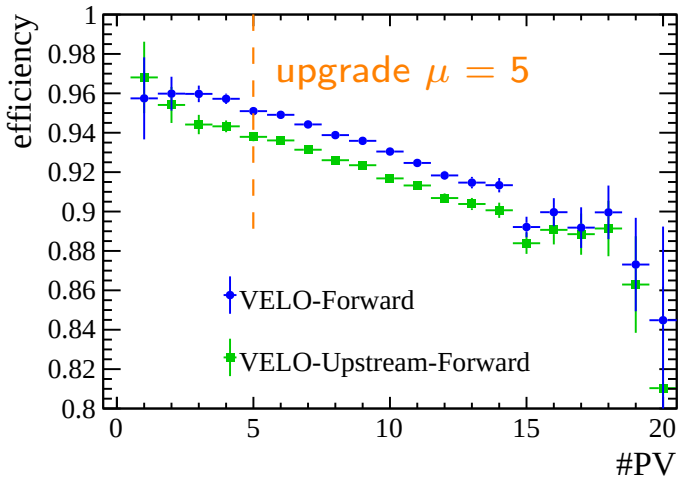
LHCb-TDR-012
LHCb-TDR-015

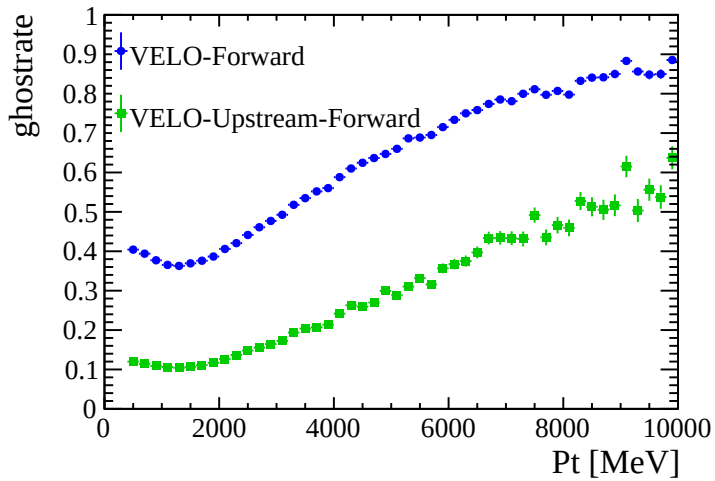


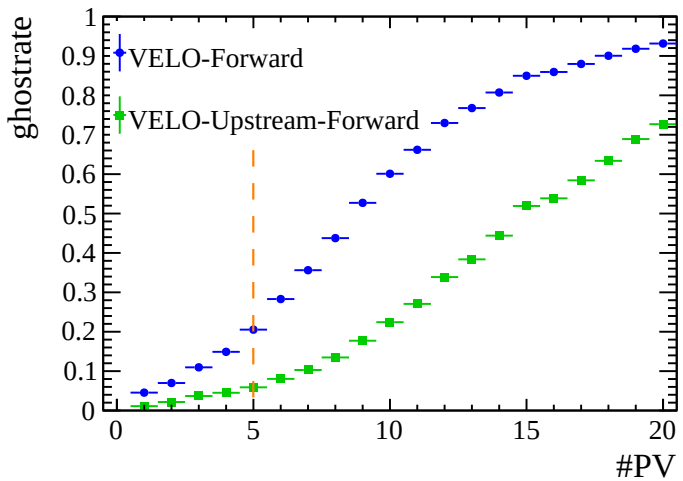
Role of Upstream Tracker (UT)

- improve p_{T} resolution and suppress ghost tracks
- trigger speed up: using Velo+UT matching, very low-p_{T} tracks can be removed ($p_{\mathrm{T}} < 0.4\,\mathrm{GeV}$) and search window in SciFi tightened





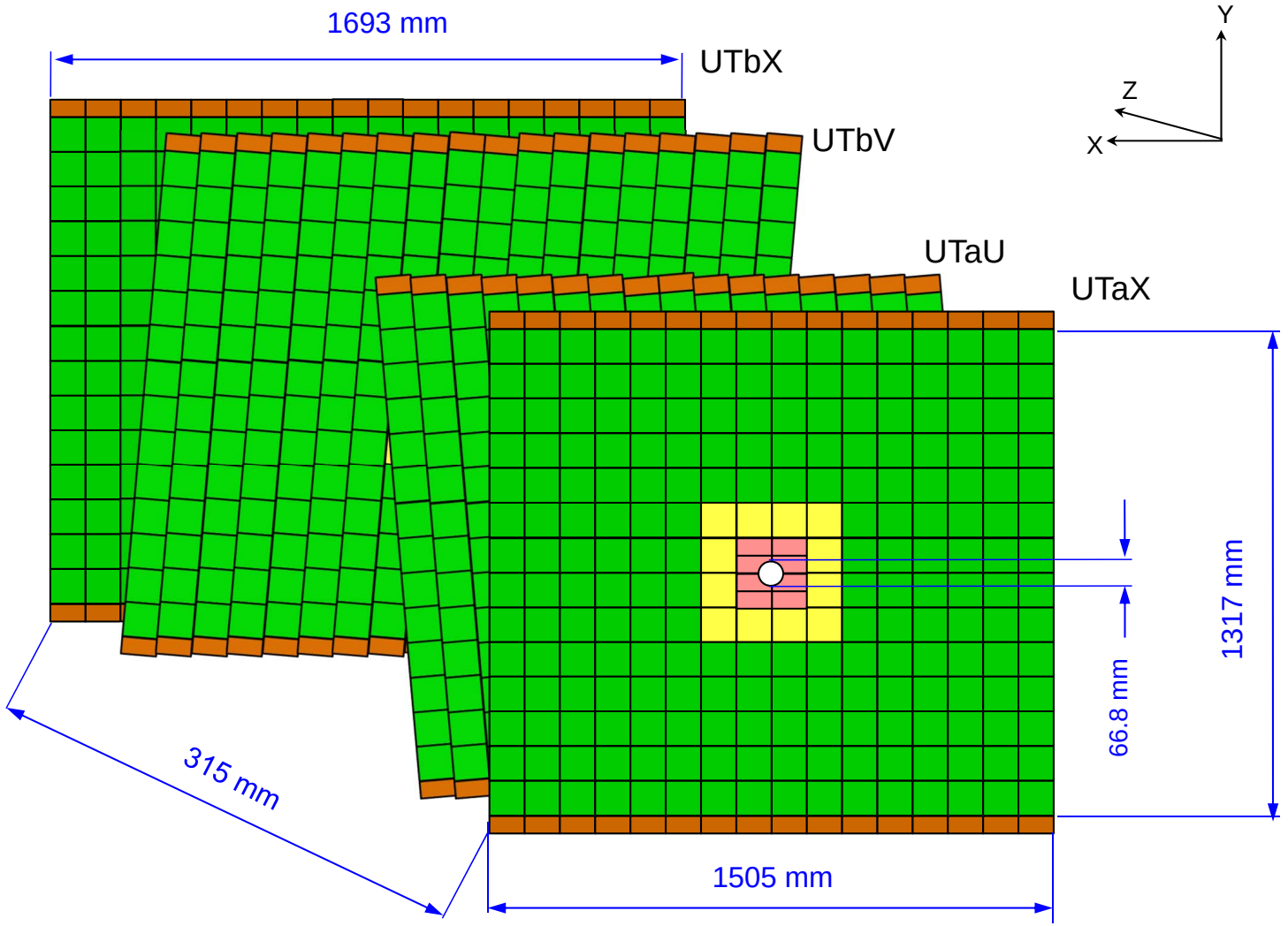




LHCb-PUB-2014-028, LHCb-PUB-2013-023

UT design

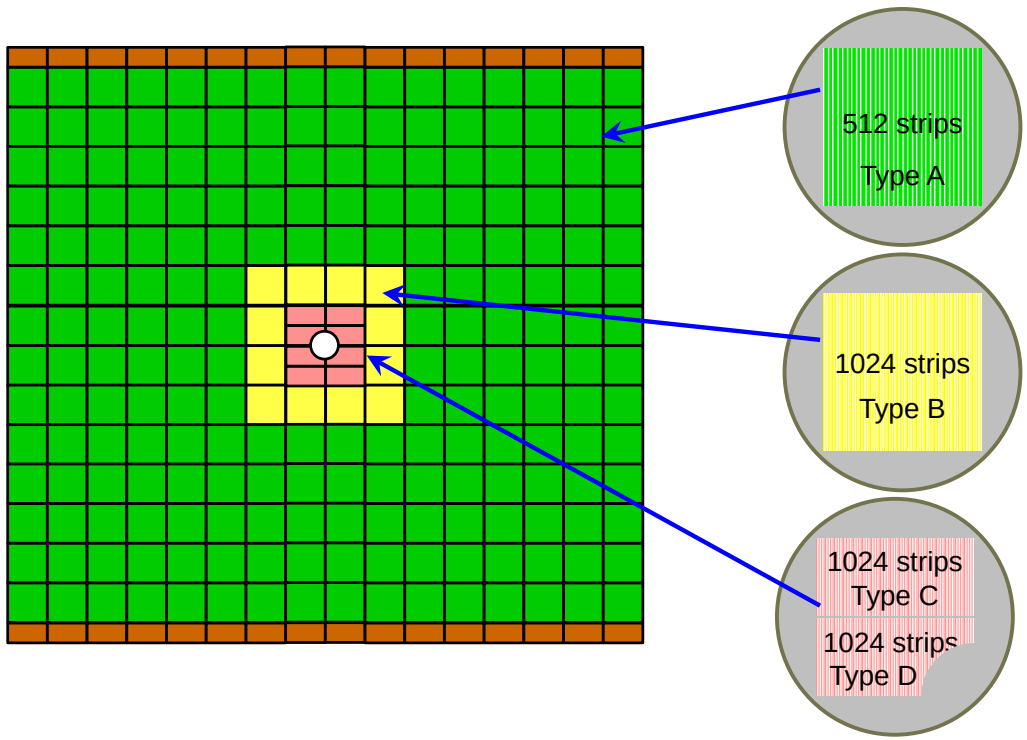
- four detection planes, $\sim 2\,\mathrm{m}^2$ each
- two planes with vertical strips, two rotated by $\pm 5^\circ$
- finer granularity than previous detector, closer to beampipe



Sensors

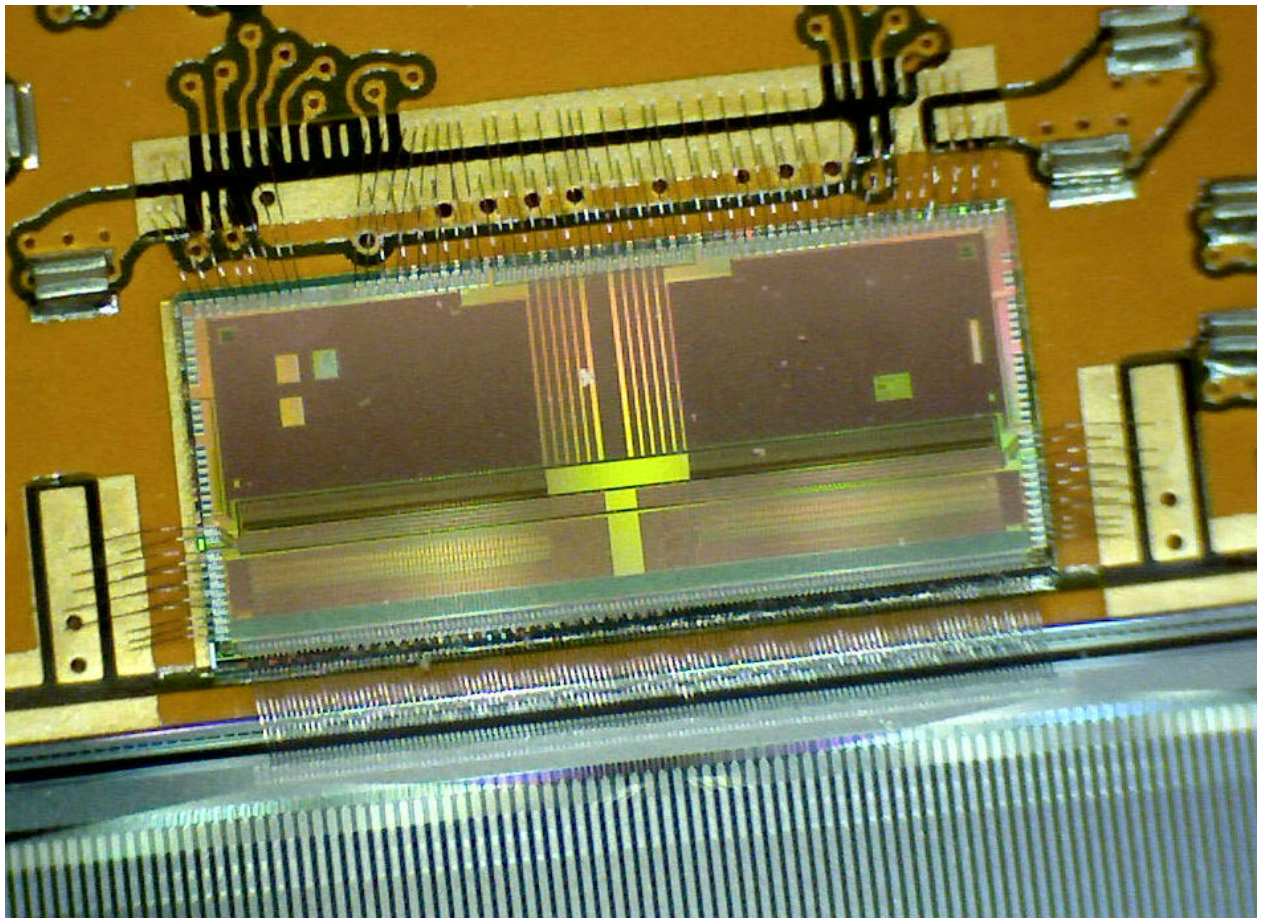
- 968 silicon strip sensors
- finer segmentation and radiation hardness in inner-most region

Sensor	Type	Thickness	Pitch	Length	Strips	# sensors
A	*p-in-n*	320 μm	187.5 μm	99.5 mm	512	888
B	*n-in-p*	250 μm	93.5 μm	99.5 mm	1024	48
C	*n-in-p*	250 μm	93.5 μm	50 mm	1024	16
D	*n-in-p*	250 μm	93.5 μm	50 mm	1024	16



Readout chip

- SALT (Silicon ASIC for LHCb Tracking)
- 128 channels, 6-bit ADC (5 bit and polarity), 40 MHz readout
- total of 4192 chips

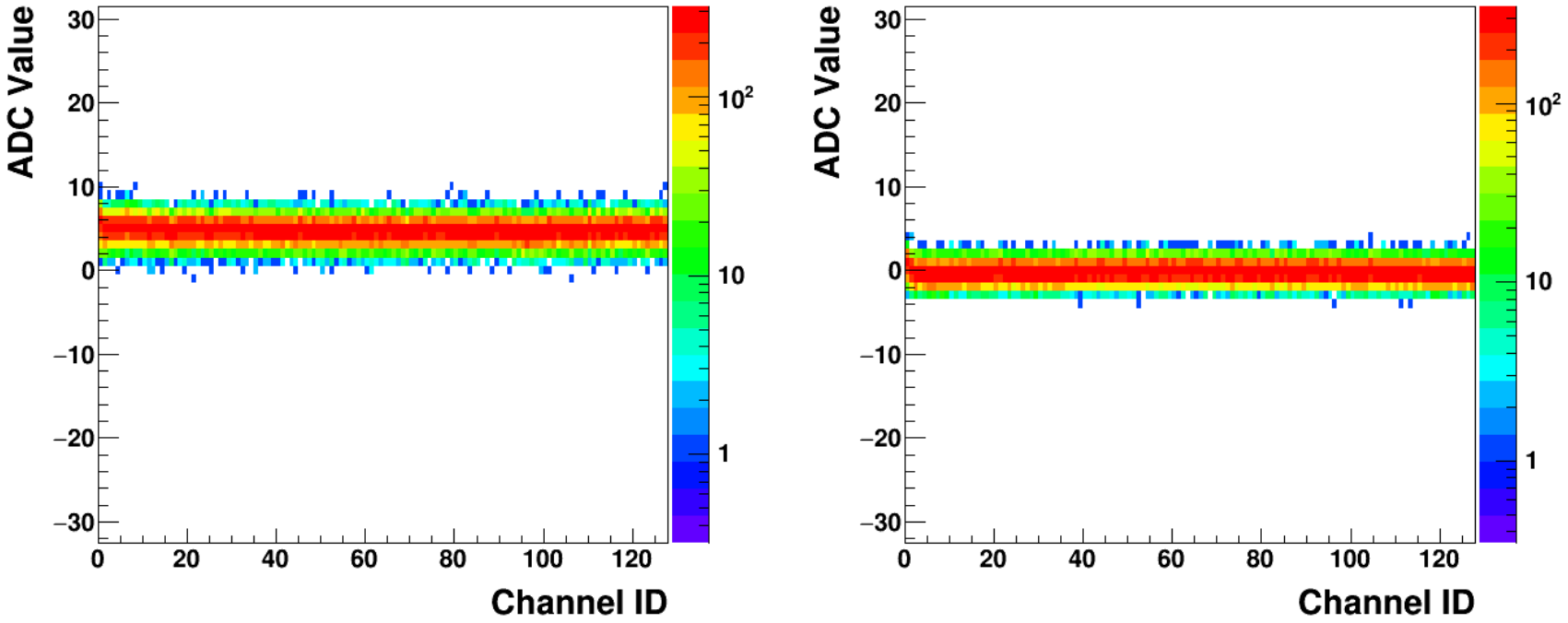


M. Artuso et al, First Beam Test of UT Sensors with the SALT 3.0 Readout ASIC, DOI:10.2172/1568842

Readout chip

- per-channel TrimDAC correction and pedestal subtraction

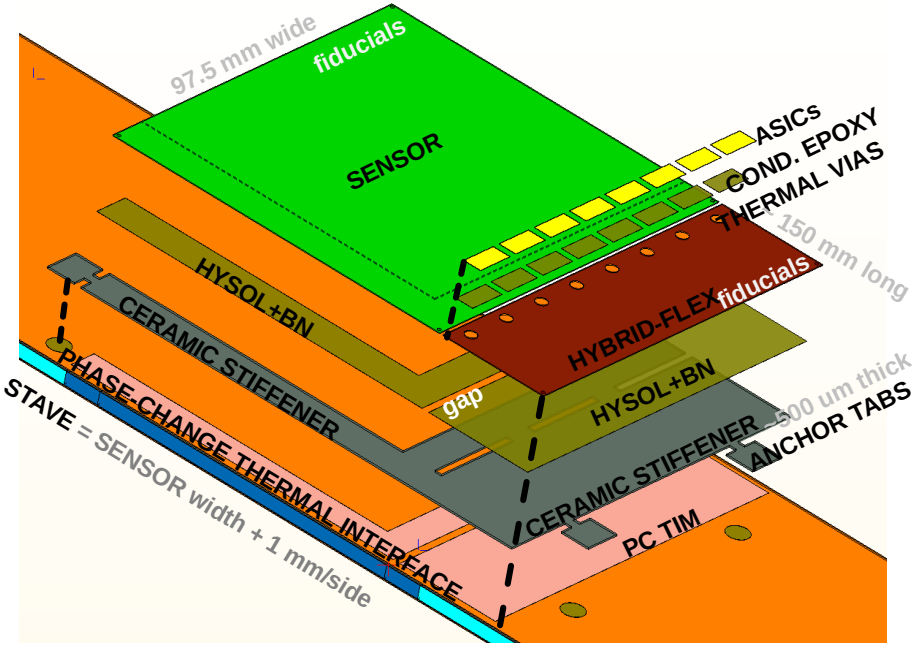
without correction (raw) → with baseline correction

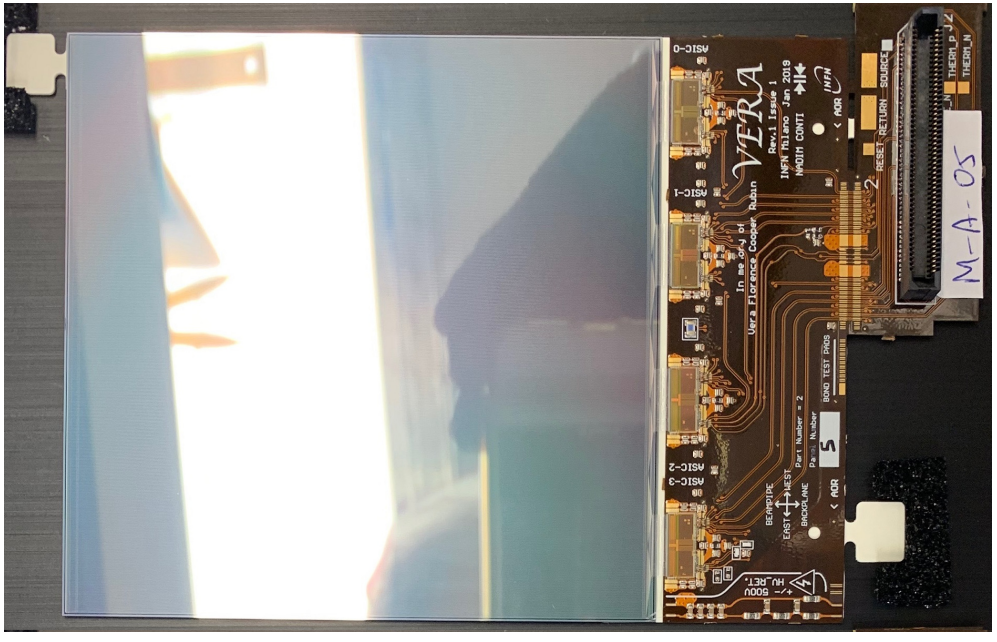


- common mode noise correction
- zero suppression
- latest version fixed baseline oscillations

Module

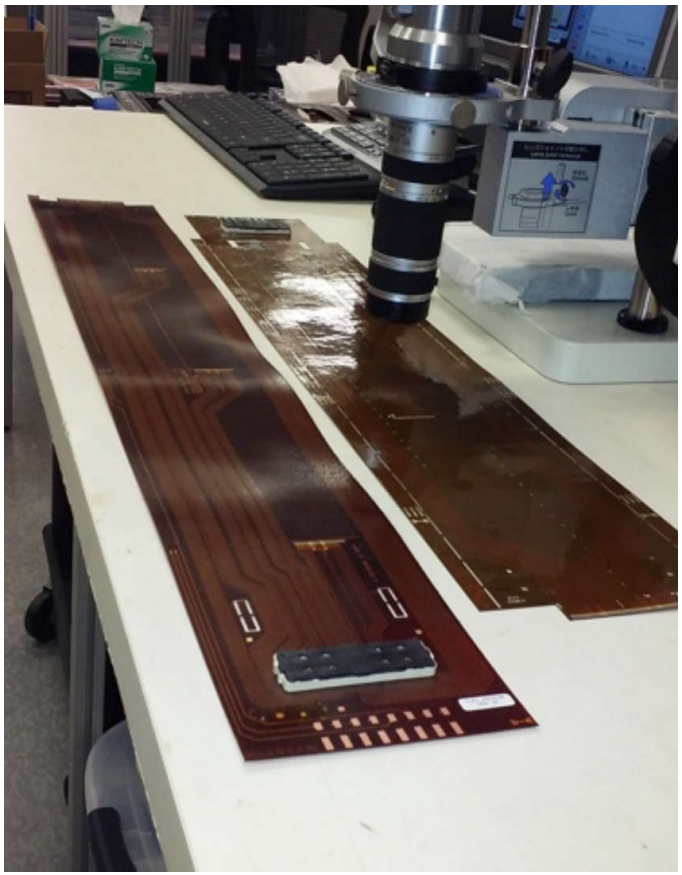
- hybrid circuit with 4 or 8 chips
- thermally decoupled from sensor
- stiffener supports 2 sides of sensor $\rightarrow$ 1 corner free to move
- total of 968 modules on 68 staves

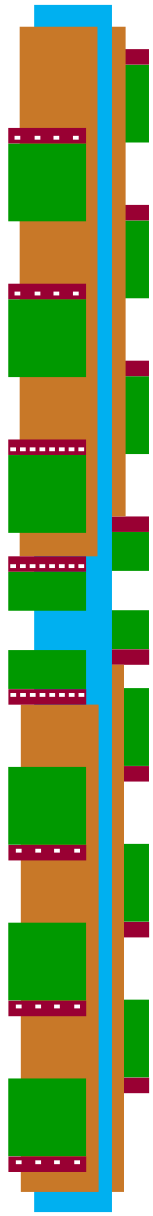


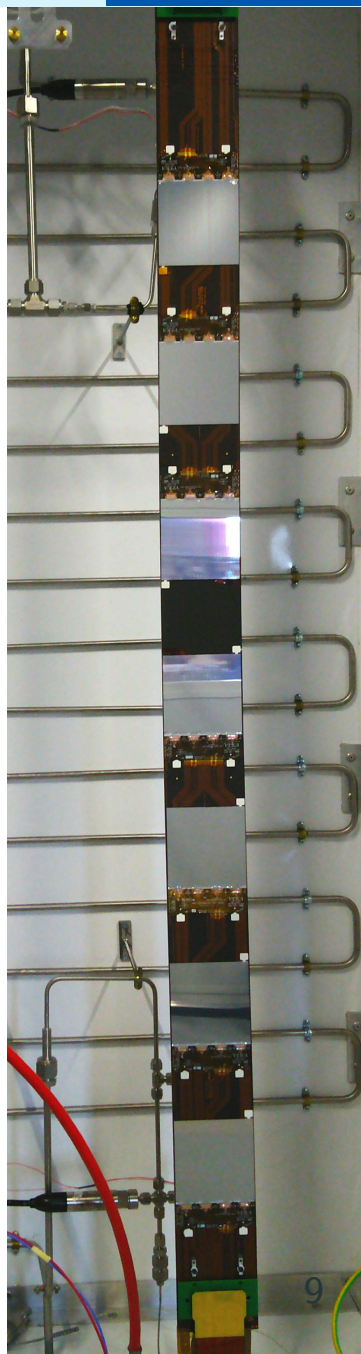


Stave

- 1.6 m x 10 cm low-mass support
- integrated Ti pipe for CO_2 cooling
- 4 low-mass Kapton flexes for readout, power and grounding (360 μm thick, copper $< 70\,\mu m$)
- sensors on front and back face overlap

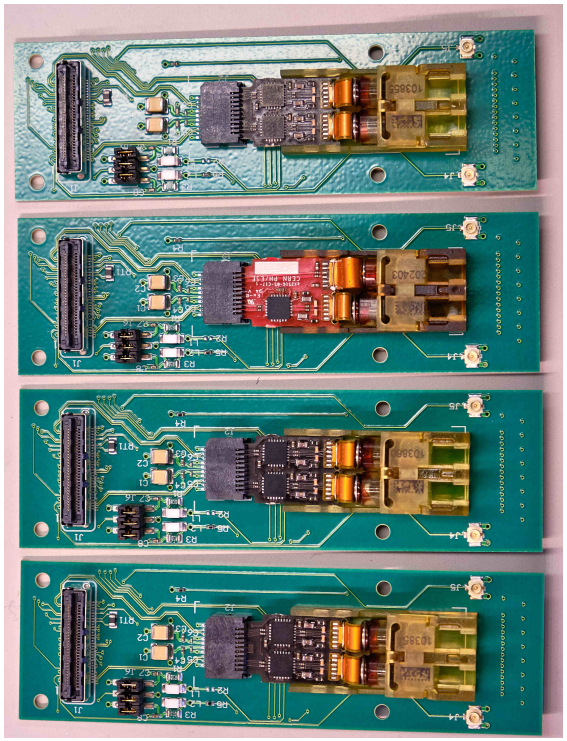


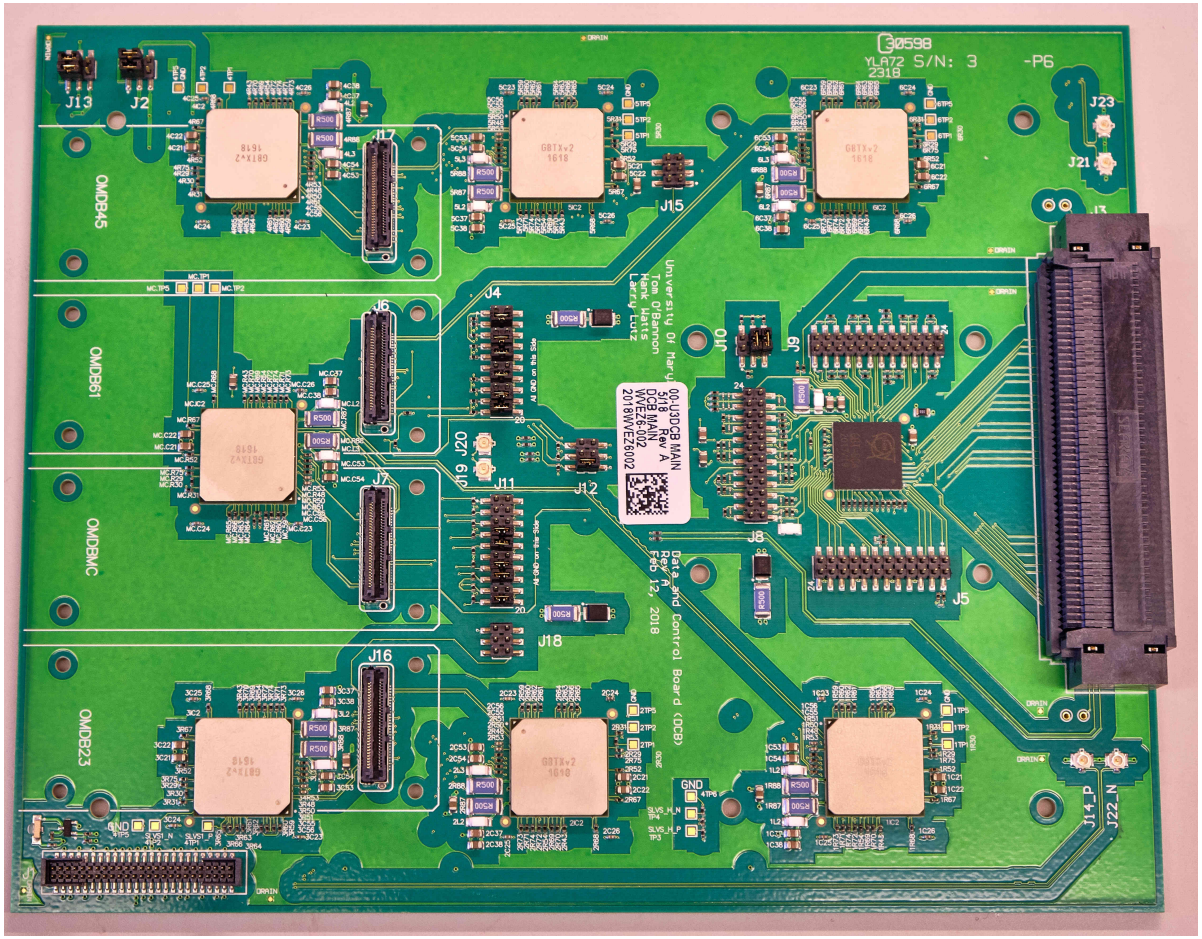




Near-detector readout electronics

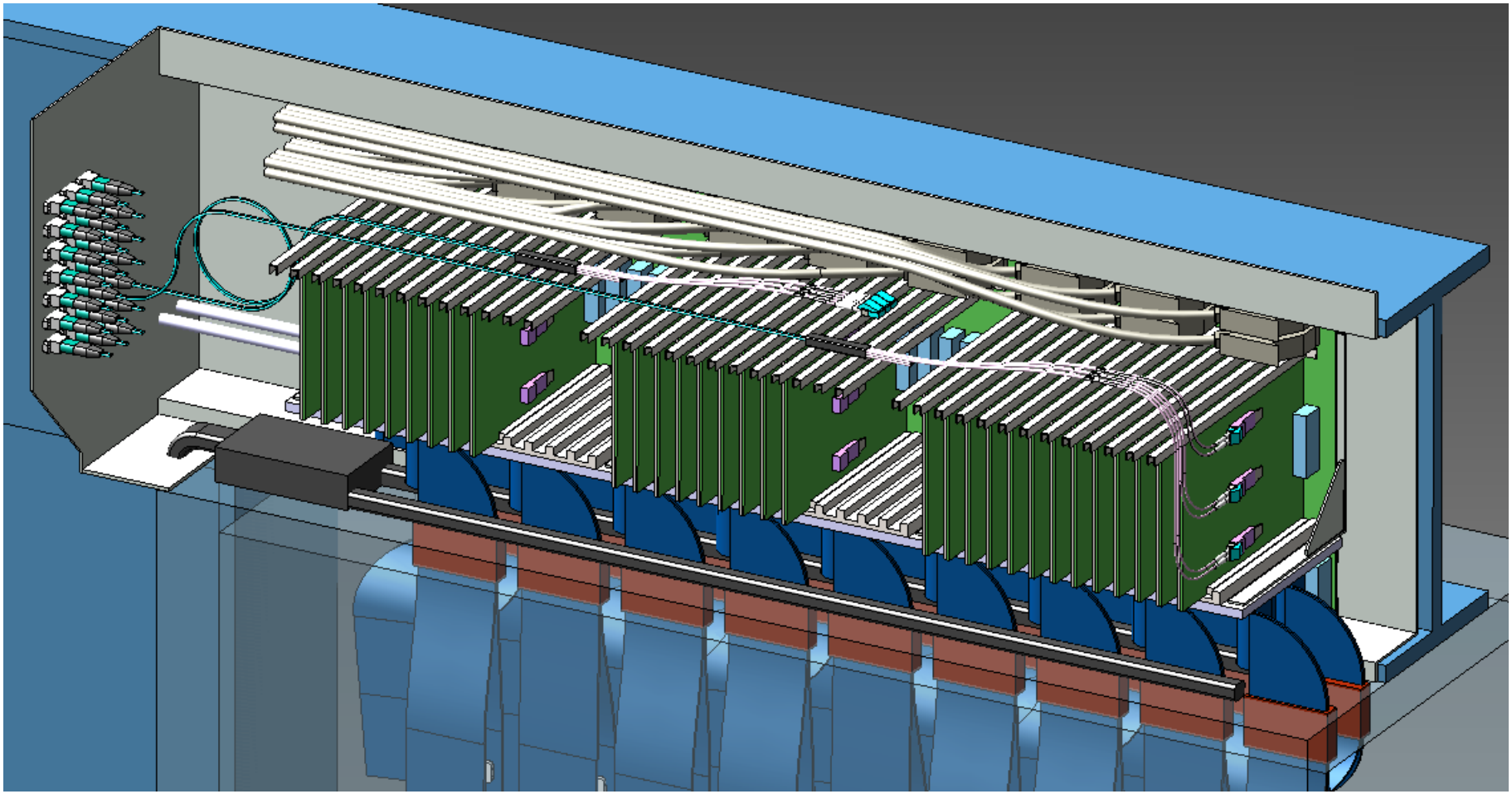
- Data Control Boards:
  - chips for data formatting, timing distribution, controls using GBT chipset (7 GBTx and 1 GBT-SCA)
  - Versatile Link optical transceivers - 3x VTTx and 1 VTRx, 4.8 Gb/s per fiber
  - 8 optic fibers





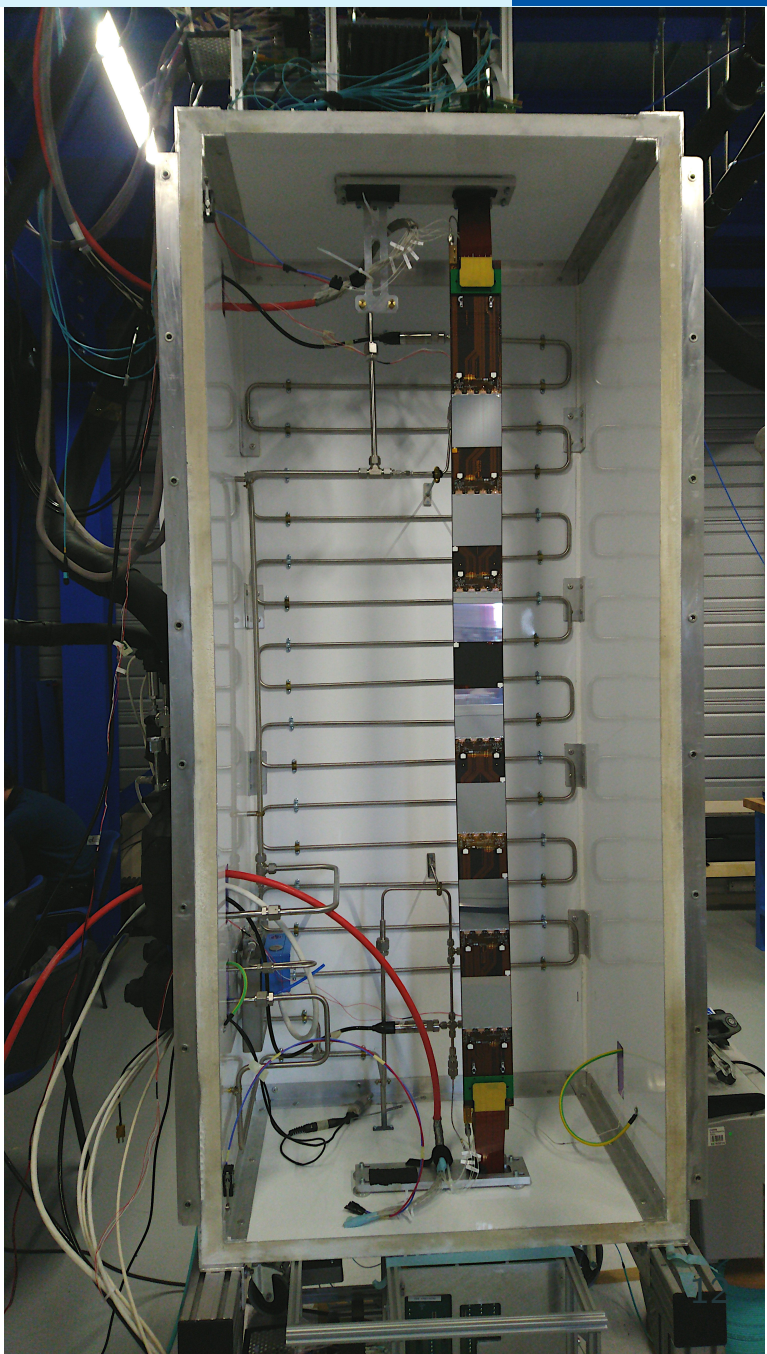
Near-detector readout electronics

- 248 DCBs in 8 PEPI crates (Peripheral Electronics Processing Interface)



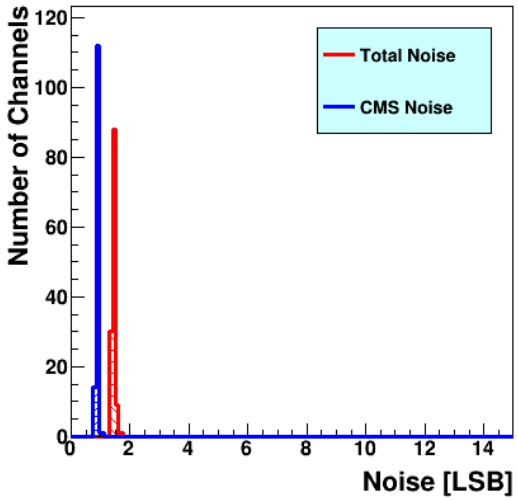
System tests at CERN

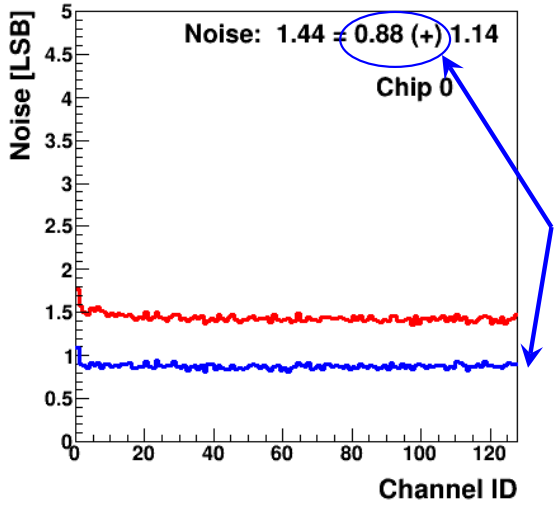
- 7 production-quality modules
- final version of powering and readout schemes
- CO_2 cooling, tested $-30\,℃$ to $20\,℃$
- check performance and long-term stability
- software development
- test of mounting procedures



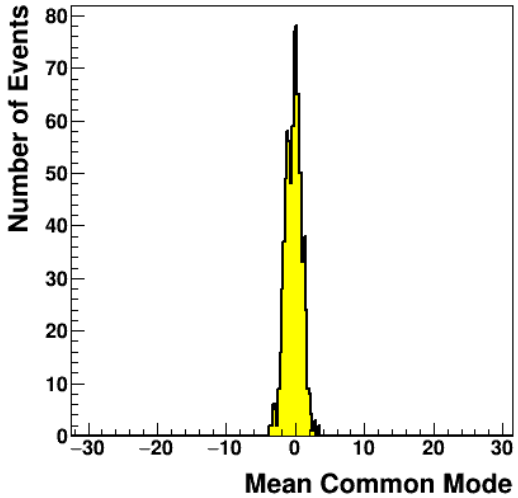
Performance

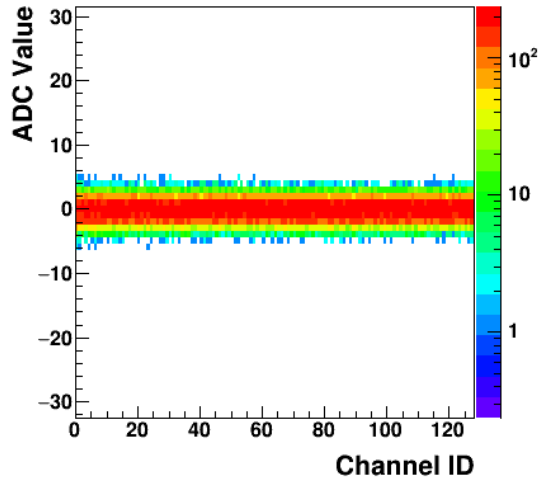
- noise on stave similar to single-module tests
- example at 5 °C, 400V bias: noise $\sim$ 0.88, MIP signal $\sim$ 13 $\rightarrow$ S/N $\sim$ 15





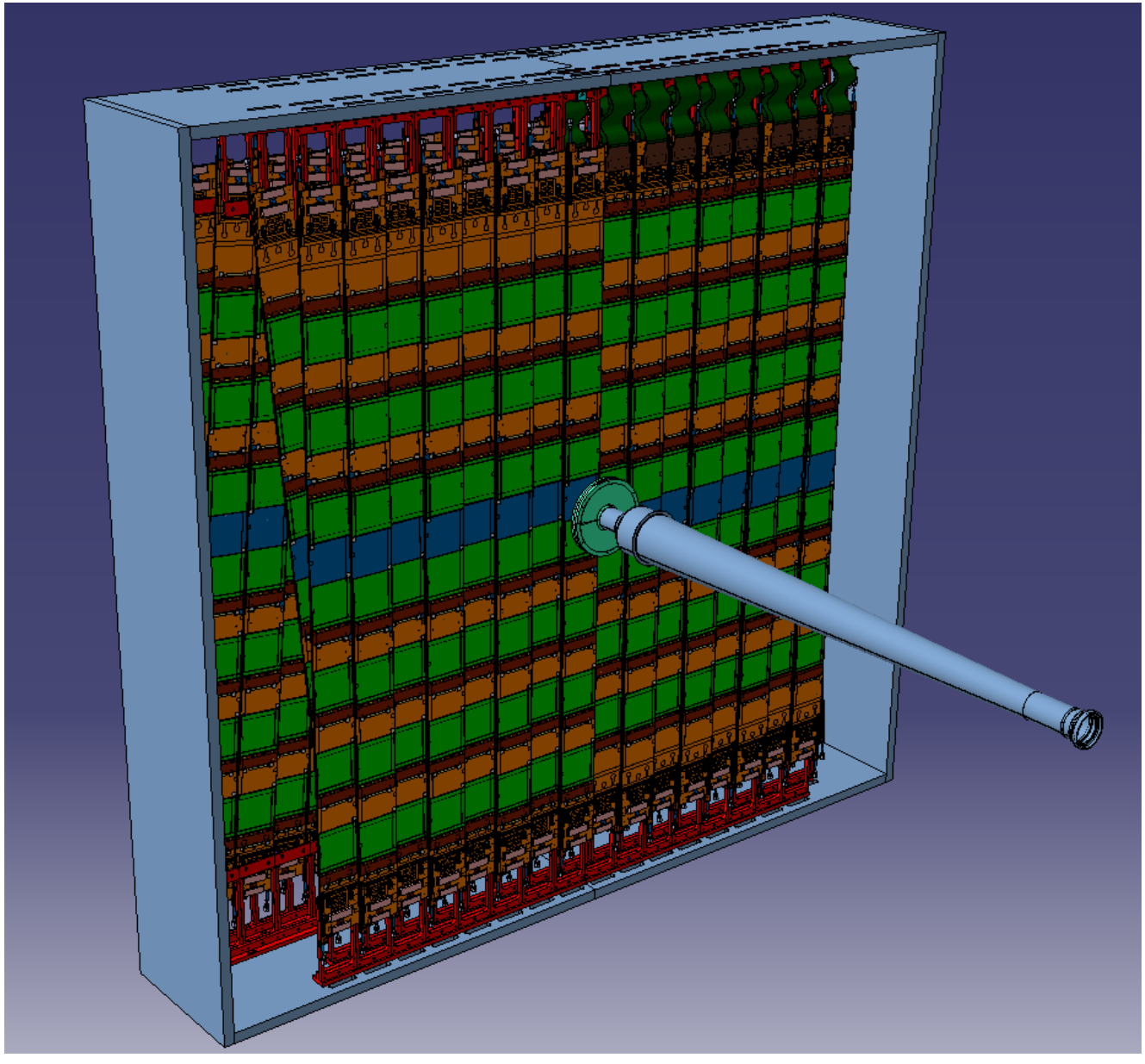
common-mode subtracted noise



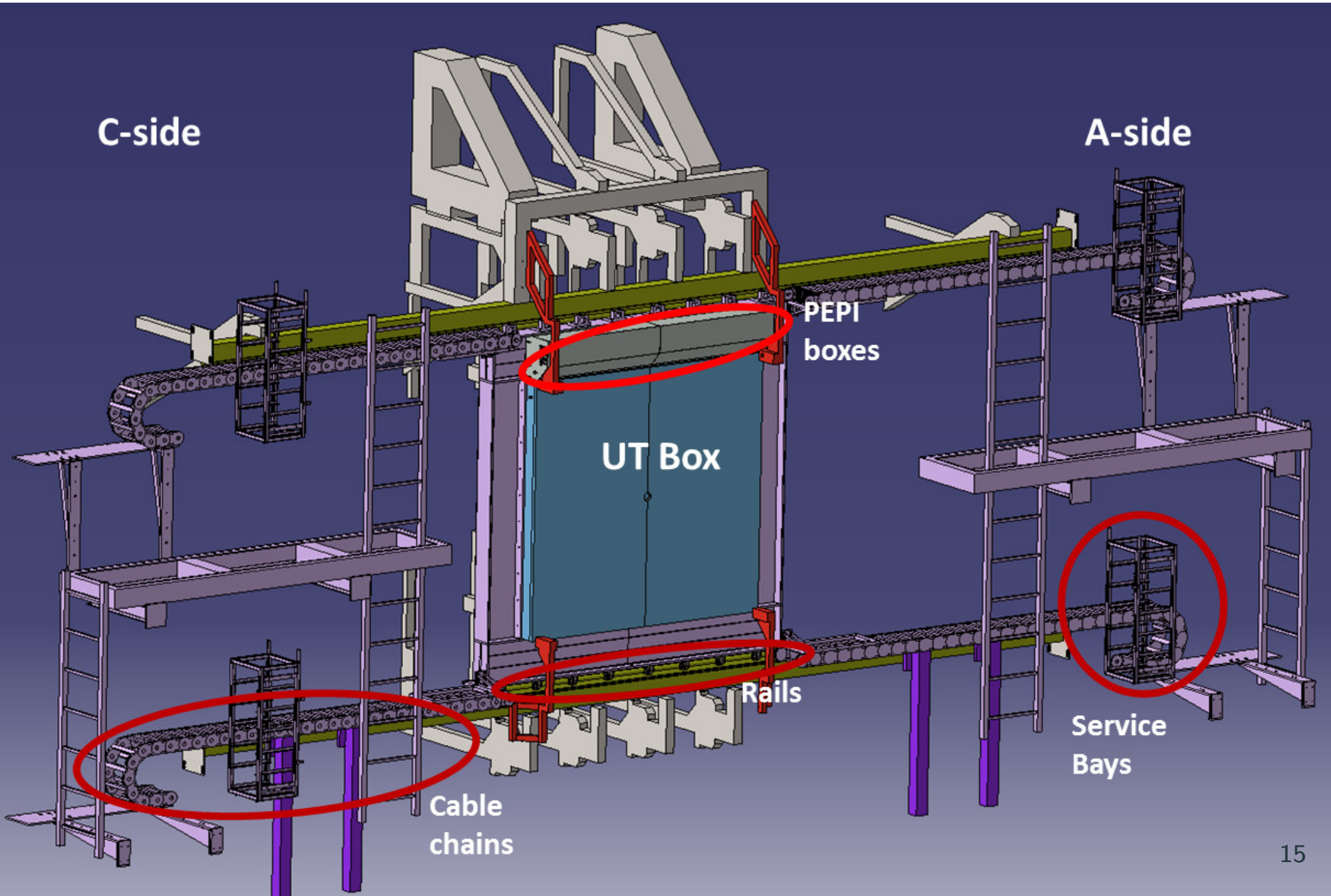


Integration

- most of mechanics and cabling delivered, being prepared at CERN

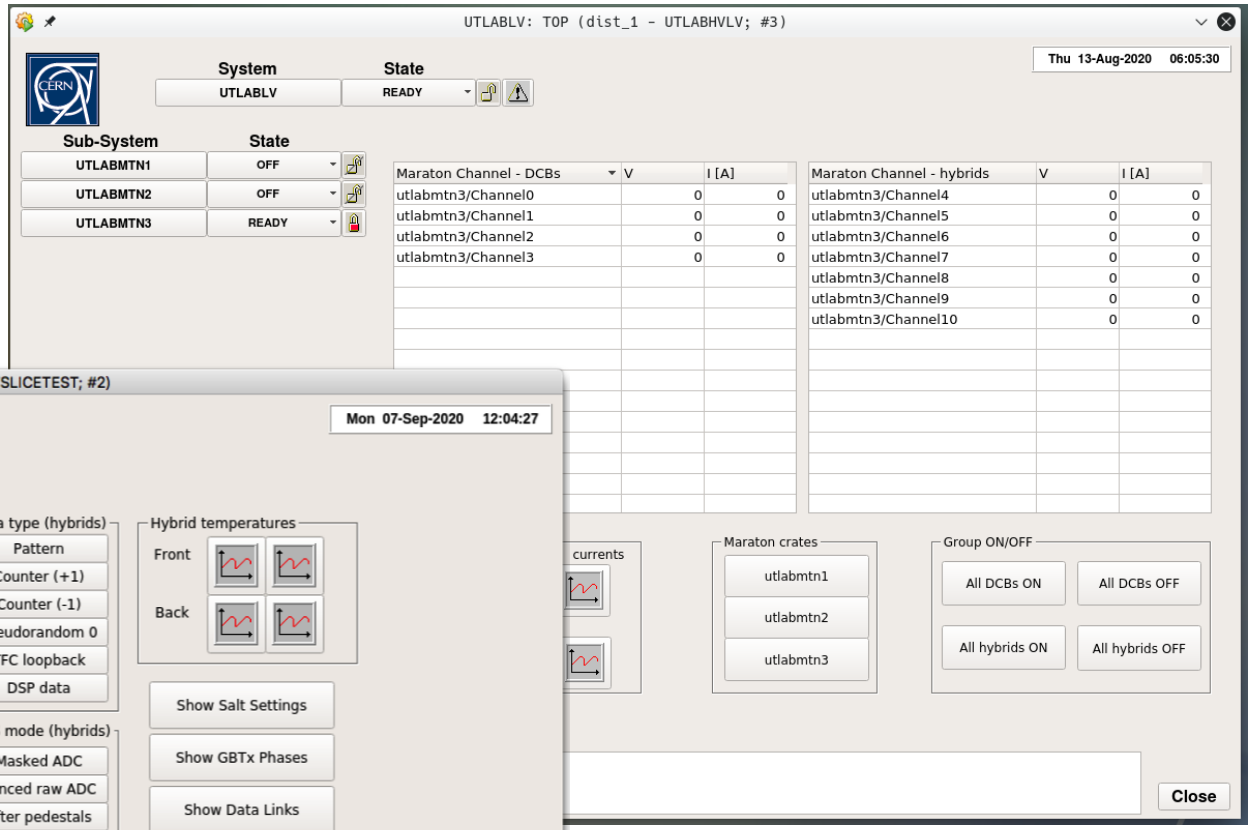


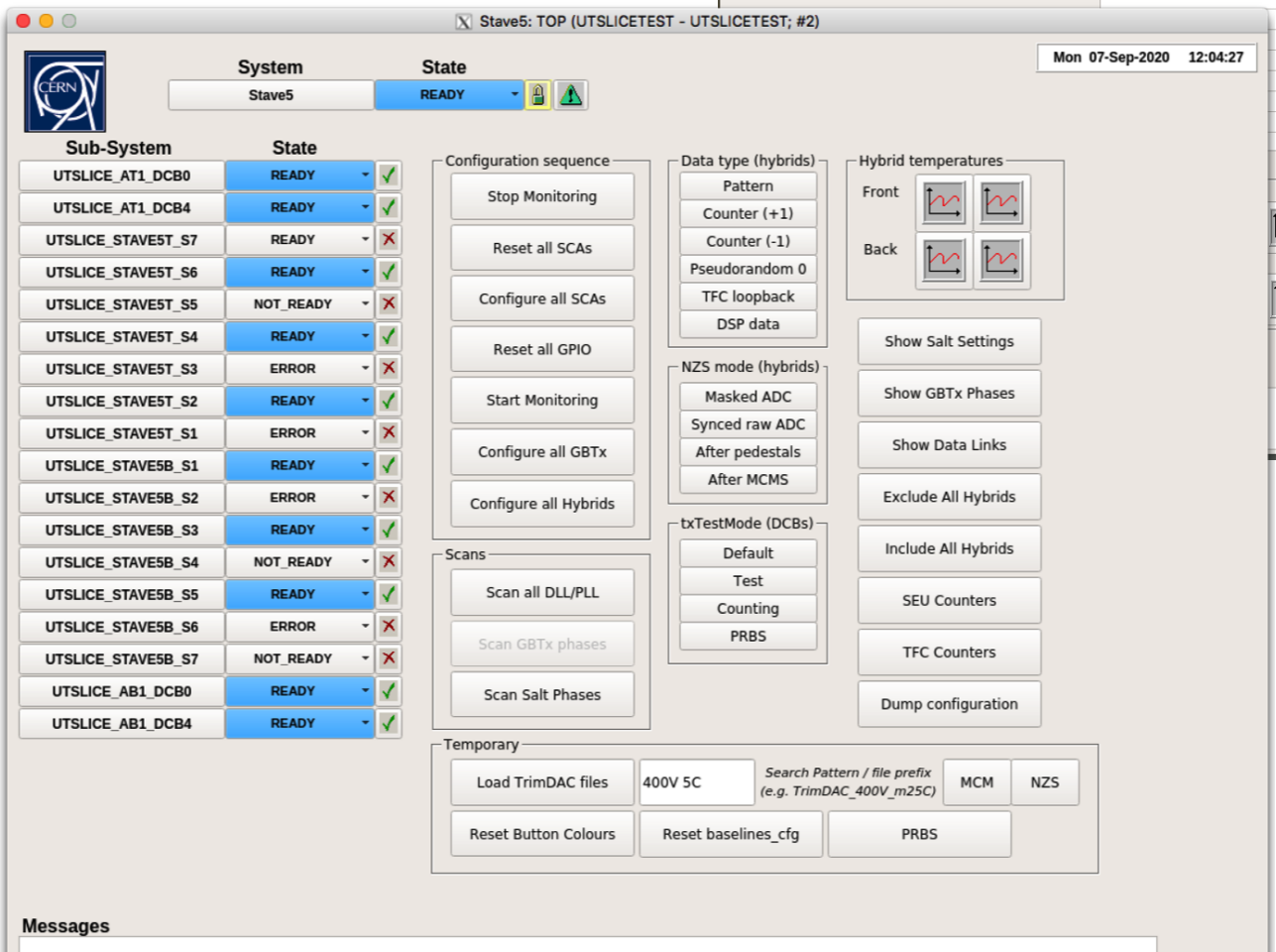
Integration



Readout and control systems (DAQ, DCS)

- developing system for commissioning
- then extend it for final system

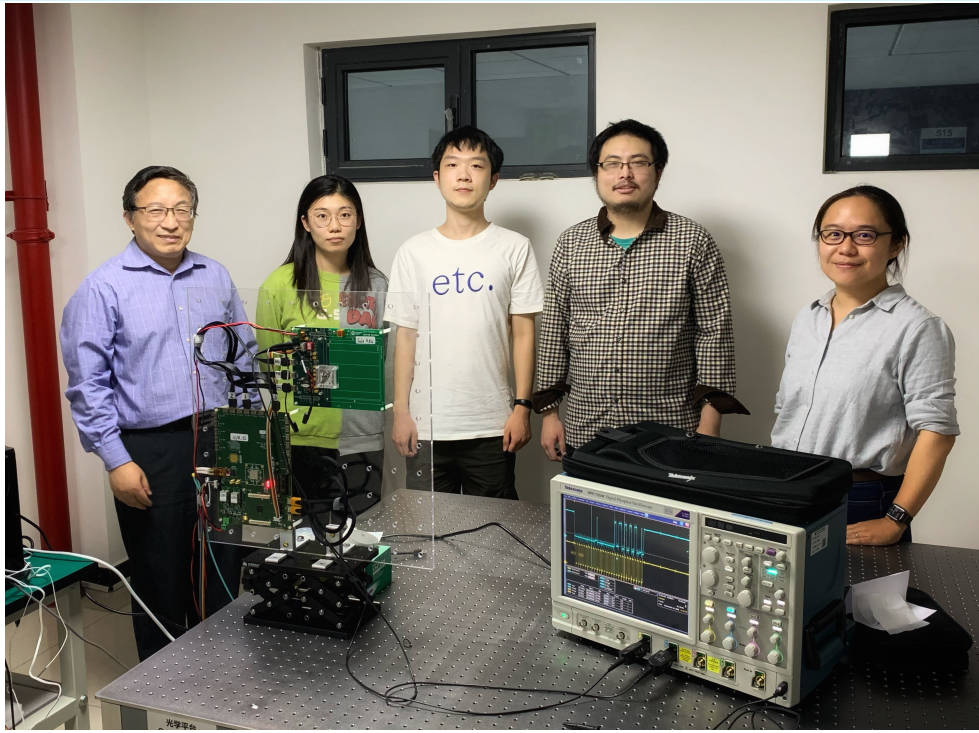


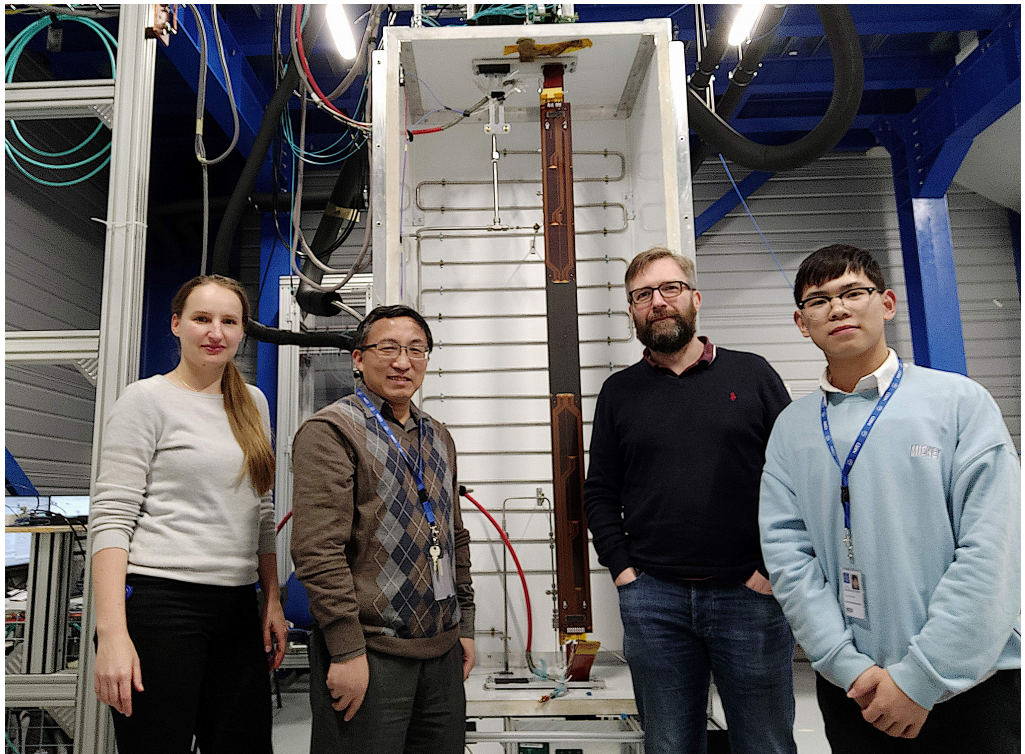


Chinese UT participation

IHEP CAS:

- 2 staff (Jianchun Wang, Yiming Li)
- 3 postdocs (Nathan Grieser, Yu Lu, Ina Carli)
- 2 visiting scientists (Mark Tobin, Petr Gorbounov in 2019)
- PhD and undergrad students (Quan Zou, Shuaiyi Liu, Yutong Li)





Other institutes:

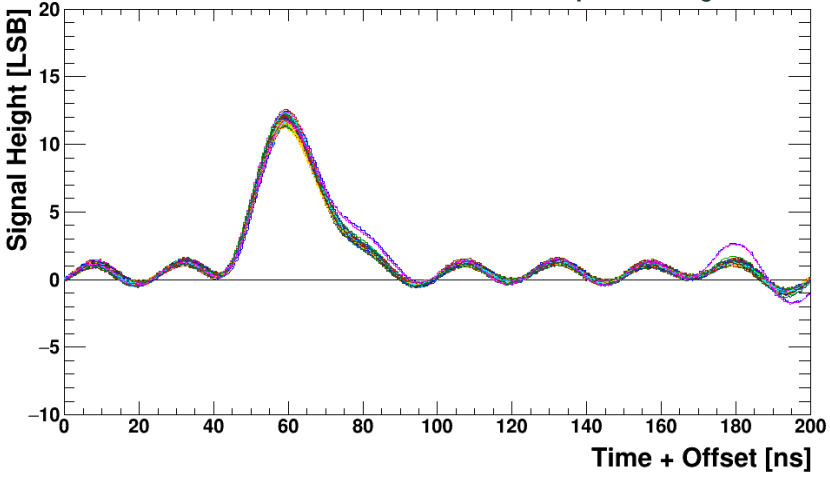
- Zan Ren (Tsinghua University)
- Feihao Zhang (IHEP + Hunan University)
- Bo Chen (Hunan University)

Chinese UT participation

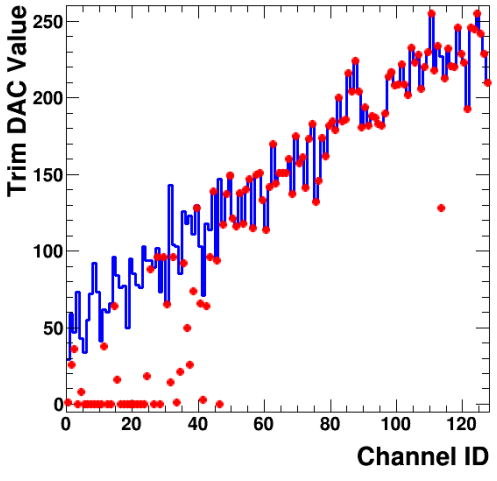
IHEP contributions:

- core members involved in UT efforts since early stage
- significant contributions to testbeam and irradiation campaigns: March '19 Fermilab, August '19 Mass. General Hospital, November '19 PSI, CIAE (China Institute of Atomic Energy) planned this November
- setup and running of system tests at CERN since June 2019
- development of readout and control systems
- infrastructure preparation (cabling, design and soldering of boards)
- talks at conferences (Mark Tobin LHCP 2020, Ina Carli ICHEP 2020)

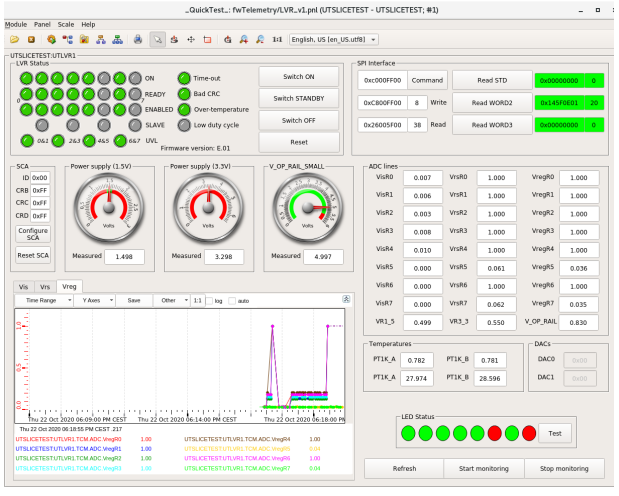
SALT test pulse injection



Trim register in testbeam



LV control panel



Current UT status

- all production sites impacted by lockdown, now restarted
- $\sim$ 60% modules built
- first 5 full staves ready to ship to CERN (out of 68)
- all near-detector electronics delivered and $\sim$ 50% tested
- aiming for installation underground before fall 2021

Thank you for your attention!

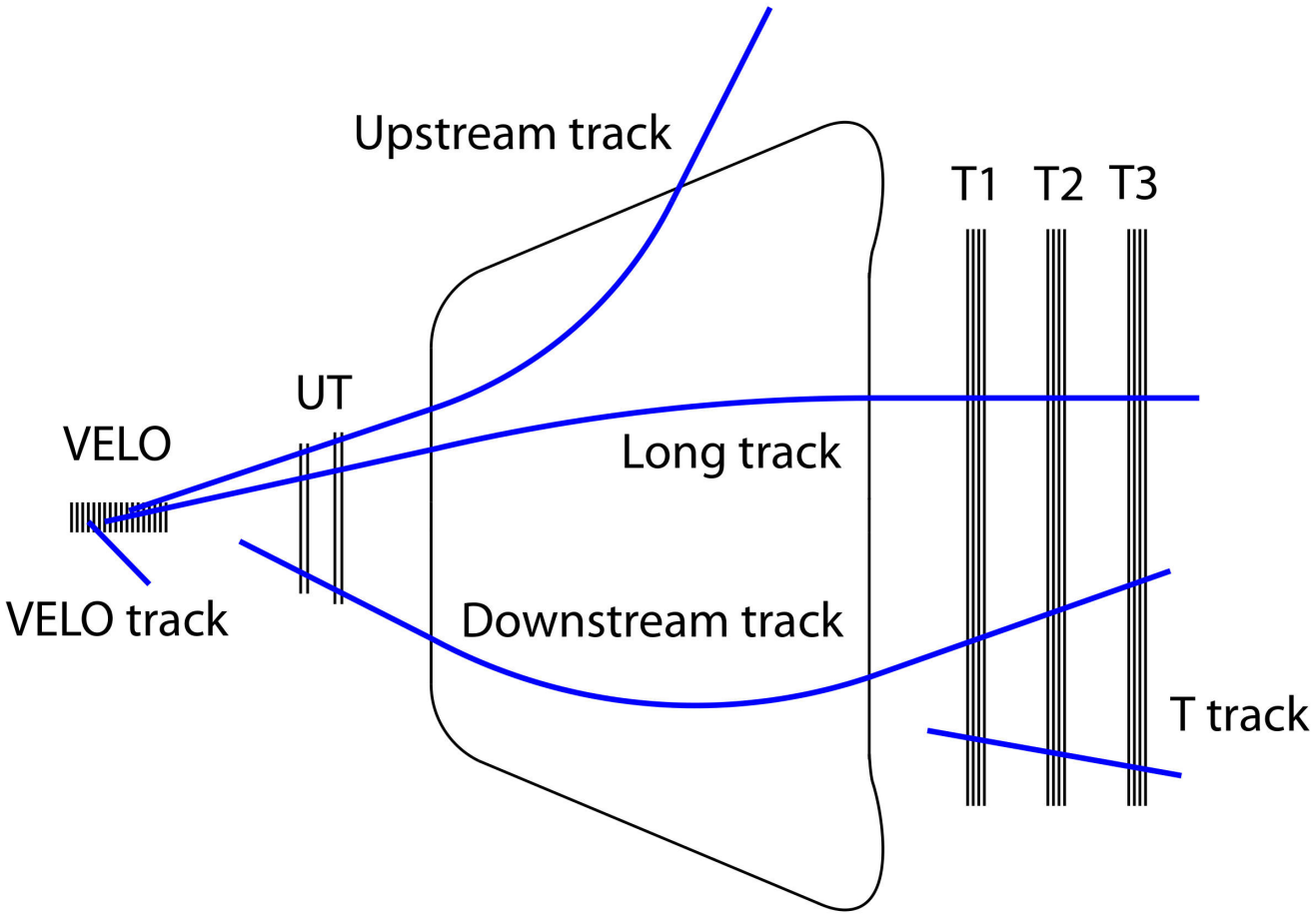
Questions?

Ina.Carli@cern.ch @Ina_Carli

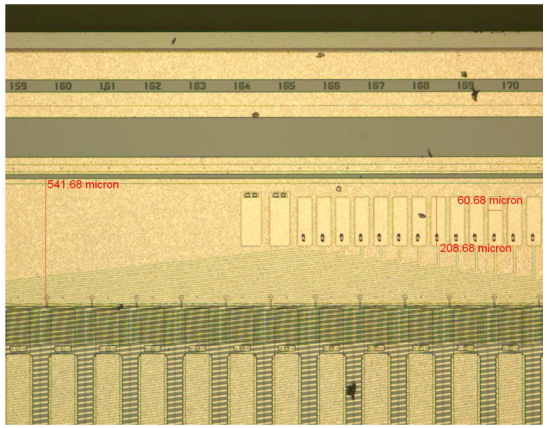
Backup slides

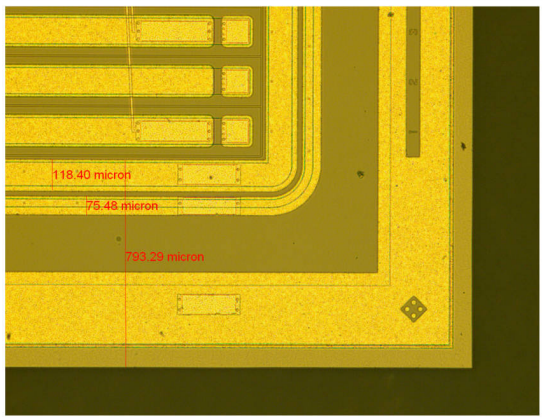
LHCb tracking detectors

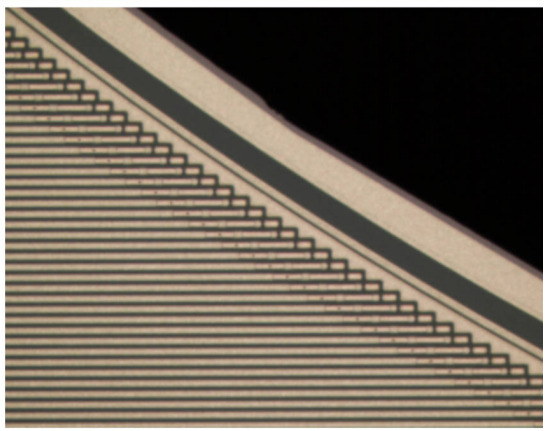
- Vertex Locator (VELO)
  - silicon pixel
  - precision tracking around IP
- Upstream Tracker (UT)
  - silicon strip
  - tracking before magnet
- SciFi
  - scintillating fibers
  - tracking after magnet



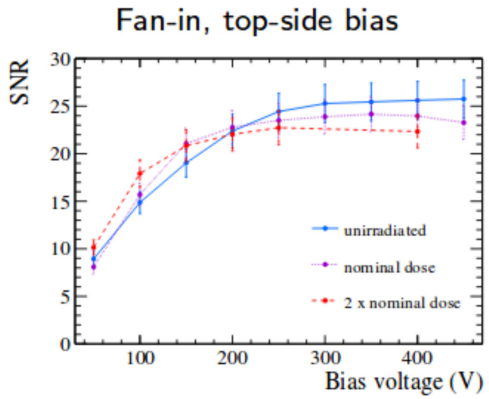
Sensor features

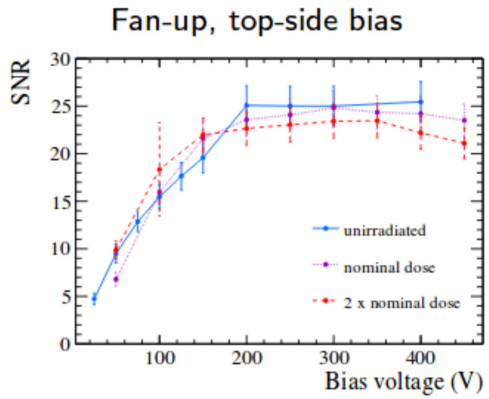


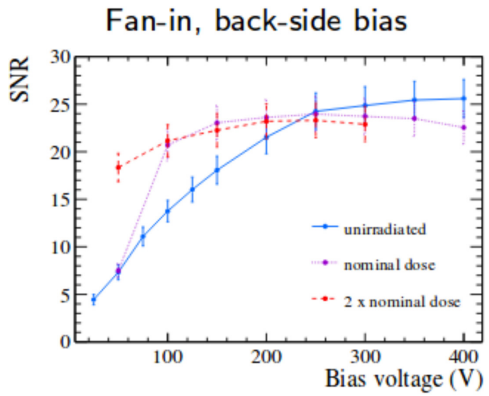


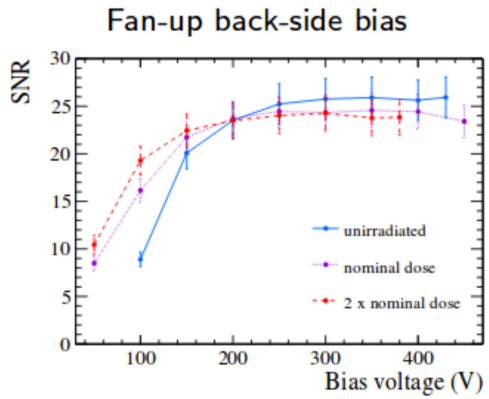


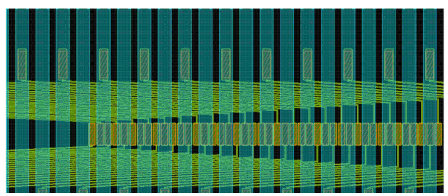
- A-type sensors: embedded pitch adapters (fan-up)
- top-side HV biasing
- cutout around beampipe → all working well

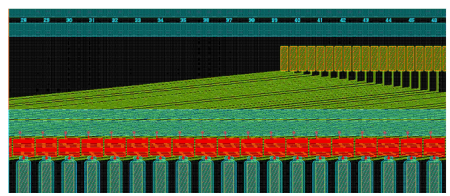






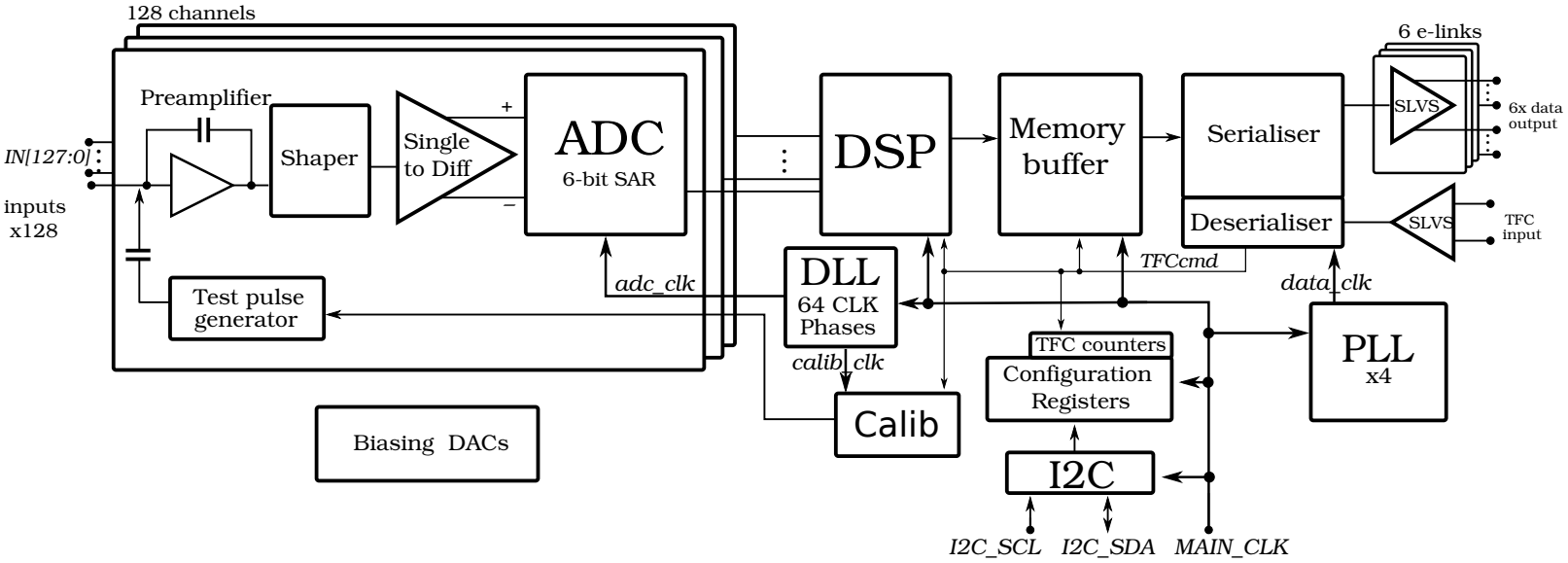






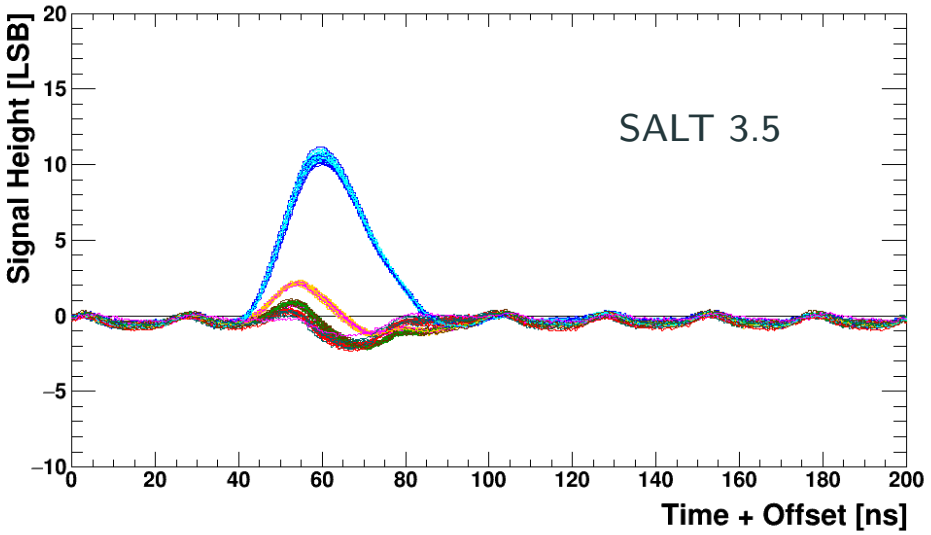
(testbeam results with mini sensors, 1.2 cm x 1.8 cm)

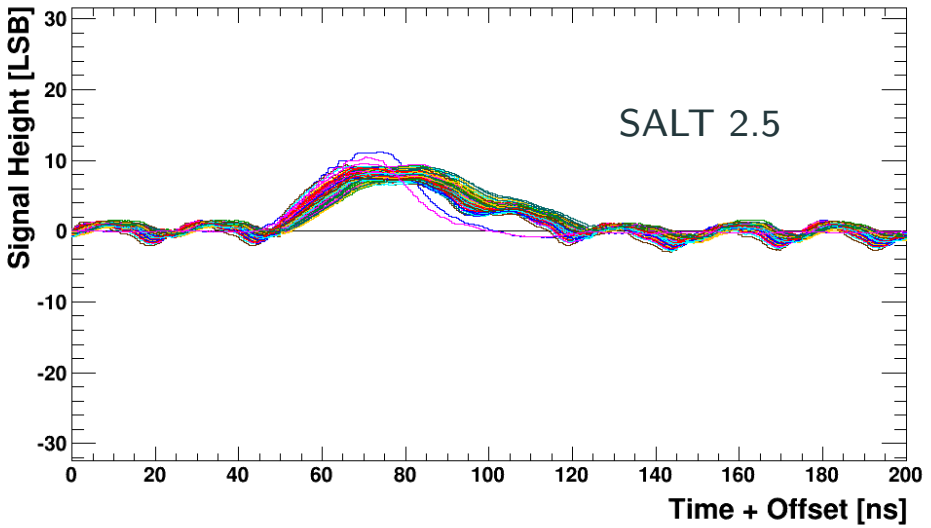
SALT block diagram



SALT pulse shape

- $T_{\text{peak}} \sim 25\,\text{ns}$
- short tail, only 5% after $2\times T_{\text{peak}}$
- crosstalk $< 5\%$
- all 128 channels plotted, test pulse injected into every 4th channel
- fixed large coupling observed in previous iterations

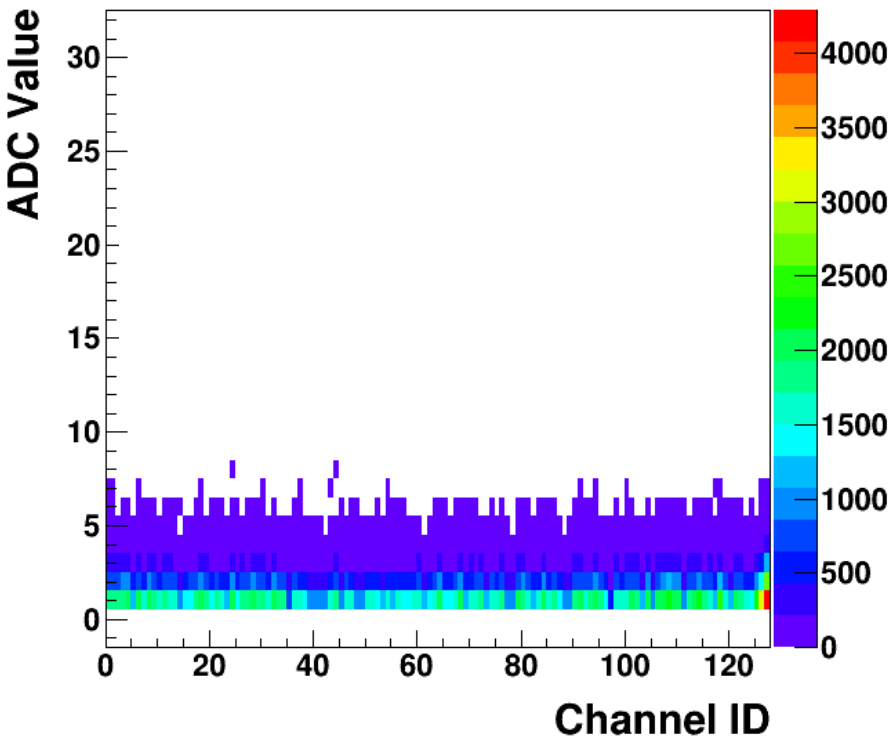




SALT zero suppression

- per-chip threshold to lower occupancy
- planned threshold value = 2–3 ADC

no ZS



ZS, th = 9 ADC