Digital Pixel Measurement of TaichuPix1

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Testing results of SPI readout

◆40MHz chip system CLK，10MHz SPI speed，with digital pulse injection.

→MASK_EN=“1”, spi_write('00110',‘00000000');MASK_EN=“0”,spi_write('00110','01111111');

MASK_EN= “1” to FE-I3
MASK_EN= “0” to ALPIDE

```
DPULSE opened
..........next read...........
valid=  1,ts=254,col= 95,row=  0,pat=  0
valid=  1,ts=254,col= 31,row=127,pat=  0
valid=  1,ts=254,col= 95,row=  1,pat=  0
valid=  1,ts=254,col= 31,row=126,pat=  0
valid=  1,ts=254,col= 95,row=  2,pat=  0
valid=  1,ts=254,col= 31,row=125,pat=  0
valid=  1,ts=254,col= 95,row=  3,pat=  0
valid=  1,ts=254,col= 31,row=124,pat=  0
valid=  1,ts=254,col= 95,row=  4,pat=  0
valid=  1,ts=254,col= 31,row=123,pat=  0
valid=  1,ts=254,col= 95,row=  5,pat=  0
valid=  1,ts=254,col= 31,row=122,pat=  0
valid=  1,ts=254,col= 95,row=  6,pat=  0
valid=  1,ts=254,col= 31,row=121,pat=  0
valid=  1,ts=254,col= 95,row=  7,pat=  0
valid=  1,ts=254,col= 31,row=120,pat=  0
valid=  1,ts=254,col= 95,row=  8,pat=  0
valid=  1,ts=254,col= 31,row=119,pat=  0
valid=  1,ts=254,col= 95,row=  9,pat=  0
valid=  1,ts=254,col= 31,row=118,pat=  0
valid=  1,ts=254,col= 95,row= 10,pat=  0
valid=  1,ts=254,col= 31,row=117,pat=  0
valid=  1,ts=254,col= 95,row= 11,pat=  0
valid=  1,ts=254,col= 31,row=116,pat=  0
valid=  1,ts=254,col= 95,row= 12,pat=  0
valid=  1,ts=254,col= 31,row=115,pat=  0
```

MASK_EN= “0” to all

```
DPULSE opened
..........next read...........
valid=  1,ts= 19,col= 95,row=  0,pat=  0
valid=  1,ts= 19,col= 63,row=  0,pat=  0
valid=  1,ts= 19,col= 95,row=  1,pat=  0
valid=  1,ts= 19,col= 63,row=  1,pat=  0
valid=  1,ts= 19,col= 95,row=  2,pat=  0
valid=  1,ts= 19,col= 63,row=  2,pat=  0
valid=  1,ts= 19,col= 95,row=  3,pat=  0
valid=  1,ts= 19,col= 63,row=  3,pat=  0
valid=  1,ts= 19,col= 95,row=  4,pat=  0
valid=  1,ts= 19,col= 63,row=  4,pat=  0
valid=  1,ts= 19,col= 95,row=  5,pat=  0
valid=  1,ts= 19,col= 63,row=  5,pat=  0
valid=  1,ts= 19,col= 95,row=  6,pat=  0
valid=  1,ts= 19,col= 63,row=  6,pat=  0
valid=  1,ts= 19,col= 95,row=  7,pat=  0
valid=  1,ts= 19,col= 63,row=  7,pat=  0
valid=  1,ts= 19,col= 95,row=  8,pat=  0
valid=  1,ts= 19,col= 63,row=  8,pat=  0
valid=  1,ts= 19,col= 95,row=  9,pat=  0
valid=  1,ts= 19,col= 63,row=  9,pat=  0
valid=  1,ts= 19,col= 95,row= 10,pat=  0
valid=  1,ts= 19,col= 63,row= 10,pat=  0
valid=  1,ts= 19,col= 95,row= 11,pat=  0
valid=  1,ts= 19,col= 63,row= 11,pat=  0
valid=  1,ts= 19,col= 95,row= 12,pat=  0
valid=  1,ts= 19,col= 63,row= 12,pat=  0
```

MASK_EN= “1” to all

```
DPULSE opened
..........next read...........
valid=  1,ts= 45,col= 31,row=127,pat=  0
valid=  1,ts= 45,col= 95,row=  0,pat=  0
valid=  1,ts= 45,col= 31,row=126,pat=  0
valid=  1,ts= 45,col= 95,row=  0,pat=  0
valid=  1,ts= 45,col= 31,row=125,pat=  0
valid=  1,ts= 45,col= 95,row=  0,pat=  0
valid=  1,ts= 45,col= 31,row=124,pat=  0
valid=  1,ts= 45,col= 95,row=  0,pat=  0
valid=  1,ts= 45,col= 31,row=123,pat=  0
valid=  1,ts= 45,col= 95,row=  0,pat=  0
valid=  1,ts= 45,col= 31,row=122,pat=  0
valid=  1,ts= 45,col= 95,row=  0,pat=  0
valid=  1,ts= 45,col= 31,row=121,pat=  0
valid=  1,ts= 45,col= 95,row=  0,pat=  0
valid=  1,ts= 45,col= 31,row=120,pat=  0
valid=  1,ts= 45,col= 95,row=  0,pat=  0
valid=  1,ts= 45,col= 31,row=119,pat=  0
valid=  1,ts= 45,col= 95,row=  0,pat=  0
valid=  1,ts= 45,col= 31,row=118,pat=  0
valid=  1,ts= 45,col= 95,row=  0,pat=  0
valid=  1,ts= 45,col= 31,row=117,pat=  0
valid=  1,ts= 45,col= 95,row=  0,pat=  0
valid=  1,ts= 45,col= 31,row=116,pat=  0
valid=  1,ts= 45,col= 95,row=  0,pat=  0
valid=  1,ts= 45,col= 31,row=115,pat=  0
valid=  1,ts= 45,col= 95,row=  0,pat=  0
valid=  1,ts= 45,col= 31,row=114,pat=  0
```

MASK_EN= “1” to ALPIDE
MASK_EN= “0” to FE-I3

```
DPULSE opened
..........next read...........
valid=  1,ts=148,col= 95,row=  0,pat=  0
valid=  1,ts=148,col= 63,row=  0,pat=  0
valid=  1,ts=148,col= 95,row=  0,pat=  0
valid=  1,ts=148,col= 63,row=  0,pat=  0
valid=  1,ts=148,col= 95,row=  0,pat=  0
valid=  1,ts=148,col= 63,row=  0,pat=  0
valid=  1,ts=148,col= 95,row=  0,pat=  0
valid=  1,ts=148,col= 63,row=  0,pat=  0
valid=  1,ts=148,col= 95,row=  0,pat=  0
valid=  1,ts=148,col= 63,row=  0,pat=  0
valid=  1,ts=148,col= 95,row=  0,pat=  0
valid=  1,ts=148,col= 63,row=  0,pat=  0
valid=  1,ts=148,col= 95,row=  0,pat=  0
valid=  1,ts=148,col= 63,row=  0,pat=  0
valid=  1,ts=148,col= 95,row=  0,pat=  0
valid=  1,ts=148,col= 63,row=  0,pat=  0
valid=  1,ts=148,col= 95,row=  0,pat=  0
valid=  1,ts=148,col= 63,row=  0,pat=  0
valid=  1,ts=148,col= 95,row=  0,pat=  0
valid=  1,ts=148,col= 63,row=  0,pat=  0
valid=  1,ts=148,col= 95,row=  0,pat=  0
valid=  1,ts=148,col= 63,row=  0,pat=  0
valid=  1,ts=148,col= 95,row=  0,pat=  0
valid=  1,ts=148,col= 63,row=  0,pat=  0
valid=  1,ts=148,col= 95,row=  0,pat=  0
valid=  1,ts=148,col= 63,row=  0,pat=  0
valid=  1,ts=148,col= 95,row=  0,pat=  0
valid=  1,ts=148,col= 63,row=  0,pat=  0
```

COL=31→FE-I3 like part   COL=63/95→ALPIDE like Part

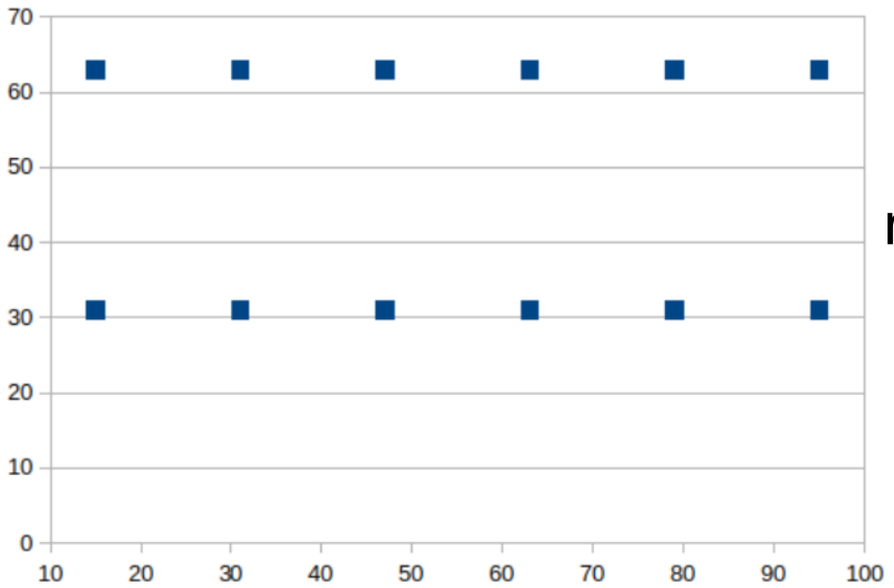
PLL & Serializer preliminary test results

- Setup the LVDS output to 160MHz bit rates, which PLL_TMOD =0 for trigger mode, DSEL =0 for periphery readout and NSEL =1 for 160M bps.
- Set the chip to default mode with TEST=00;
- Setup periphery with Triggerless mode, which TRIGN=1,CPRN=1,SMOD=0.
- Inject the digital pulse to all of the pixels.
- Create a 8K depth FIFO from ZC706 to be a buffer for data storage.

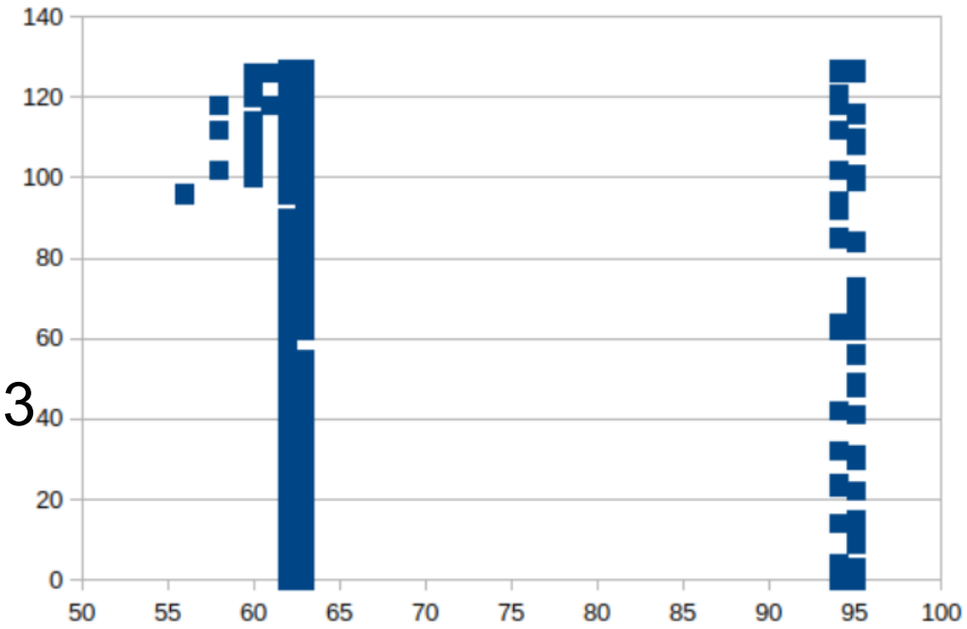
- Remove the repeat data with the SoC.
  - → There are around 300 – 500 valid data inside of the 8000 data. (It should be more or this is the limit of periphery?)
  - → I repeat the experiment as the SPI method, but with more data.
  - → Without the frame header, I could only analyze the data by hand, may be I should improve my firmware to make the data readable.

PLL & Serializer preliminary test results

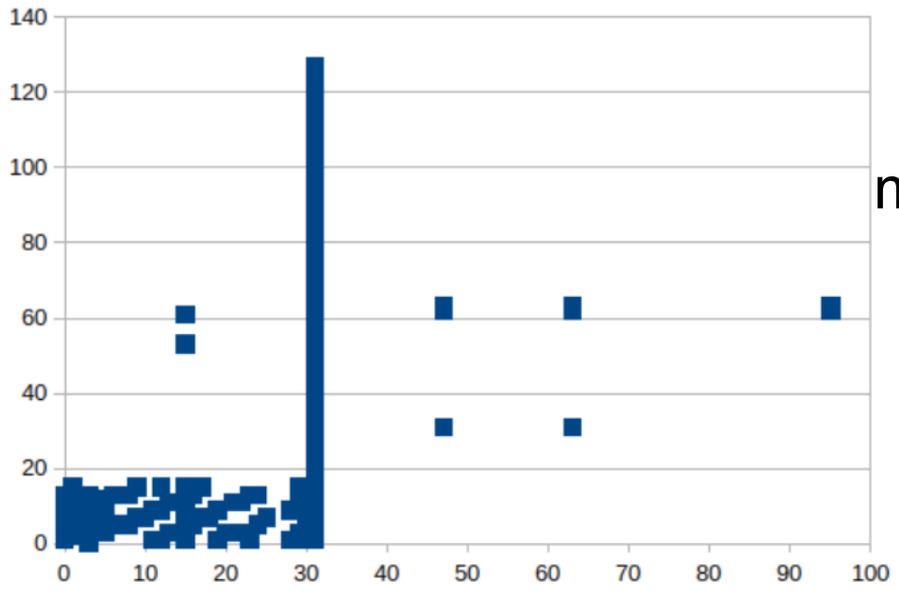
Here is the preliminary results with digital pulse injection in 4 different masking mode.



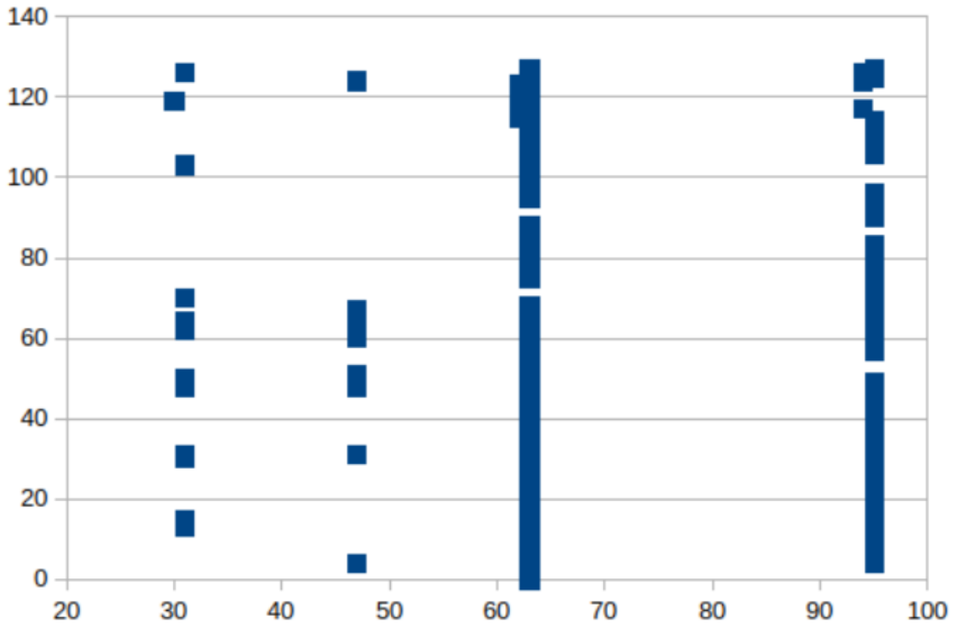
masking all



masking FE-I3



masking ALPIDE



no masking

Summary and outlook

- I received a lot of data which double column was exceeding to 95, such as Col126 or Col127? But I removed the first bit to force it below 95.
- When do the masking to all the pixels, there still exist some data from row31 and row63. It will need a filter to remove the invalid data among them.

→Then we are supposed to do more test on the pixel masking ensure there is no data loss of my system.

→ After that, we will test the chip together with analog front end.

→ Then start to test TaichuPix2.

Thanks for your attention.