Digital Pixel Measurement of TaichuPix1

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PLL & Serializer preliminary test results

- Setup the LVDS output to 160MHz bit rates, which PLL_TMOD =0 for trigger mode, DSEL =0 for periphery readout and NSEL =1 for 160M bps.
- Set the chip to default mode with TEST=00;
- Setup periphery with Triggerless mode, which TRIGN=1,CPRN=1,SMOD=0.
- Inject the digital pulse to all of the pixels.
- Set the VRESET PIN open and shading the chip，totally power supply of TCX1 is 1.953V/0.789A.
- Shielding all the pixels.
- Create a 8K depth FIFO from ZC706 to be a buffer for data storage.
- Remove the repeat data with the SoC.

```
total_num=3
8fc000be valid=  1,ts= 31,col=  0,row= 11,pat= 14
ac8fc000  valid=  1,ts= 89,col= 63,row=  0,pat=  0
ac97c000 valid=  1,ts= 89,col= 95,row=  0,pat=  0

total_num=4
00bc8fc0  valid=  0,ts=  1,col=114,row=124,pat=  0
3c900000 valid=  0,ts=121,col= 64,row=  0,pat=  0
e697c000 valid=  1,ts=205,col= 95,row=  0,pat=  0
e68fc000  valid=  1,ts=205,col= 63,row=  0,pat=  0
```

```
total_num=10
b297c000 valid=  1,ts=101,col= 95,row=  0,pat=  0
00b29140 valid=  0,ts=  1,col= 74,row= 20,pat=  0
00b29100 valid=  0,ts=  1,col= 74,row= 16,pat=  0
00b290c0 valid=  0,ts=  1,col= 74,row= 12,pat=  0
00b29080 valid=  0,ts=  1,col= 74,row=  8,pat=  0
00b29040 valid=  0,ts=  1,col= 74,row=  4,pat=  0
00b29000 valid=  0,ts=  1,col= 74,row=  0,pat=  0
00329000 valid=  0,ts=  0,col= 74,row=  0,pat=  0
009c97c0 valid=  0,ts=  1,col=114,row=124,pat=  0
009c8fc0 valid=  0,ts=  1,col=114,row=124,pat=  0
```

From the left data, we can see clearly that C95/R0 & C63/R0 can not be shielding and the number of data is different in each run.

Preliminary test results(Chip1)

Following the configuration above, we do the further test of the matrix. Here is the results of firing one row of TCX1.

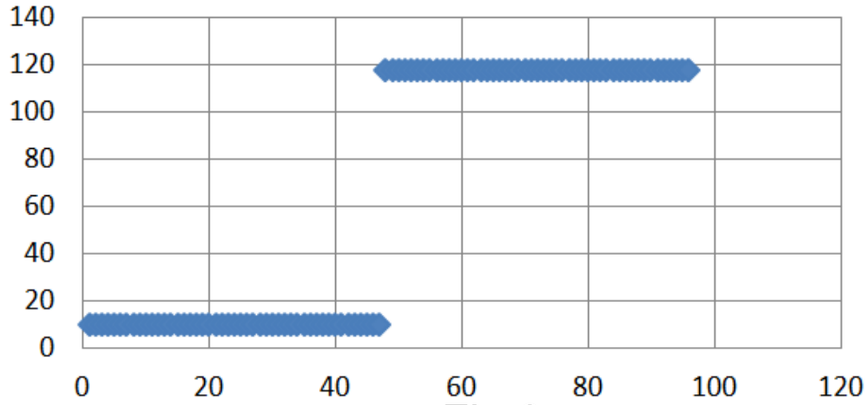

Fig 0

- Fig0 is the plot what we expect.
- Fig1 and Fig2 are the Chip1 at 1.95V/0.79A
- Fig3 and Fig4 are the Chip1 at 1.99V/0.81A
- X axis is the Double_Column index, and Y is the ROW.

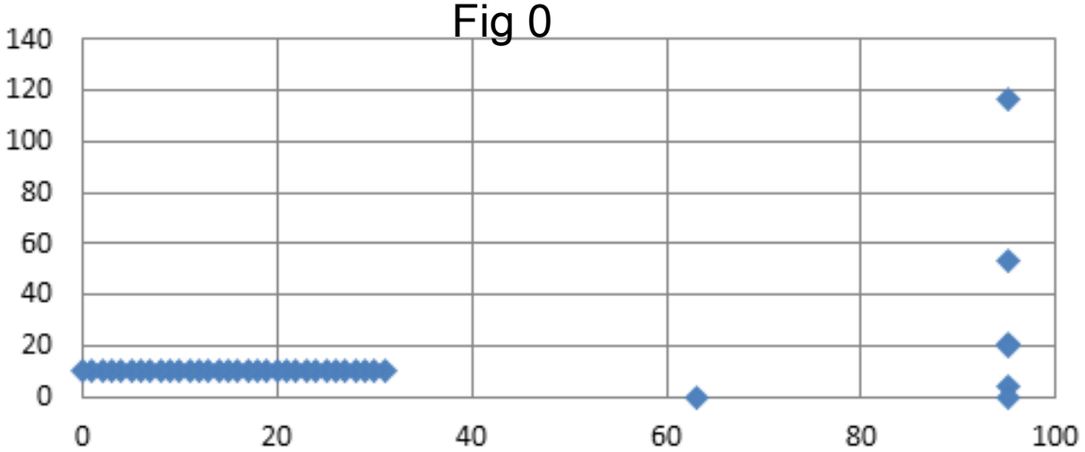

Fig 1

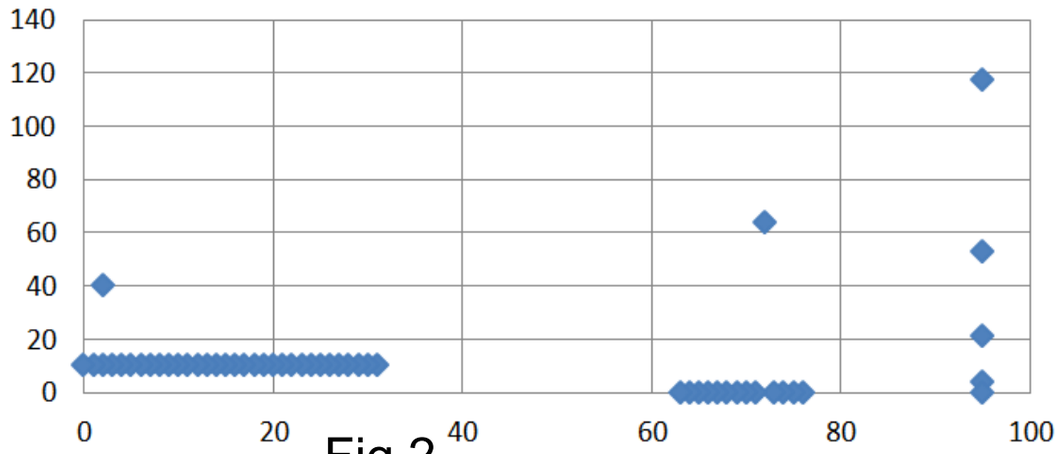

Fig 2

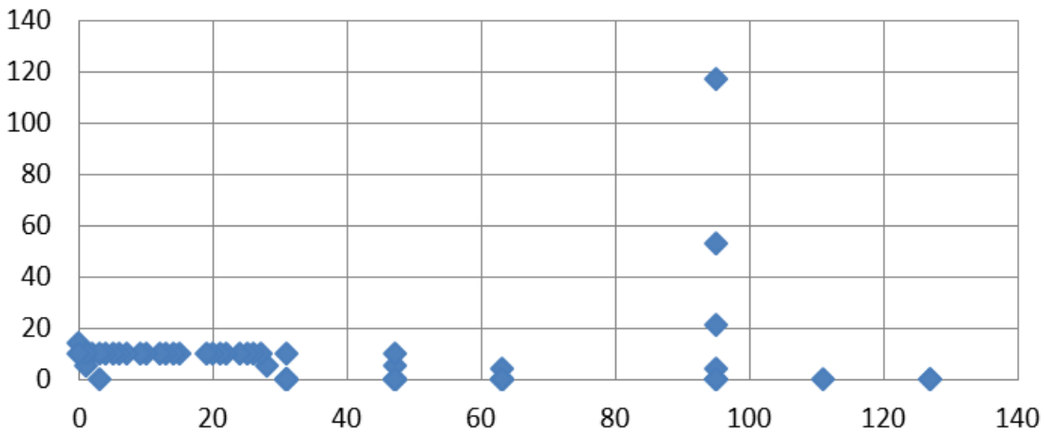

Fig 3

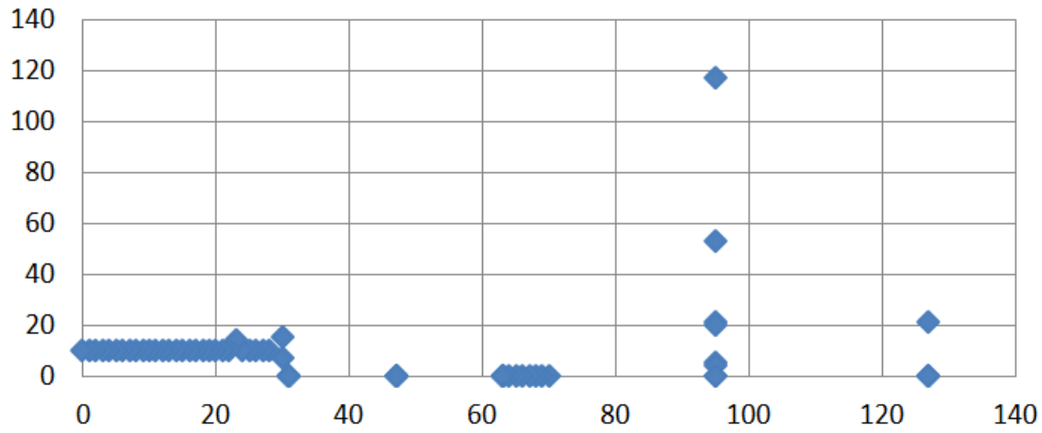

Fig 4

Preliminary test results(Chip2)

Here is the results of firing one row of TCX1.

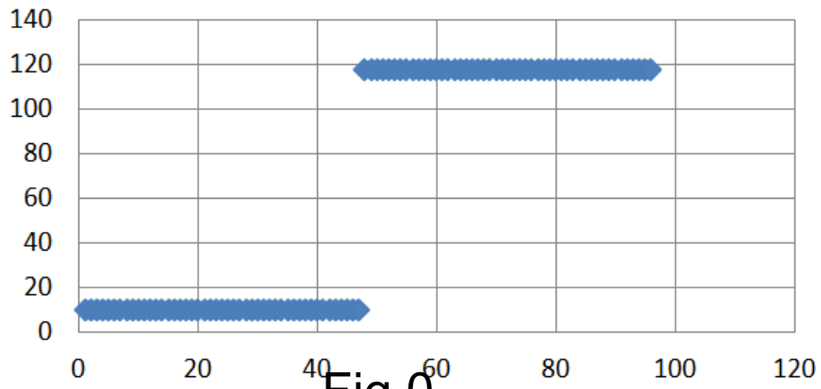

Fig 0

- Fig0 is the plot what we expect.
- Fig1 and Fig2 are the Chip2 at 1.95V/0.78A
- Fig3 and Fig4 are the Chip2 at 1.99V/0.80A

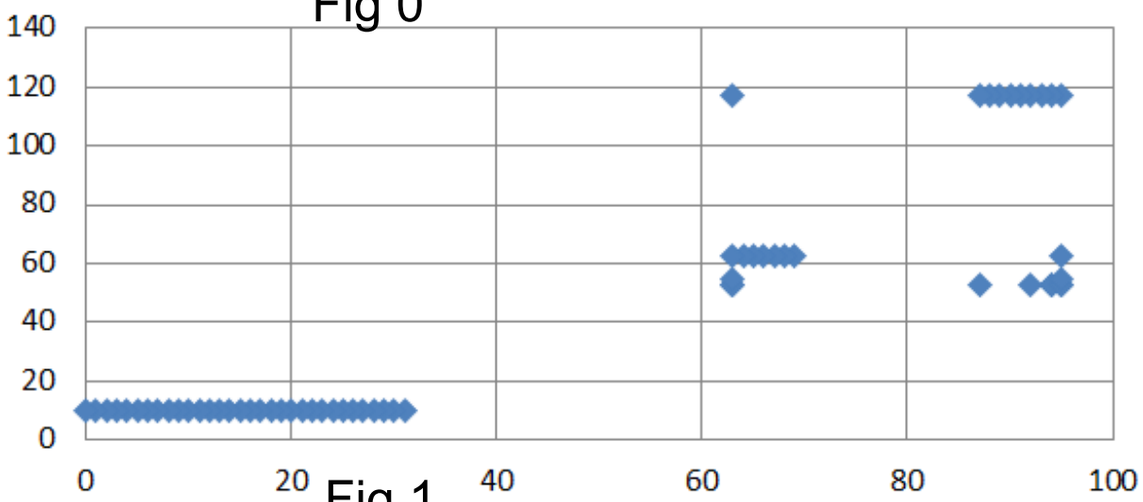

Fig 1

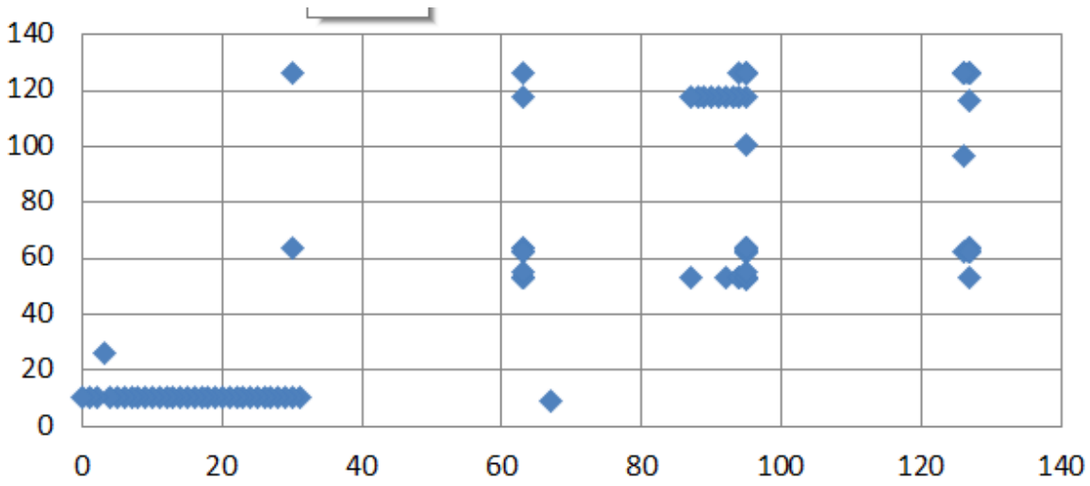

Fig 2

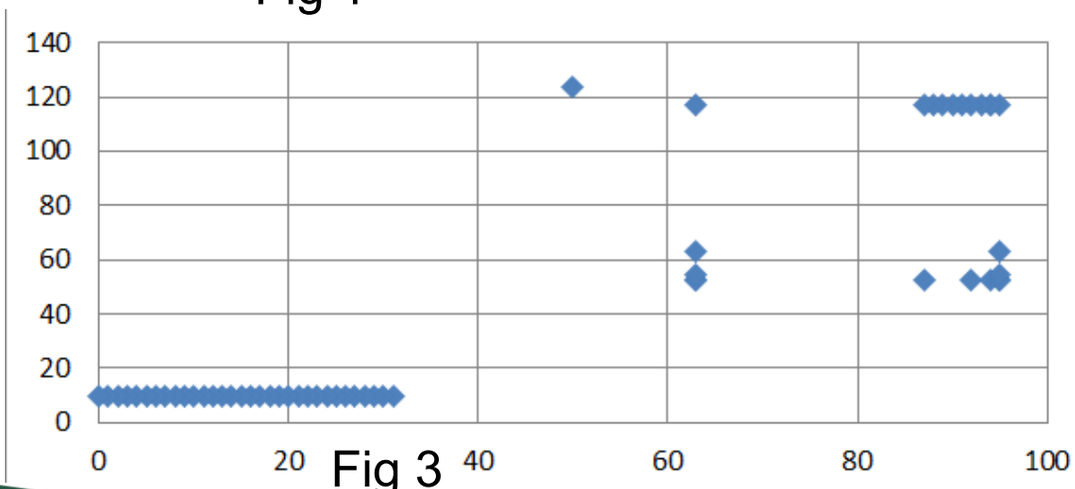

Fig 3

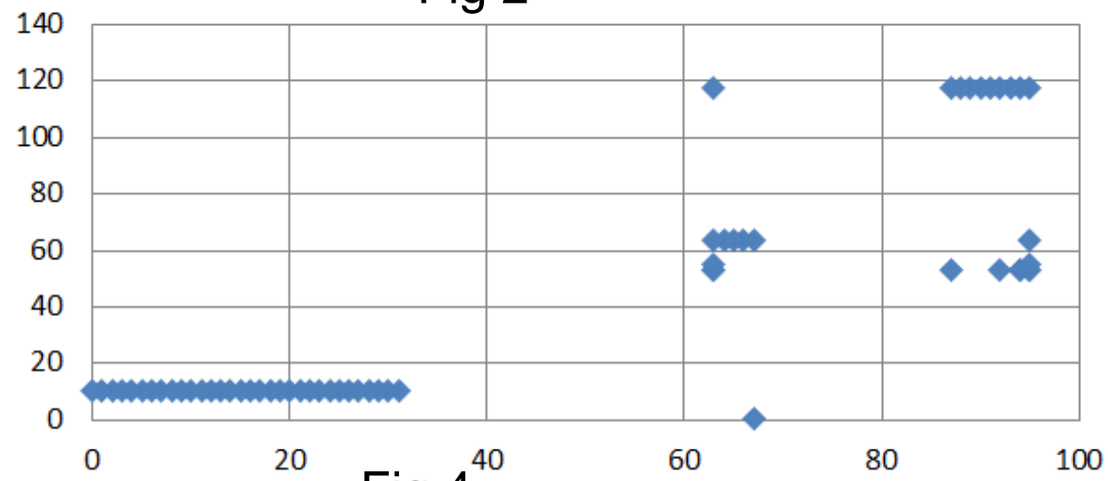

Fig 4

Preliminary test results(Chip1)

Here is the results of firing one row of TCX1-Chip1, and set the digital pulse to constant high.

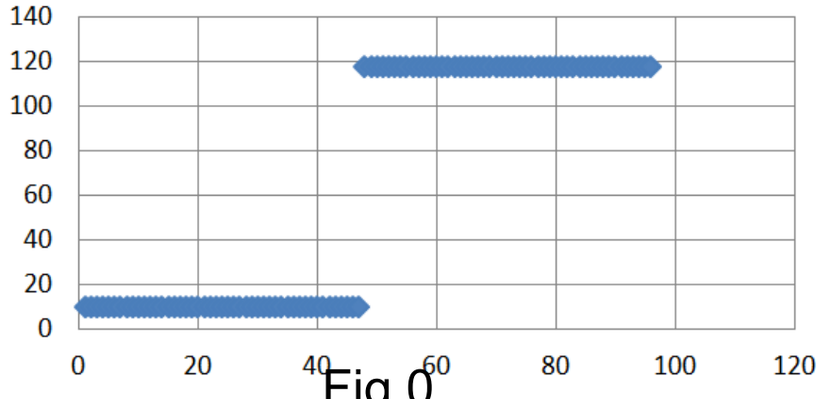

Fig 0

- Fig0 is the plot what we expect.
- Fig1 and Fig2 are the Chip1 at 1.95V/0.79A
- It is clear that the COL0-COL47 could read out the Row10 correctly
- COL48-COL95 read out the ROW0(This should be ROW117, Only COL95&63 is the row 117)

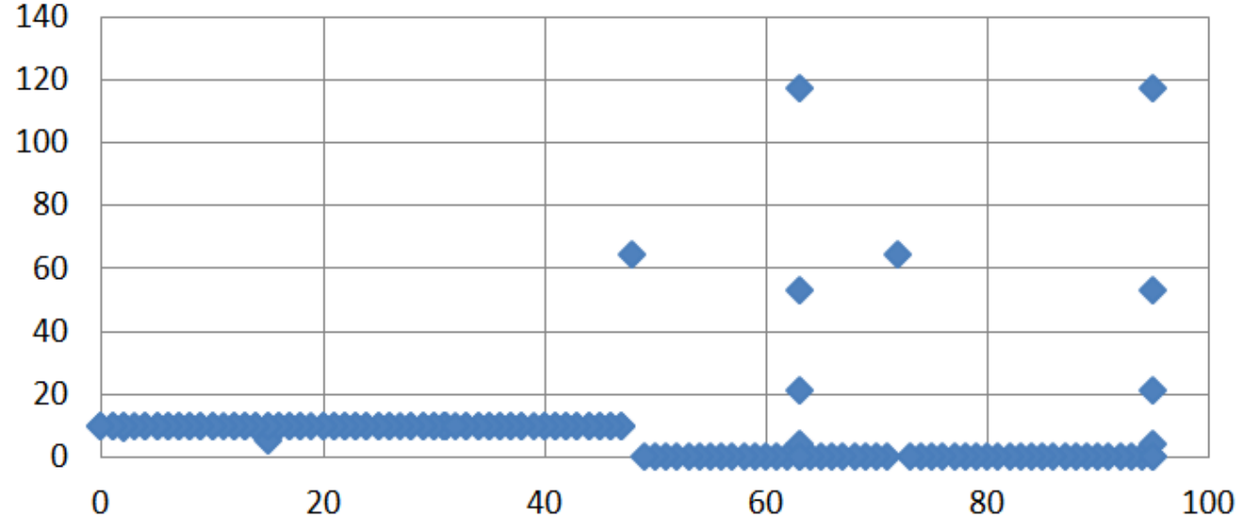

Fig 1

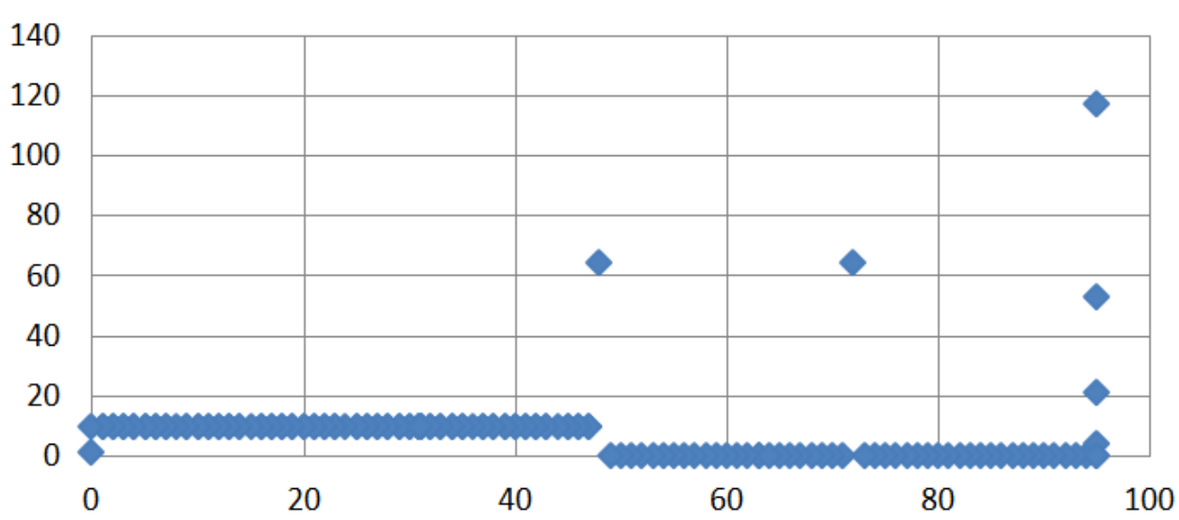

Fig 2

Preliminary test results

Fig1~4 are the results of firing Col16 of Chip2.

Fig5~6 are the plot of firing Col0 of Chip1

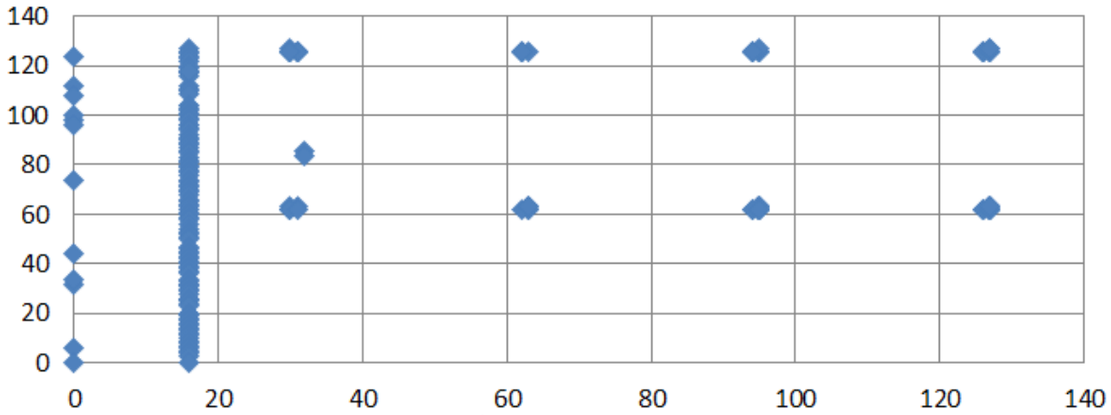

Fig 1

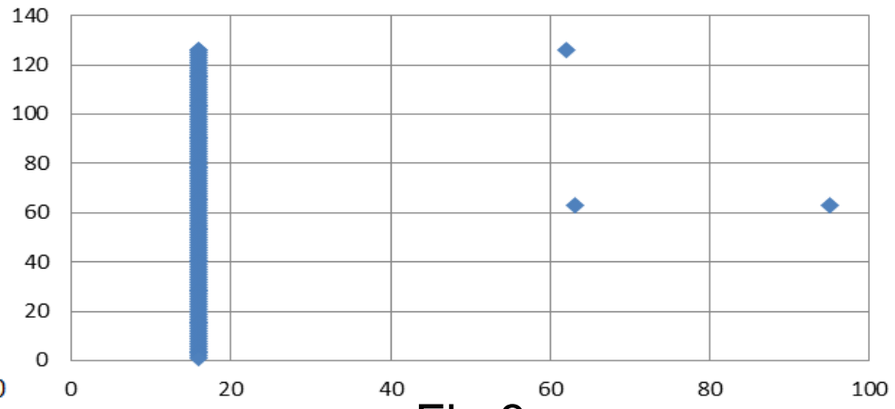

Fig 3

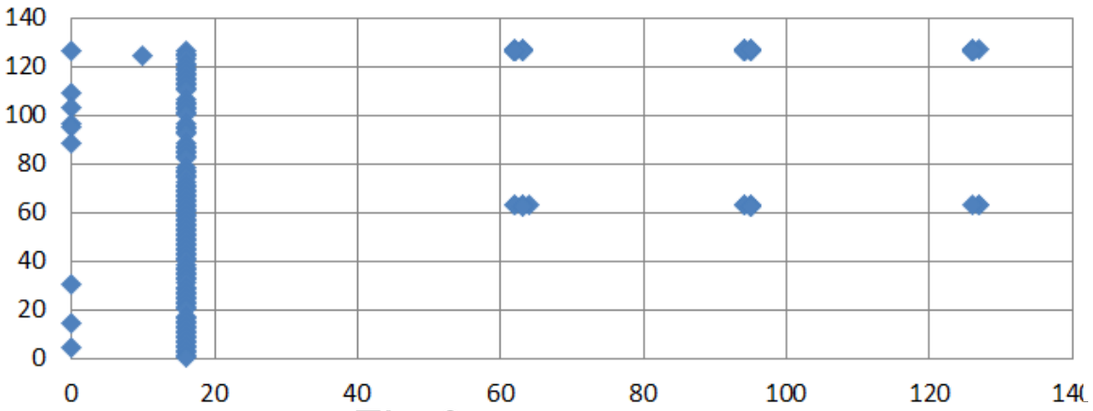

Fig 2

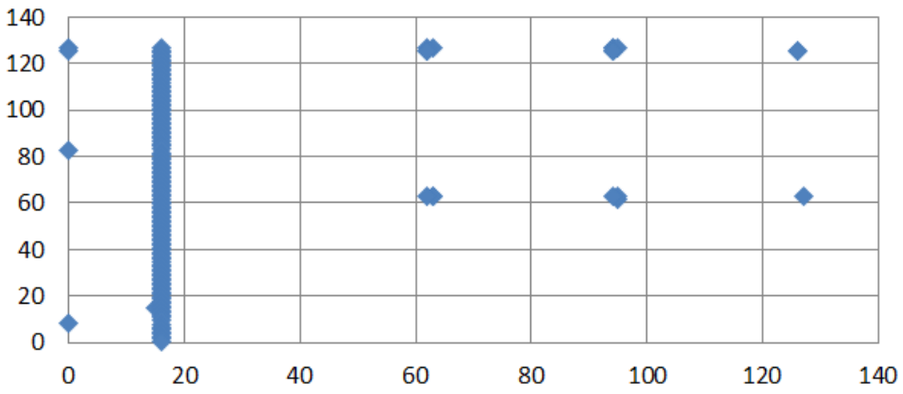

Fig 4

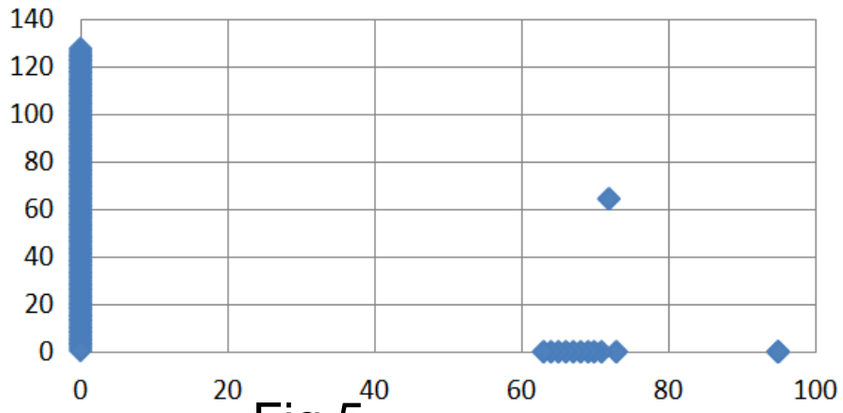

Fig 5

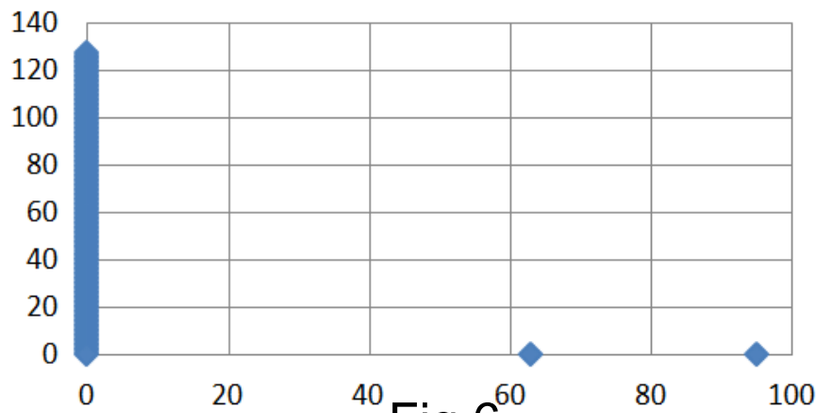

Fig 6

- Fig1 and Fig2 are the Chip2 at 1.95V/0.78A
- Fig3 and Fig4 are the Chip2 at 1.99V/0.80A
- Fig5 and Fig6 are the Chip1 at 1.95V/0.79A

Preliminary test results(ALPIDE like)

Fig1 is the plot of firing column of COL87 and COL86.
Fig2 is the plot of firing column of COL95 and COL63.

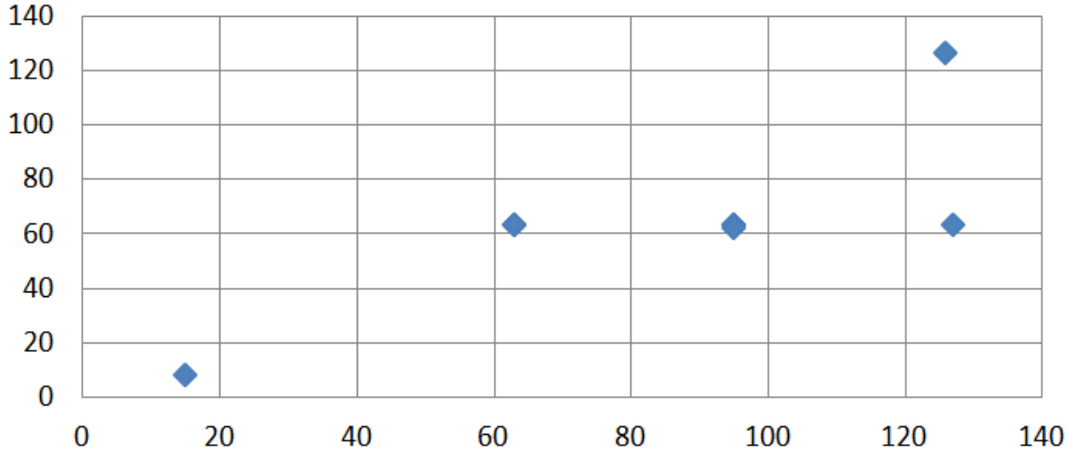

Fig 1

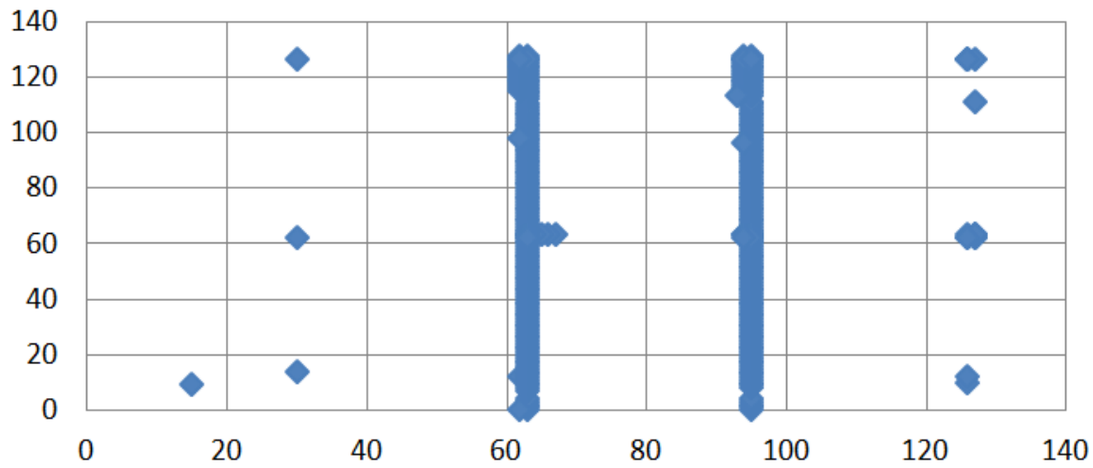

Fig 2

- With the same configuration of FE-I3 like part, the ALPIDE can not reach the same performance as FE-I3 part.
- Only the top priority column 95&63 could be read out in time, the other columns will be thrown away.
- The Fig1 only read out the random data.

Preliminary test results(FE-I3 like)

This is the data of firing 8 pixels of COL30/31/32/33 ROW98/97

```
total_num=14
8fc000b5valid=  1,ts= 31,col=  0,row= 11,pat=  5
b5914000valid=  1,ts=107,col= 69,row=  0,pat=  0
b5910000valid=  1,ts=107,col= 68,row=  0,pat=  0
b590c000valid=  1,ts=107,col= 67,row=  0,pat=  0
b5908000valid=  1,ts=107,col= 66,row=  0,pat=  0
b5904000valid=  1,ts=107,col= 65,row=  0,pat=  0
b5900000valid=  1,ts=107,col= 64,row=  0,pat=  0
35900000valid=  0,ts=107,col= 64,row=  0,pat=  0
c997c000valid=  1,ts=147,col= 95,row=  0,pat=  0
c987c620valid=  1,ts=147,col= 31,row= 98,pat=  0
c987c610valid=  1,ts=147,col= 31,row= 97,pat=  0
c9878620valid=  1,ts=147,col= 30,row= 98,pat=  0
c9878610valid=  1,ts=147,col= 30,row= 97,pat=  0
c98fc000valid=  1,ts=147,col= 63,row=  0,pat=  0
```

```
total_num=8
c0008597valid=  1,ts=128,col=  2,row= 89,pat=  7
05900000valid=  0,ts= 11,col= 64,row=  0,pat=  0
ed97c000valid=  1,ts=219,col= 95,row=  0,pat=  0
ed87c620valid=  1,ts=219,col= 31,row= 98,pat=  0
ed87c610valid=  1,ts=219,col= 31,row= 97,pat=  0
ed878620valid=  1,ts=219,col= 30,row= 98,pat=  0
ed878610valid=  1,ts=219,col= 30,row= 97,pat=  0
ed8fc000valid=  1,ts=219,col= 63,row=  0,pat=  0
```

This is the data of firing 16 pixels of COL9/8/7/6 ROW7/6/5/4

```
total_num=20
00d717c0valid=  0,ts=  1,col= 92,row=124,pat=  0
57100000valid=  0,ts=174,col= 64,row=  0,pat=  0
9d17c000valid=  1,ts= 58,col= 95,row=  0,pat=  0
9d024070valid=  1,ts= 58,col=  9,row=  7,pat=  0
9d024060valid=  1,ts= 58,col=  9,row=  6,pat=  0
9d024050valid=  1,ts= 58,col=  9,row=  5,pat=  0
9d024040valid=  1,ts= 58,col=  9,row=  4,pat=  0
9d020070valid=  1,ts= 58,col=  8,row=  7,pat=  0
9d020060valid=  1,ts= 58,col=  8,row=  6,pat=  0
9d020050valid=  1,ts= 58,col=  8,row=  5,pat=  0
9d020040valid=  1,ts= 58,col=  8,row=  4,pat=  0
9d01c070valid=  1,ts= 58,col=  7,row=  7,pat=  0
9d01c060valid=  1,ts= 58,col=  7,row=  6,pat=  0
9d01c050valid=  1,ts= 58,col=  7,row=  5,pat=  0
9d01c040valid=  1,ts= 58,col=  7,row=  4,pat=  0
9d018070valid=  1,ts= 58,col=  6,row=  7,pat=  0
9d018060valid=  1,ts= 58,col=  6,row=  6,pat=  0
9d018050valid=  1,ts= 58,col=  6,row=  5,pat=  0
9d018040valid=  1,ts= 58,col=  6,row=  4,pat=  0
9d0fc000valid=  1,ts= 58,col= 63,row=  0,pat=  0
```

The priority of whole matrix is divided to 3 parallel parts: Col95-Col64 Col63-Col32 Col31-Col0

Preliminary test results(Analog Front End)

Fig1 is the plot of shielding all the digital pulse and setting VRESET at 1.6V.
Fig2 is the same condition with the VRESET PIN open

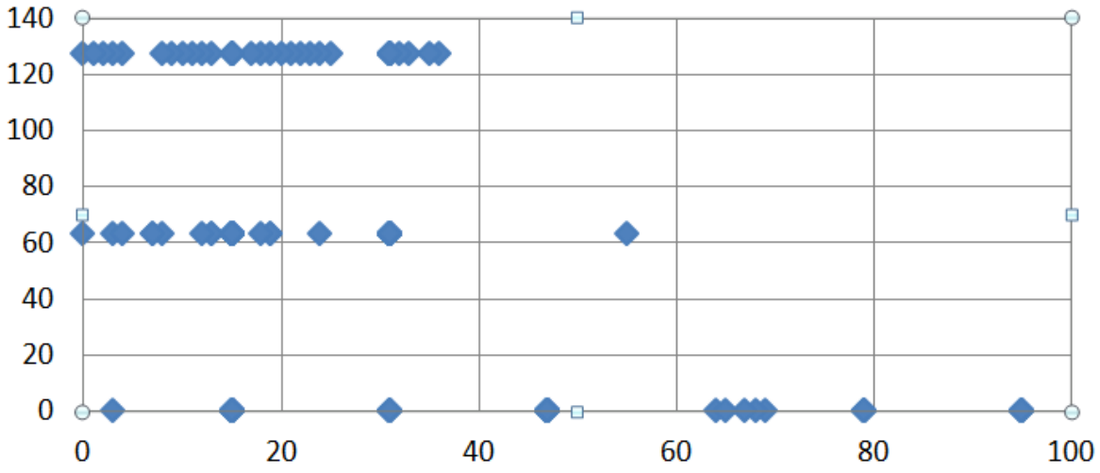

Fig 1

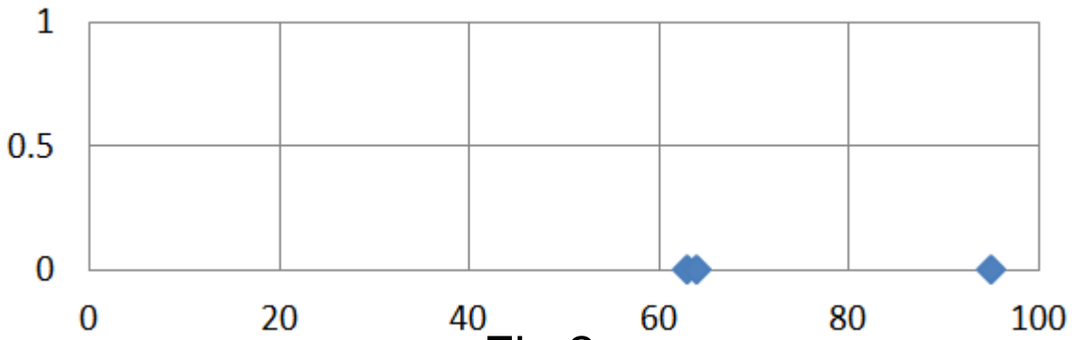

Fig 2

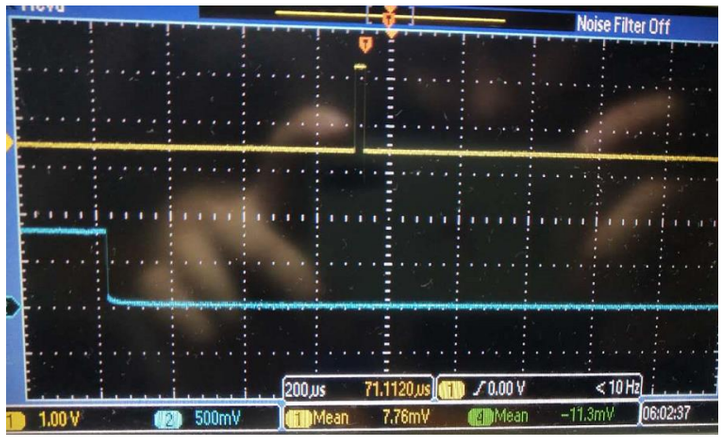

Fig 3

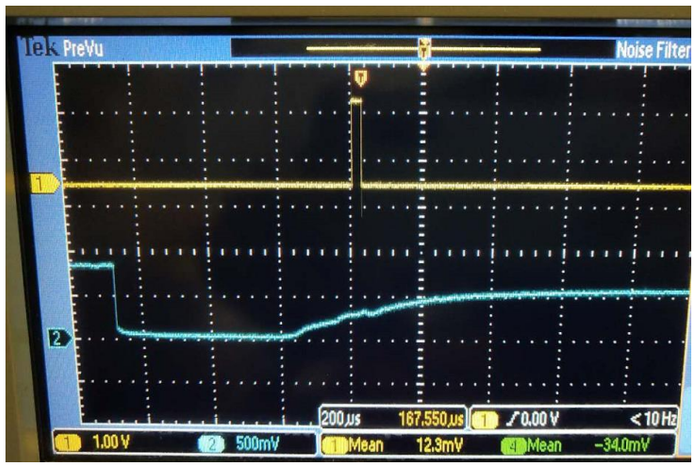

Fig 4

- The blue curve of Fig3&4 is the OUTA_Probe and the yellow one is APULSE
- Fig3 shows the plot after internal DACs configuration, fig4 is the other DAC parameter.
- The voltage level of OUTA will going to low(from 813mV to7mV),and changes the status of FE-I3 part input.

Summary and outlook

- At this moment, the FE-I3 like part is working fine within the range of COL31 to COL0;
- The response of COL63 to COL32 is more complicated due to the ALPIDE like part is not working so well.
- ALPIDE like part didn't perform so well except the COL95 and COL63.
- Analog front end needs to adjust to the right bias point.

→Then we will solve the problem of Apulse first.

→Test the fully chip together with analog front end.

Thanks for your attention.