TaichuPix1 Measurement

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Preliminary test results(Analog Front End)

Here are schematic of Analog front end with the design parameters and the waveform result from Ying Zhang.

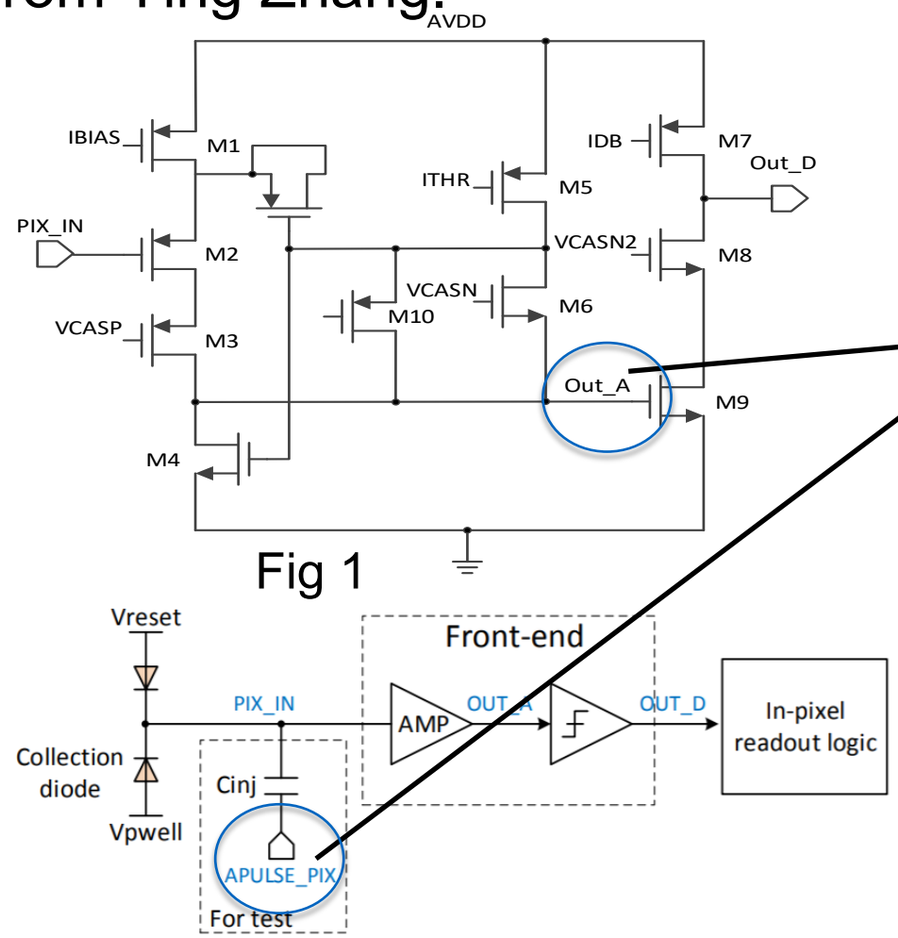


Fig 1

Fig 2 Block diagram of a pixel.

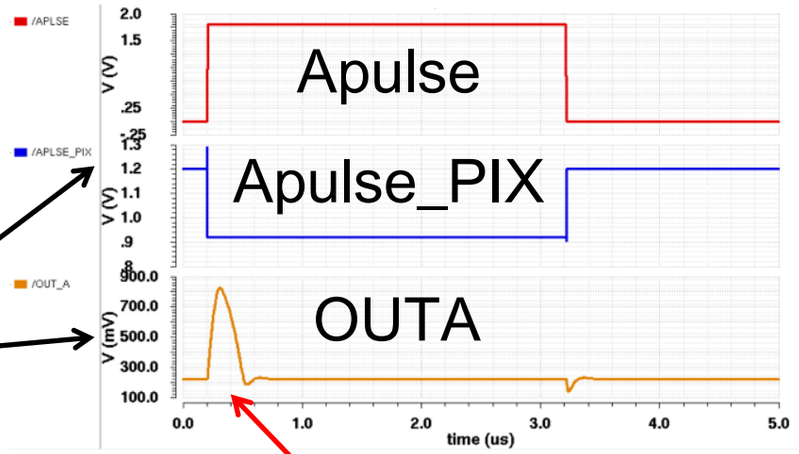


Fig 3

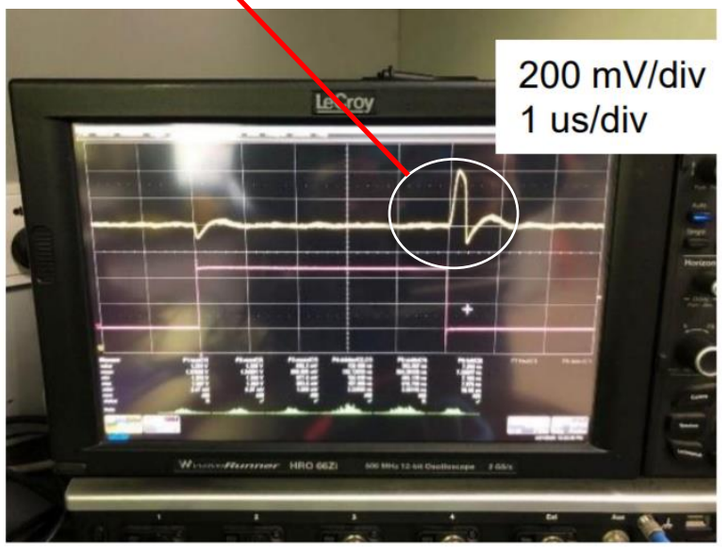


Fig 4

There will be a 400mV pulse generated at the rising edge of the Apulse.

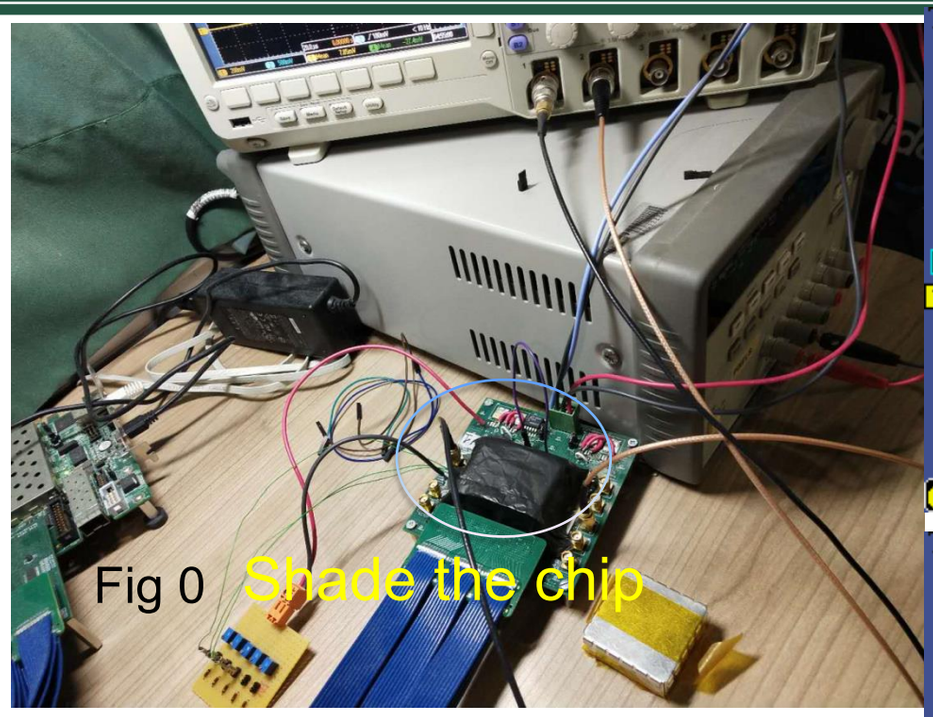
OUTA should be response at the rising edge

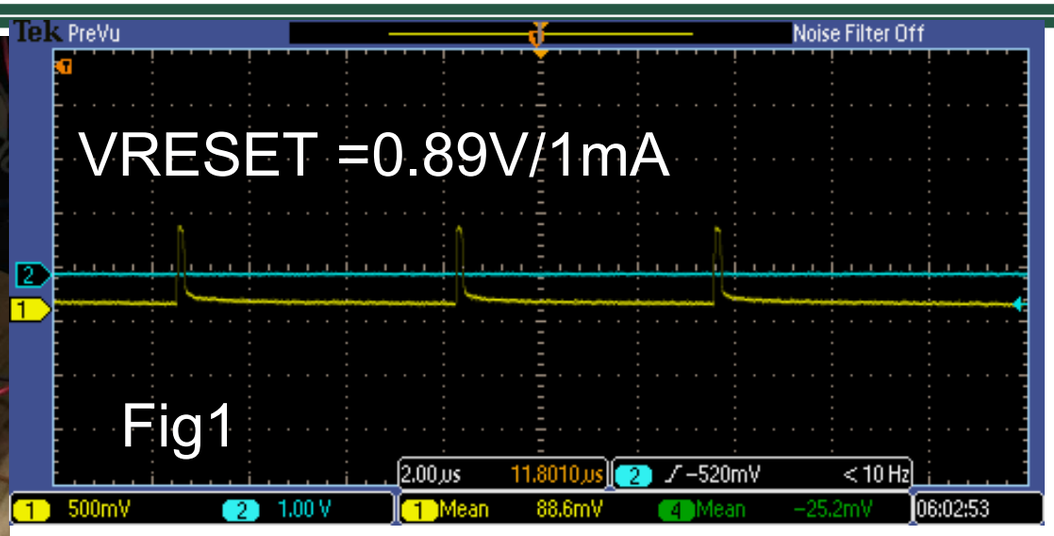
The DC bias of OUTA is around 800mV

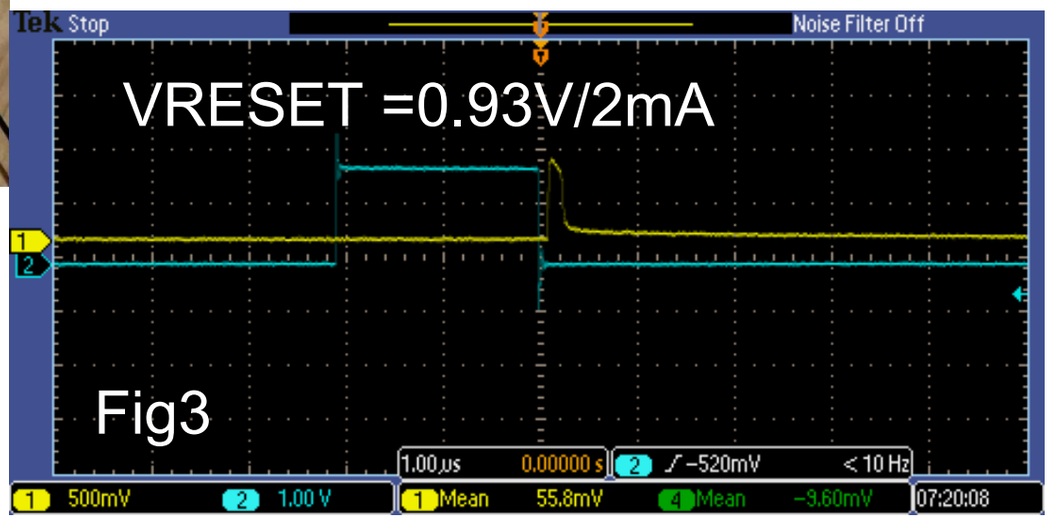
Table 1

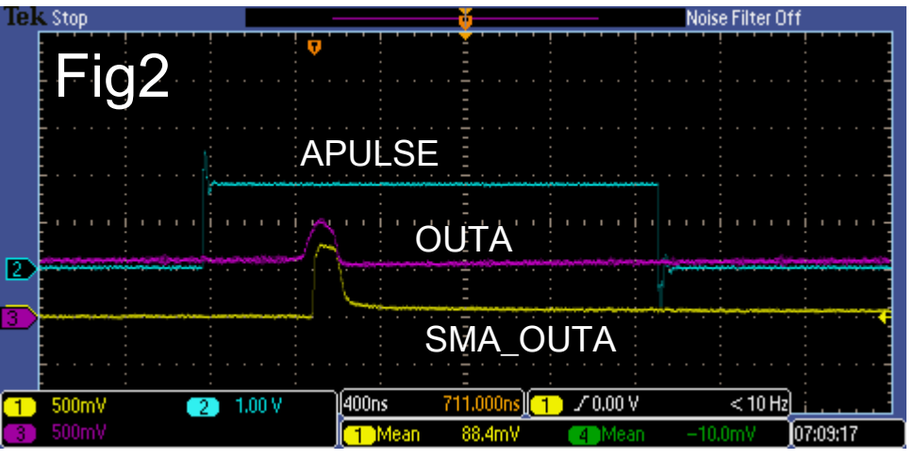
Bias	IBIAS	ITHR	IDB	VCLIP	VCASP	VCASN	VCASN2	VRESET
Design value	440 nA	4.5 nA	1 μA	0/0.2 V	0.6 V	0.55 V	0.5 V	1.4 V
Chip1 Config. value	450nA	1.16nA	1uA	0.068V	0.6V	0.073V ?	0.5V	0.93V

Preliminary test results(Analog Front End)









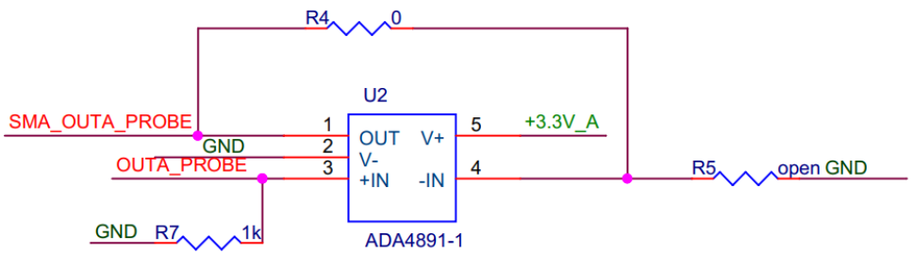
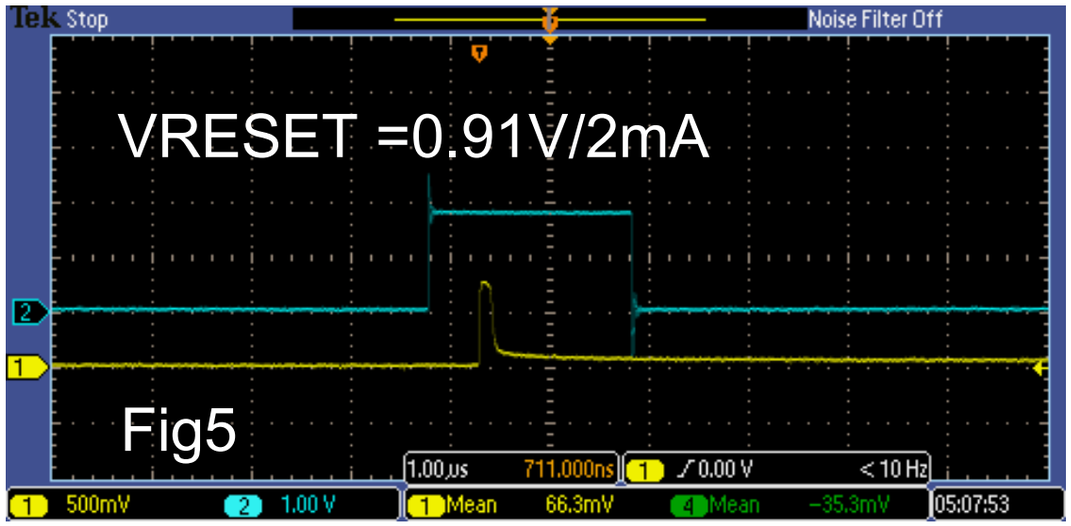


Fig 4 External OUTA buffer



I forgot enabling the DAC bias for VCASN but I got these signals?

Power Supply: 1.85V/0.7A.

Sometimes OUTA will be response at the falling edge and sometimes at the rising edge

The DC level of OUTA is around 630 mV and to SMA_OUTA is 0.

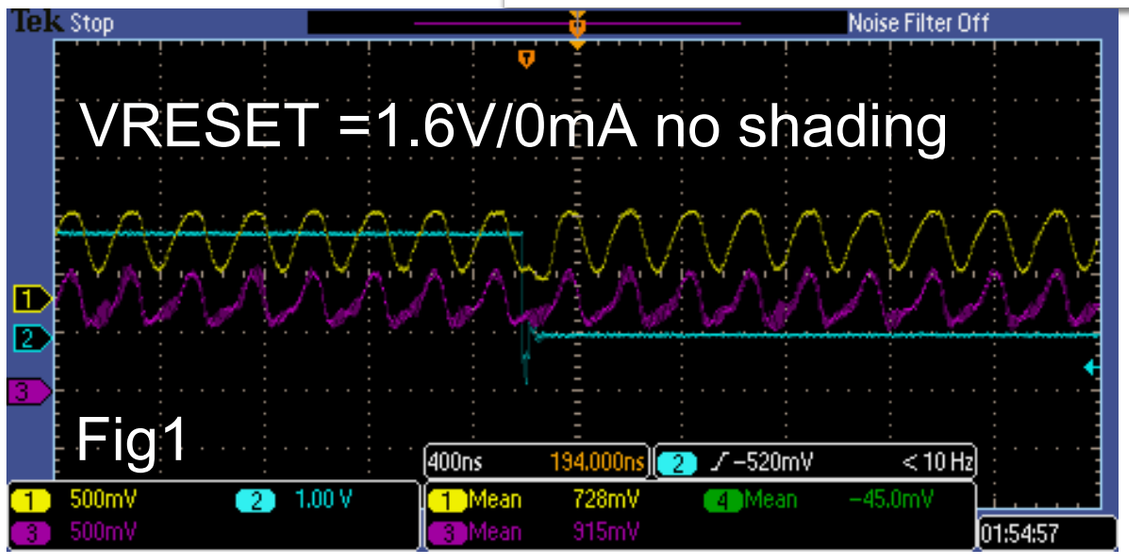
It seems there exists a short circuit at the PIN of VRESET, so Chip1 can not working well.

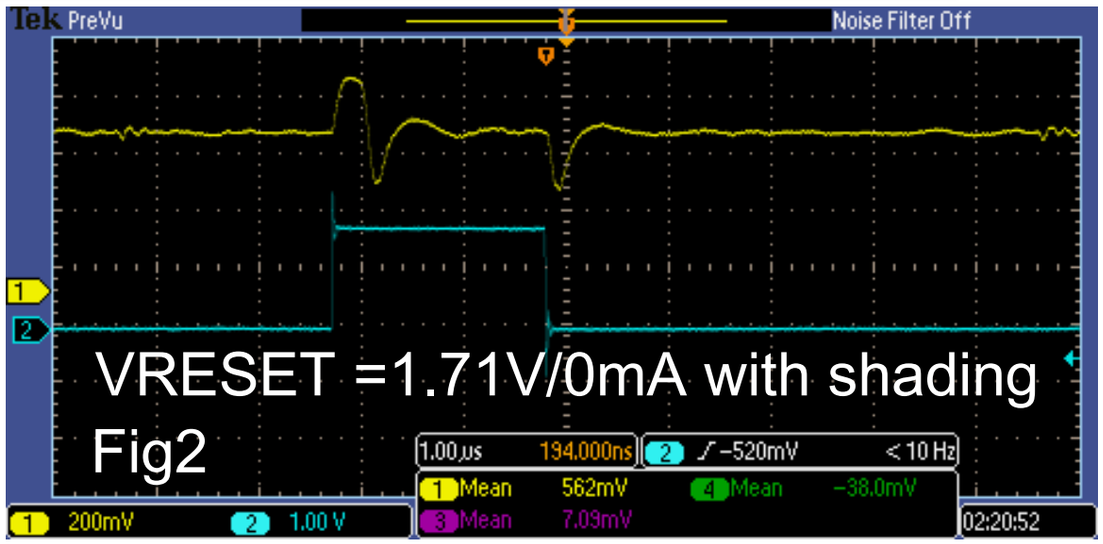
Preliminary test results(Analog Front End)

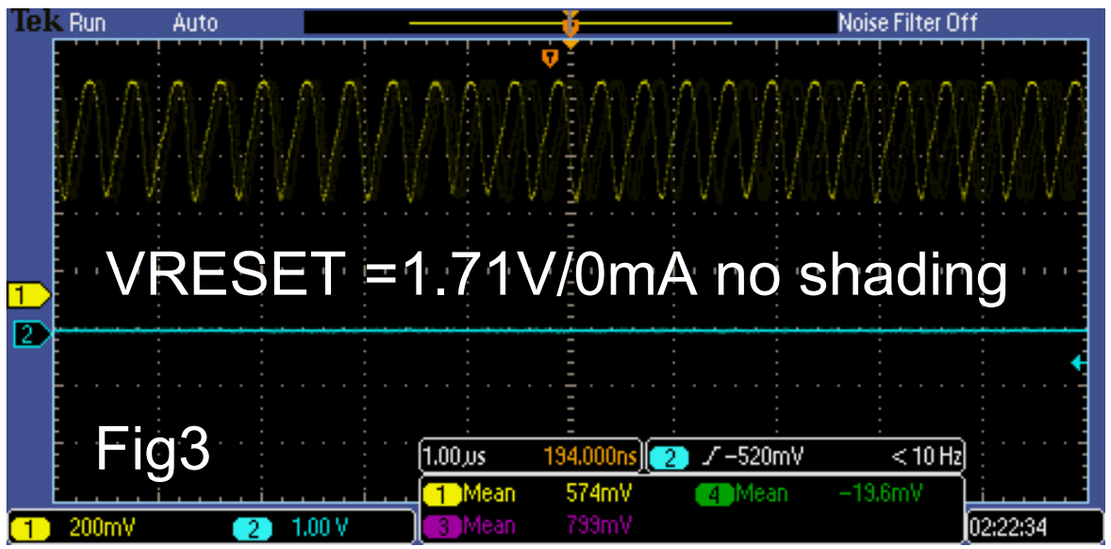
Table 1

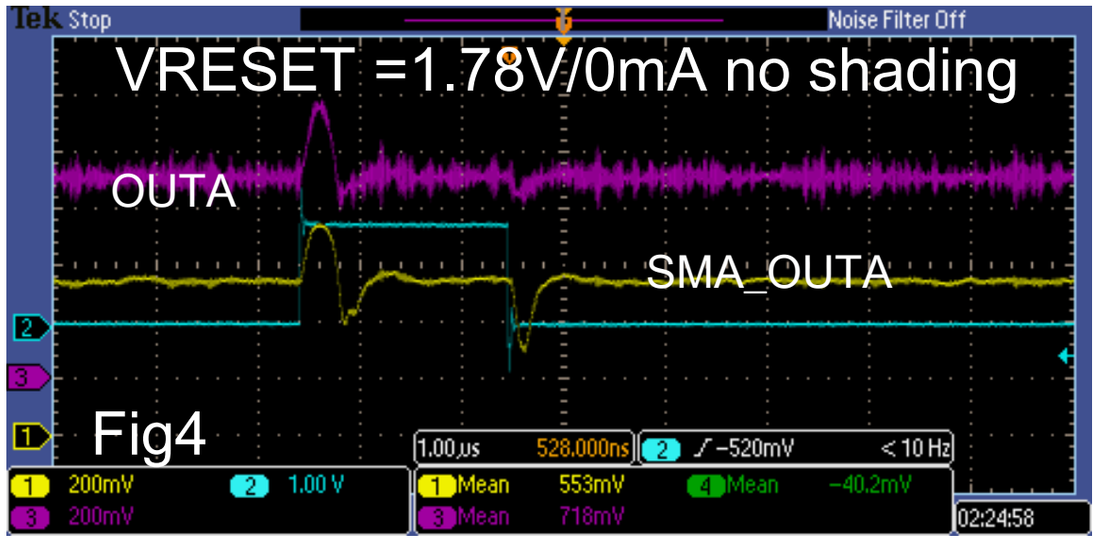
Bias	IBIAS	ITHR	IDB	VCLIP	VCASP	VCASN	VCASN2	VRESET
Design value	440 nA	4.5 nA	1 μA	0/0.2 V	0.6 V	0.55 V	0.5 V	1.4 V
Config. value	440nA	1.5nA	1uA	0.068V	0.6V	0.55V	0.5V	1.71V

Chip2









Chip2 performance is the same as what I expect, and consistent with Ying as well.

Preliminary results together with circuits behind

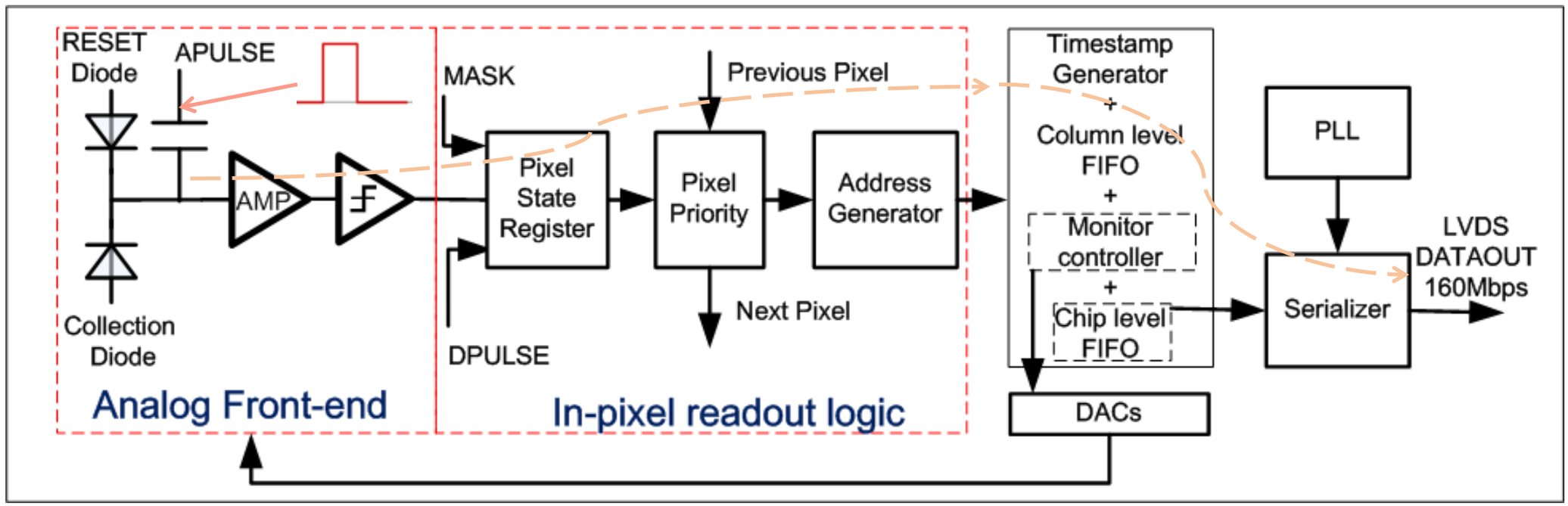


Fig 1 Readout flow diagram for one pixel

- Following the DACs configuration parameters as the previous slide.
- Give a pulse as the injection to the test capacitor inside analog front end.
- Turn on the in-pixel readout logic , periphery and PLL blocks.
- Readout the data from the LVDS output interface.

Preliminary results together with circuits behind

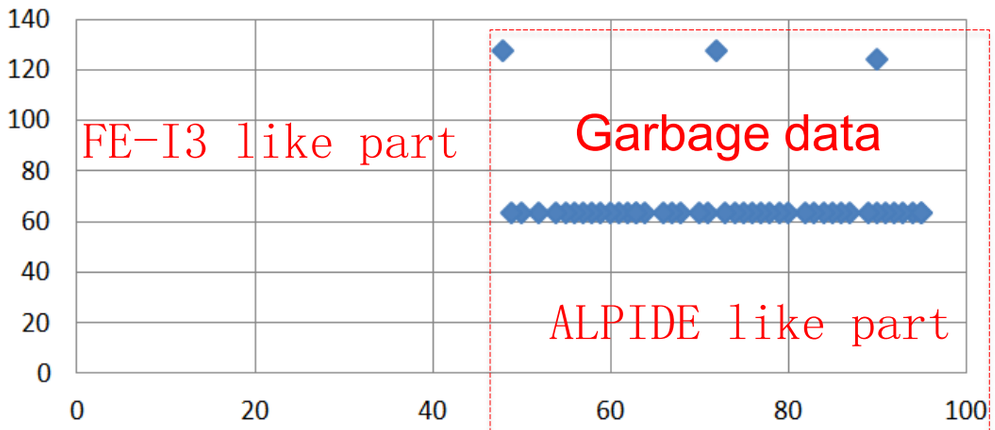


Fig 1 Baseline of Chip2

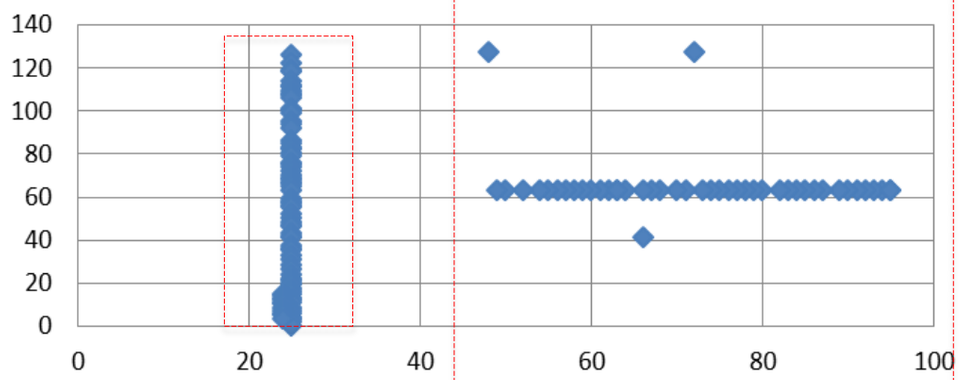


Fig 2 Turn on COL25&COL24

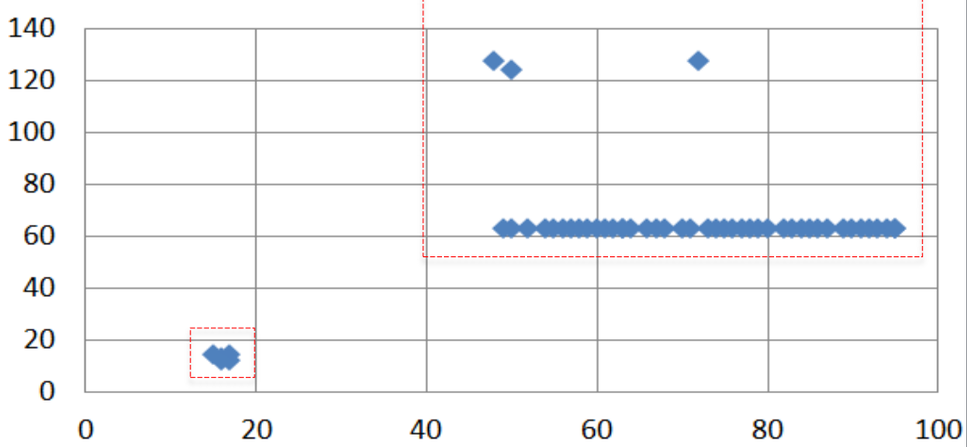


Fig 3 Turn on 4x3 adjacent pixels

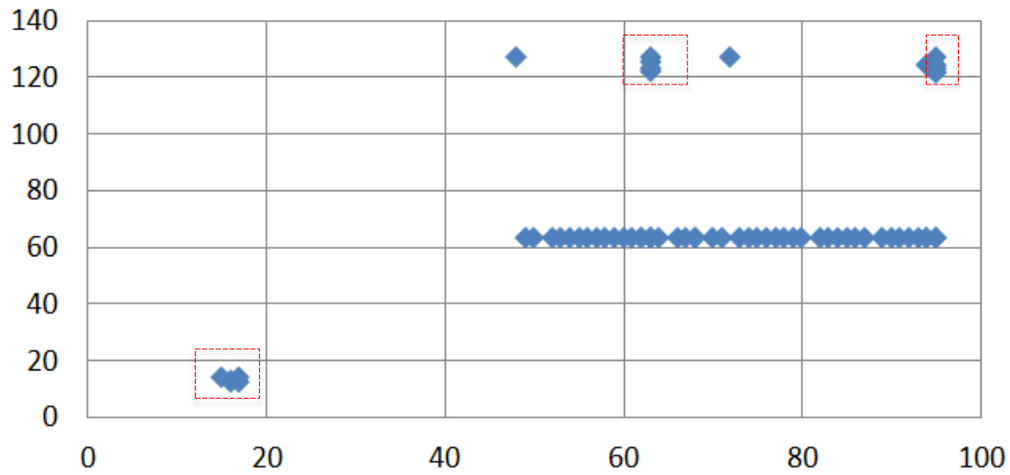


Fig 4 Turn on more pixels from COL95/63

- The Chip2 is working at 1.85V/0.716A.
- Fig1 is the original state of the chip without any injection. The ALPIDE like part has hot pixels due to the power.(2V is better).
- Fig2 and Fig3 show the FE-I3 like part performance. Only part of data were read out. (I guess it is the power reason)
- Fig4 shows the COL95&COL63 is working fine.

→From the preliminary test, digital readout part is not working at the best state with 1.85V power supply.

Preliminary results together with circuits behind

- Set up the Chip with 1.9V/0.76A and VRESET of 1.76V with shading.
- Turn on （COL30，ROW0）to observe analog OUTA signal
- Open a specific region and do APULSE injection.(COL17/16/15/14,ROW14/13/12) and fire COL15/14

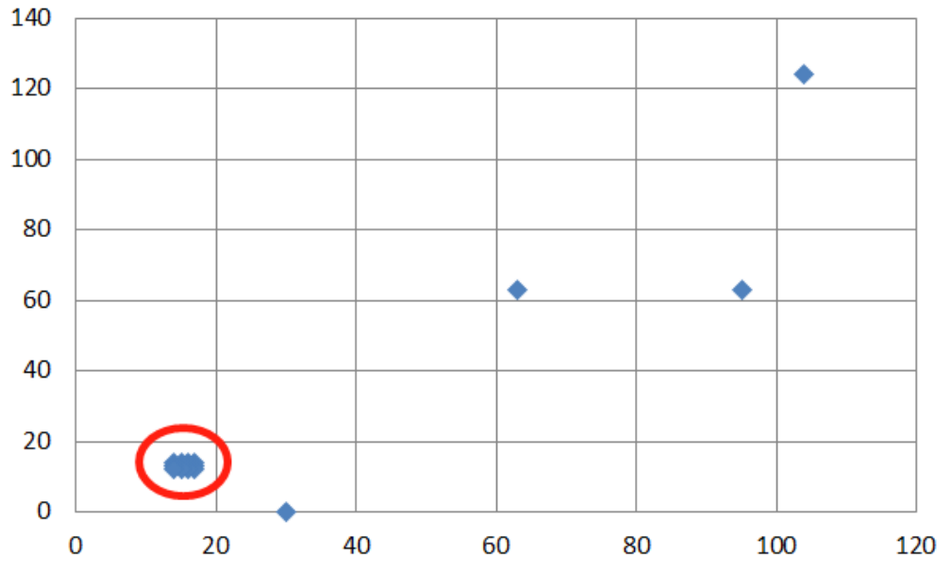


Fig1 LVDS DATA from the 1st run.

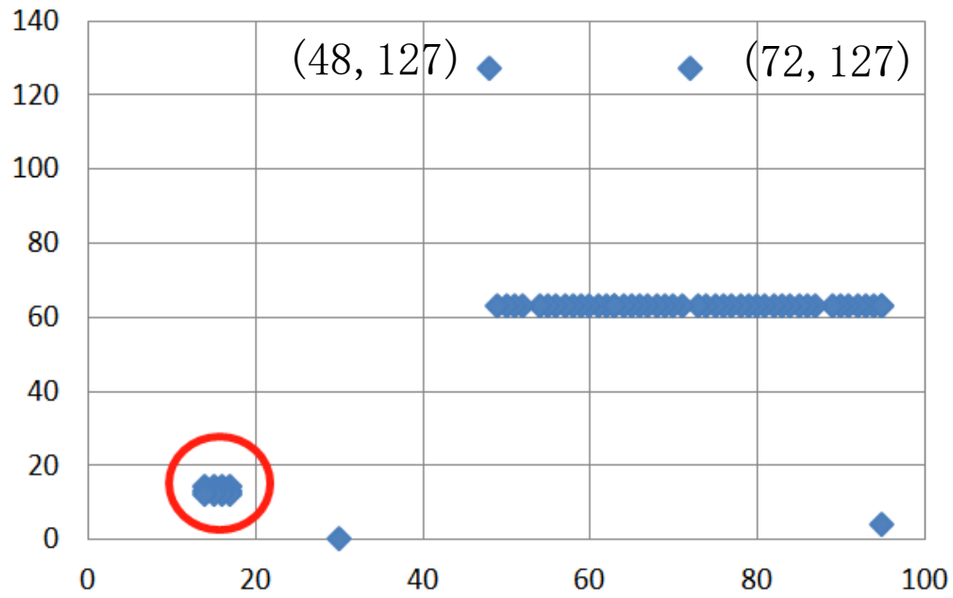


Fig2 LVDS DATA from the 2nd run.

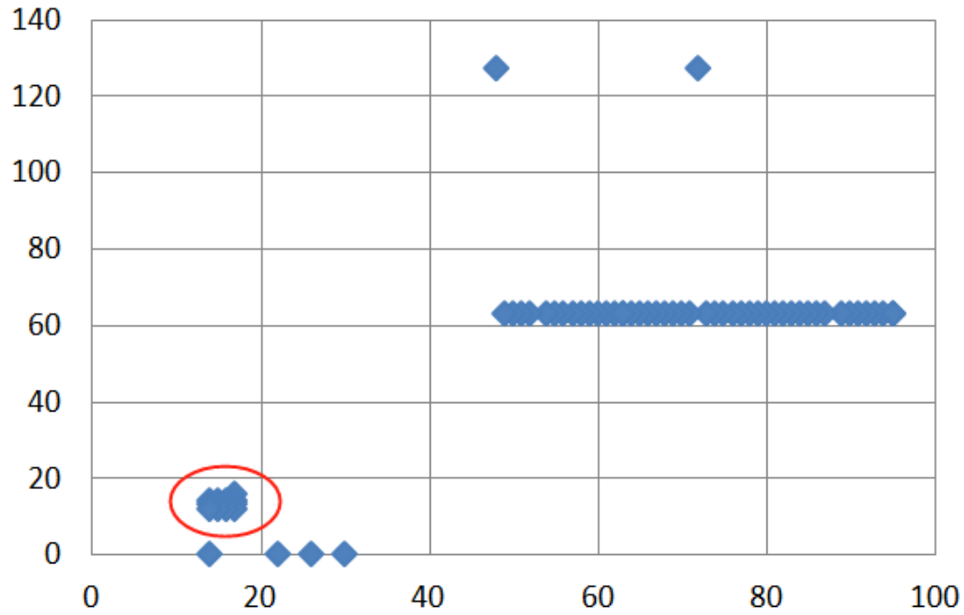


Fig3 LVDS DATA from the 3rd run.

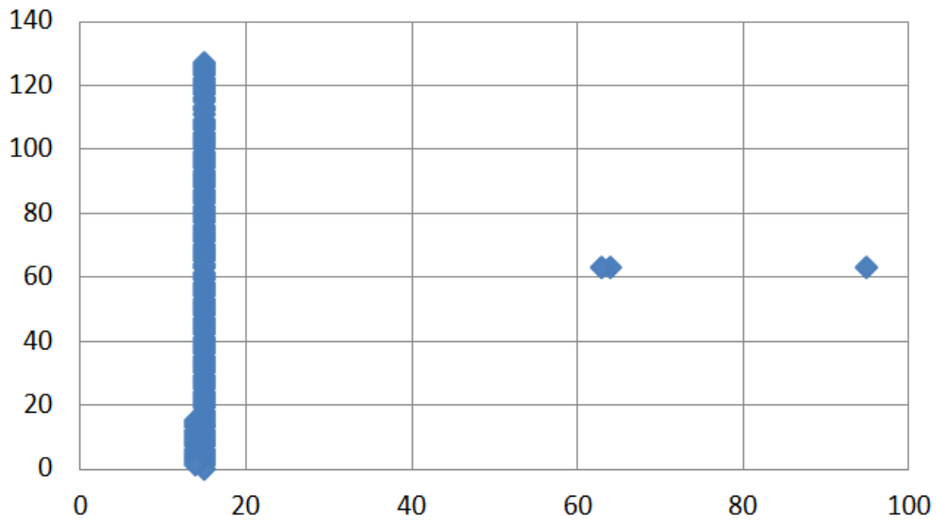


Fig4 Fire the Col15/14

Comparing with1.85V power supply, 1.9V is more reliable.

Here is no valid data loss.

It meets what we expect, when there are too many pixels, may throw away some blocked data.

VDD 1.9V and VRESET 1.76V are good operating point for my Chip2.

Further test with full chip

- Set up the Chip with 1.9V/0.76A and VRESET of 1.78V without shading.
- Expose the chip to mouse infrared or cell phone flashlight.

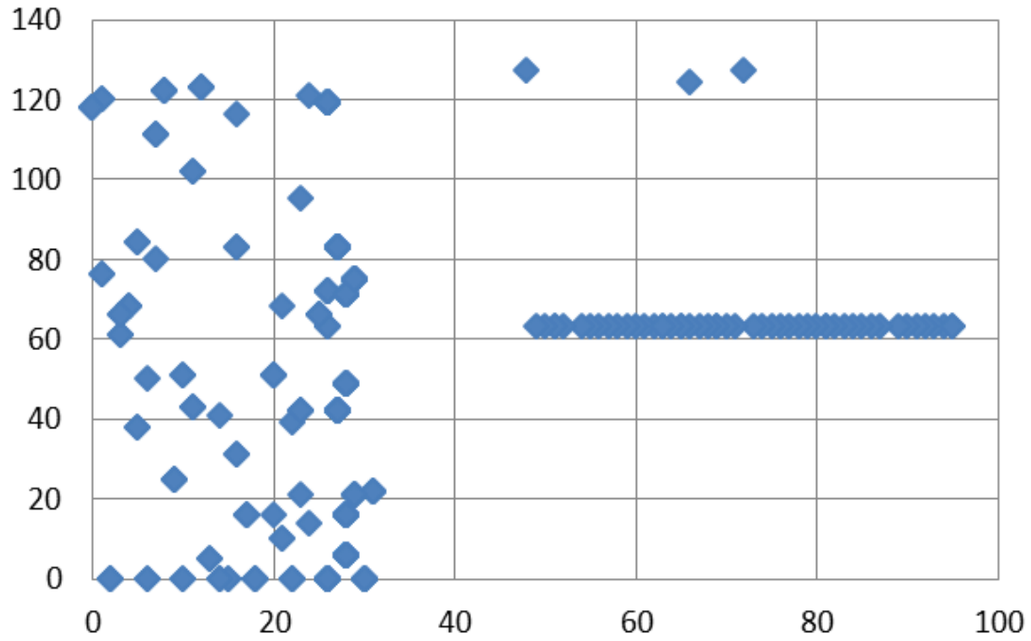


Fig1 LVDS DATA from exposure to infrared .

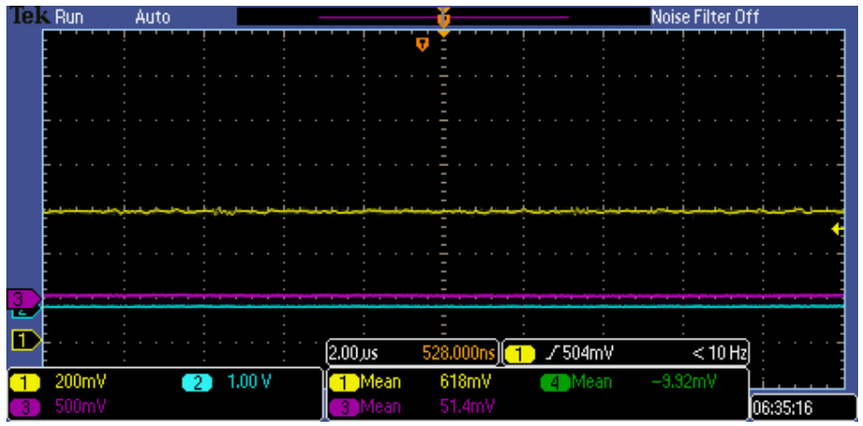
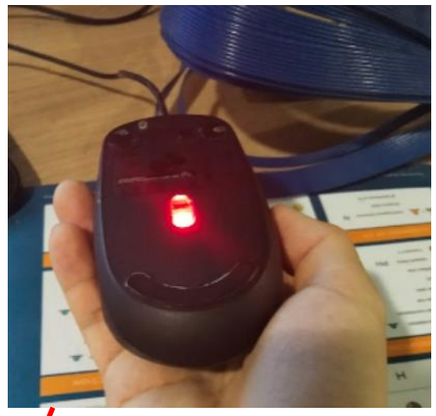


Fig3 OUTA signal with daylight condition



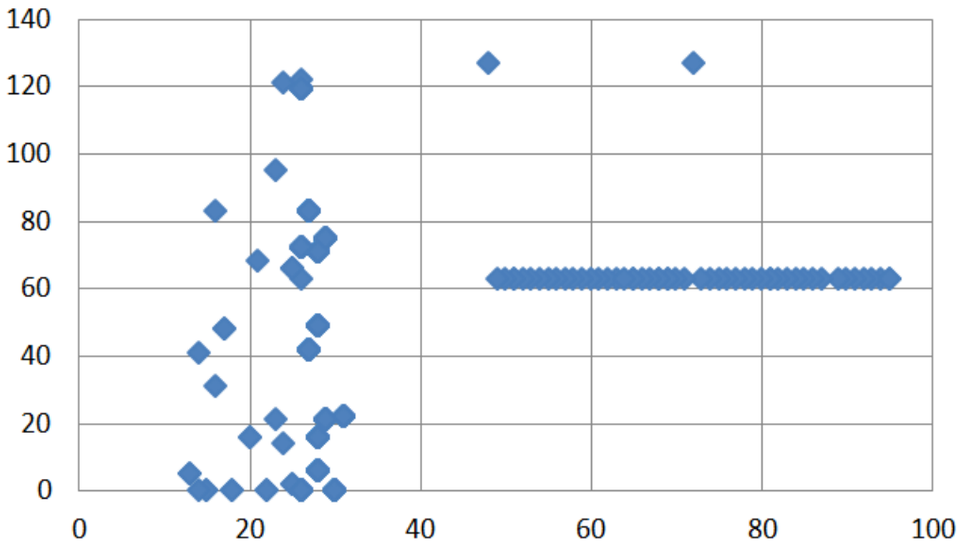


Fig2 LVDS DATA from exposure to flashlight

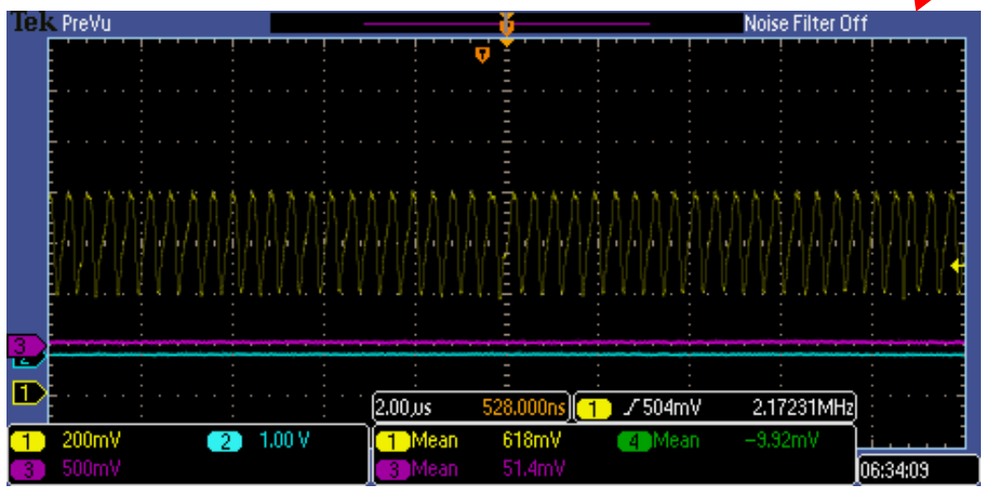


Fig4 OUTA signal with infrared exposure

It seems the pixel sensors could collect the light charge and the ROW0 is more sensitive.

Further test with full chip

- Set up the Chip with 1.9V/0.76A and VRESET of 1.78V without shading.
- Expose the chip to mouse infrared.

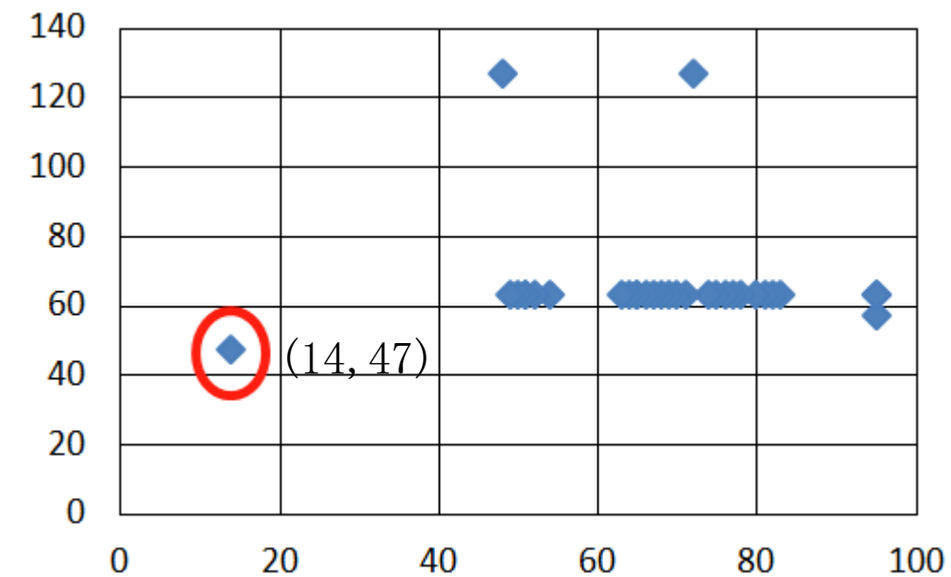


Fig1 Turn on COL15&COL14

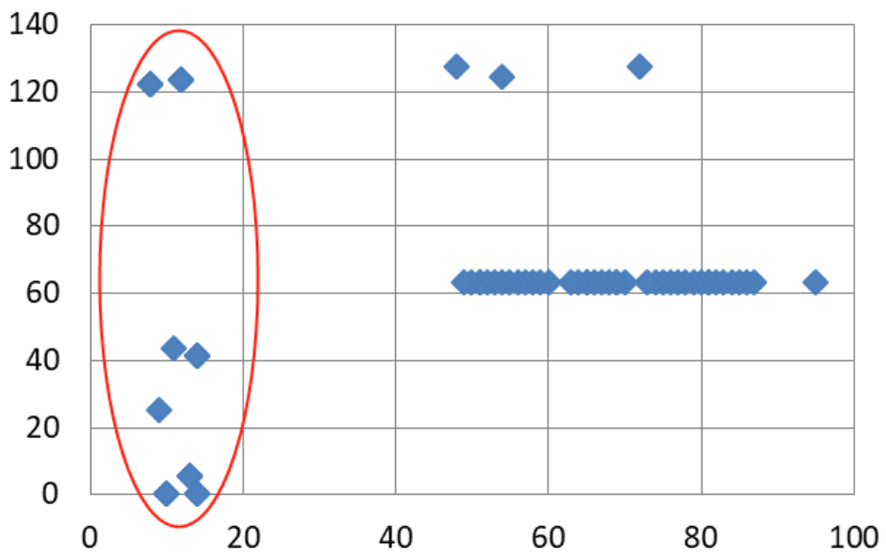


Fig2 Turn on COL15/14/13/12/11/10/9/8

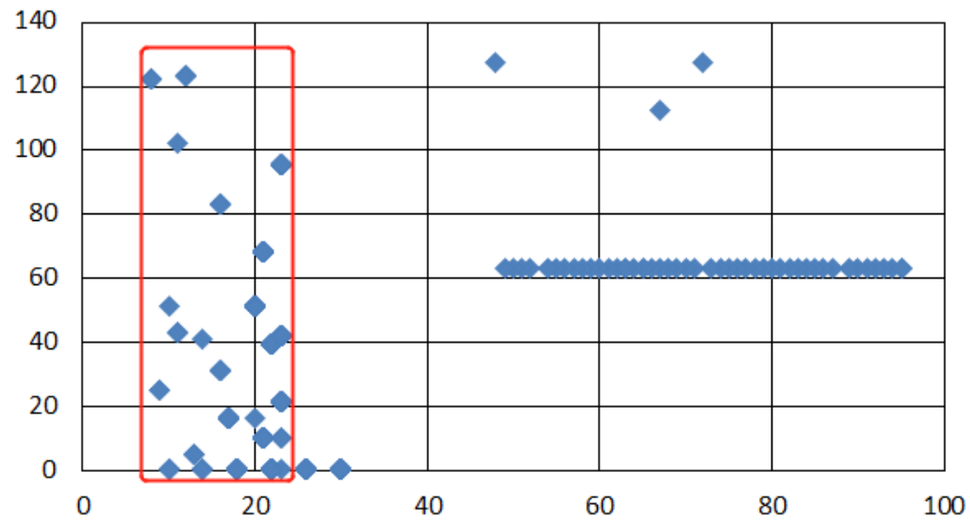


Fig3 Turn on Row0 and COL[23:8]

- There are many positions with multiple hits, this is not the real hit map.
- It seems around 1 infrared hit per double column.
- It proves the function of MASKING PIXELS is working fine.
- The ROW0 is the bound to digital periphery, and it is more sensitive.
- The function of COL31~COL0 satisfies the design requirement.

Summary and outlook

- Analog front end of Chip2 is working properly.
- Analog front end of Chip1 is not so good, and the circuits behind can not detect the signal correctly， because the low VRESET make the pixels more sensitive.
- The FE-I3 like section (COL0~COL31)is working fine at the power supply of 1.9V/0.76A ;
- ALPIDE like part could perform at the COL95 and COL63.

→Then I will try to do more test and draw the real hit map.

→ Start to organize the preliminary results into a paper.

Thanks for your attention.