Status report on the CEPC Silicon tracker

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On behalf of the CEPC Silicon Tracker Working Group

Outline

Project background

➢Ongoing activities

- ATLASPix3 characterization
- Demonstrator (module and stavelet)
- Tracker layout optimization
- Mechanical design

➤Summary

Project Background

CEPC tracker

- Mixed Tracker (TPC/DC + Silicon)
- Full silicon layout

Similar requirements to ATLAS/ALICE

- O(100)m² area, bunch spacing(25 ns) at Z-pole
- Lower radiation levels and per-event occupancy
- Plenty of experience to learn from

>International Collaboration

- Depleted CMOS pixel sensor
- Demonstrator for concept/system verification
- Tracker layout (software), Mechanical Design





To start with existing components

International collaboration



Biweekly meeting And Twiki page

November 2020

- 19 Nov Silicon Tracker biweekly meeting (protected) (New!
- 05 Nov Silicon Tracker biweekly meeting (protected)

October 2020

- 22 Oct Silicon Tracker biweekly meeting (protected)
- 08 Oct Silicon Tracker biweekly meeting (protected)

September 2020

- 24 Sep Silicon Tracker biweekly meeting (protected)
- 10 Sep Silicon Tracker biweekly meeting (protected)

August 2020

- 27 Aug Silicon Tracker biweekly meeting (protected)
- 13 Aug Silicon Tracker biweekly meeting (protected)

July 2020

CEPC MediaV	Viki Website Page Discussion View source History							
Main Menu Home Meetings Datasets	Si Tracker A task force was formed in 2019 towards a fully CMOS-based silicon outer tracker for CEPC.							
Working Groups Accelerator Theory Physics and Detector Docs & Links Documentation Code and Infos Recent Talks Physics Tools Useful Links Navigation Help Recent changes Search Go Search	Contents [hide] 1 Presentations 2 Group meetings 3 ATLASPix references 3.1 Publications on ATLASPix: 3.2 Useful documentation: 3.3 Instructions on setting up ATLASPix with Gecco readout							
	Presentations Progress and status on the project are reported in the following events: CEPC workshop @ Oxford, June 2019: talk by Daniel Muenstermann et al. B CEPC workshop @ IHEP, November 2019: talk by Harald Fox et al. B CEPC day, 27 March 2020: talk by Harald Fox et al. B A first estimation on DAQ requirement, 14 Oct 2020: talk by Jens Dopke a CEPC workshop @ Shanghai, Oct 2020: Status of silicon tracker demonstrator by Attilio Andreazza B, From ATLASPix3 to CEPCPix1 by Hui Zhang and Ivan Peric B, Requirement (on DAQ) from silicon tracker by Jens Dopke a							
	Group meetings Indico links to SITracker meetings ATLASPix references Currently the sensor option is based on High-Voltage CMOS developed for ATLAS inner trackers (ITLASPIN)							
	Publications on ATLASPix:							

HV-CMOS

>HV-CMOS

- Larger collection diode + Deeper depletion region
- Providing:
 - Larger and fast signal (collected by drifting)
 - Radiation tolerance
 - Can be thinned: material budget
 - No hybridization, lower cost

Sensor proposal: ATLASPix3

- ATLASPix3 was designed in 2019
- A CMOS sensor developed to fulfill the requirement for the ATLAS ITK outer layer upgrade
- Functional sensor available for prototyping optimization for CEPC Tracker





- Pixel size $50X150 \ \mu m^2$
- Chip Size: 2.02 cm by 2.1 cm
- 132 columns of 372 pixels
- TSI 180 nm HV process on 200 Ω cm substrate

- Up to 1.28 Gbps downlink
- Digital part of the matrix located on periphery
- Both triggerless and triggered readout possible

ATLASPix3: Test setup

Lab Measurement setup (developed by KIT)

- Artrix-7 FPGA board
- GECCO board(GEneric Configuration and COntrol system)
 - PCIe connector (with DUT)
 - Highly modular with function cards(versatile)
 - Easy changing of DUT sample (no cabling)
 - 90° Adapter
- ATLASPix3 Carrier PCB

GECCO system boards manufactured and distributed





ATLASPix3: DAQ software

Powerful DAQ software (KIT)

- Using on ATLASPix3 testing since the end of 2019
- Based on C++ with **Qt** framework
- Graphical User Interface
- Managing the Configurations for DUT and Firmware
- Very helpful for system debugging

>We were able to install the system at IHEP

ASIC Settings					Tests		
Connection	ol/Row/TDAC	Configuration Pins	TDAC	* *	Voltages/Injections	Injections	UDP Readout
Search Devices					Write VoltageBoards (!)	tart Injections (Restart	Reset Sender
Digilent USB Device A 🔹 💌		TDAC_in_col_1			Threshold a second th	Injection 0.00(- +	Reset FIFO
Open Device Close Device		TDAC_in_col_2				# 100 - +	Debug Mode
oad/Save Configuration		TDAC_III_COL_3			VNDet 0.000 V E	Pulses/Trai 0 - +	10 - +
config_default.xml 💌		TDAC_in_col_5			VNAmp 0.000 \ 🖻	Init. Delay: 500 🗕 🕂	167772 - +
AC_Settings_20201112.dat 🔻		TDAC_In_col_6			Baseline 0.000 \ 🗠	Period: 100 - +	192.168.1.128
Load Config Save Config		TDAC_in_col_8			VPLoad 0.000 \ ±	ClockDiv: 60 - +	255.255.255.0
Register Reading/Writing		TDAC_in_col_9			VNBiasRec 0.000 \ 🗄	async 🔹	::00:00:00:00:00
Addr 0 ± Value 0 ±		TDAC_in_col_11			Trigger Control	ATLASPix3 💌	Update (!)
Read Write		TDAC_in_col_12			Pos Edge Send Trigger	Fast Readout	
		DAC_in_col_14			Trigger Source:	Stop Fast Clock	Readout
		TDAC_in_col_15			Injection 💌	Reset Fast Readout	Decode Dataset
		TDAC_IN_COL_17			Noise Rejection Level:	Reset State Machine	Complete Readout
		TDAC_in_col_18			0 ± Reset ID	Reset Readout FIFO	Binary Output
		TDAC_In_col_19			0 ± Undate	Debug Mode	🔲 via DataMux
		TDAC_in_col_21				Triggered Readou	S Phase: 0 E
Jse Shift Registers 💌 🗌 Auto		TDAC_in_col_22			DAC	Num Signals: 0 - Ti	igger Spacing: 15
Mode		TDAC_in_col_24			Config	Print Data	igger Length: 1
Update ASIC Update All		TDAC_in_col_25			VDAC	Decode Data	um Triggers: 0
		DAC_in_col_27			Column/R	160Mbit/s 💌	Data Rec Clock Edg
29 📃 Auto Update		TDAC_in_col_28			🖌 Auto Change) Shift Data Rec Cloc

Test setup **@IHEP**



Tremendous help from Rudolf (KIT)

Boards manufactured and assembled in China

Chip wire bonded in IHEP clean room

• 10 of the arrived 18 chips





Sensor IV



• Low leakage current of < 100 nA @ -60V



Front-end verification





Threshold scan of #2

- Threshold scan of one pixel
 - Varies TDAC
 - Trimming to be done
- Threshold scan of one row
 - Distribution of Vt50





Threshold scan of #5

• Threshold scan of one row



Sensor development

Complete ATLASPix3 characterization with laser and radioactive source tests

Sensor design towards the CEPC tracker

- Sensor design (CEPCPix: smaller pixel size $25 \times 160 \ \mu m^2$) for CEPC under preparation
- Switch to Chinese foundry (under discussion)

MoU with KIT to be signed



Demonstrator project

Build a short stave (stavelet) to verify the concept and system design

Stavelet demonstrator (12 QuadModules)

design under optimization

- **Detector element** consisting of multiple modules on low mass composite support
- Water cooling proposed and used in thermal analysis





QuadModule

Design concept from ATLAS ITk pixel

QuadModule design: readout unit based on 4 ATLASPix3 chips

- Shared services among 4 sensors by common power connections and configuration lines
- Benefits of in-chip regulators to reduce connections
- Avoids complications with stitching
- QuadModule flex being tested @ Milano



Power integrity simulation

U1

Data distribution

Adaptor Card

➢Quad Module interfacing to GECCO

➤Connection to GECCO system

- Adapter Card (design completed)
- Commercial data pigtail
- Custom power pigtail

Design completed @ Edinburgh





Tracker layout optimization +software

Tracker geometry implemented in ACTS (Track Reconstruction Software)



Important to coordinate the layout optimization of the Vertex/Tracker as a whole system

Mechanical Design

Light weighted support structure (stave core)

 Design inspired by ALICE/ATLAS truss structure, longer extension, higher rigidity and stability (challenging to align detector elements with less tracks)



Integrated into the detector design

CEPC Work Day

Summary

• International collaboration group on CEPC Silicon Tracker

- Ongoing activities including
 - ATLASPix3 characterization
 - **Demonstrator** design/development
 - layout optimization
 - Mechanical design



Backup: ATLASPix3

Block scheme of the pixel matrix and column circuits



HV-CMOS structure



backup



Pixel Trimming

Activities and status

DAC linearity characterization (Milano)

- Threshold, Baseline, Injection pulse
- Ampout, ToT



Supporting Structure

ALICE Outer Layer Stave ~0.8% X₀



ATLAS-ITK: 0.5% X₀ ITK alpine stave (+module)



ALICE Inner Layer Stave ~0.3% X₀



CEPC design target:

 $0.65\% X_0$ for stave + modules

Crucial elements:

- Light-weighted carbon truss structure
- Al based flex (prototype with Cu)

Readout systems

Da

niel Muenstermann	Universi
ATLASPix3 readout systems	
KIT system	
 Nexys Video+GECCO based, well supported (as KIT uses it for ch characterisation), cheap (< 1kEUR), comparatively slow 	ip
Would require a dedicated order of GECCO cards	
Compatible to KIT's single chip card and "Telescope card"	
■ Needs a simple adapter board to fit the Milano flex → Edinburgh	
■ CaRIBou	
 UniGe+BNL developed, KC706+CaR-board based, ATLASPix3 is implemented, but maintainer (Mathieu Benoit) left UniGe, continue support thus unclear, comparatively expensive (~4 kEUR) Currently, an order for more (and slightly updated) CaR-boards is by CERN, I have requested 4 CaR boards for us via RD50 	ed prep a red
 A long-term major redesign of CaRIBou is underway, with the goa replacing the (comparatively expensive) KC706 board. I was assur the Soft- and Firmware modifications would be "downward comp 	l of red that atible"
• YARR	
 ATLAS/RD53 readout, TEF1001+GECCO based, ATLASPix3 not implemented yet, comparatively cheap (~1 kEUR) and scalable 	

- Main issue is software implementation of ATLASPix3 in YARR
- No clear timescale for this yet

Universit

Sensor distribution

ATLASPix3: Readout

> Digital Part(10% total area):

- configuration registers
- hit buffer for each pixel
- Untriggered and triggered End of Column(EoCs)
- Content addressable buffer(CAB)
- Readout Control Unit(RCU main and auxiliary)
- Hit information from one pixel transmitted to the hit buffer through long routing metal lines
- HitBuffer stores the global time stamp(TS) and generate a hit word

Triggered and Triggerless readout

- Triggered: transferred to CAB where the hits are filtered based on a trigger signal
- Triggerless: transferred to EOC for untriggered readout

