Status report on the CEPC Silicon tracker

Weiguo Lu (IHEP)

On behalf of the CEPC Silicon Tracker Working Group

Outline

- Project background
- Ongoing activities
  - ATLASPix3 characterization
  - Demonstrator (module and stavelet)
  - Tracker layout optimization
  - Mechanical design
- Summary

Project Background

➢CEPC tracker

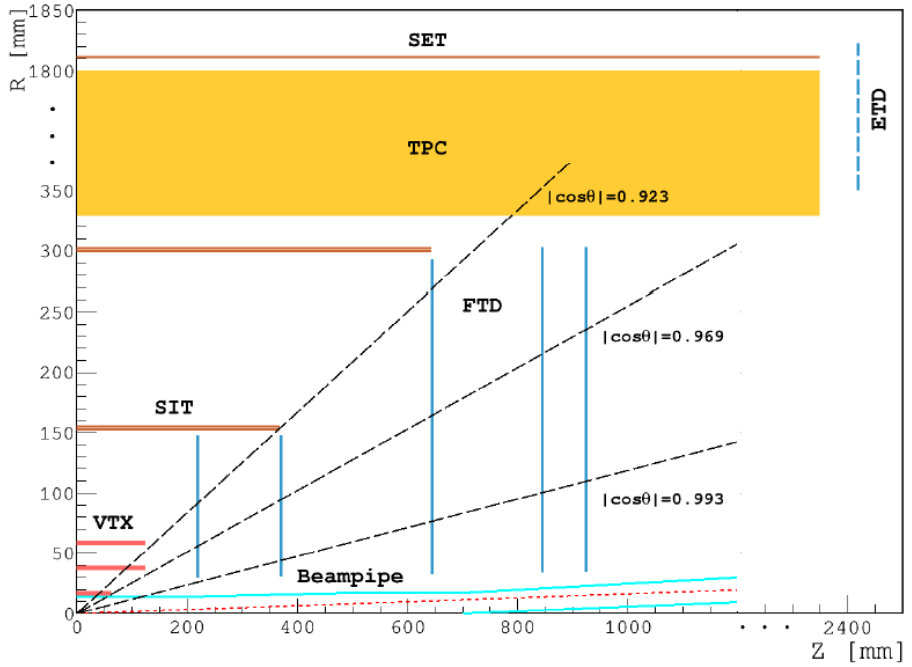
- Mixed Tracker (TPC/DC + Silicon)
- Full silicon layout

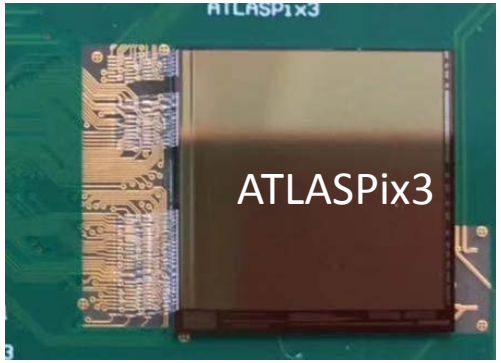
➢Similar requirements to ATLAS/ALICE

- O(100)m² area, bunch spacing(25 ns) at Z-pole
- Lower radiation levels and per-event occupancy
- Plenty of experience to learn from

➢International Collaboration

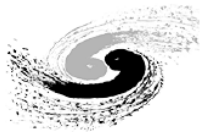
- Depleted CMOS pixel sensor
- Demonstrator for concept/system verification
- Tracker layout (software), Mechanical Design





To start with existing components

International collaboration



Institute of High Energy Physics
Chinese Academy of Sciences

清華大學 Tsinghua University

李政道研究所 Tsung-Dao Lee Institute | 上海交通大學 Shanghai Jiao Tong University

山东大学 Shandong University

INFN Istituto Nazionale di Fisica Nucleare — Milano Pisa Torino

哈爾濱工業大學(威海) Harbin Institute of Technology

中国科学技术大学 University of Science and Technology of China

KIT Karlsruhe Institute of Technology

西北工業大學 Northwestern Polytechnical University

The University Of Sheffield.

University of Bristol

UKRI Science and Technology Facilities Council

University of Liverpool

Warwick The University of Warwick

The University of Edinburgh

Queen Mary University of London

Physics | Lancaster University

University of Oxford

南華大學 University of South China

Biweekly meeting And Twiki page

CMOS Tracker

November 2020

- 19 Nov Silicon Tracker biweekly meeting (protected) New!
- 05 Nov Silicon Tracker biweekly meeting (protected)

October 2020

- 22 Oct Silicon Tracker biweekly meeting (protected)
- 08 Oct Silicon Tracker biweekly meeting (protected)

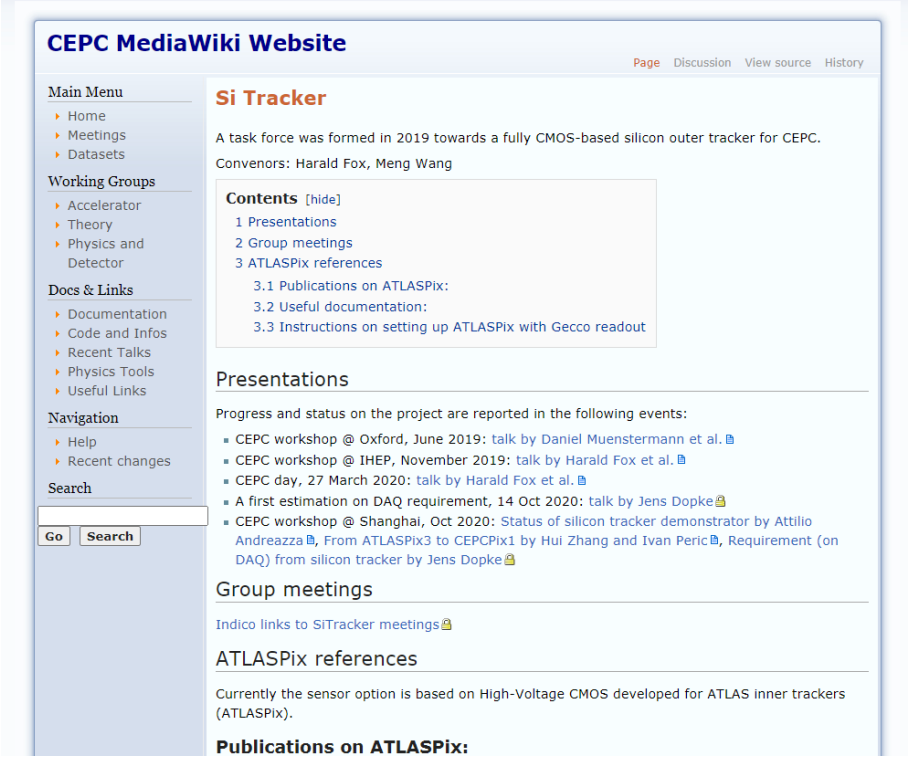
September 2020

- 24 Sep Silicon Tracker biweekly meeting (protected)
- 10 Sep Silicon Tracker biweekly meeting (protected)

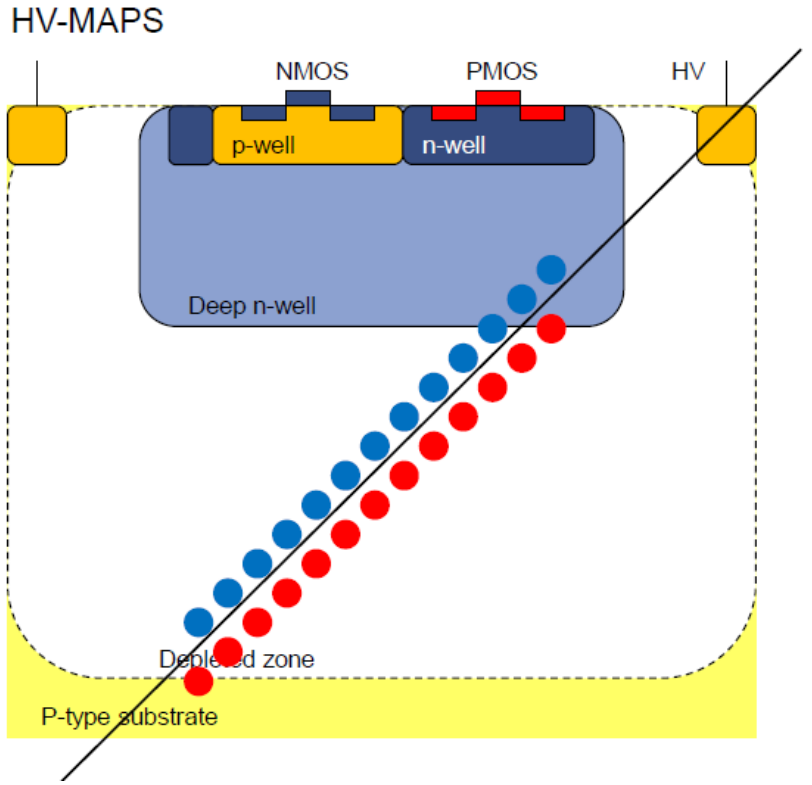
August 2020

- 27 Aug Silicon Tracker biweekly meeting (protected)
- 13 Aug Silicon Tracker biweekly meeting (protected)

July 2020



HV-CMOS



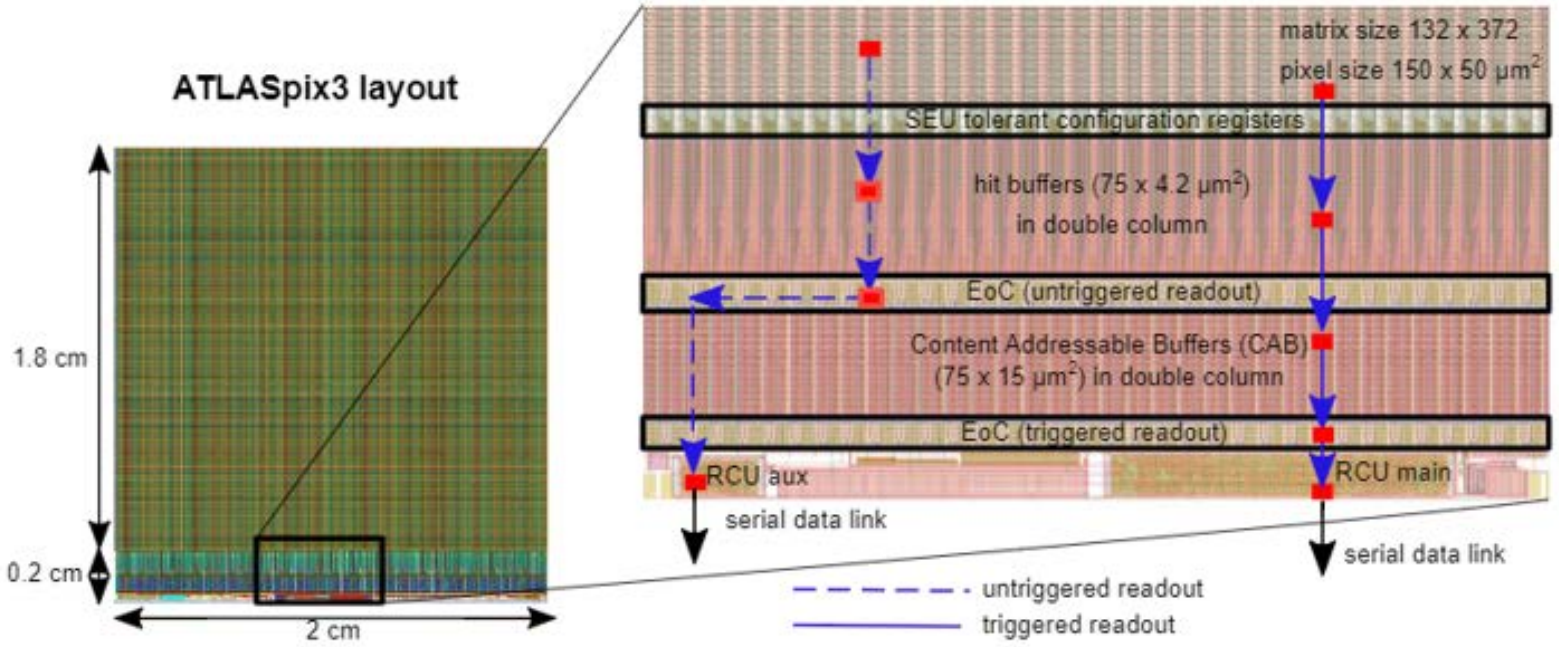
➢HV-CMOS

- Larger collection diode + Deeper depletion region
- Providing:
  - Larger and fast signal (collected by drifting)
  - Radiation tolerance
  - Can be thinned: material budget
  - No hybridization, lower cost

➢Sensor proposal: ATLASPix3

- ATLASPix3 was designed in 2019
- A CMOS sensor developed to fulfill the requirement for the ATLAS ITK outer layer upgrade
- Functional sensor available for prototyping optimization for CEPC Tracker

ATLASPix3



- Pixel size 50X150 μm^2
- Chip Size: 2.02 cm by 2.1 cm
- 132 columns of 372 pixels
- TSI 180 nm HV process on 200 Ω cm substrate

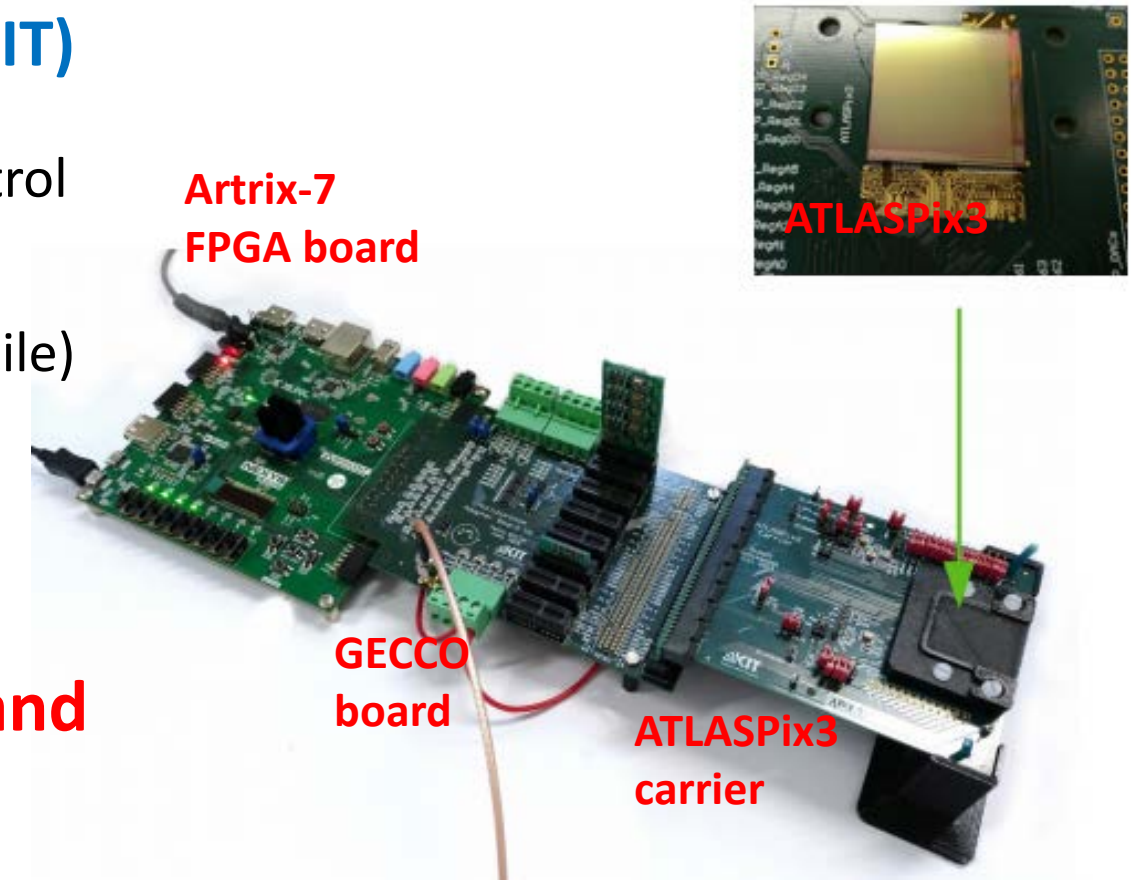
- Up to 1.28 Gbps downlink
- Digital part of the matrix located on periphery
- Both triggerless and triggered readout possible

ATLASPix3: Test setup

➢Lab Measurement setup (developed by KIT)

- Artrix-7 FPGA board
- GECCO board(GEneric Configuration and COntrol system)
  - PCIe connector (with DUT)
  - Highly modular with function cards(versatile)
  - Easy changing of DUT sample (no cabling)
  - 90° Adapter
- ATLASPix3 Carrier PCB

➢GECCO system boards manufactured and distributed

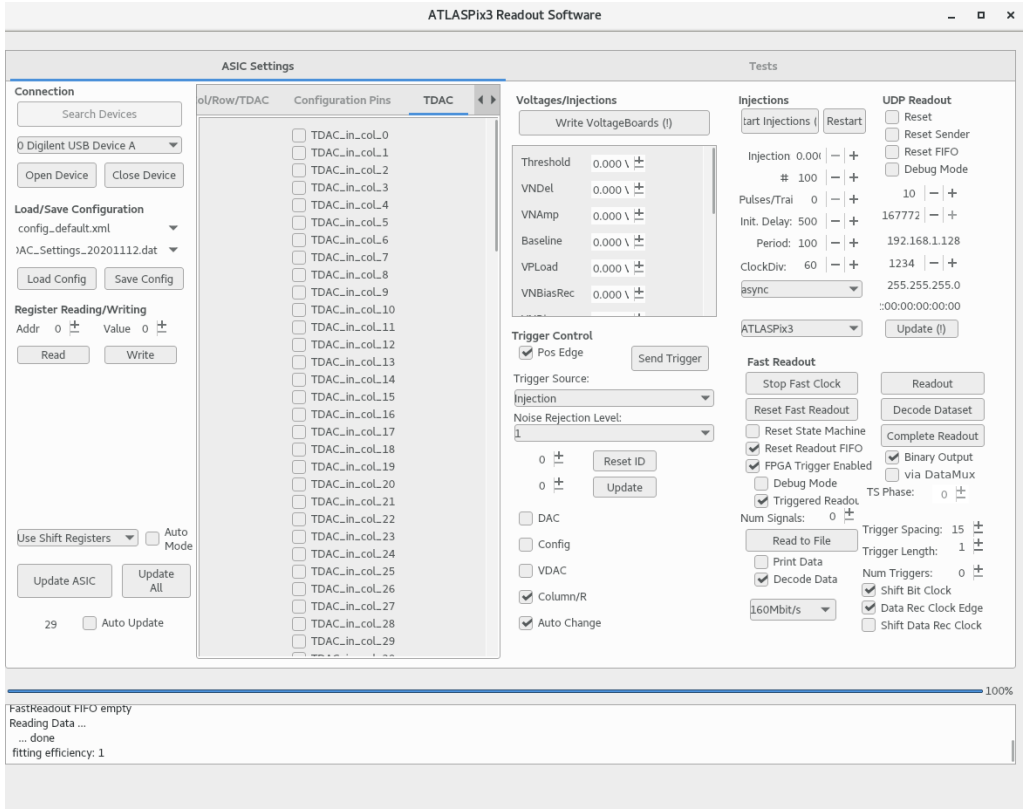


ATLASPix3: DAQ software

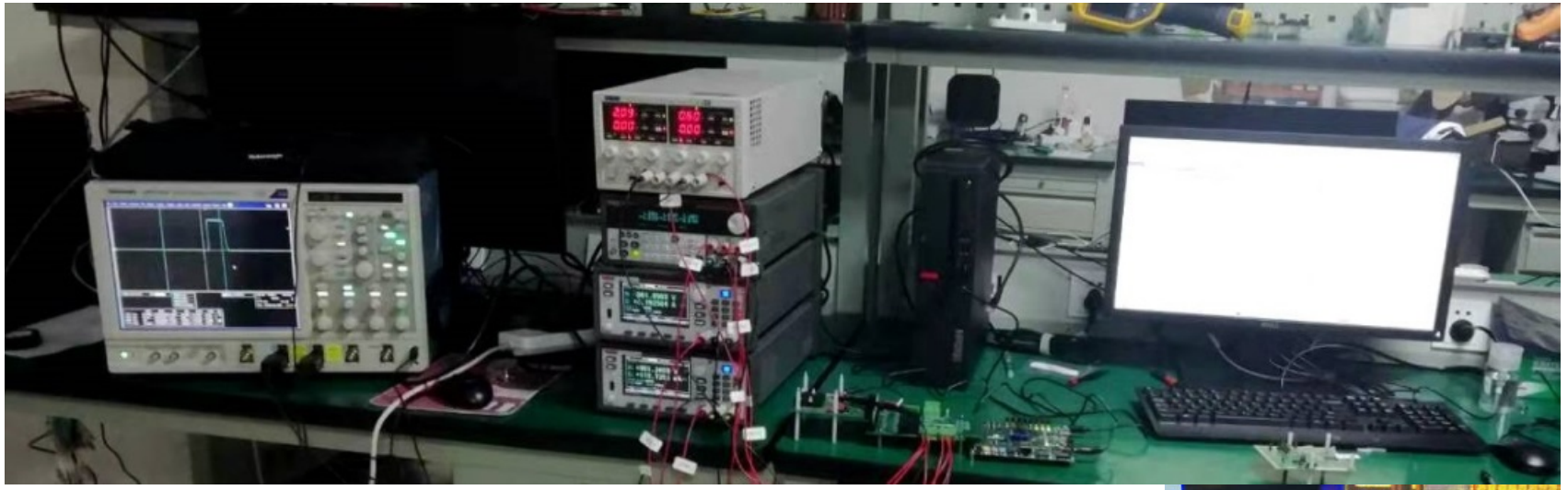
➢Powerful DAQ software (KIT)

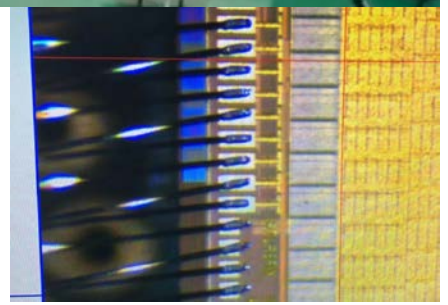
- Using on ATLASPix3 testing since the end of 2019
- Based on C++ with Qt framework
- Graphical User Interface
- Managing the Configurations for DUT and Firmware
- Very helpful for system debugging

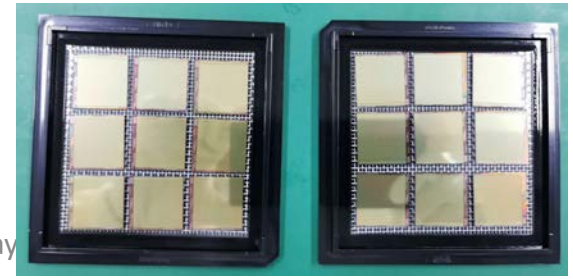
➢We were able to install the system at IHEP

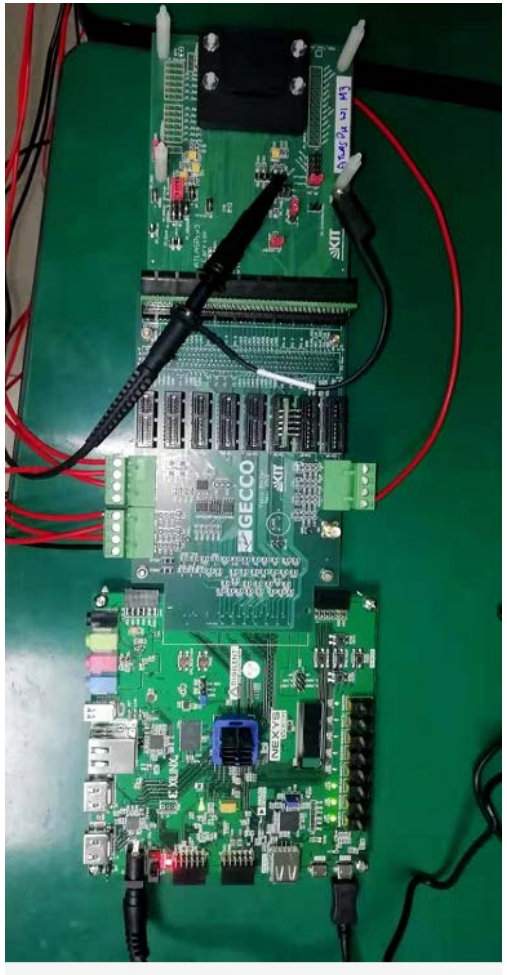


Test setup @IHEP



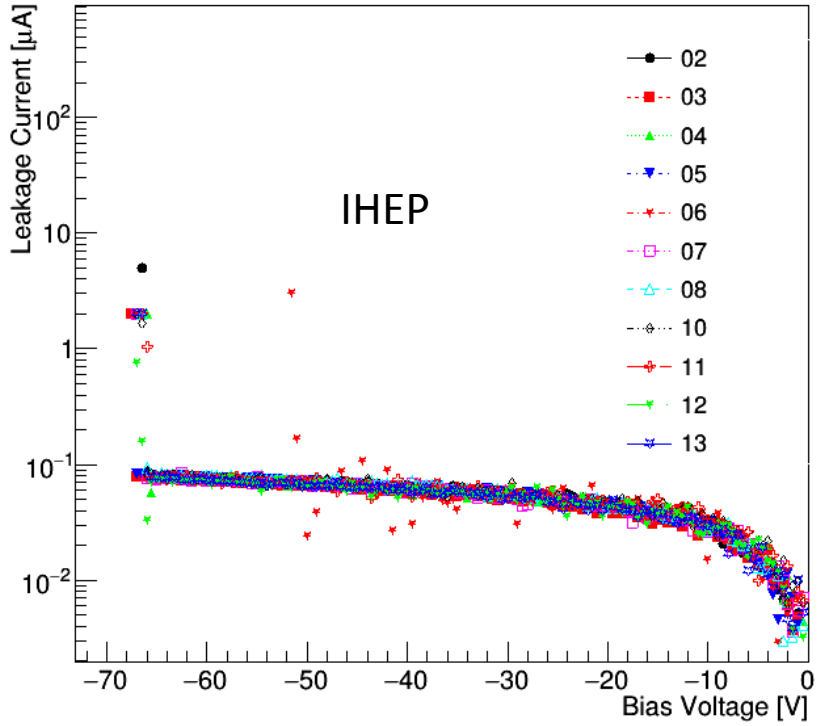


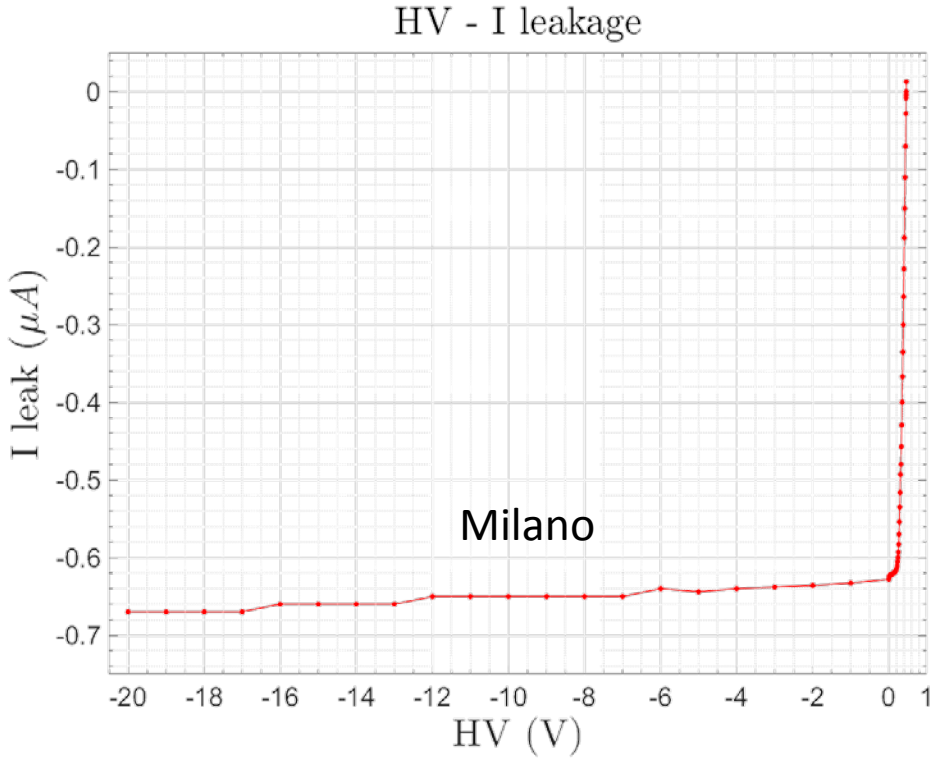




- **Tremendous help from Rudolf (KIT)**
- **Boards manufactured and assembled in China**
- **Chip wire bonded in IHEP clean room**
  - 10 of the arrived 18 chips

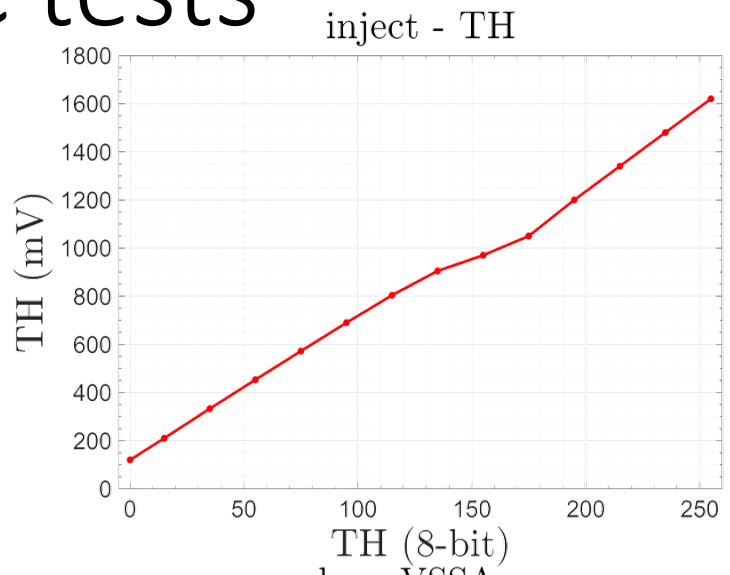
Sensor IV

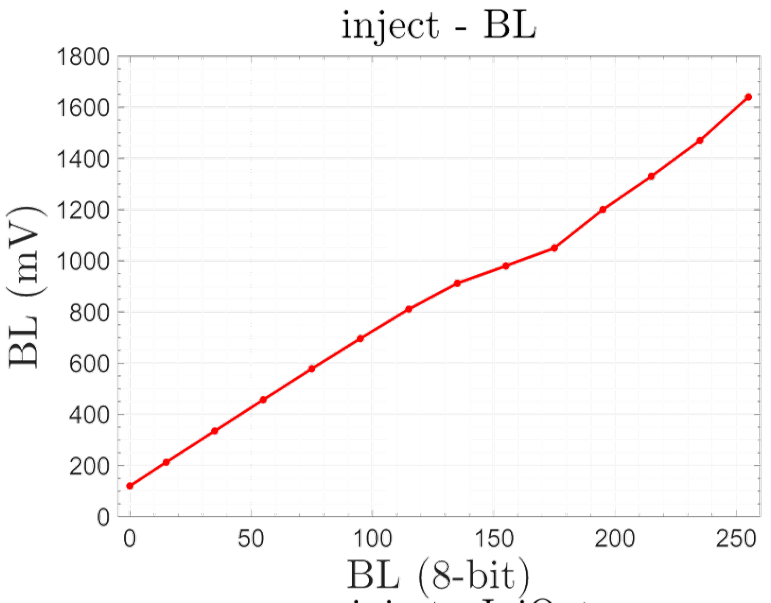


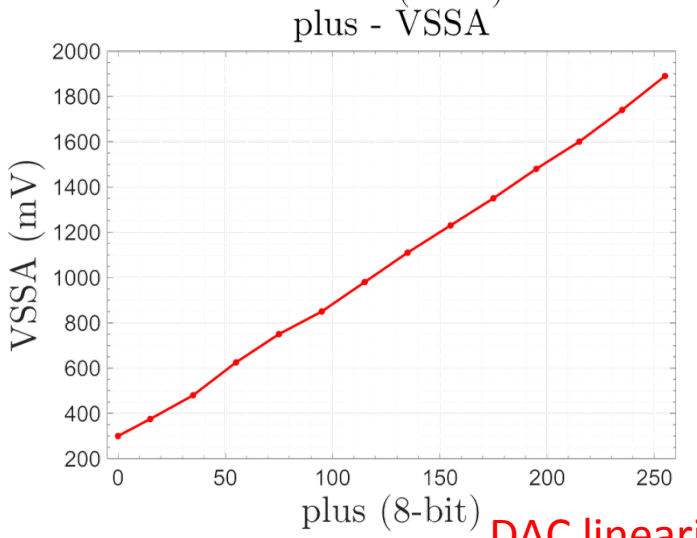


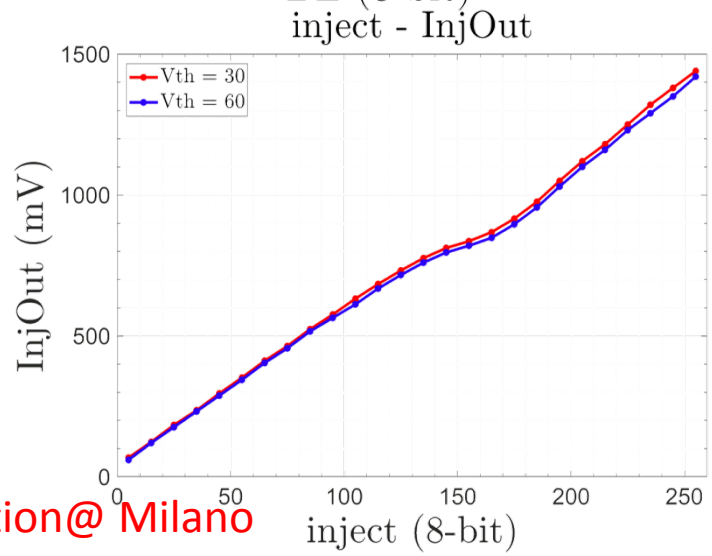
- Low leakage current of < 100 nA @ -60V

DAC tests



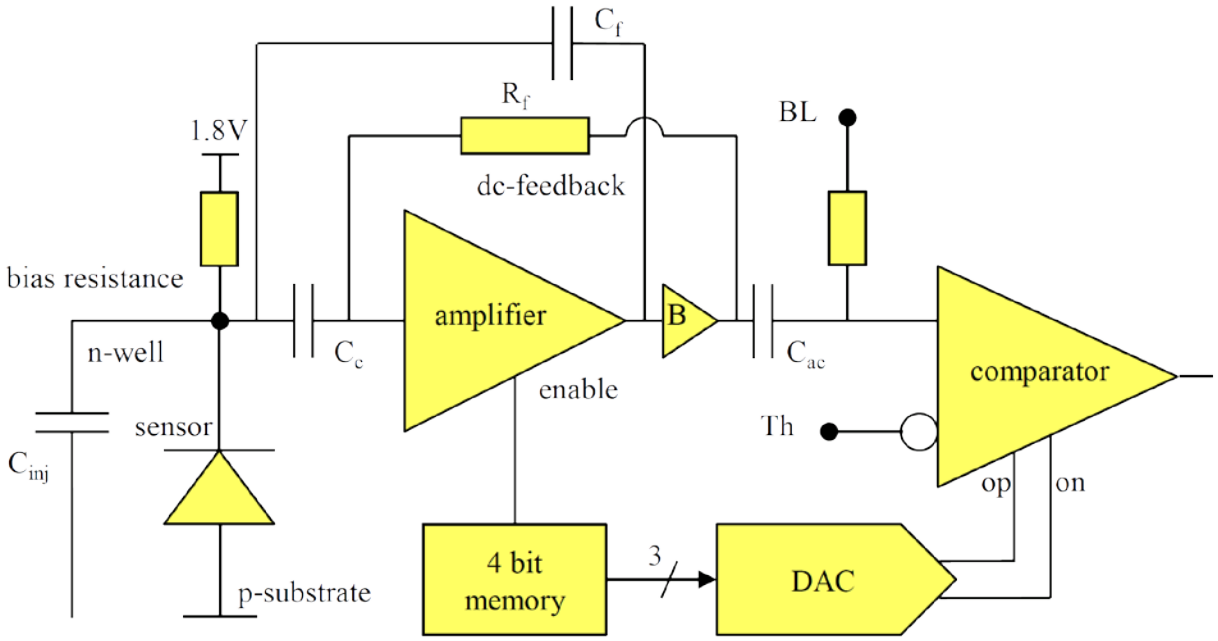


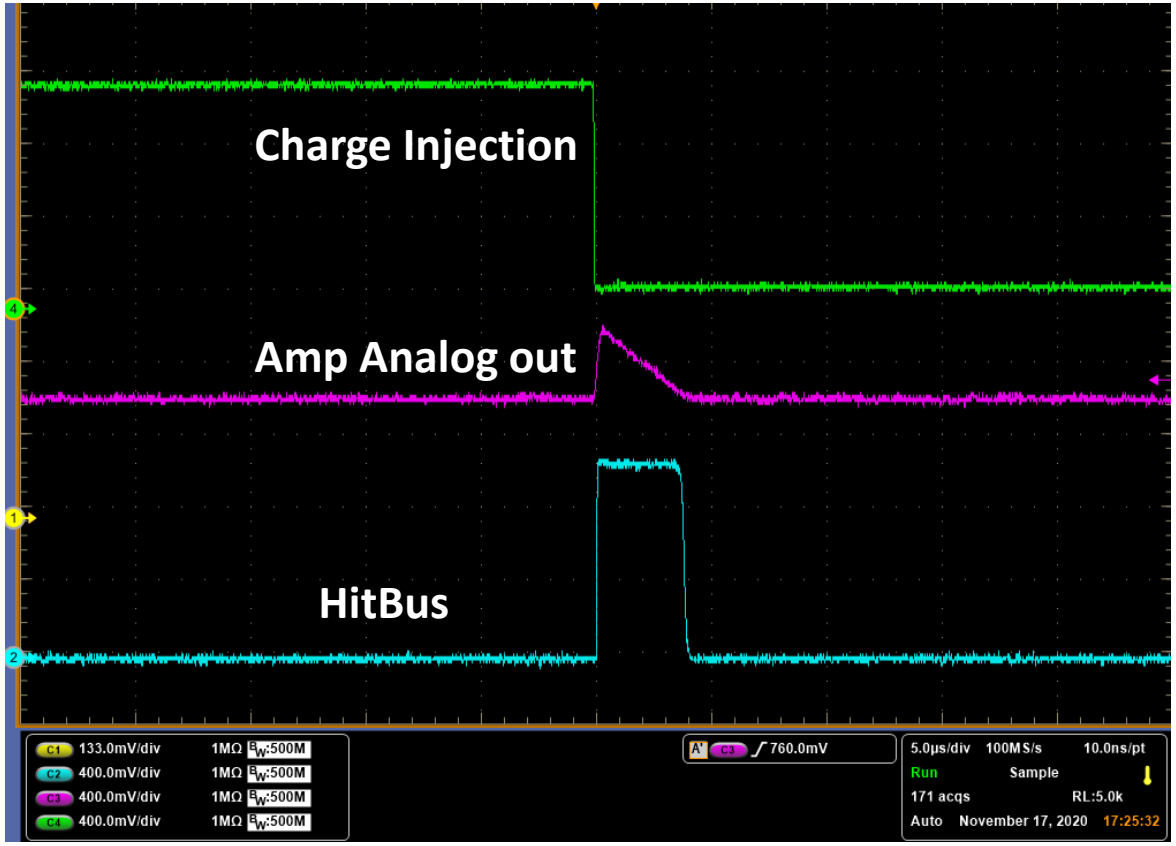




DAC linearity characterization@ Milano

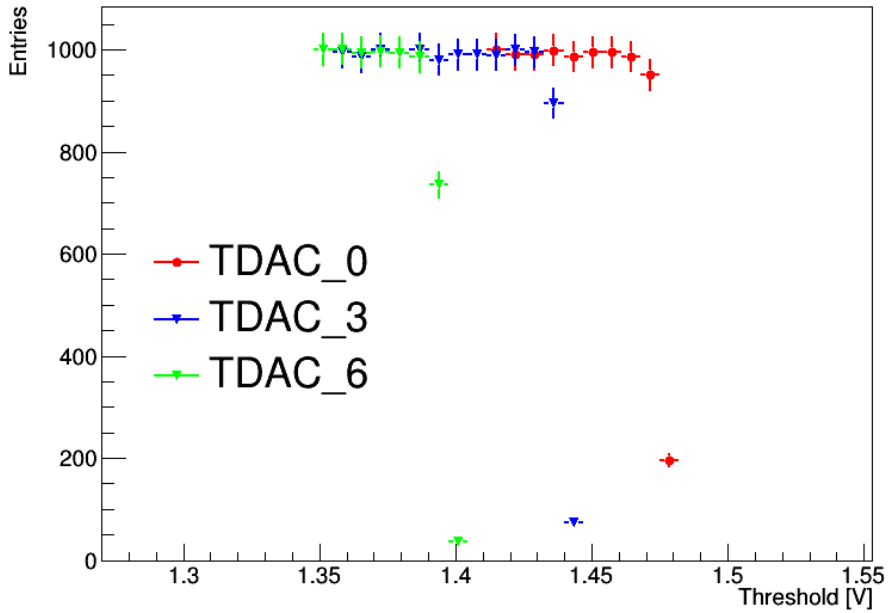
Front-end verification

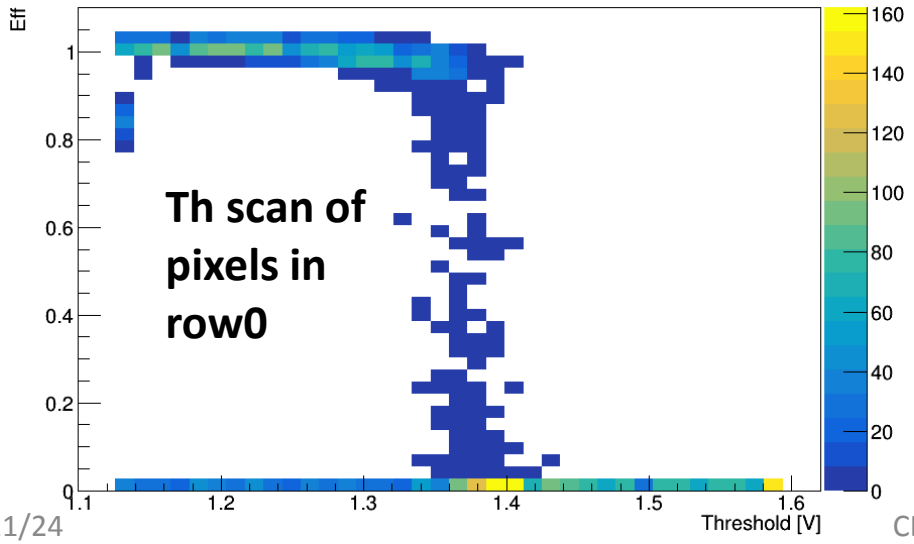


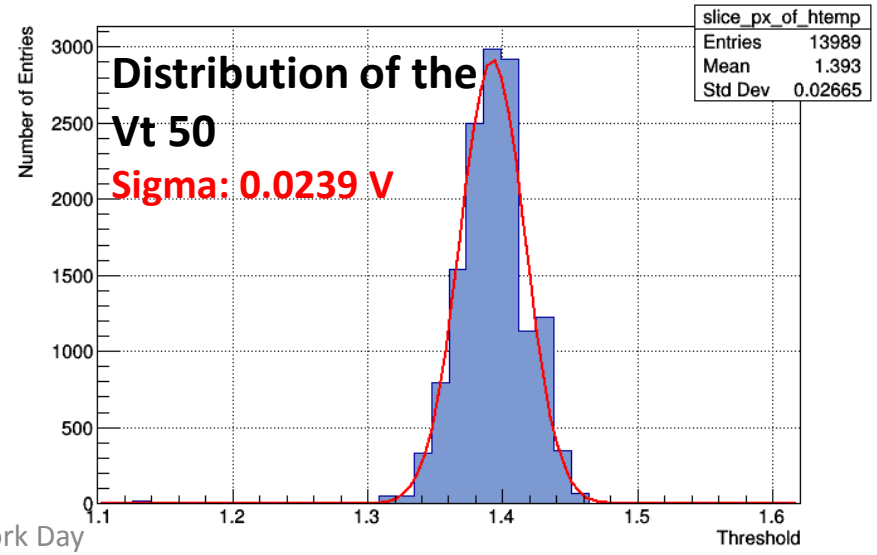


Threshold scan of #2

- Threshold scan of one pixel
  - Varies TDAC
  - Trimming to be done
- Threshold scan of one row
  - Distribution of Vt50

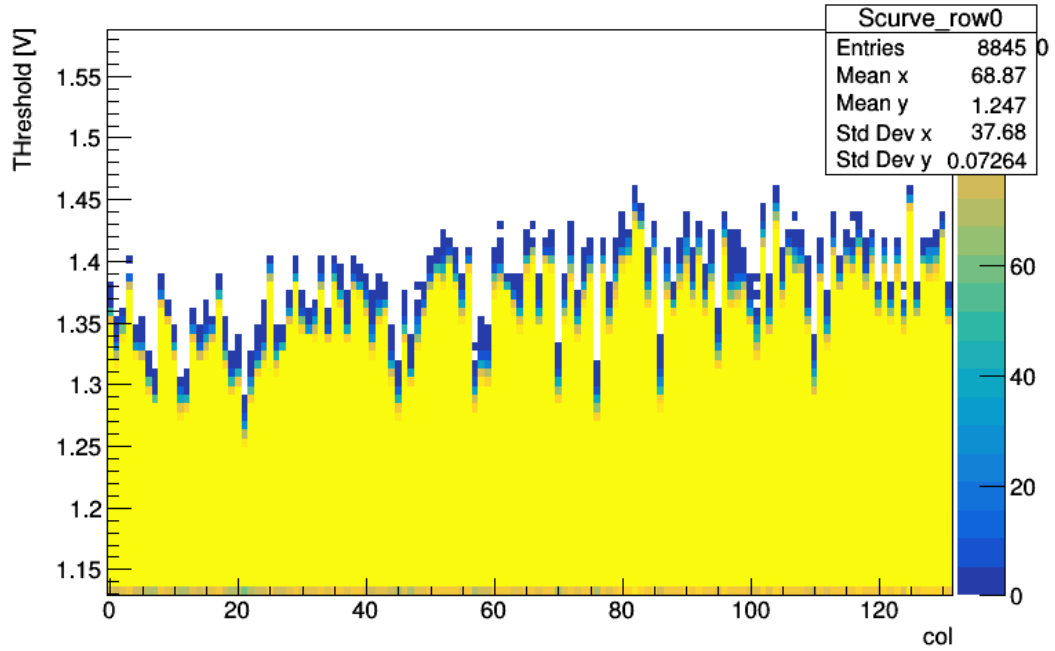


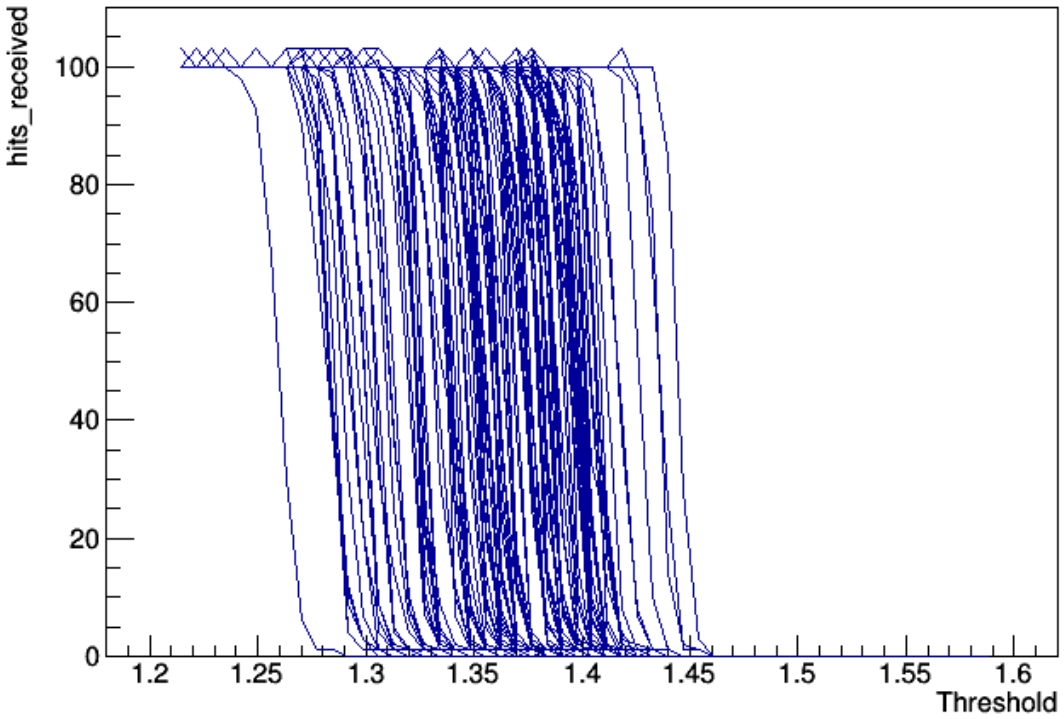




Threshold scan of #5

- Threshold scan of one row





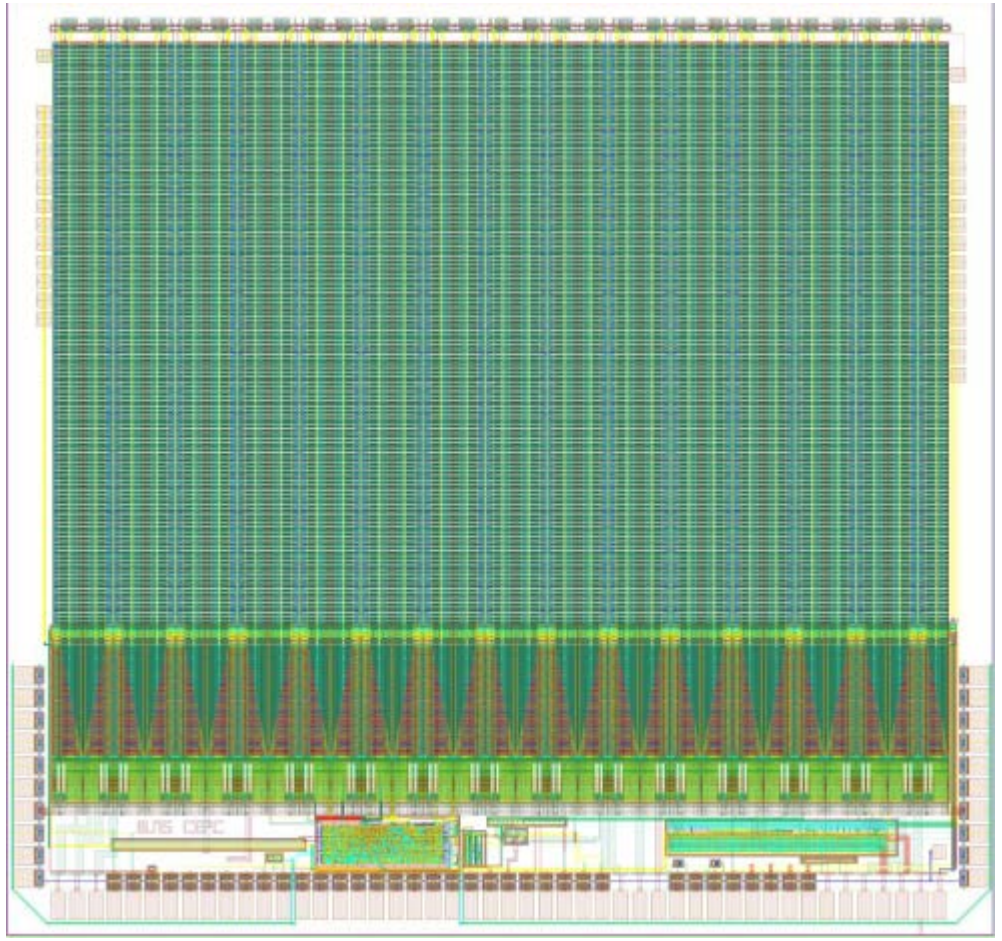
Sensor development

➢**Complete ATLASPix3 characterization with laser and radioactive source tests**

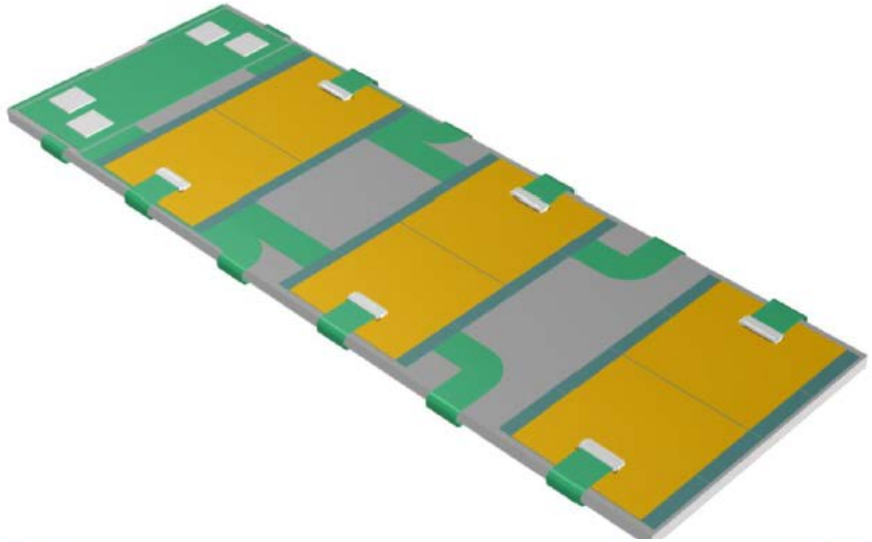
➢Sensor design towards the CEPC tracker

- Sensor design (CEPCPix: smaller pixel size 25 × 160 μm²) for CEPC under preparation
- Switch to Chinese foundry (under discussion)

MoU with KIT to be signed



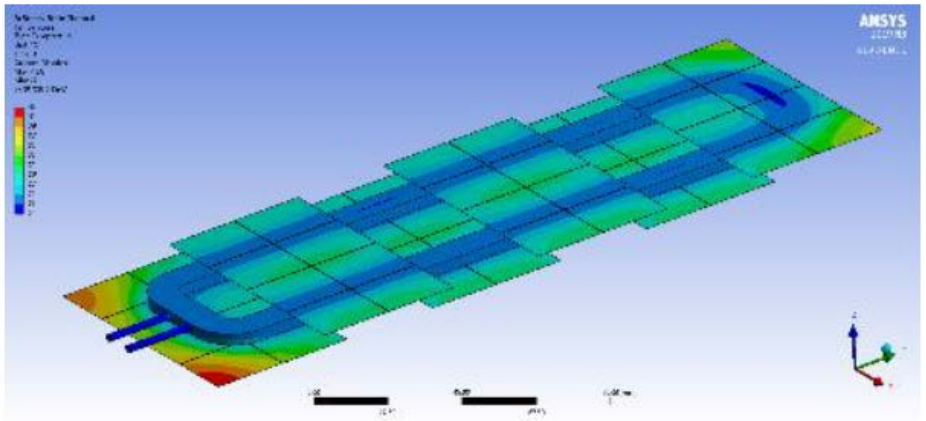
Demonstrator project



➢**Build a short stave (stavelet) to verify the concept and system design**

➢**Stavelet demonstrator** (12 QuadModules) design under optimization

- **Detector element** consisting of multiple modules on low mass composite support
- Water cooling proposed and used in thermal analysis

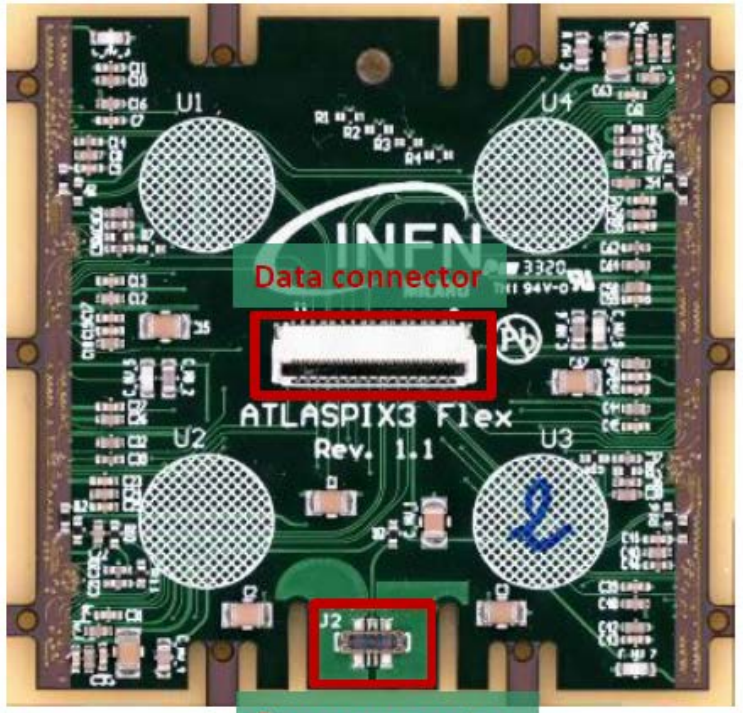


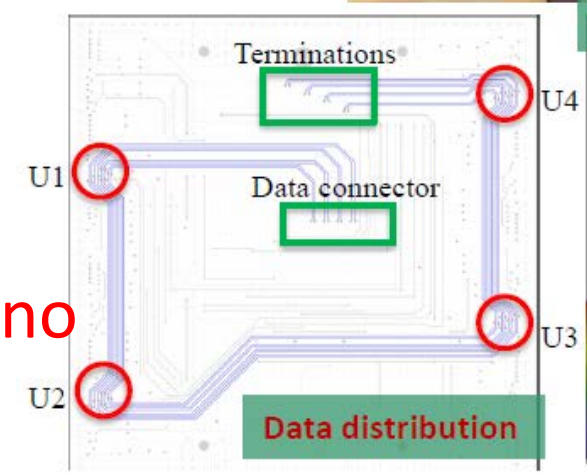
QuadModule

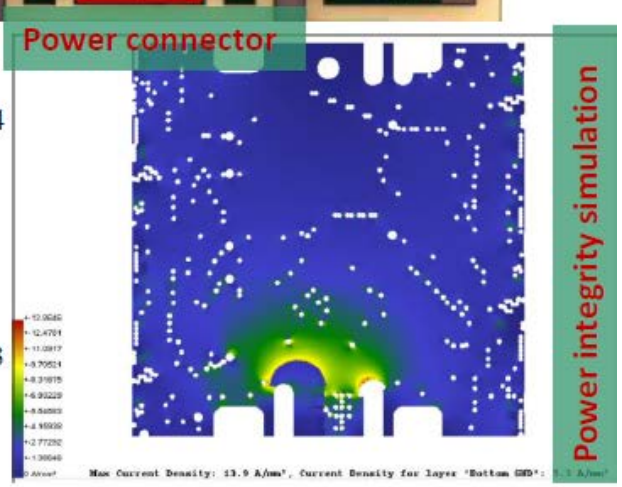
- Design concept from ATLAS ITk pixel

- **QuadModule design**: readout unit based on 4 ATLASPix3 chips
  - Shared services among **4 sensors** by common power connections and configuration lines
  - Benefits of in-chip regulators to reduce connections
  - Avoids complications with stitching

- QuadModule flex being tested @ Milano



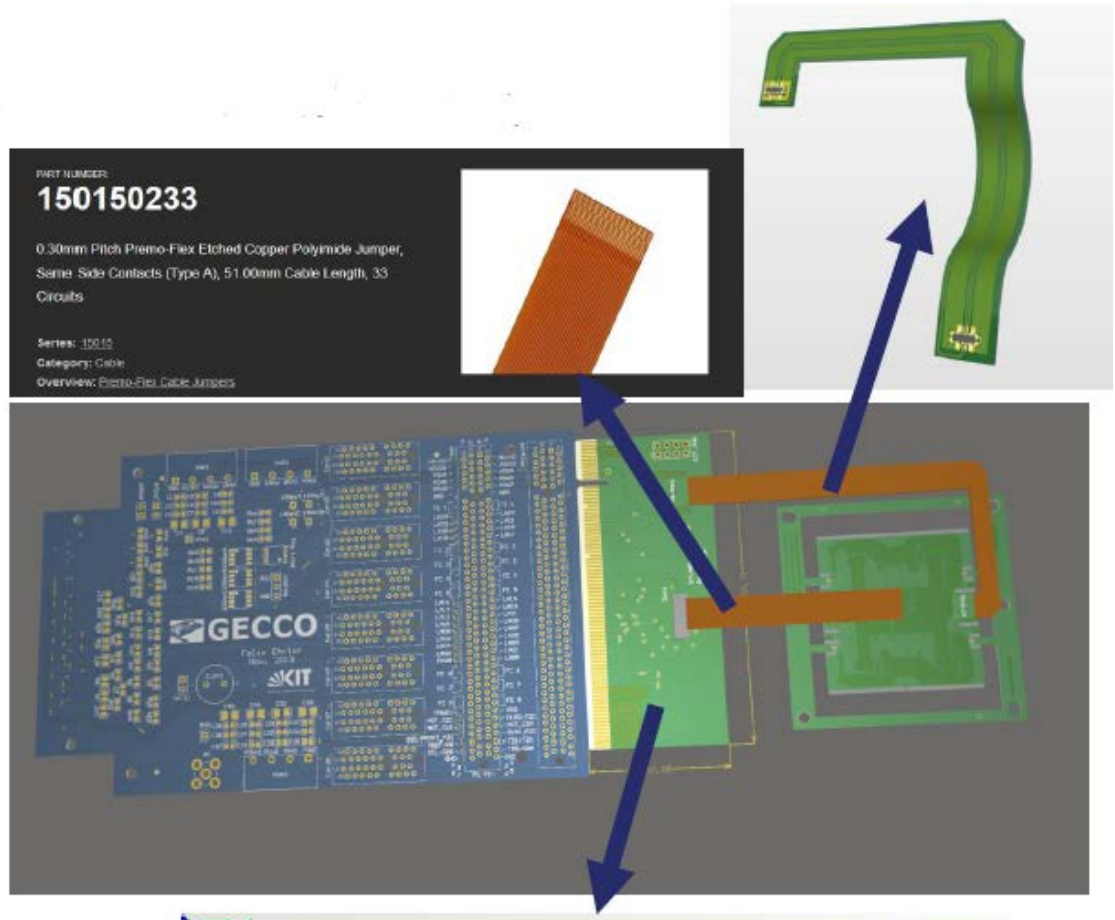


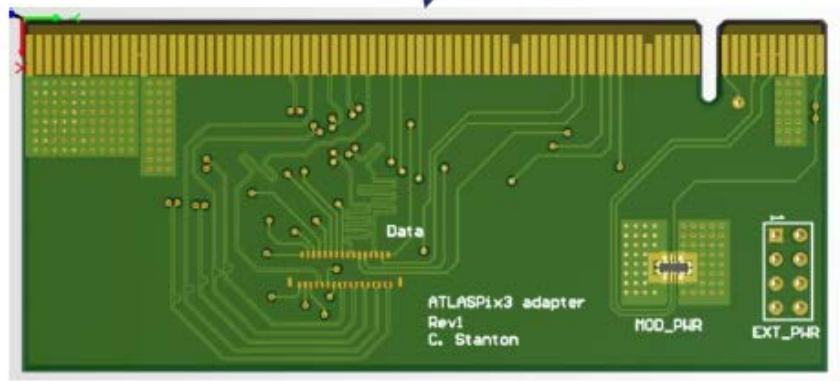


Adaptor Card

- Quad Module interfacing to GECCO

- Connection to GECCO system
  - **Adapter Card** (design completed)
  - Commercial data pigtail
  - Custom power pigtail

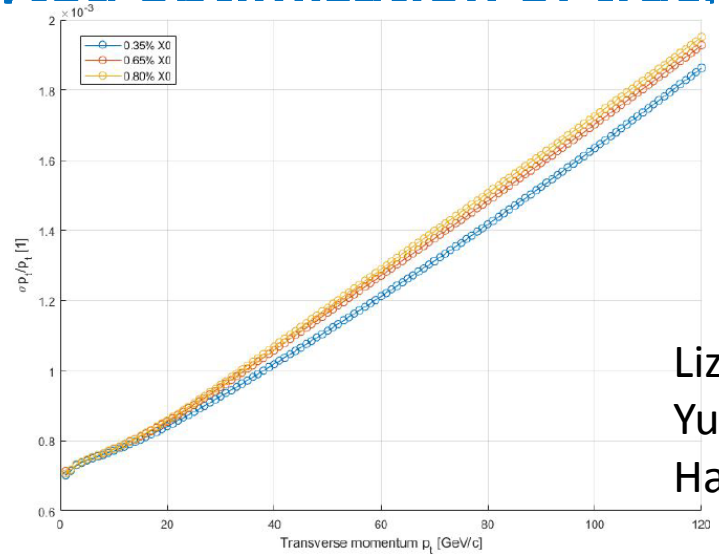




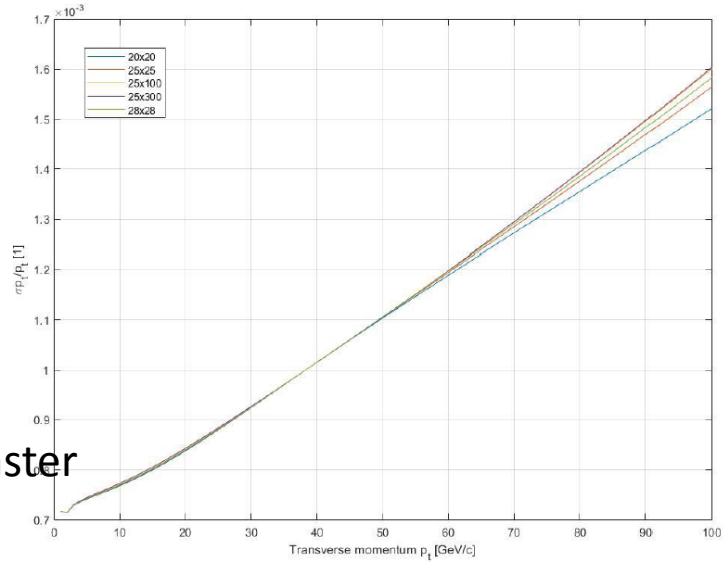
Design completed @ Edinburgh

Tracker layout optimization +software

- **Tracker geometry implemented in ACTS (Track Reconstruction Software)**
- **Started optimization of tracker layout with LDT**



Lizi Hutchinson
Yubin Zhong
Harald Fox @ Lacaster

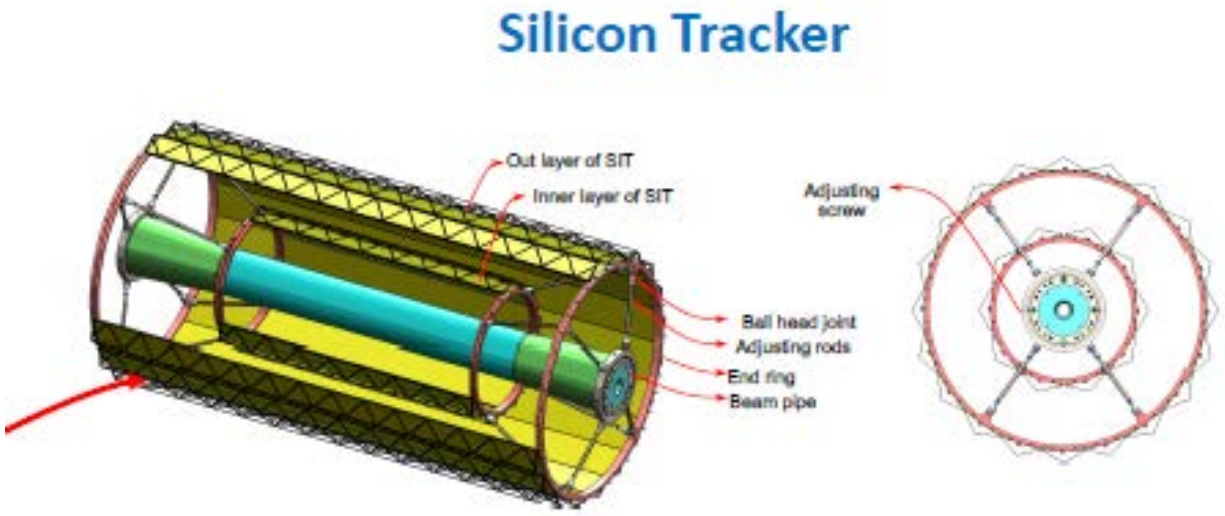


- Important to coordinate the layout optimization of the Vertex/Tracker as a whole system

Mechanical Design

➢Light weighted support structure (stave core)

- Design inspired by ALICE/ATLAS truss structure, longer extension, higher rigidity and stability (challenging to align detector elements with less tracks)



Integrated into the detector design

Summary

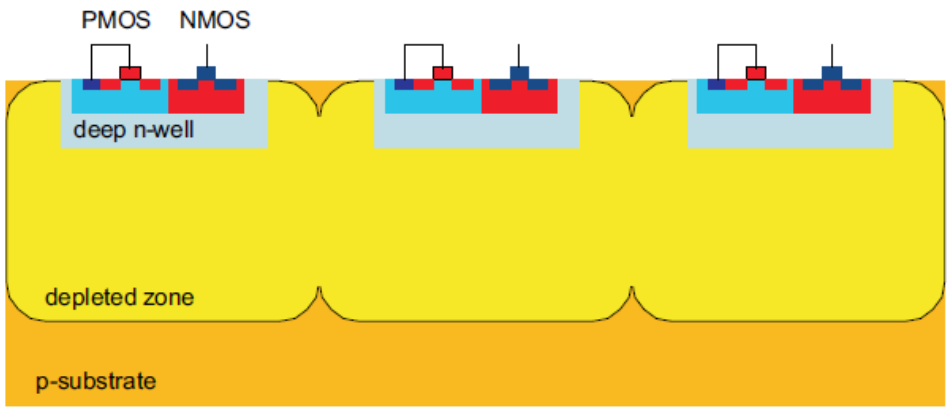
- **International collaboration group on CEPC Silicon Tracker**

- Ongoing activities including
  - **ATLASPix3** characterization
  - **Demonstrator** design/development
  - **layout optimization**
  - **Mechanical design**

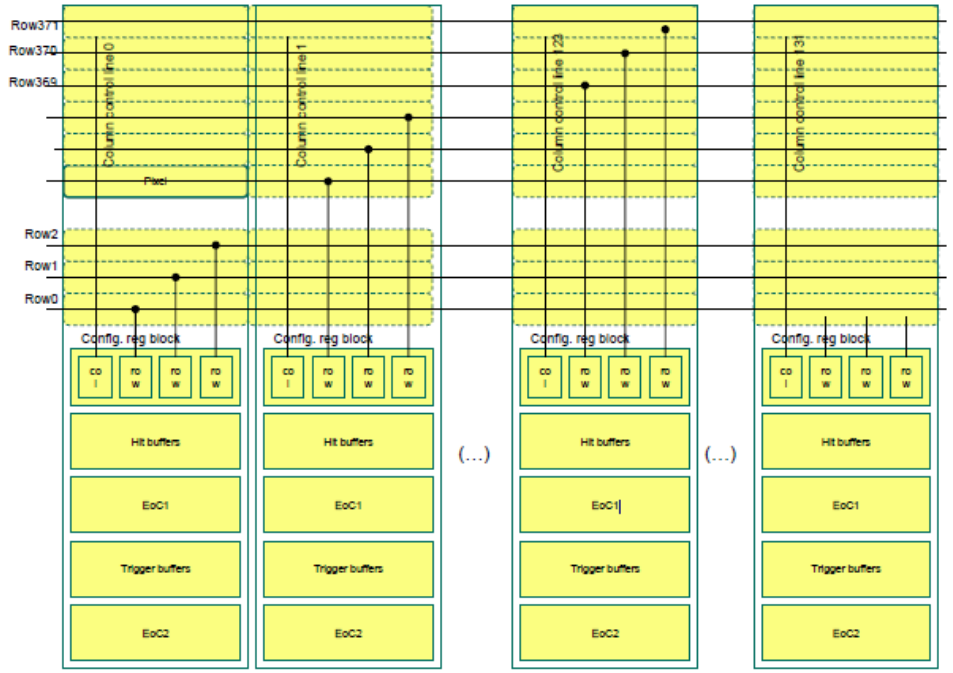
Thanks

Backup: ATLASPix3

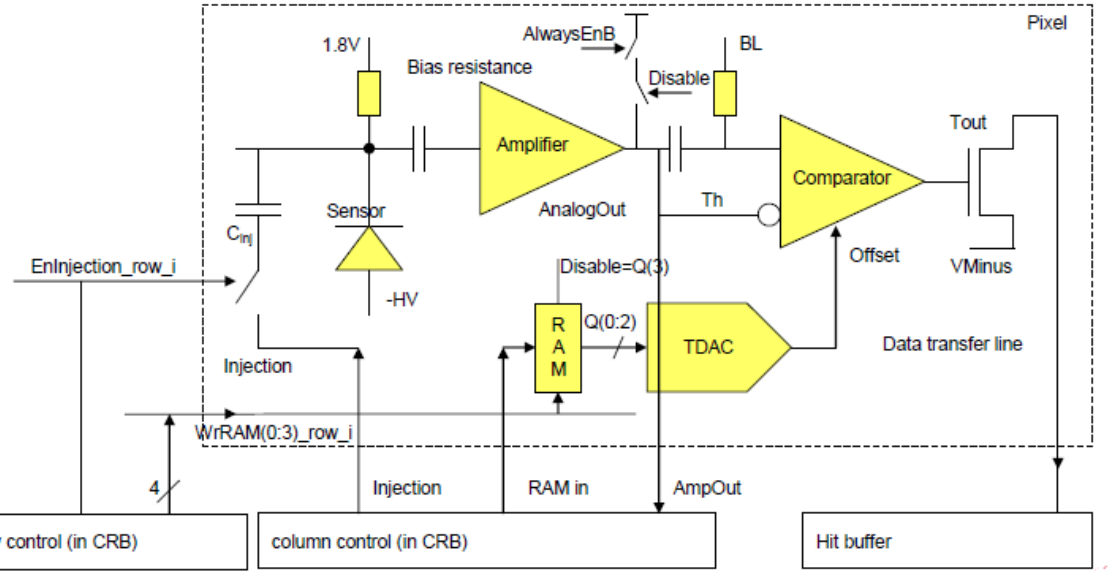
HV-CMOS structure



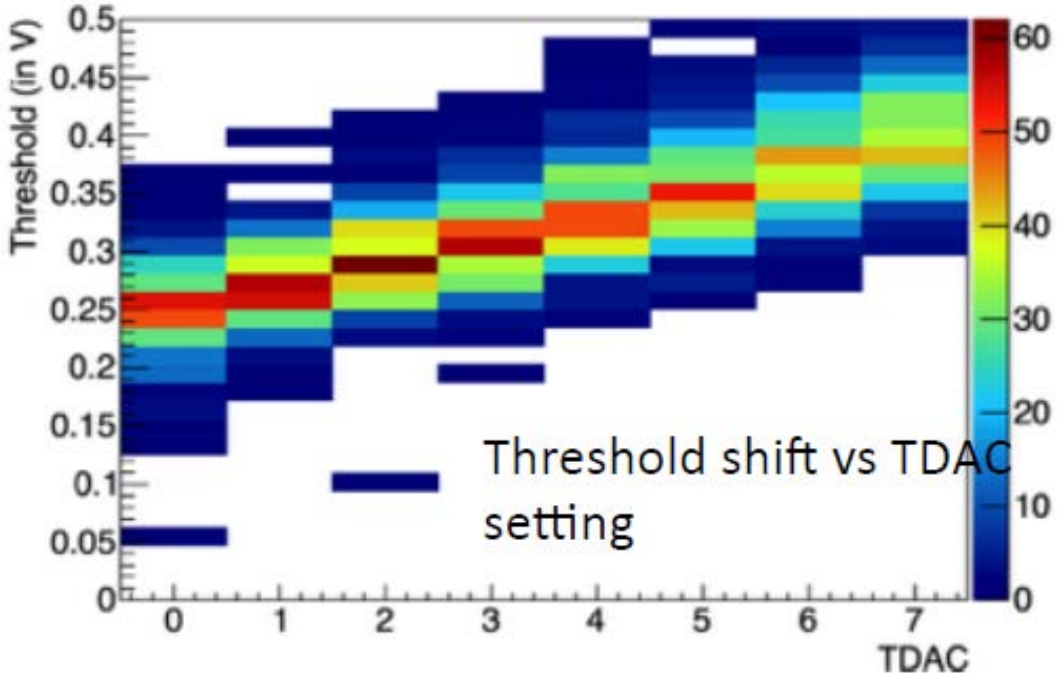
Block scheme of the pixel matrix and column circuits

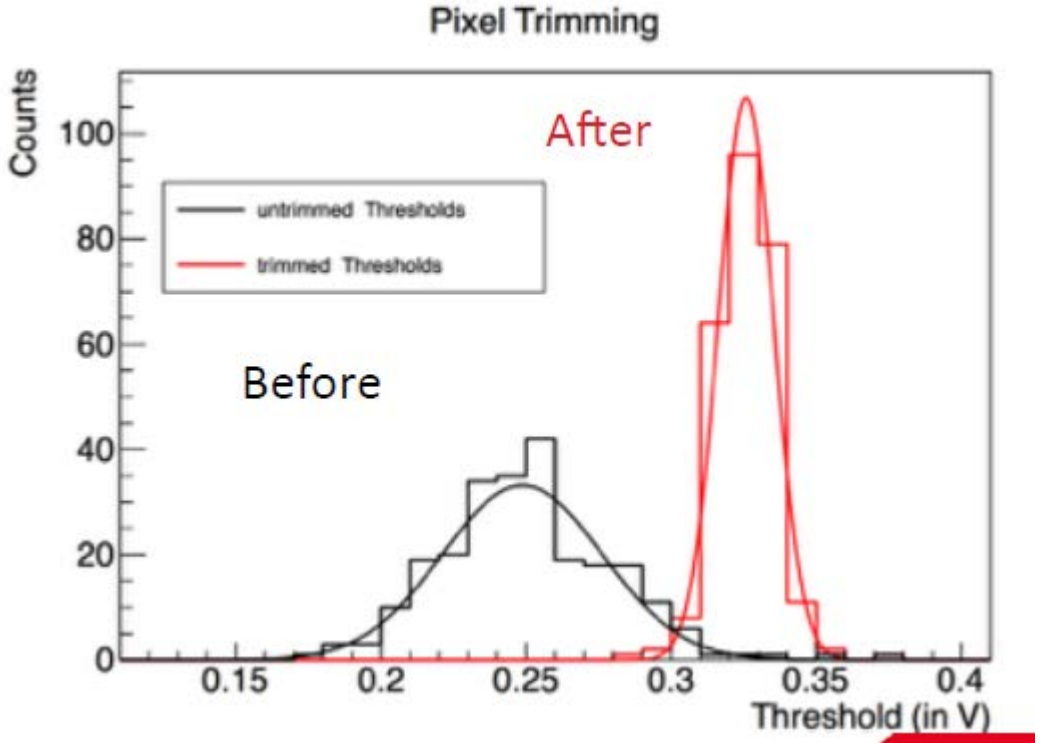


Pixel Schematics



backup

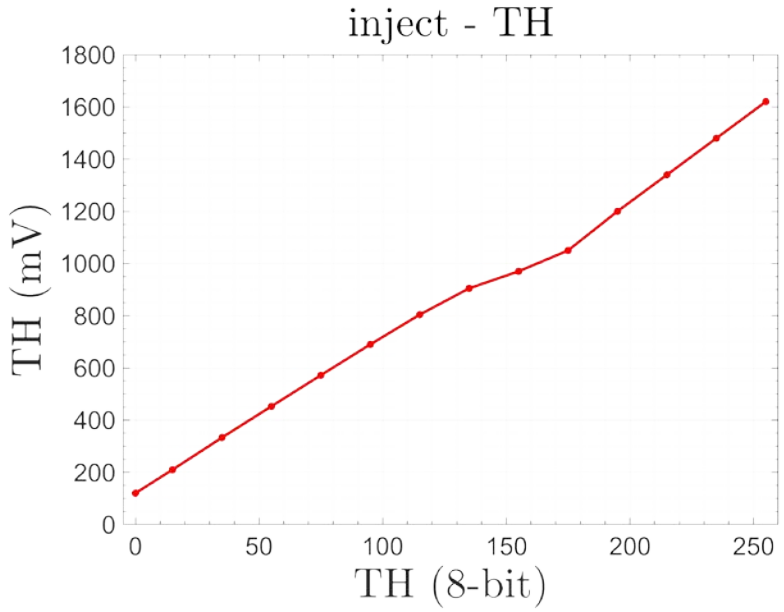

Threshold (in V)
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
0 1 2 3 4 5 6 7
TDAC
60
50
40
30
20
10
0
Threshold shift vs TDAC setting

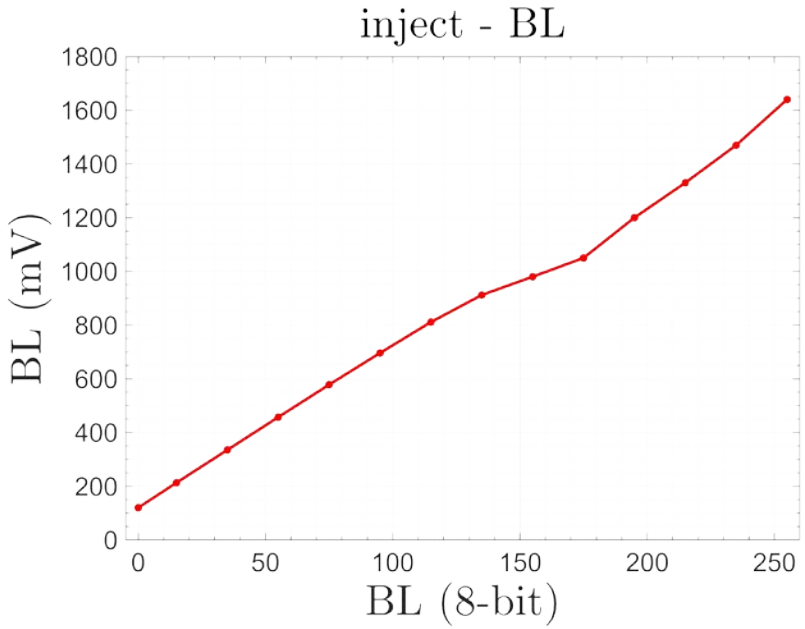

Pixel Trimming
Counts
100
80
60
40
20
0
untrimmed Thresholds
trimmed Thresholds
After
Before
0.15 0.2 0.25 0.3 0.35 0.4
Threshold (in V)

Activities and status

DAC linearity characterization (Milano)

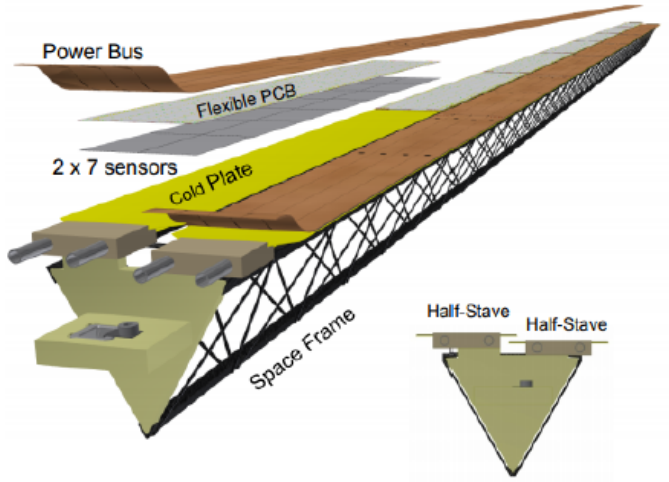
- Threshold, Baseline, Injection pulse
- Ampout, ToT



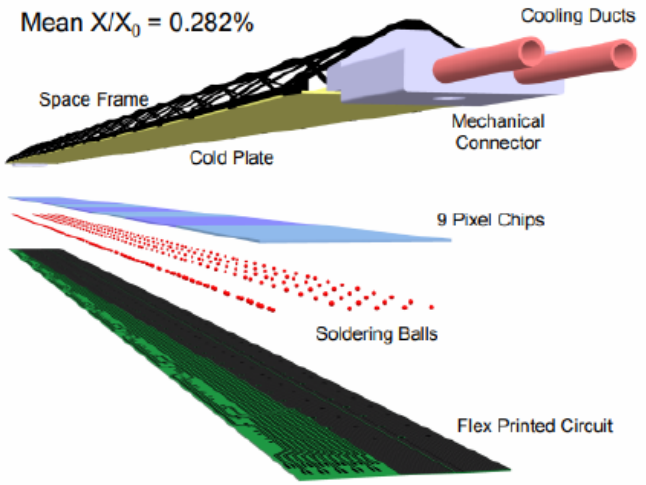


Supporting Structure

ALICE Outer Layer Stave ~0.8% X_0

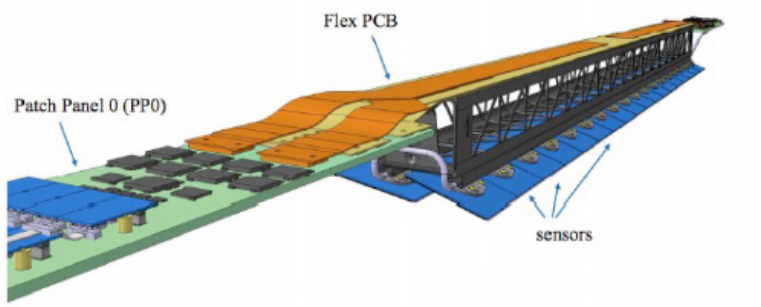


ALICE Inner Layer Stave ~0.3% X_0



ATLAS-ITK: 0.5% X_0 ITK alpine stave (+module)

ATLAS IBL: 0.7% X_0 IBL stave, (+module)



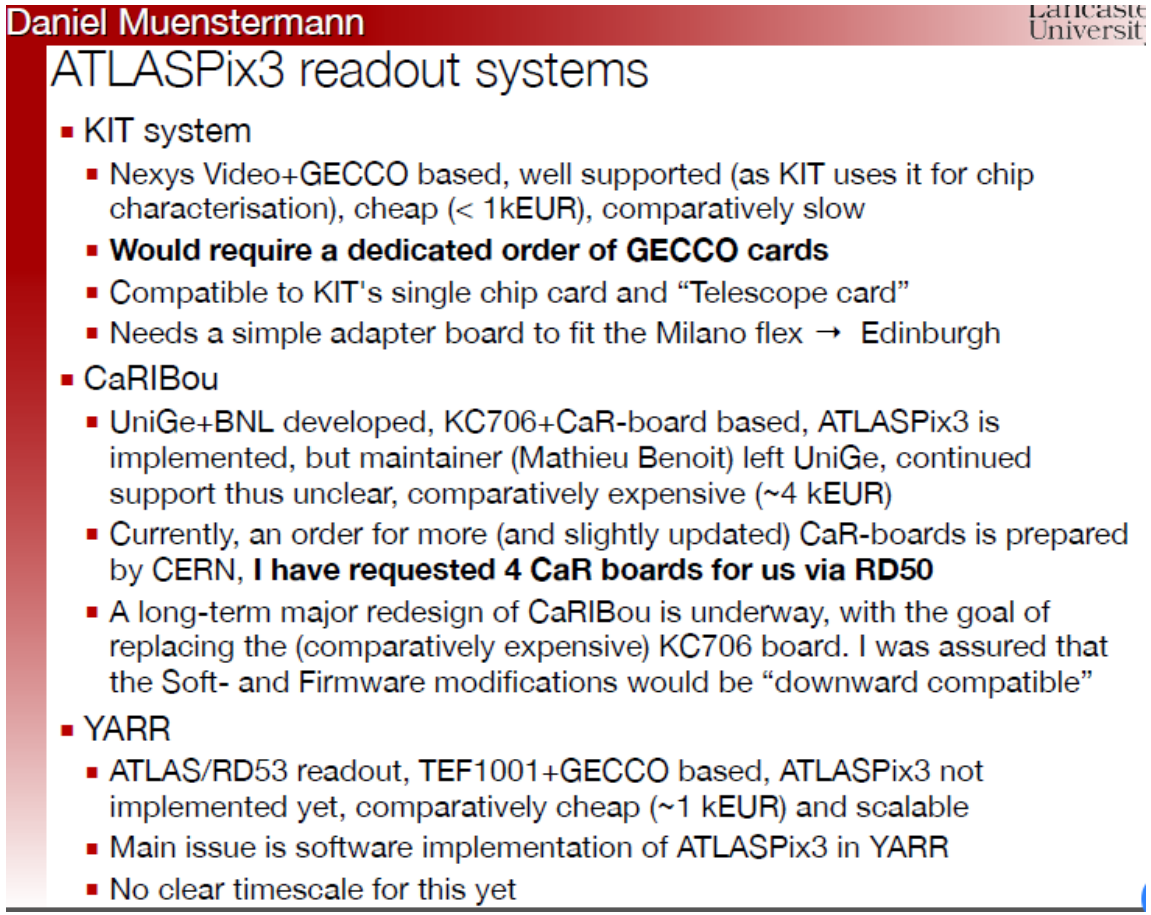
CEPC design target:

0.65% X_0 for stave + modules

Crucial elements:

- Light-weighted carbon truss structure
- Al based flex (prototype with Cu)

Readout systems



Sensor distribution

ATLASPix3: Readout

- **Digital Part(10% total area):**
  - configuration registers
  - hit buffer for each pixel
  - Untriggered and triggered End of Column(EoCs)
  - Content addressable buffer(CAB)
  - Readout Control Unit(RCU main and auxiliary)
- Hit information from one pixel transmitted to the hit buffer through long routing metal lines
- HitBuffer stores the global time stamp(TS) and generate a hit word
- **Triggered and Triggerless readout**
  - Triggered: transferred to CAB where the hits are filtered based on a trigger signal
  - Triggerless: transferred to EOC for untriggered readout