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TaichuPix-2 test results

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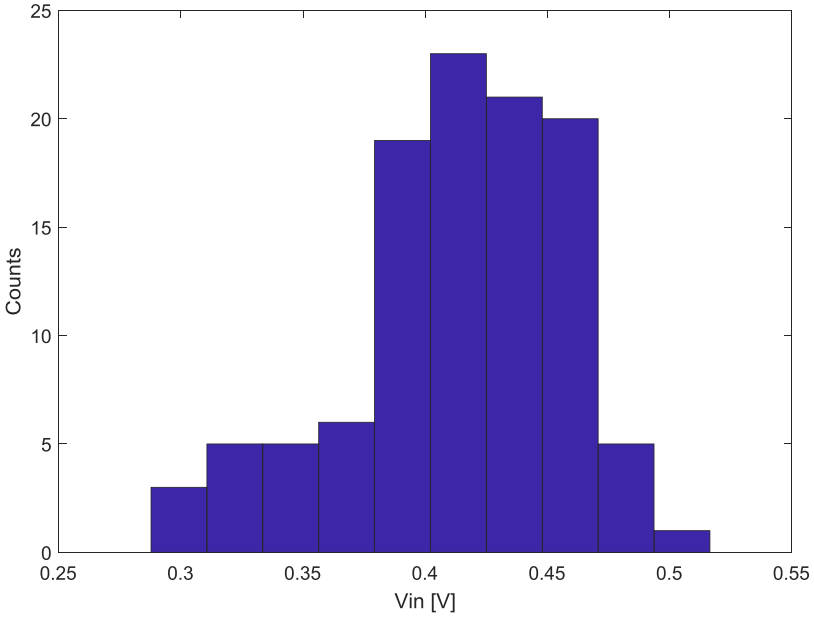
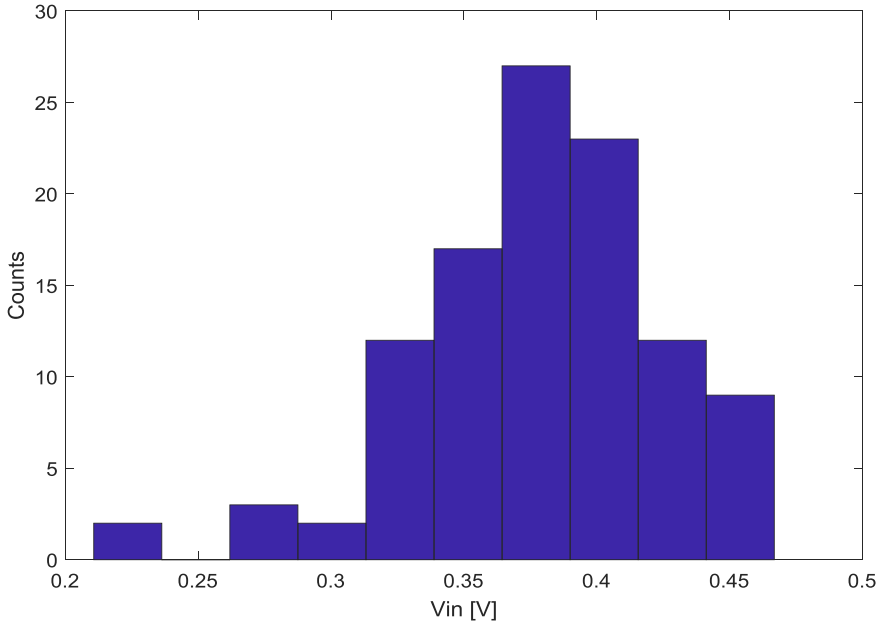
Pixel analog threshold

- **S-curve scanning for one double column, with one pixel enable every time**

Column 2 in sector 1

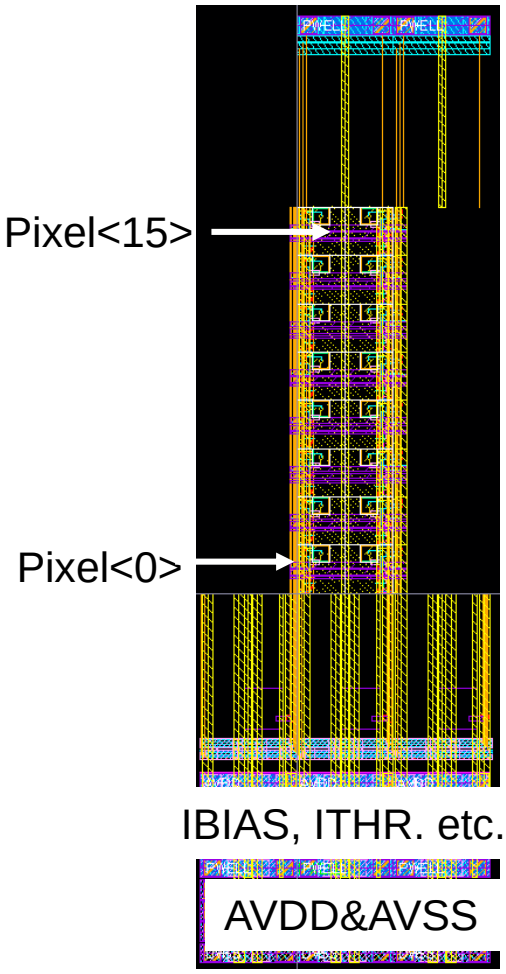


Column 2 in sector 2

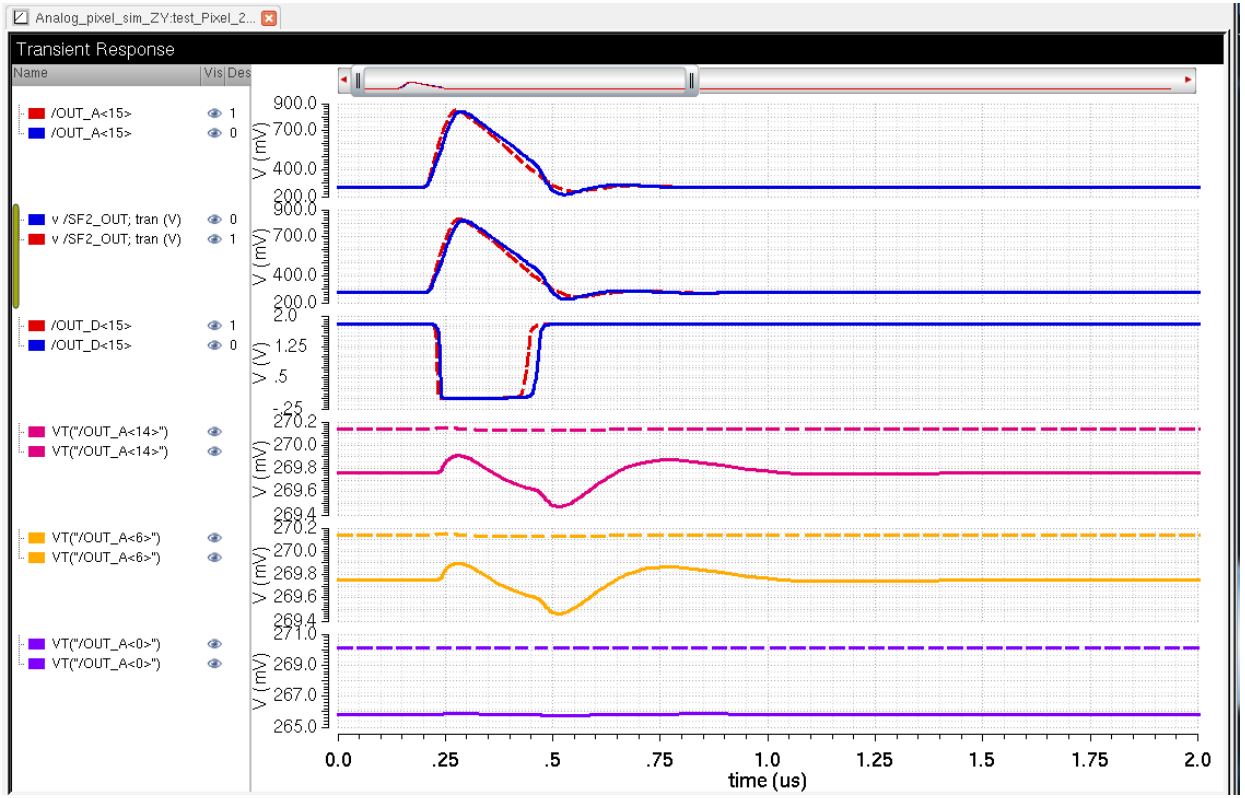


Effect of IR-Drop on power

- **2x8 pixels (include only analog part) modeled with power & bias bus routed as in TC2**



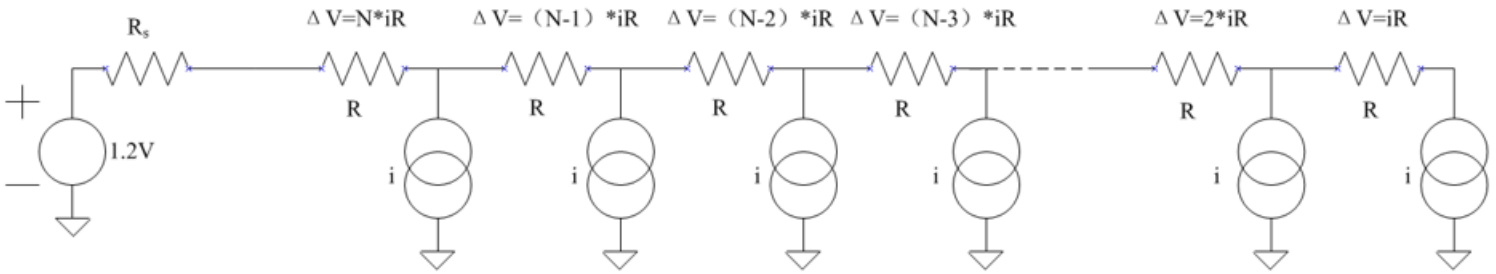
Simulation with schematic and caliber -RCC view for pixel<15>



Results show slight difference, no IR-drop effect observed

Effect of IR-Drop on power

- **IR-drop evaluation, assuming**
  - Each pixel consumes same current
  - R is the parasitic resistance, from one pixel to the next one along the power line



  - The largest IR Drop: $\Sigma_{\Delta V} = (1+2+\cdots N)*iR$
    $= N(N+1)*iR/2$

  - Extract the point-to-point parasitic resistance on the layout by PEX

    R_{avdd}= 3.4 ohm/pixel; R_{avss}= 2.8 ohm/pixel;

  ➔ $\Delta V\mathrm{max} = 23\ \mathrm{mV}$

Effect of IR-Drop on power

- **Simulation with one pixel, AVDD = 1.8 V & 1.77 V**

Outputs Setup | Results | Diagnostics

Detail | Append

Test	Output	Nominal	Spec	Weight	Pass/Fail
Analog_pixel_sim_ZY:sim_Front-End_mpw2:1	Vsig	580.7m			
Analog_pixel_sim_ZY:sim_Front-End_mpw2:1	Qin(e)	400			
Analog_pixel_sim_ZY:sim_Front-End_mpw2:1	Peaking time	75.39n			
Analog_pixel_sim_ZY:sim_Front-End_mpw2:1	Duration	211.2n			
Analog_pixel_sim_ZY:sim_Front-End_mpw2:1	Delay of leading edge	31n			
Analog_pixel_sim_ZY:sim_Front-End_mpw2:1	/PIX_IN				
Analog_pixel_sim_ZY:sim_Front-End_mpw2:1	/OUT_A				
Analog_pixel_sim_ZY:sim_Front-End_mpw2:1	/OUT_D				
Analog_pixel_sim_ZY:sim_Front-End_mpw2:1	/I20/PLUS				
Analog_pixel_sim_ZY:sim_Front-End_mpw2:1	CVF	1.452m			
Analog_pixel_sim_ZY:sim_Front-End_mpw2:1	v /SF1_OUT; tran (V)				
Analog_pixel_sim_ZY:sim_Front-End_mpw2:1	v /SF2_OUT; tran (V)				
Analog_pixel_sim_ZY:sim_Front-End_mpw2:1	Vsig_SF2	552.7m			
Analog_pixel_sim_ZY:sim_Front-End_mpw2:1	Vsig_SF1	567.3m			
Analog_pixel_sim_ZY:sim_Front-End_mpw2:1	SF_Gain(percent)	95.17			

AVDD =1.8 V

AVDD =1.77 V

agnostics

Append

Test	Output	Nominal	Spec	Weight	Pass/Fail
Analog_pixel_sim_ZY:sim_Front-End_mpw2:1	Vsig	575.8m			
Analog_pixel_sim_ZY:sim_Front-End_mpw2:1	Qin(e)	400			
Analog_pixel_sim_ZY:sim_Front-End_mpw2:1	Peaking time	78.77n			
Analog_pixel_sim_ZY:sim_Front-End_mpw2:1	Duration	209.2n			
Analog_pixel_sim_ZY:sim_Front-End_mpw2:1	Delay of leading edge	31.04n			
Analog_pixel_sim_ZY:sim_Front-End_mpw2:1	/PIX_IN				
Analog_pixel_sim_ZY:sim_Front-End_mpw2:1	/OUT_A				
Analog_pixel_sim_ZY:sim_Front-End_mpw2:1	/OUT_D				
Analog_pixel_sim_ZY:sim_Front-End_mpw2:1	/I20/PLUS				
Analog_pixel_sim_ZY:sim_Front-End_mpw2:1	CVF	1.44m			
Analog_pixel_sim_ZY:sim_Front-End_mpw2:1	v /SF1_OUT; tran (V)				
Analog_pixel_sim_ZY:sim_Front-End_mpw2:1	v /SF2_OUT; tran (V)				
Analog_pixel_sim_ZY:sim_Front-End_mpw2:1	Vsig_SF2	548.4m			
Analog_pixel_sim_ZY:sim_Front-End_mpw2:1	Vsig_SF1	563m			
Analog_pixel_sim_ZY:sim_Front-End_mpw2:1	SF_Gain(percent)	95.25			