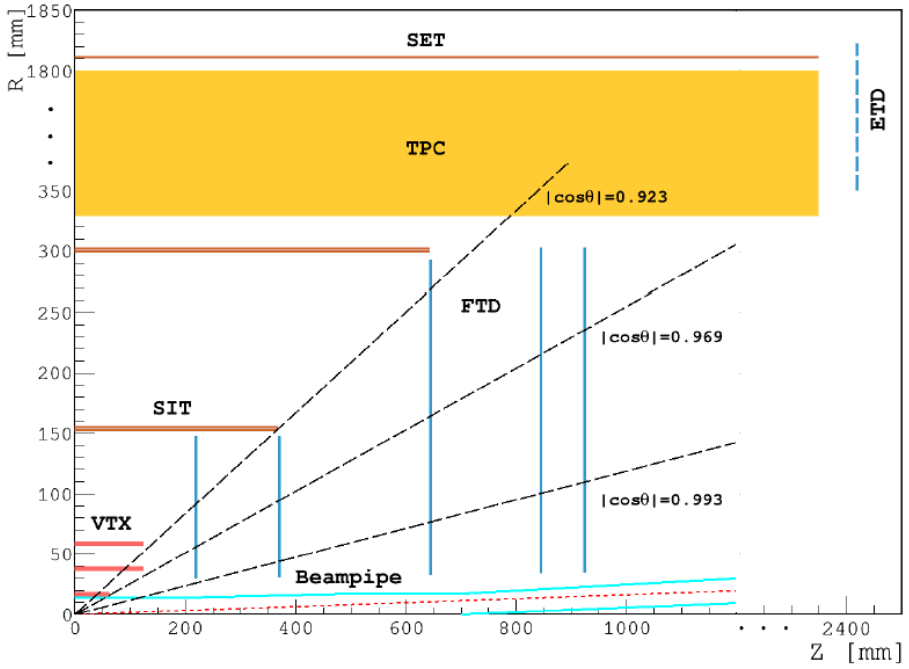
Bench test of the ATLASPix3 at IHEP

Silicon Tracker working group

Outline

- Background and Introduction to ATLASPix3
- Activities going on @IHEP
- Summary and outlook

Backgrounds



➢ CEPC Baseline tracker

- Mixed Tracker (TPC + Silicon)
  - 3 layers, 5 disks of silicon sensors
  - Large area (50 m² if built in pixels) to be covered
- Limited R&D time
- Comparable requirements with ATLAS/ALICE
  - Bunch spacing, material budget, spatial resolution …
  - Plenty of experience to learn from

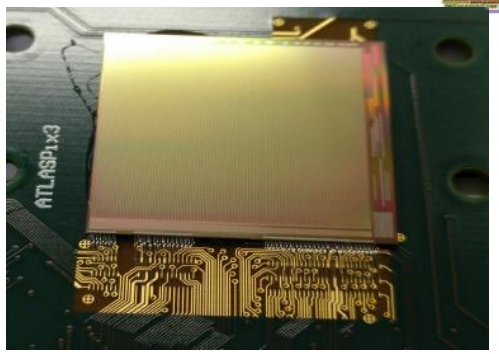
➢ ATLASPix/ATLASPix3

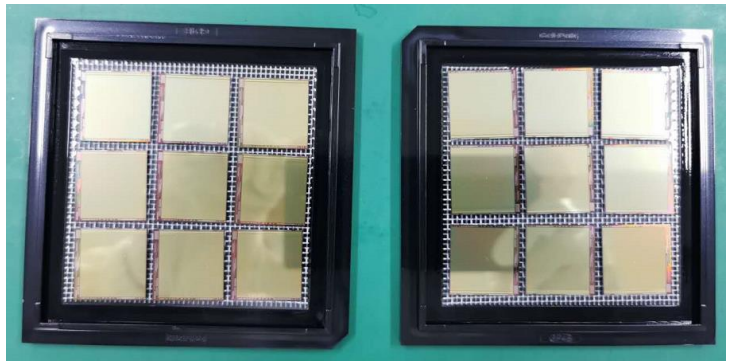
- A CMOS sensor developed to fulfill the requirement for the ATLAS ITK outer layer upgrade
- Functional sensor available for prototyping Optimization for CEPC Tracker

Introduction to ATLASPix3

ATLASPix3

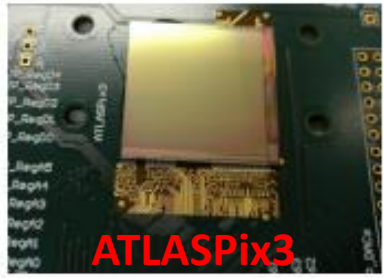
- HV-CMOS Monolithic chip
- Chip Size: 2.02 cm by 2.1 cm (Full reticule size)
- TSI 180 nm HV process on 200 Ω cm substrate
- 132 cols each contains 372 pixels(50 µm x 150 µm)
- Each Pixel :
  - Charge sensitive Amplifier
  - Comparator with threshold tune DAC
  - 4 bit RAM
- 1.25 GBit/s downlink
- Chips(18+1) arrived @IHEP ~ a month ago

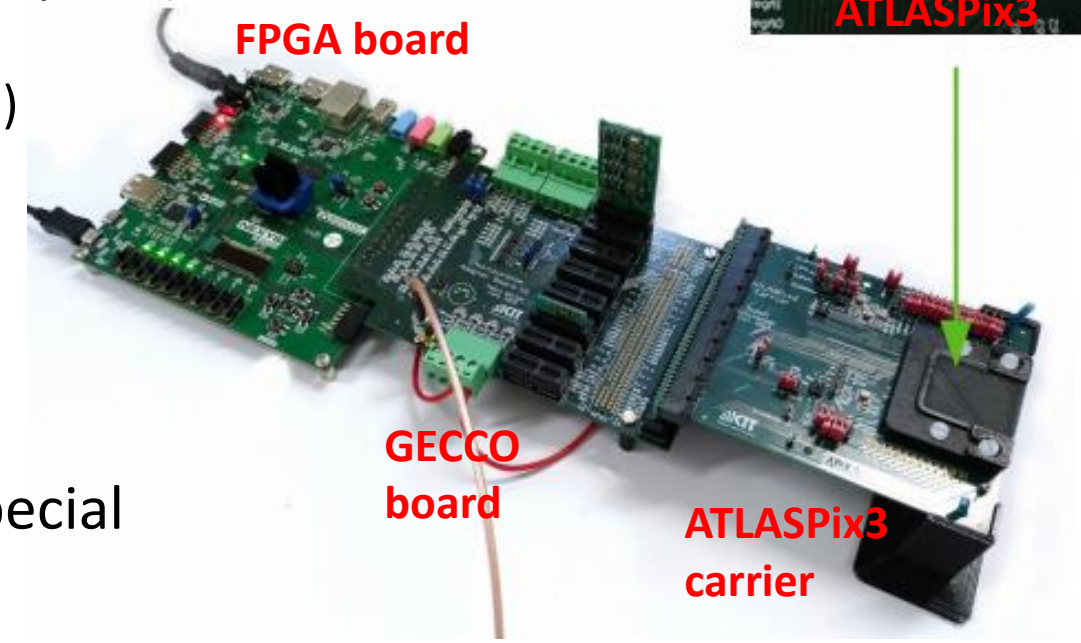


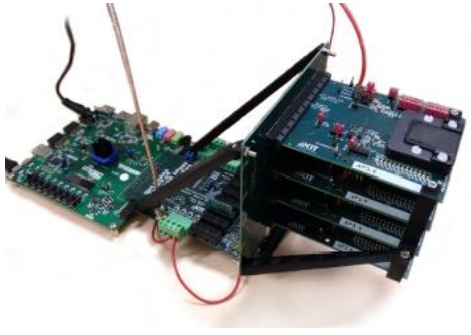


Introduction: Test setup

- Lab Measurement setup (developed by KIT)
  - Artrix-7 FPGA board
  - GECCO board(GEneric Configuration and COntrol system)
    - PCIe connector (with DUT)
    - Highly modular with function cards(versatile)
    - Easy changing of DUT sample (no cabling)
    - 90° Adapter
  - ATLASPix3 Carrier PCB
  - Firmware
  - Software(Qt based)
- ATLASPix3 Telescope setup (feasible using special structure)

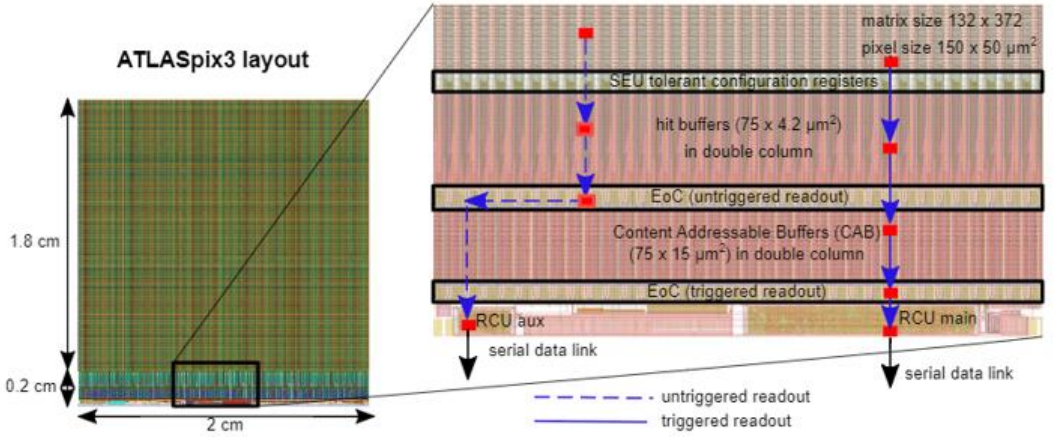


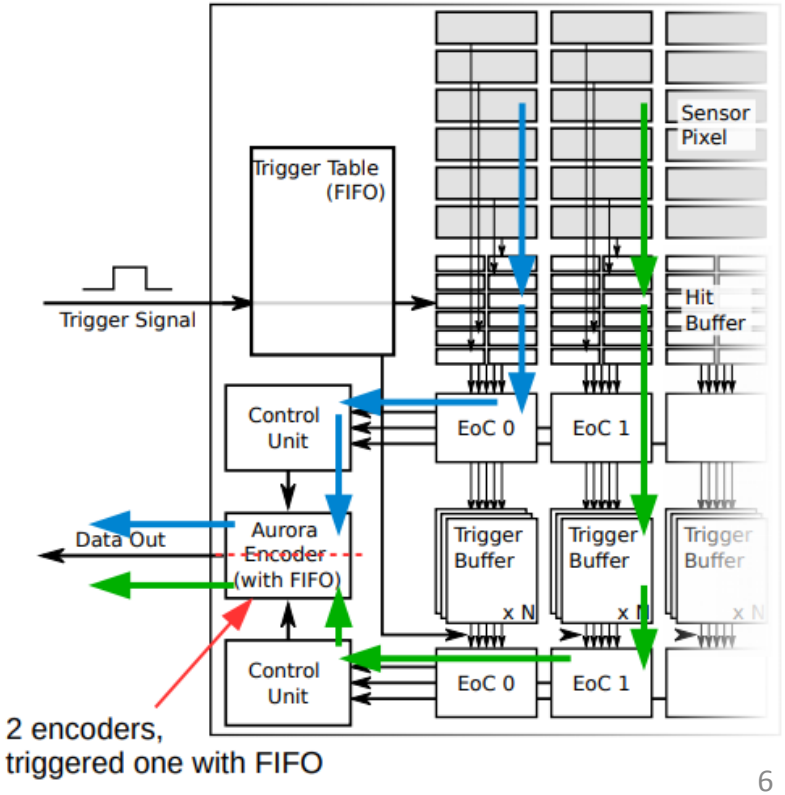




Introduction: Readout

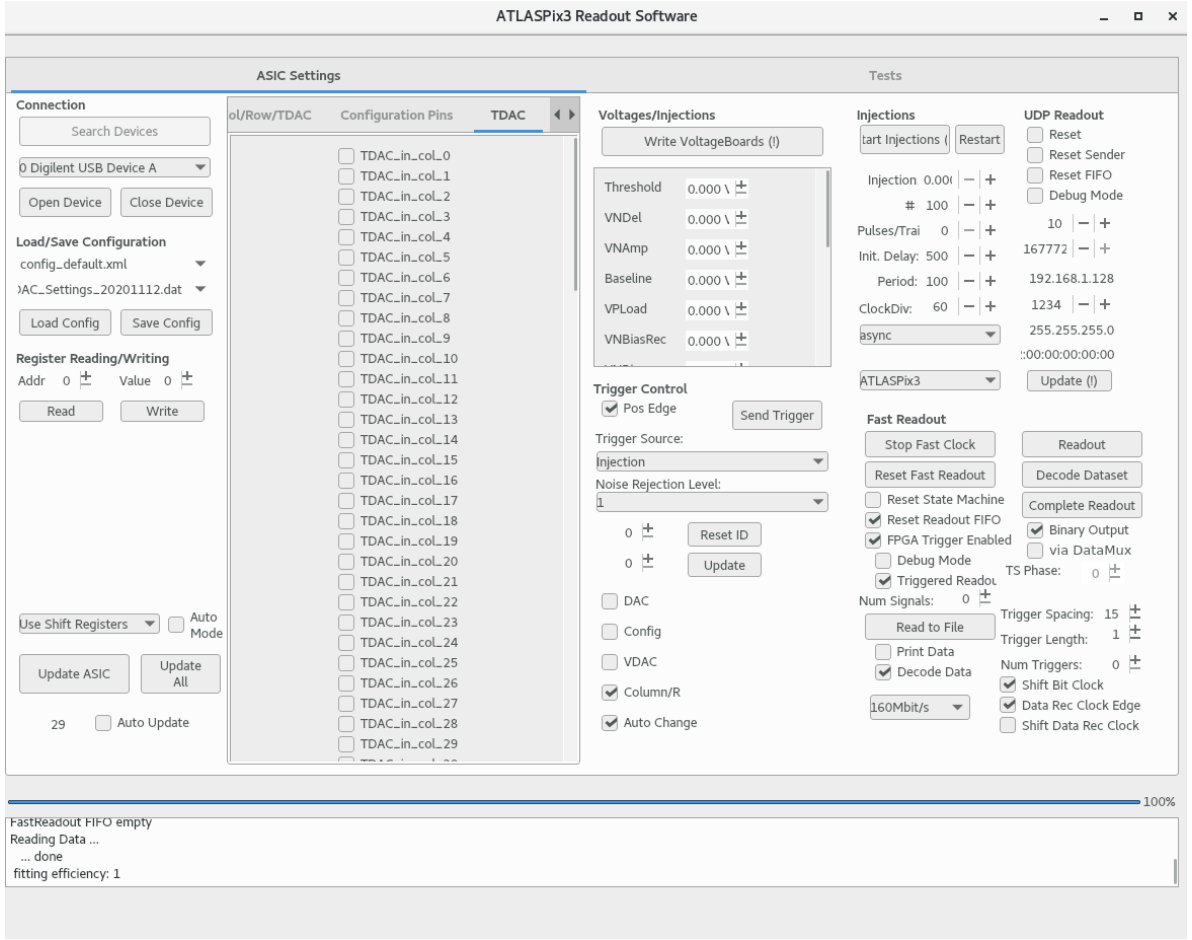
- Digital Part(10% total area):
  - configuration registers
  - hit buffer for each pixel
  - Untriggered and triggered End of Column(EoCs)
  - Content addressable buffer(CAB)
  - Readout Control Unit(RCU main and auxiliary)
- Hit information from one pixel transmitted to the hit buffer through long routing metal lines
- HitBuffer stores the global time stamp(TS) and generate a hit word(32 bit)
- Triggered and Triggerless readout
  - Triggered: transferred to CAB where the hits are filtered based on a trigger signal
  - Triggerless: transferred to EOC for untriggered readout





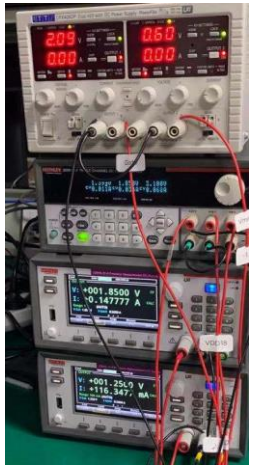
Introduction: DAQ software

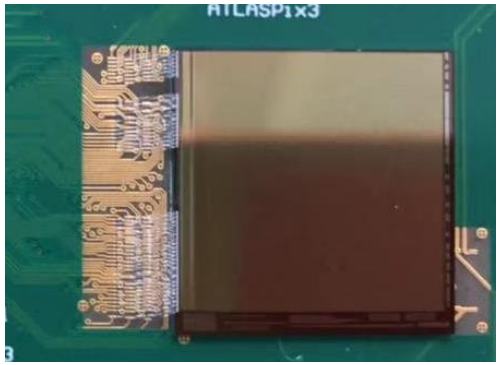
- Powerful DAQ software (KIT)
  - Using on ATLASPix3 testing since the end of 2019
  - Based on C++ with Qt framework
  - Graphical User Interface
  - Managing the Configurations for DUT and Firmware
  - Very helpful for system debugging
- It works

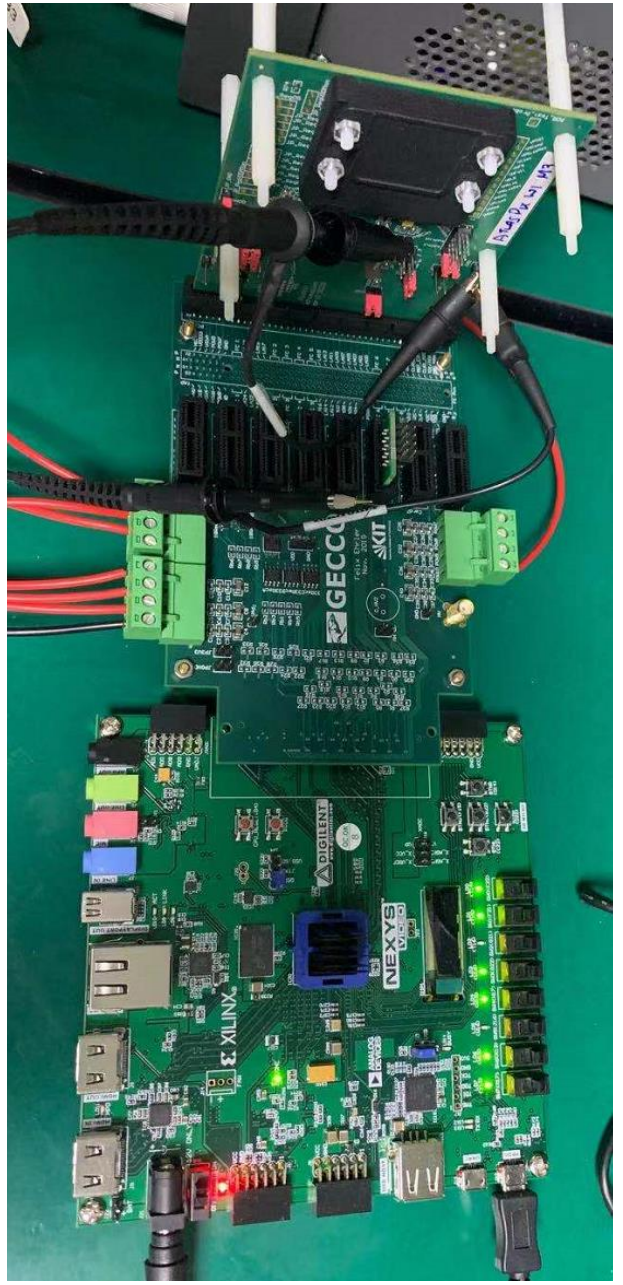


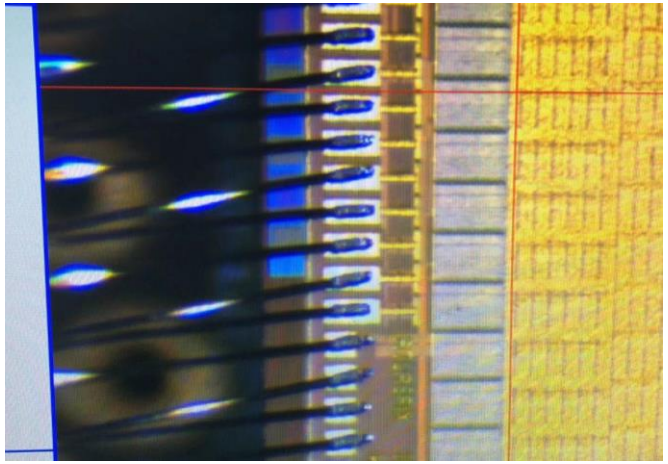
Activities and status

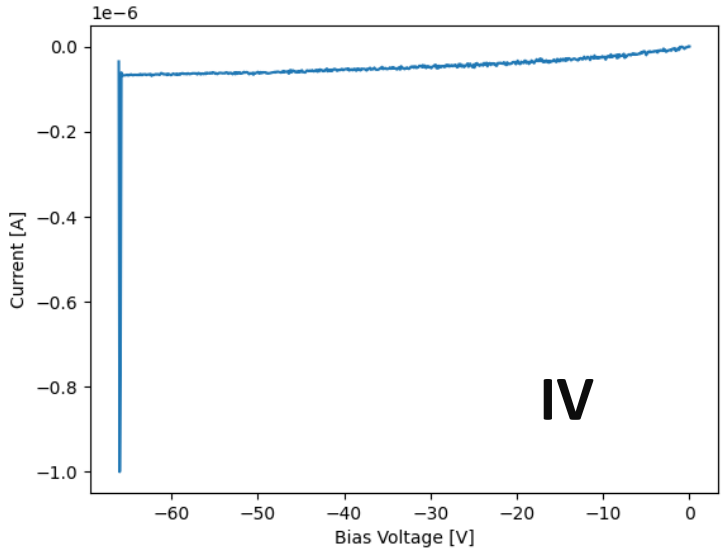
- Test system @IHEP (Tremendous help from Rudolf)
- Wired Bonded in IHEP clean room
  - 5 out of 6 bonded chips work
- Basic IV and analog output
  - Low leakage current of < 70 nA @ -60V





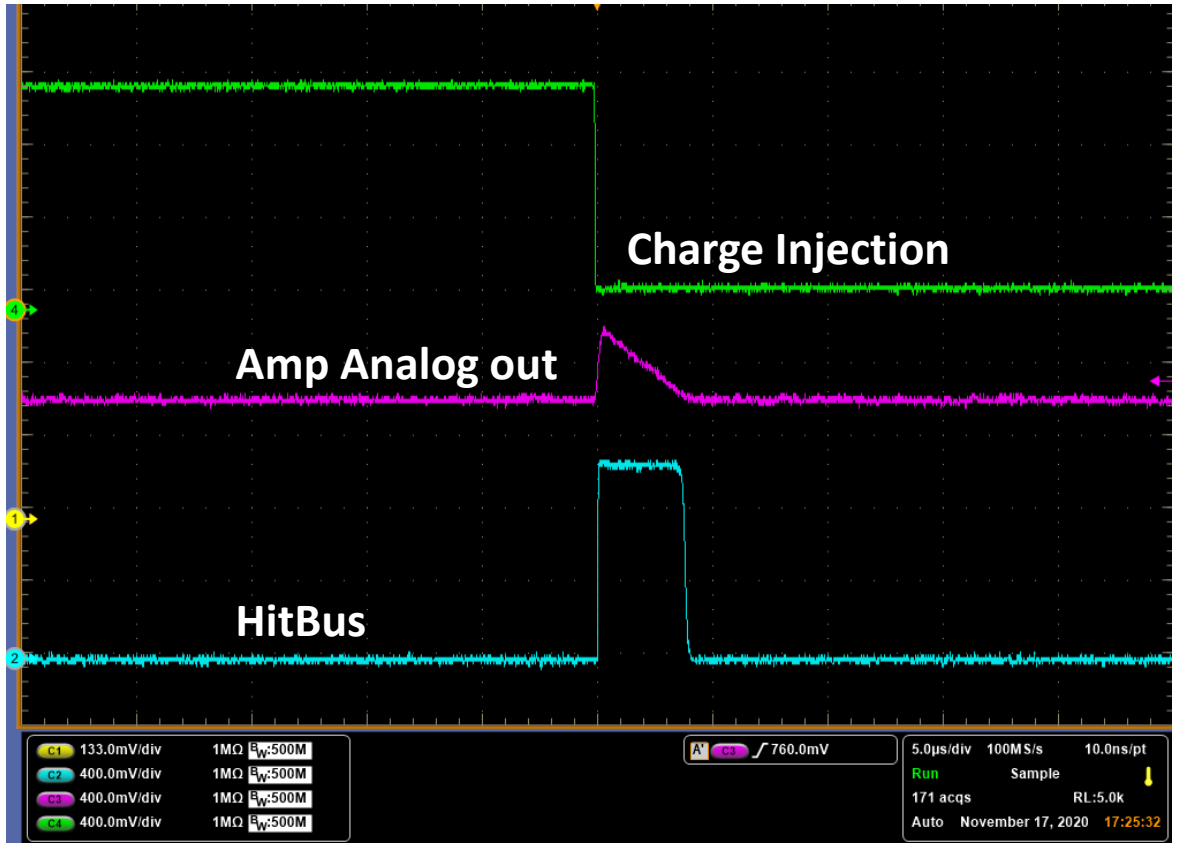






Activities and status

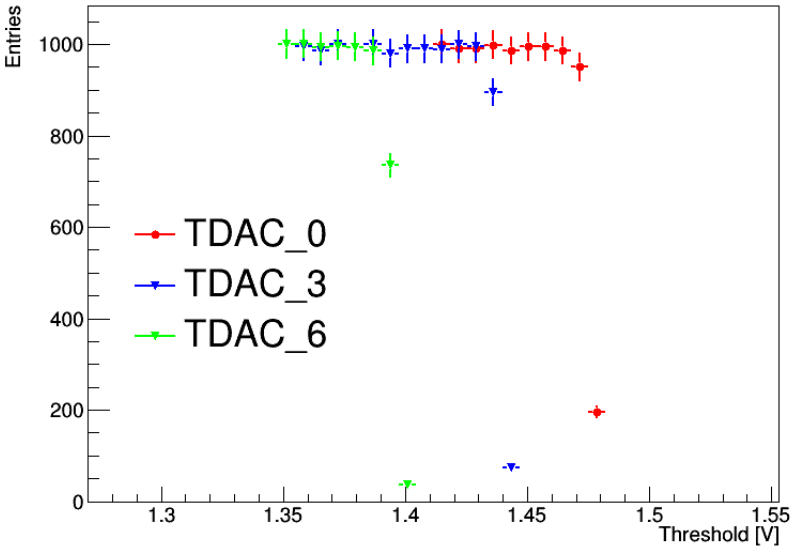
- Test system @IHEP
- Wired Bonded in IHEP clean room
  - 5 out of 6 bonded chips working
- Basic IV and analog output
- Decoding processes understood

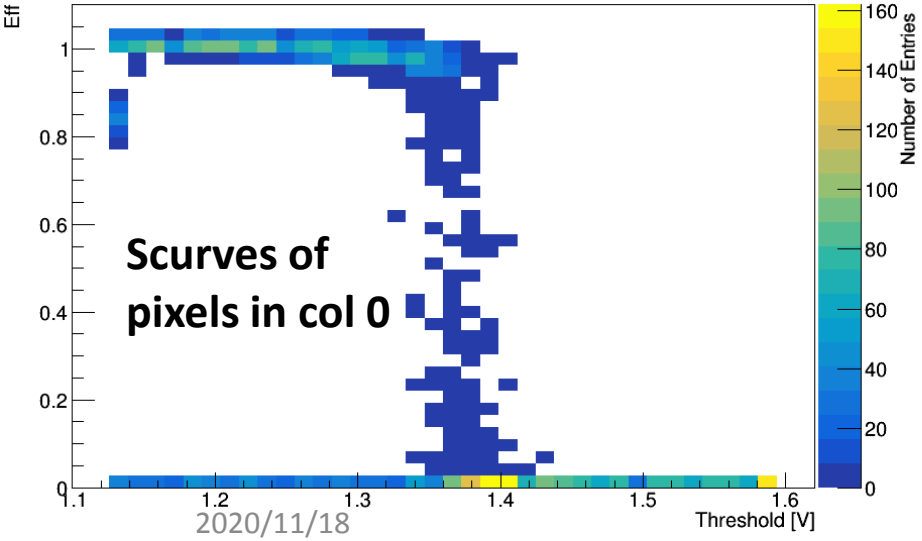


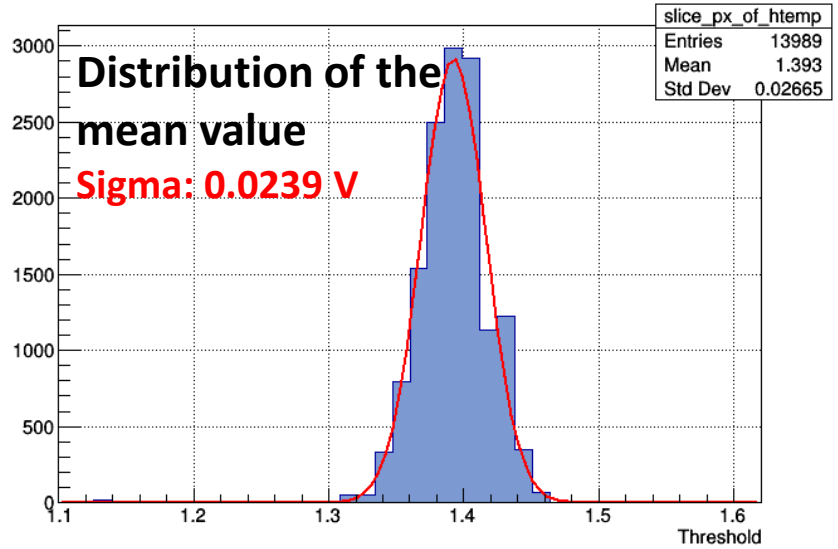
Activities and status

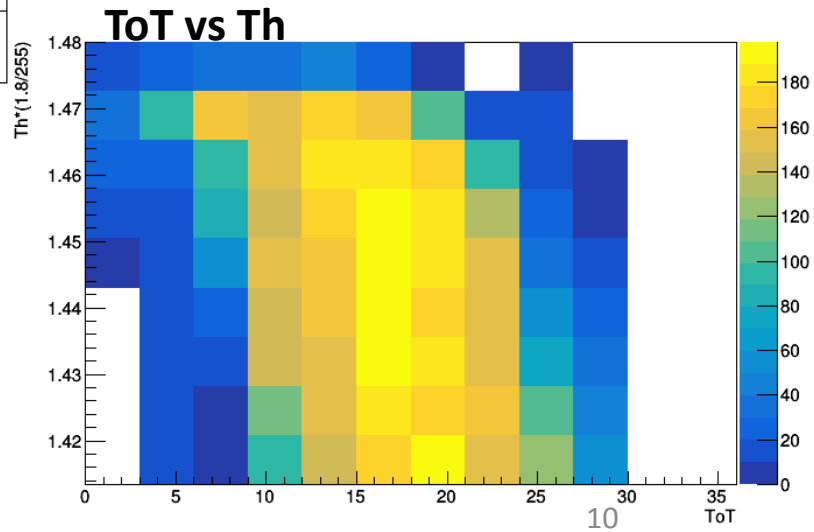
Tests with Triggered readout @IHEP

- Scurve for large area of pixels
  - Distribution of mean value (sigma: 0.0239 V)
- ToT vs Threshold
- Threshold scan (varies TDAC): Trimming to be done







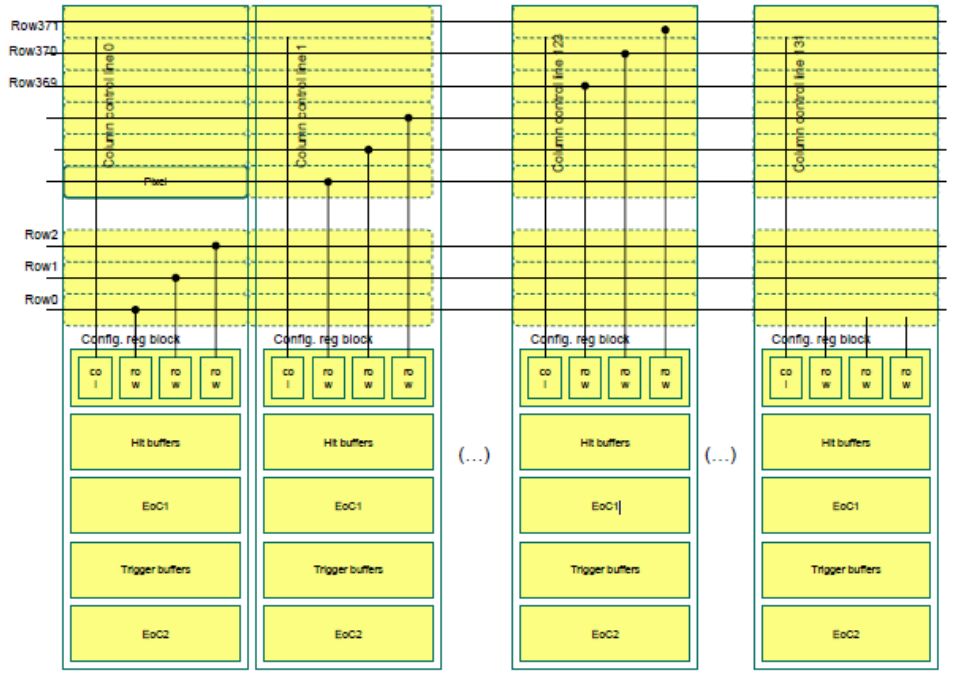


Summary and Outlook

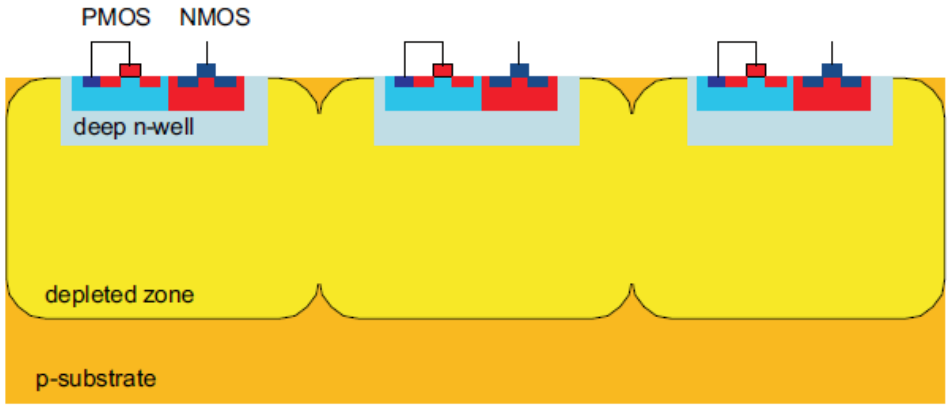
- ATLASPix3 chips arrived at IHEP last month
  - ✓ Wire bonding, Test setup, software
  - ✓ IV curve, Analog signal
  - ☐ Digital readout, SCurve, Trimming, ToTCalibration to be done very soon
- **Chips and System work**, configurations to be further fine tuned
- (future) Pixel sensor design optimization toward the CEPC tracker
  - QuardModule for the demonstrator being prepared @Milano
  - Sensor design (smaller pixel size 25×160 μm²) for CEPC under preparation
  - Switch to Chinese foundry (under discussion)

Backup: ATLASPix3

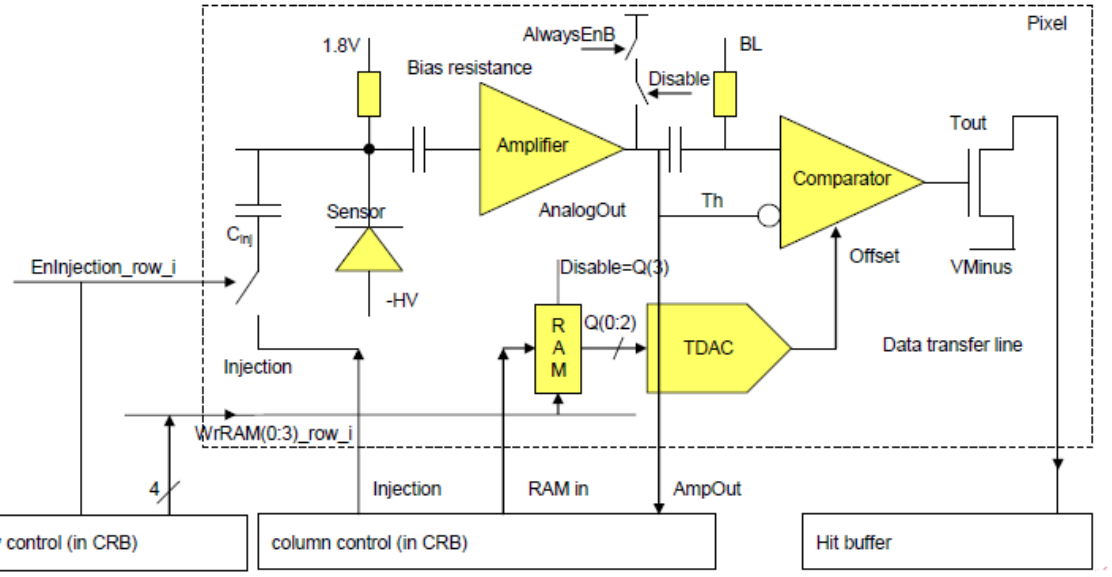
Block scheme of the pixel matrix and column circuits



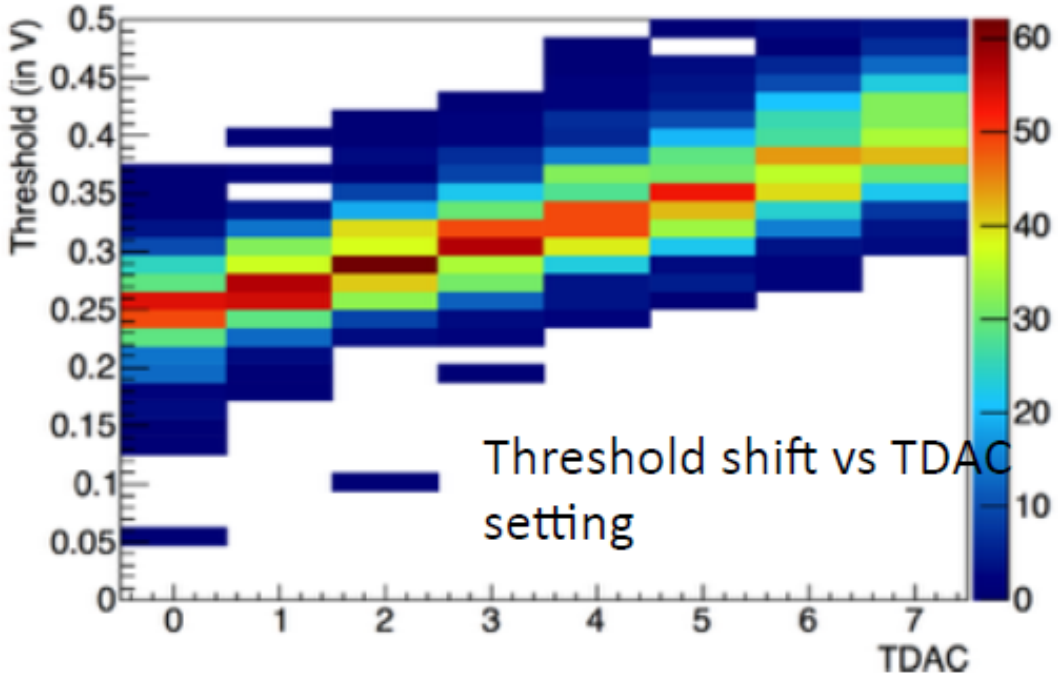
HV-CMOS structure

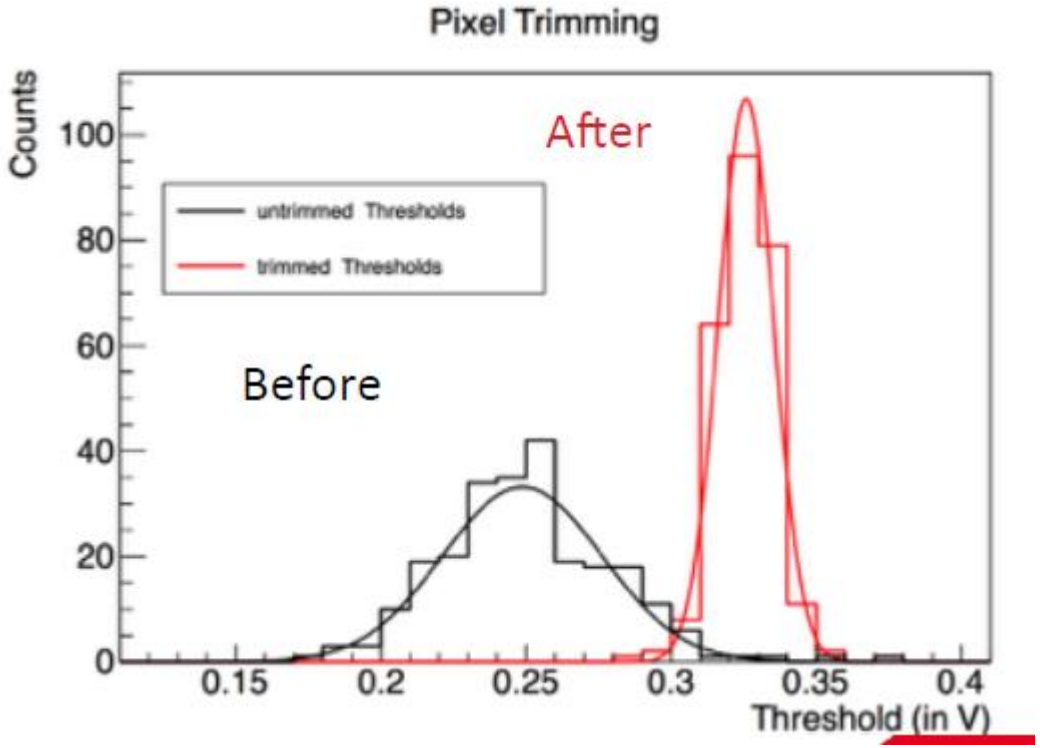


Pixel Schematics



backup


Threshold (in V)
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
0 1 2 3 4 5 6 7
TDAC
60
50
40
30
20
10
0
Threshold shift vs TDAC setting


Pixel Trimming
Counts
100
80
60
40
20
0
After
untrimmed Thresholds
trimmed Thresholds
Before
0.15 0.2 0.25 0.3 0.35 0.4
Threshold (in V)

Activities and status

DAC linearity characterization (Milano)

- Threshold, Baseline, Injection pulse
- Ampout, ToT