TaichuPix1 Measurement

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Further test with full chip

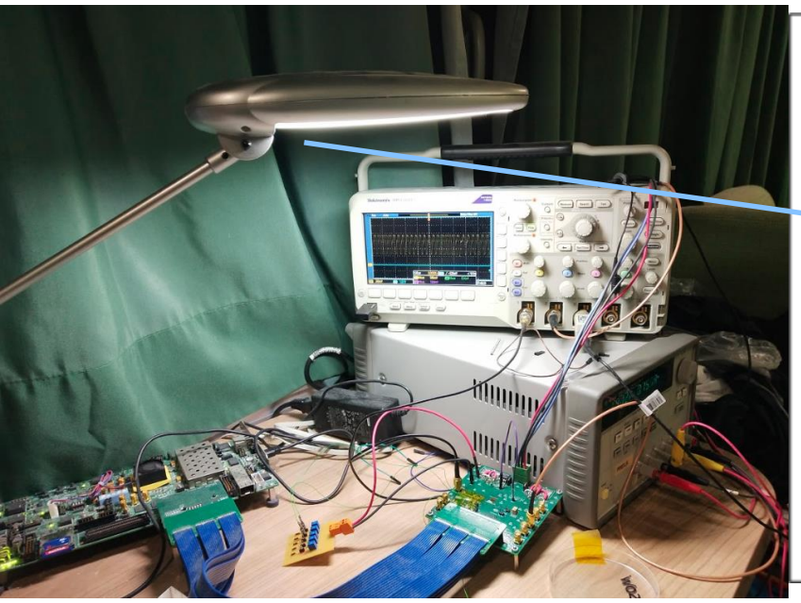
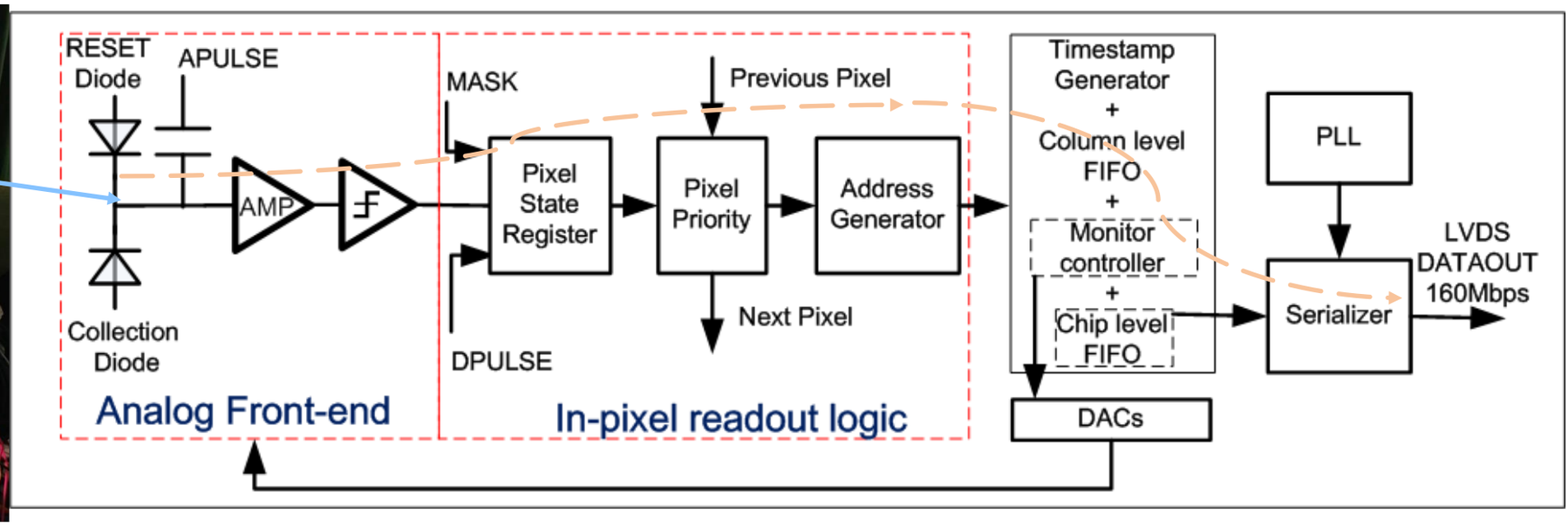


Fig1 test platform for TaichuPix1



- Fig2 shows the hit map of desk lamp shines to the chip.
- It is working at triggerless mode
- Do a loop data acquisition via Ethernet.
- It throws away the repeating data.
- It shields col62~191 with the MASKING and turn on col0~61.(matrix of 192x64)

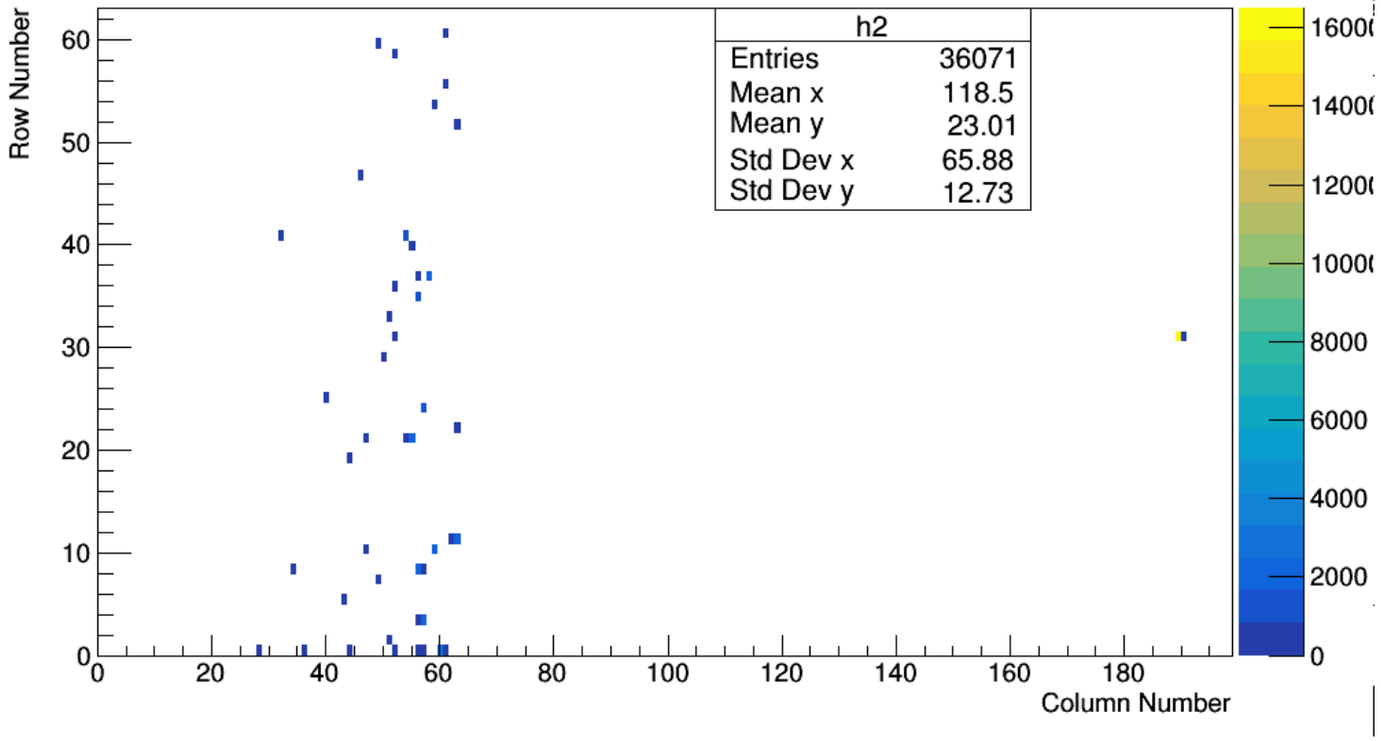


Fig2 LVDS DATA from exposure to desk lamp.

The principle of operation of periphery

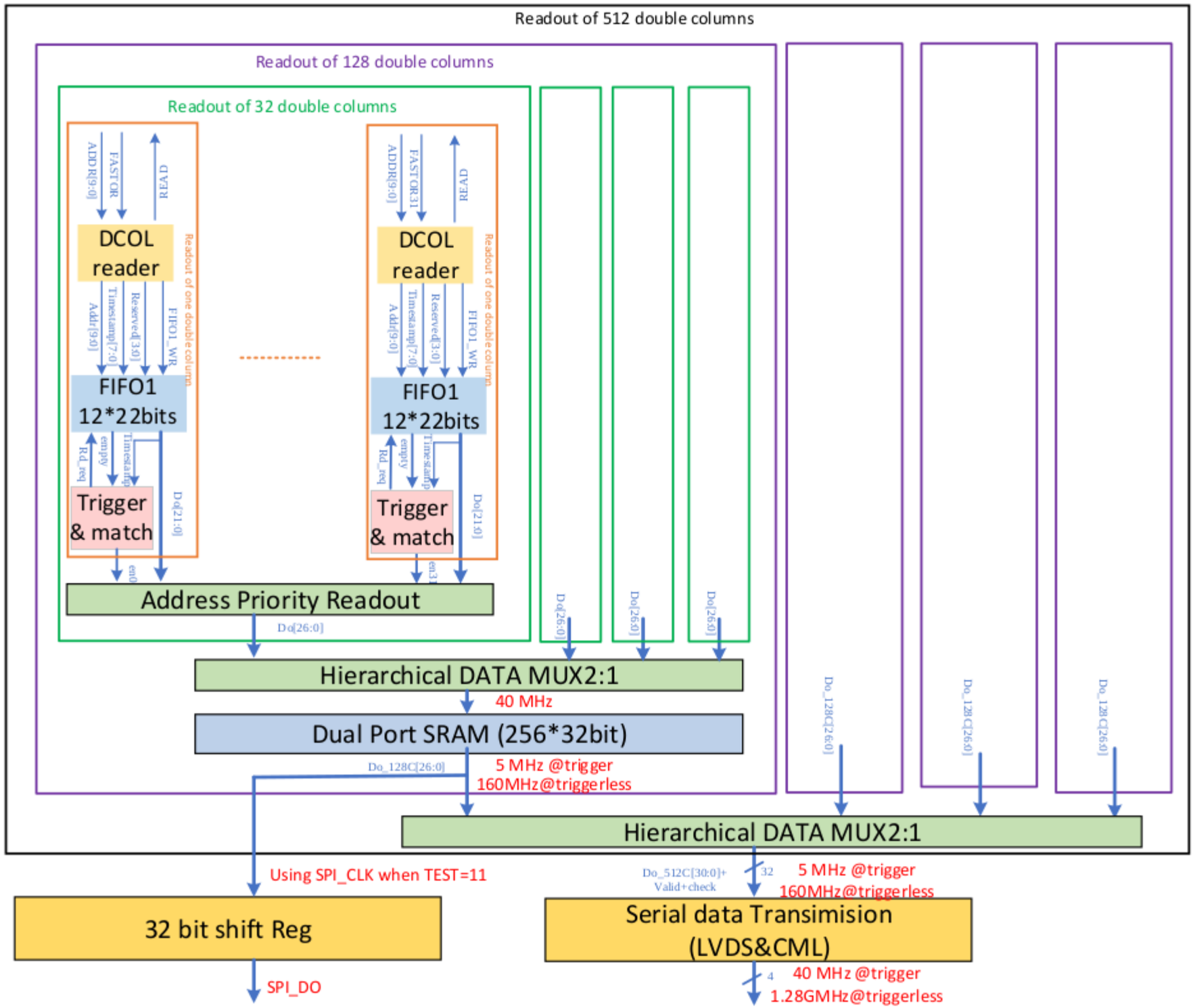
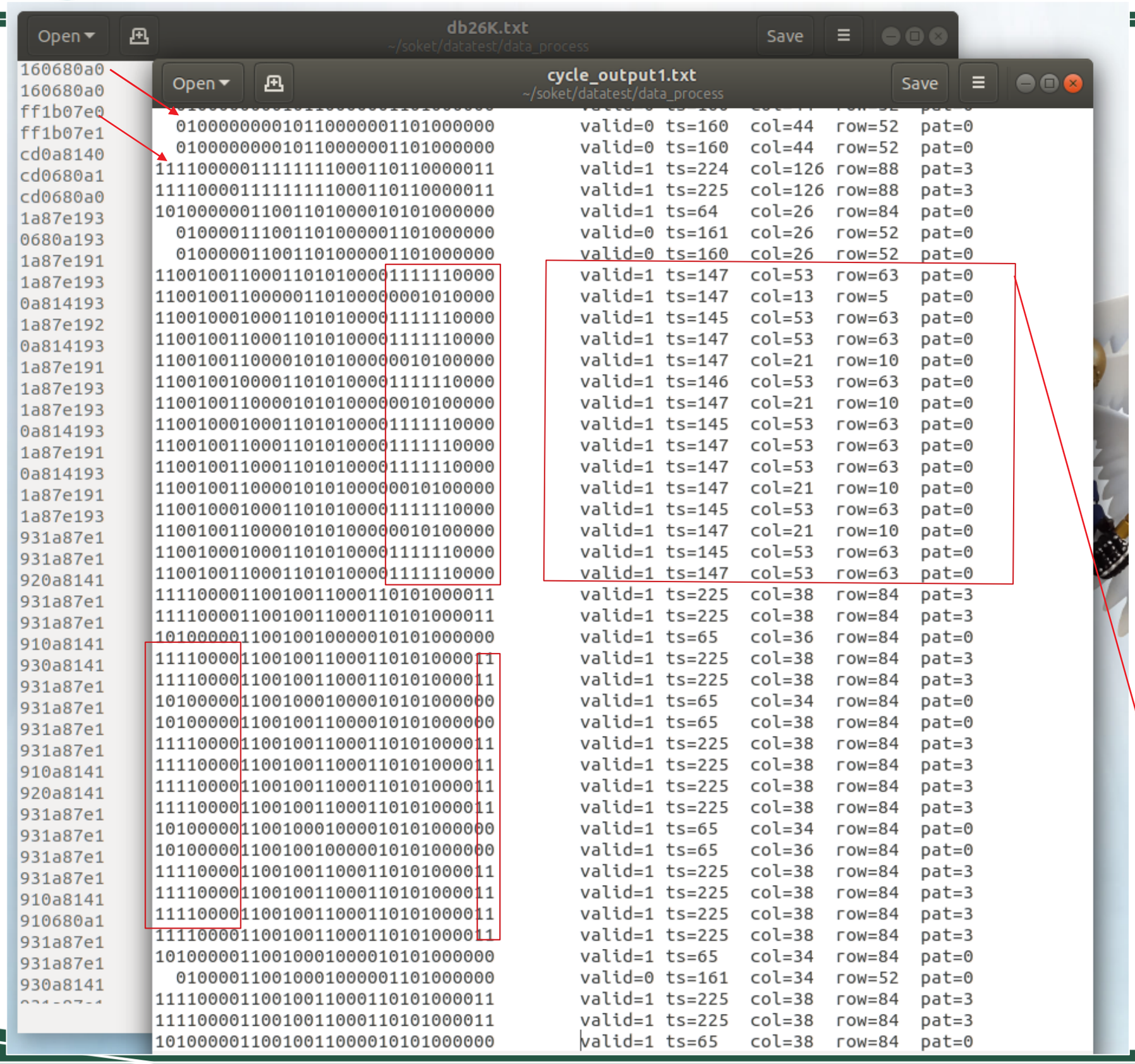


Fig1 block of periphery

- It supports two readout modes: Trigger and Triggerless
- The full speed of Trigger mode is 160Mbps. And for triggerless mode is 4Gbps
- For triggerless mode, it is supposed to read out all the events happens from injection.
- For trigger mode, you could set up a maxium 175ns window to capture the data where you want to record.
- At this moment,LVDS output is at the speed of 160MHz, so that the trigger mode will be better.
- When the output speed is mismatch with the input. It will throw away the rest of data directly.

Strategy to process the raw data



- Here is the example to show how I process the data.
-

a) I received the 32bits raw data via Ethernet.(Here is a 5.8M file with 650K data)

b) Then try to find pattern(1111110000).

c) Because there is no frame header of LVDS output, and the order of 32 bits data will shift from time to time. As it shows here,the upper half is different the lower half.

d) Then shift the proper bits for all the data.(here raw data shift 23bits to the left)

e) Then keep the data with valid==1 and pattern==0

f) To improve the accuracy,add an extra condition with Timestamp=147, so that I could throw away most of garbage data.

Further test with full chip (Internal DAC)

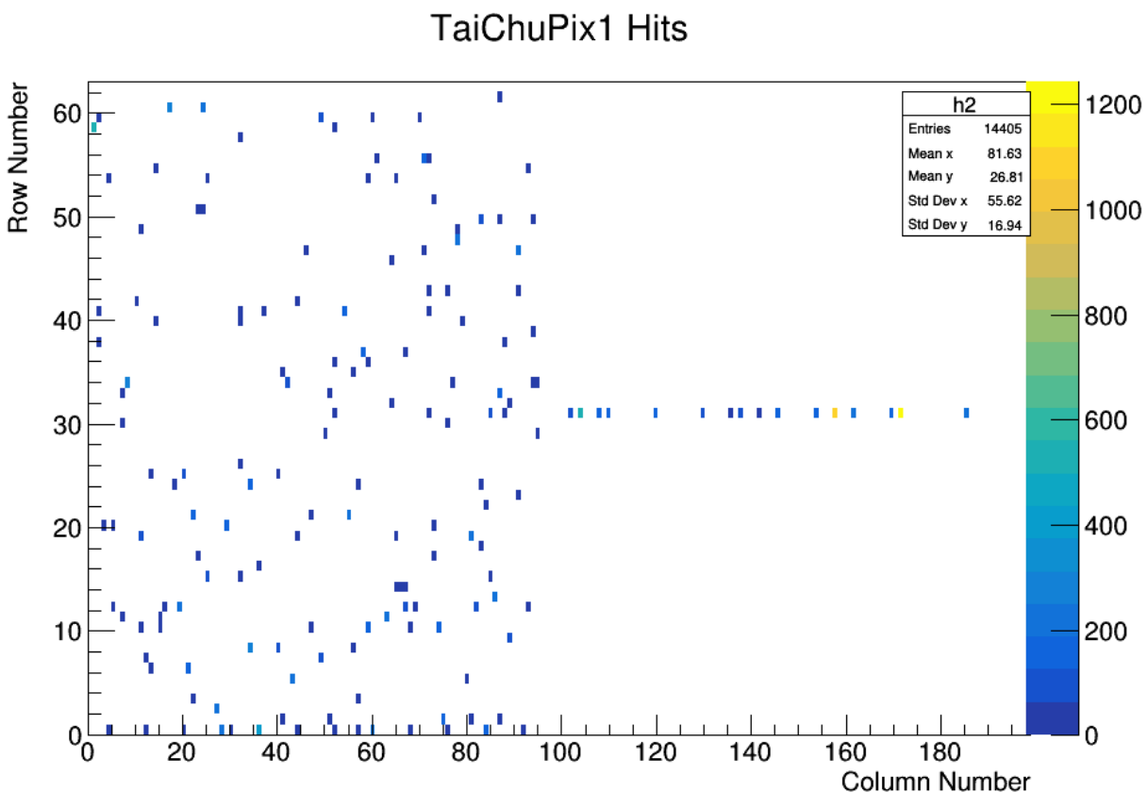


Fig1 Trigger mode with lamp injection

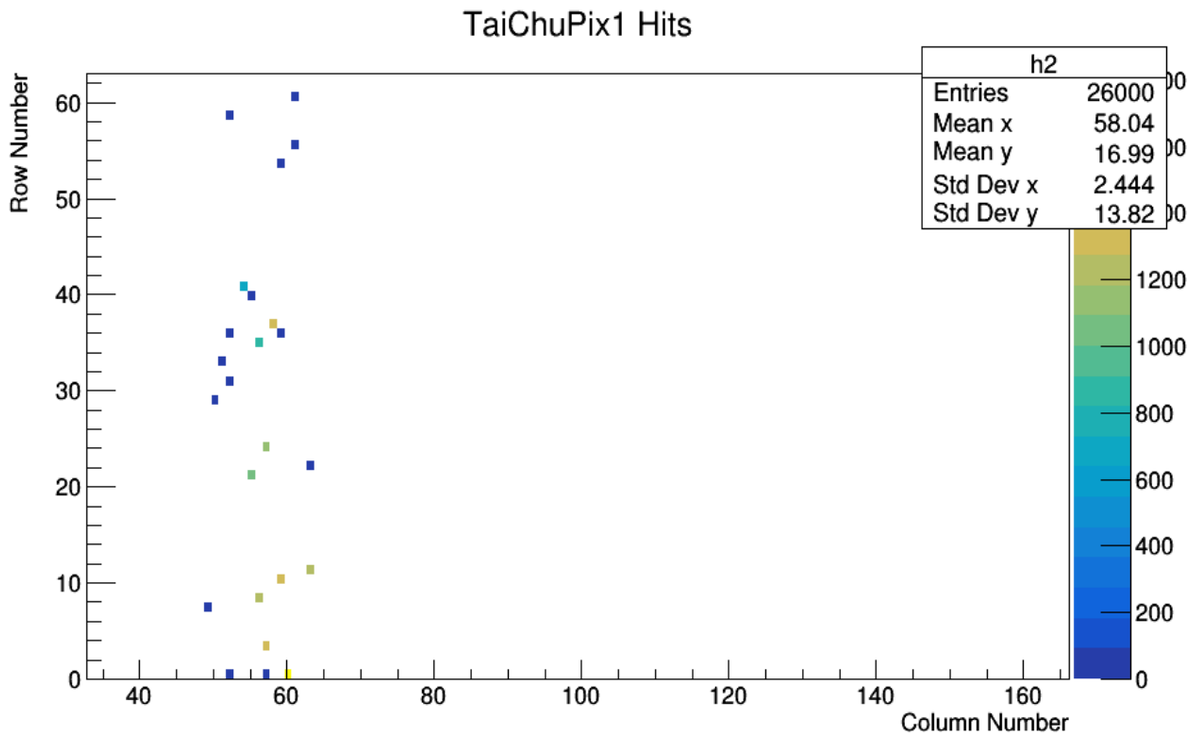


Fig2 Triggerless mode with lamp injection

- In same condition of the test platform with different readout mode setup.
- Only left half of FE-I3 like part turns on.
- Trigger mode could show up a larger scale of hits region.
- Triggerless mode could only readout a small range of data due to the readout speed
- The plot results was from internal DAC bias to analog front end.

Baseline of the TaichuPix1 chip

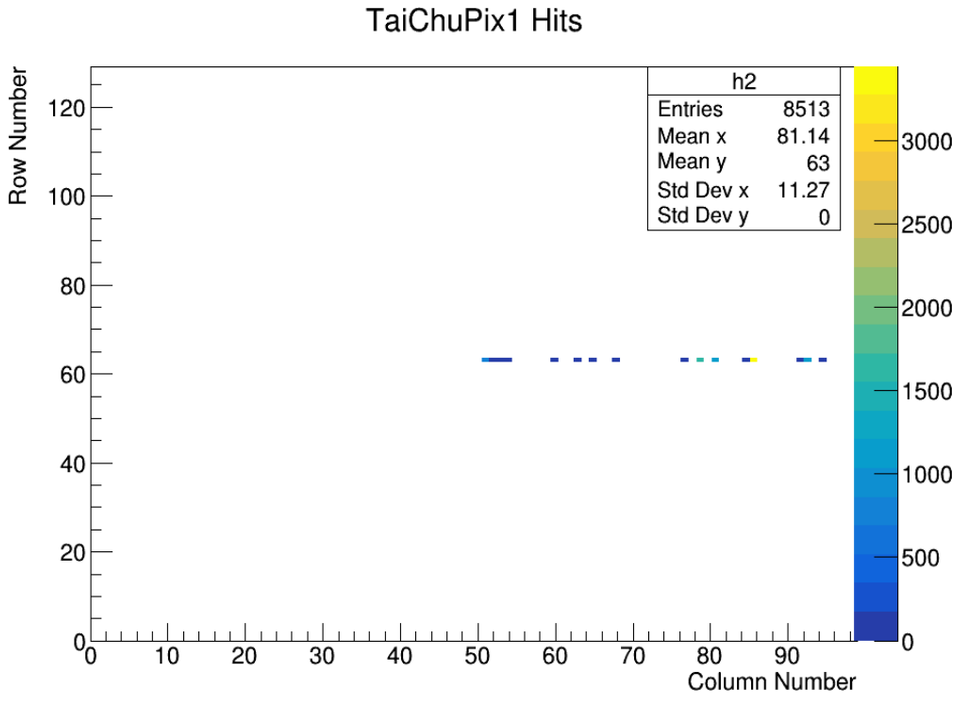


Fig1 Turn on FE-I3 like part without light injection

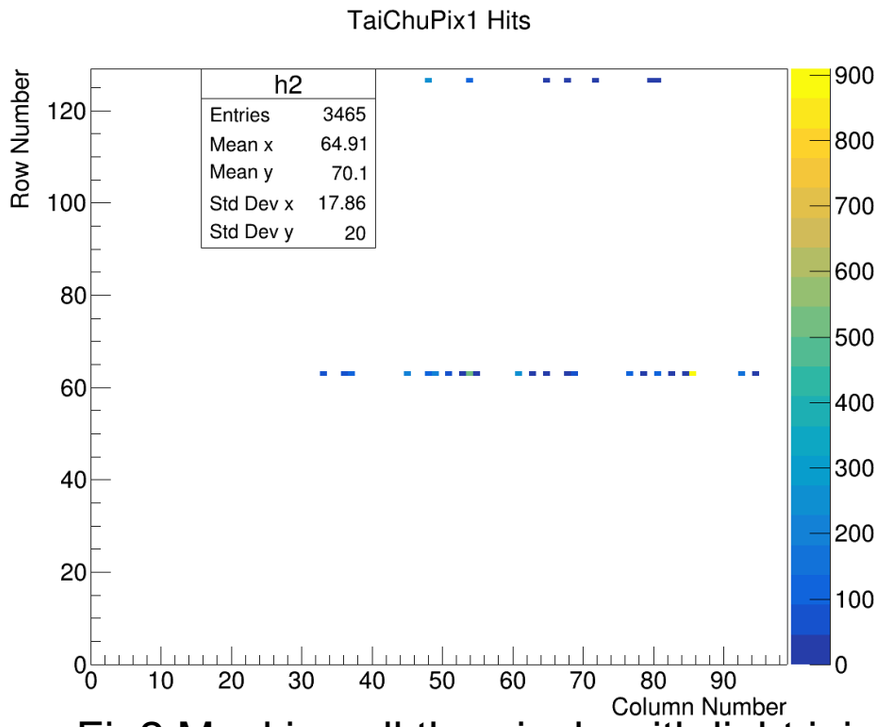


Fig2 Masking all the pixels with light injection

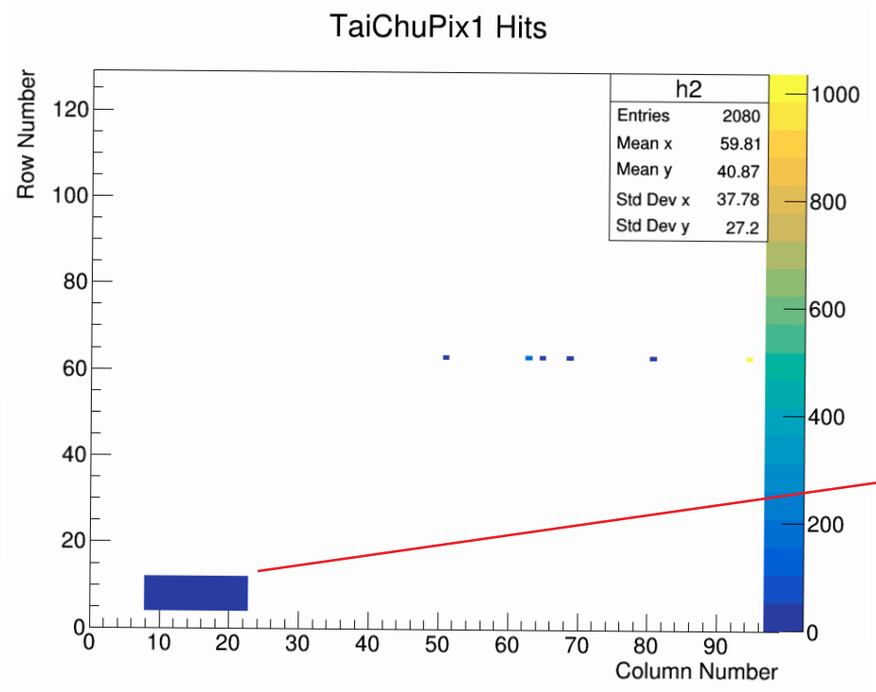


Fig3 SPI readout with analog pulse injection at triggerless mode. (Specify array of 8×15)

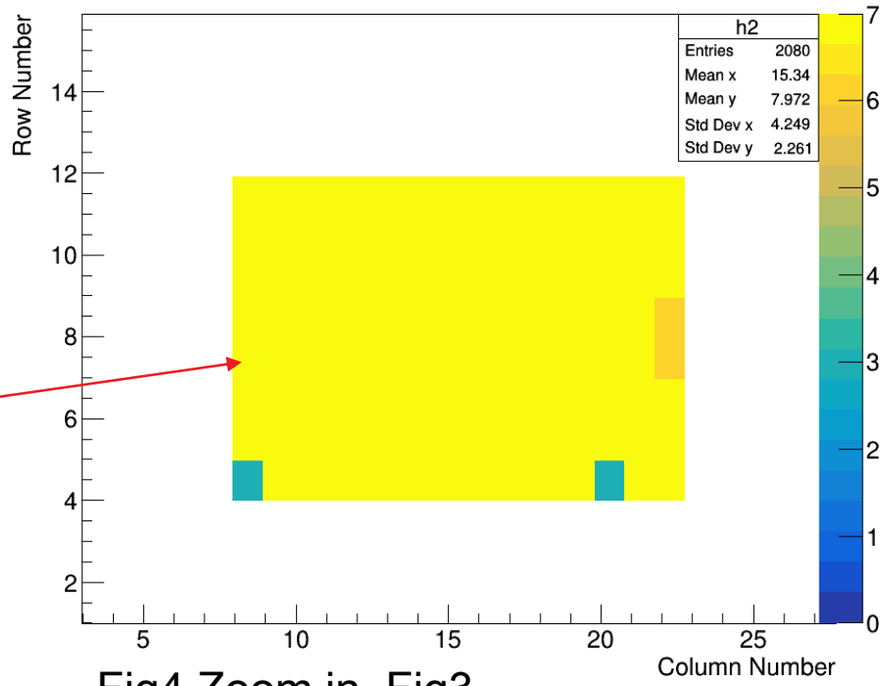


Fig4 Zoom in Fig3

Further test with a particular region

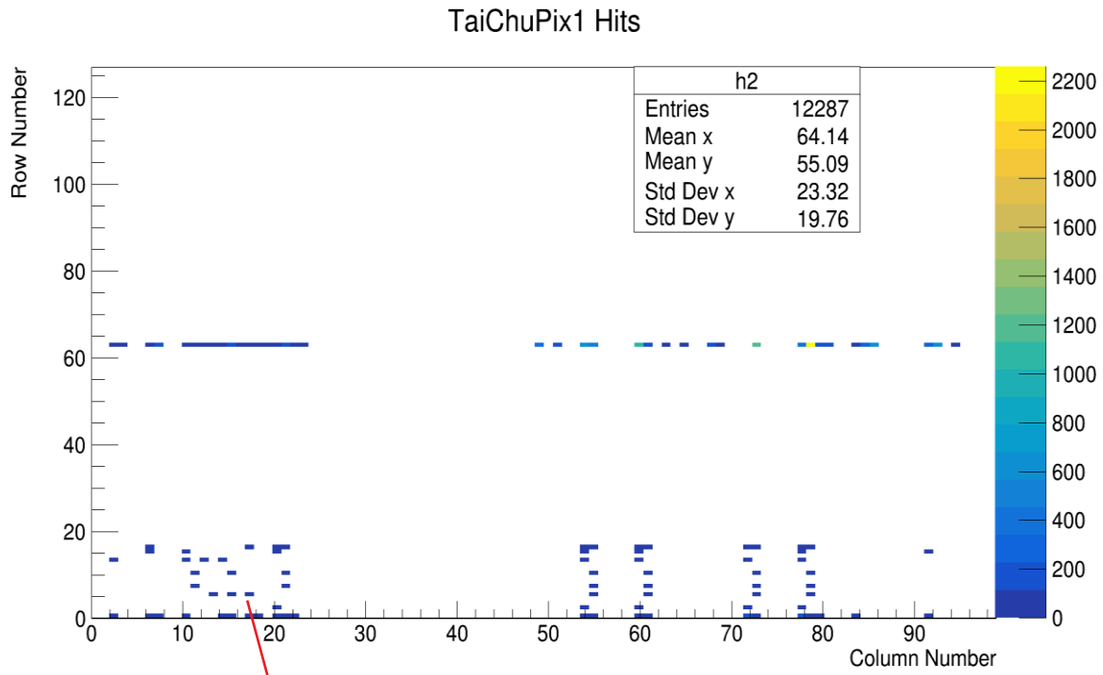


Fig1 Trigger mode with lamp injection (small array of 20×24)

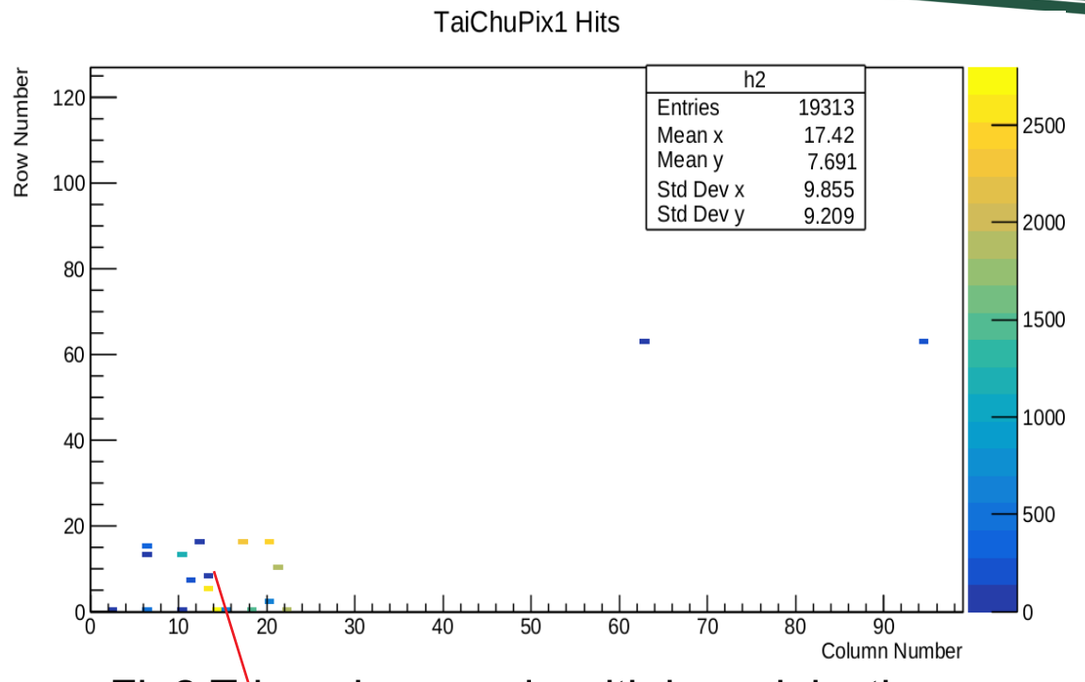


Fig2 Triggerless mode with lamp injection (Specify timestamp==81 or 63)

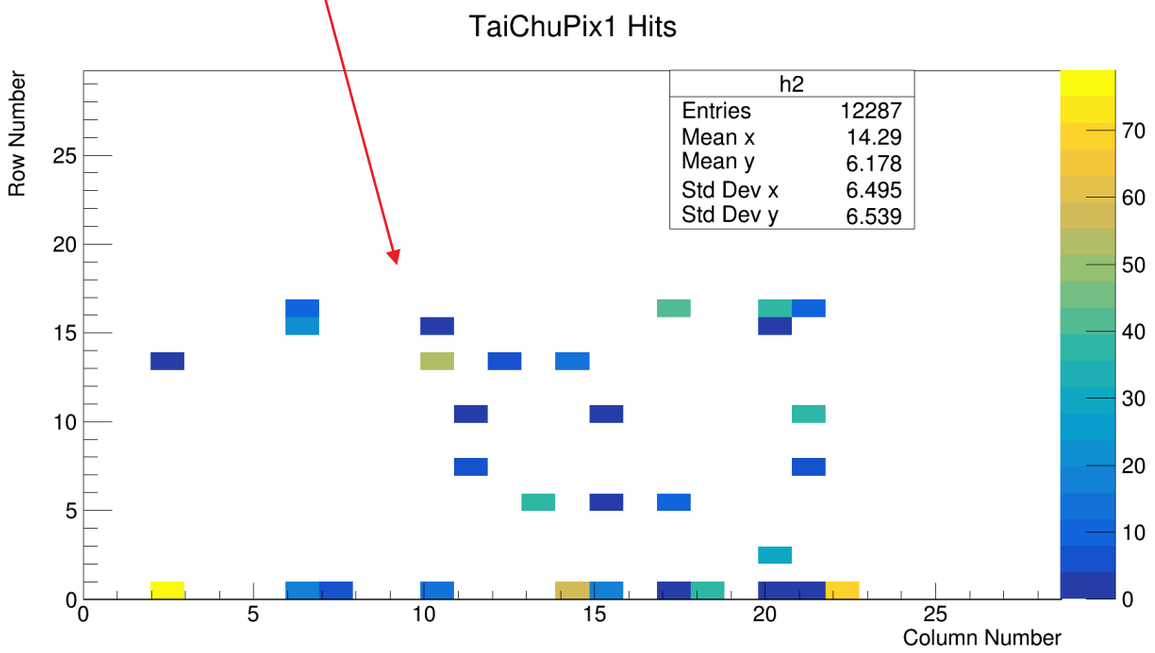


Fig3 Zoom in Fig1

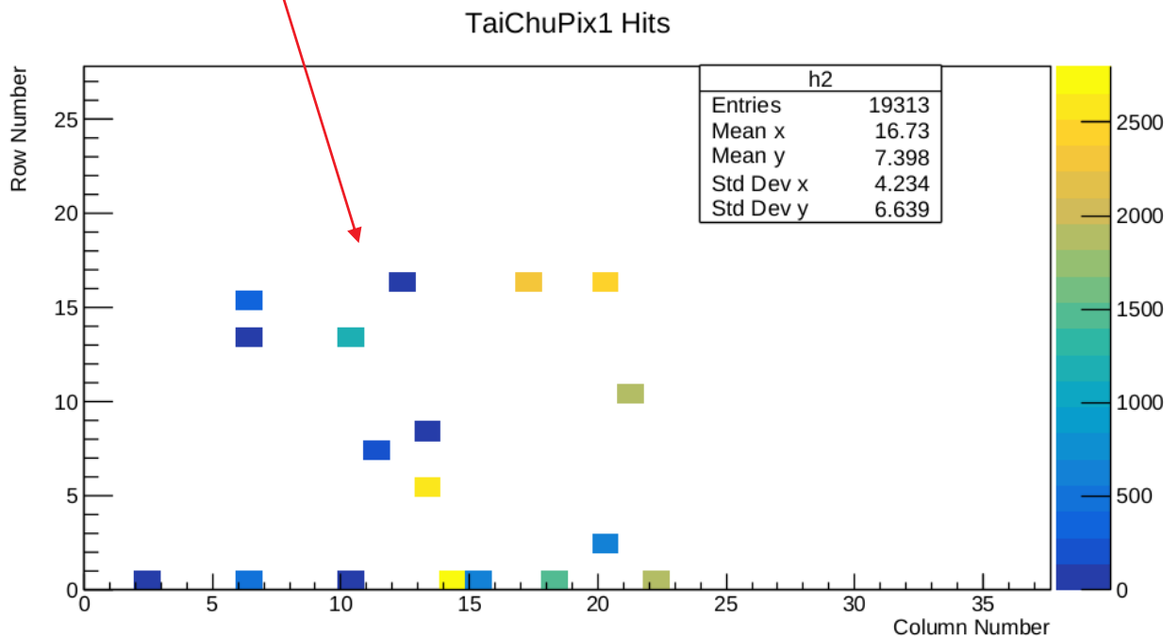


Fig3 Zoom in Fig2

DATA Analysis(COL0~COL95)

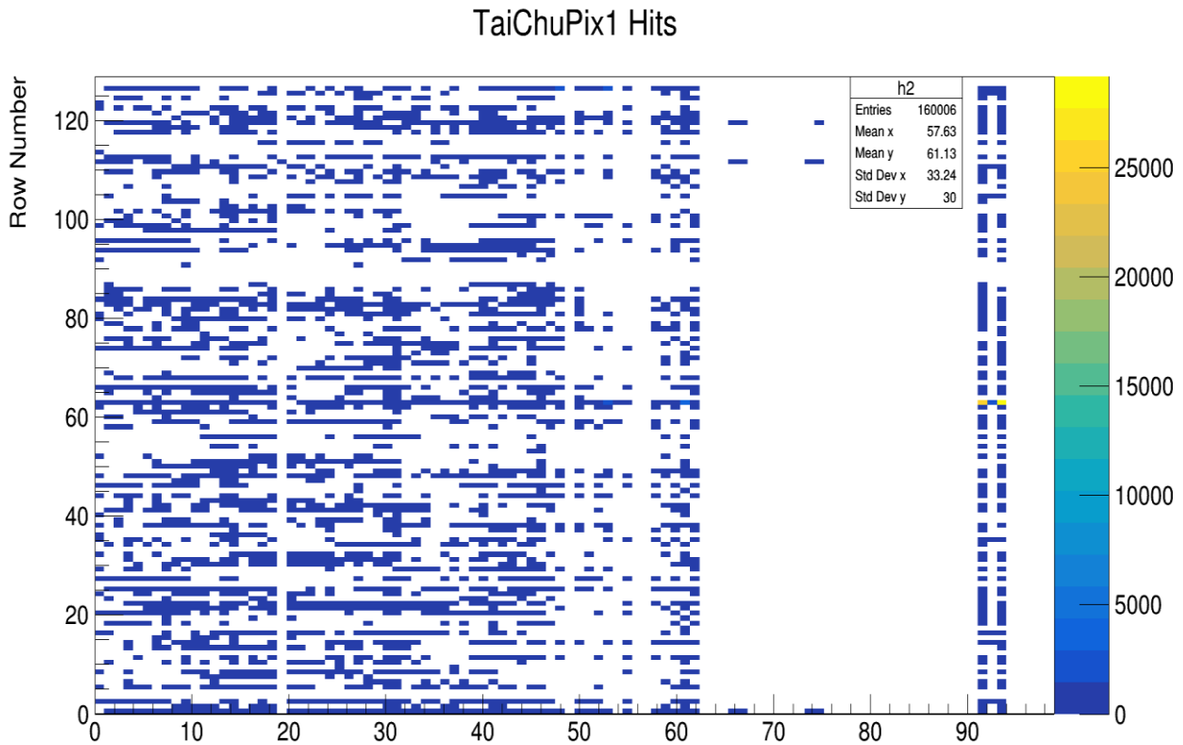


Fig1 Raw data shift 11 bits to the left

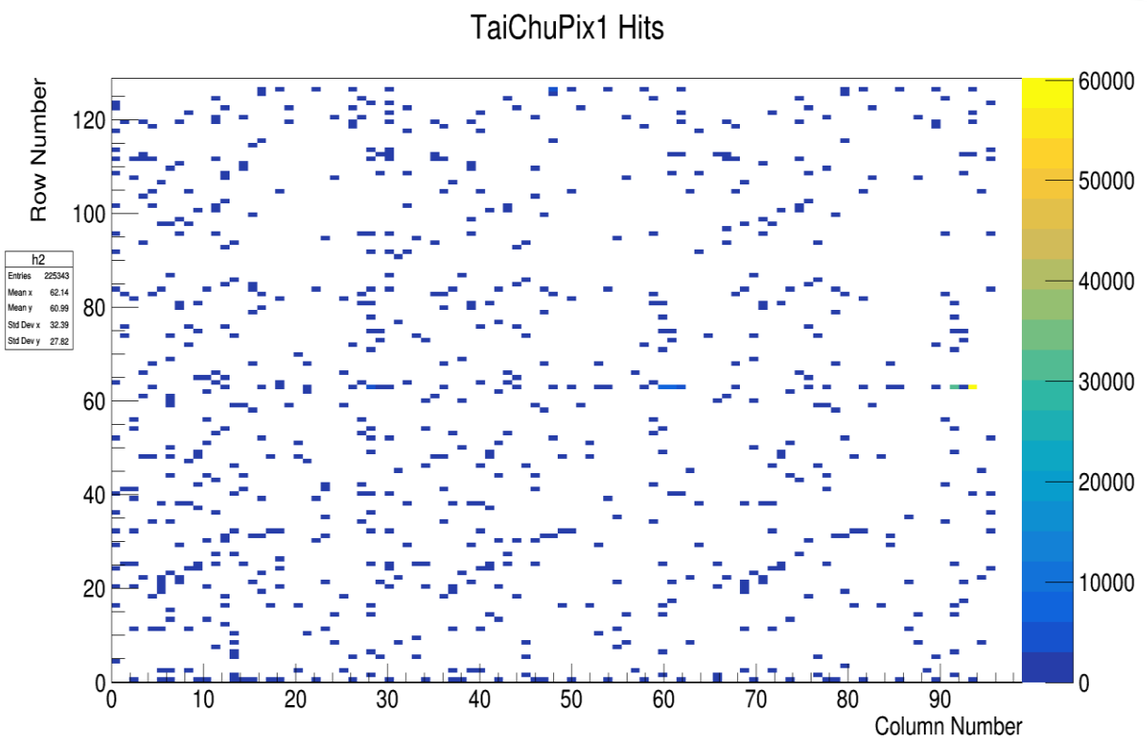


Fig2 Raw data shift 19 bits to the left

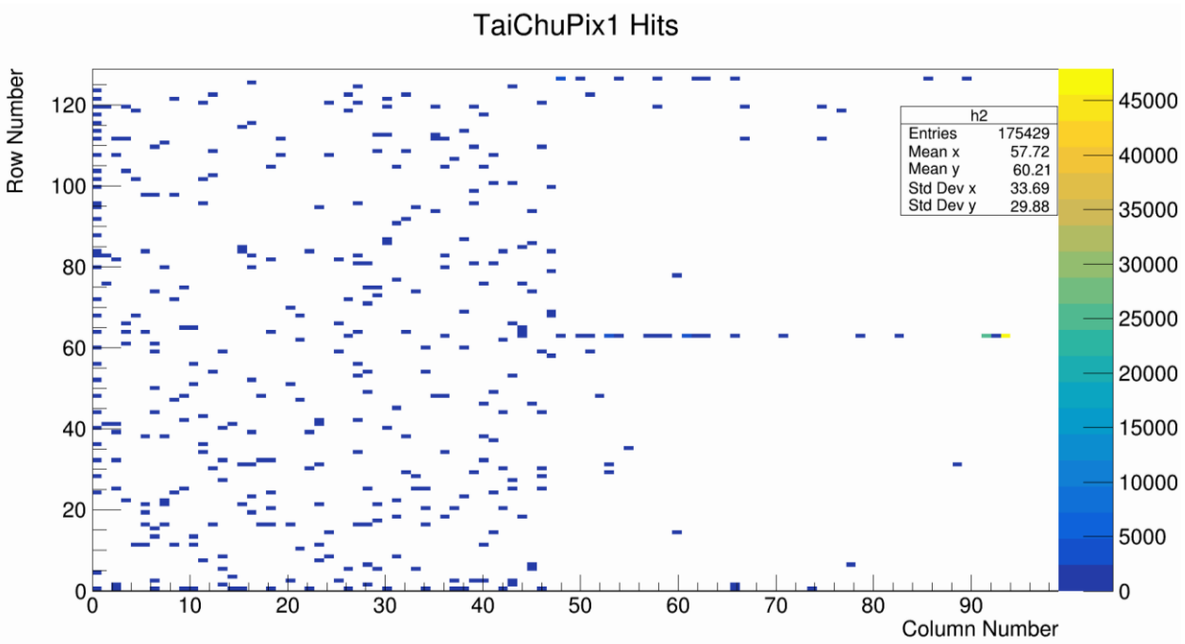


Fig3 Raw data shift 3 bits to the left

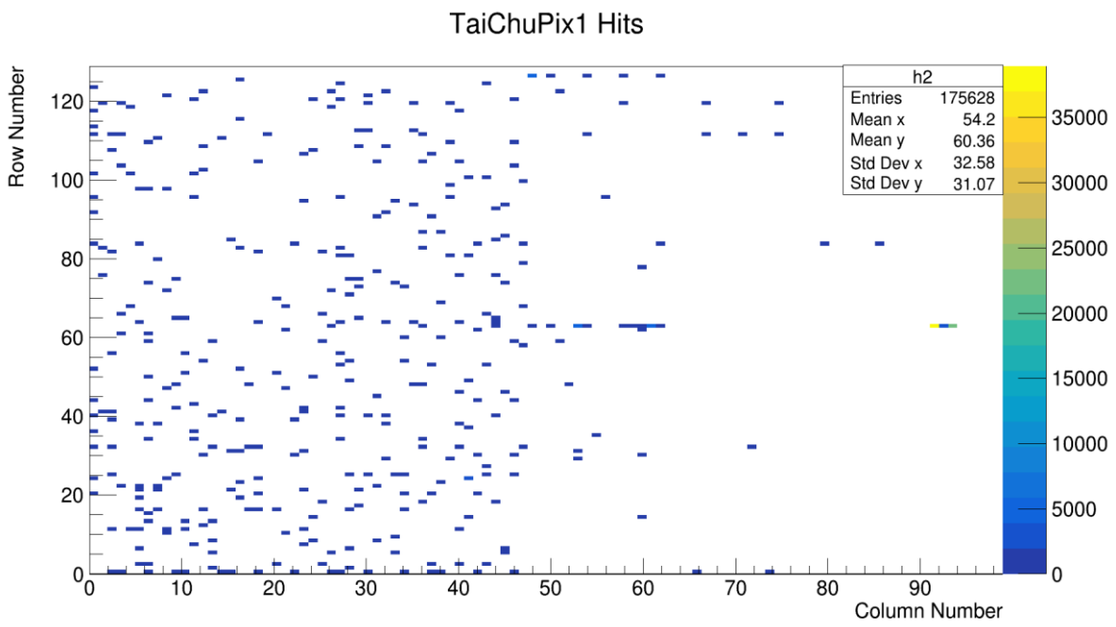


Fig4 Raw data shift 27 bits to the left

Analog front end parameter

Table 1 (Chip2 Internal DAC)

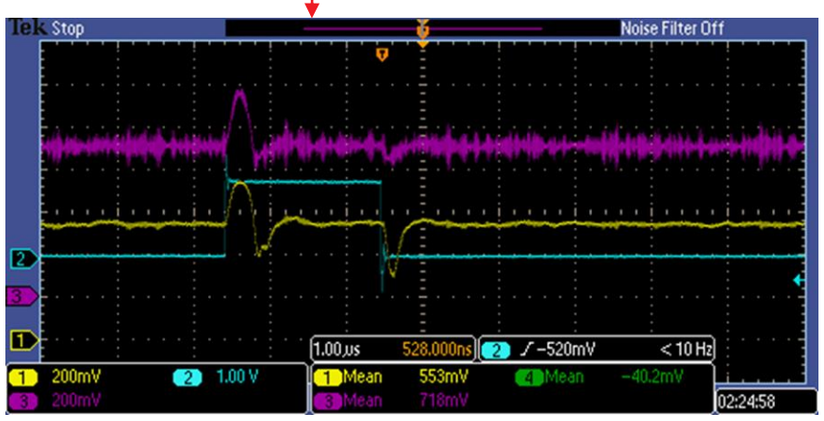
Bias	IBIAS	ITHR	IDB	VCLIP	VCASP	VCASN	VCASN2	VRESET
Design value	440 nA	4.5 nA	1 μA	0/0.2 V	0.6 V	0.55 V	0.5 V	1.4 V
Config. value	440nA	1.5nA	1uA	0.068V	0.6V	0.55V	0.5V	1.71V

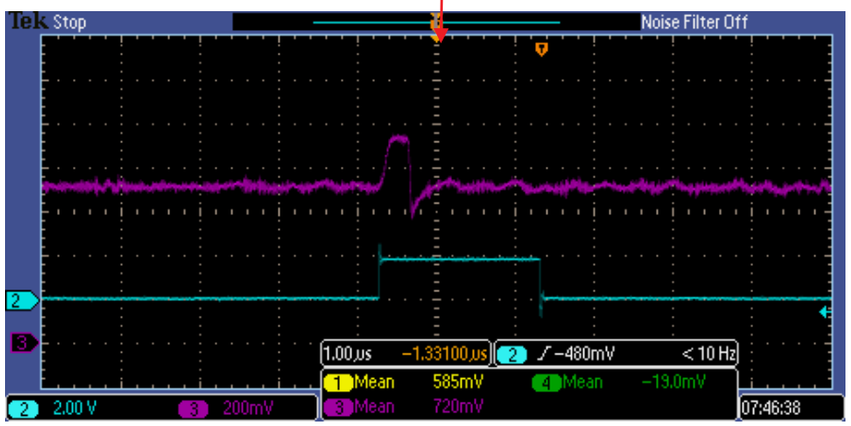
Table 2 (Chip2 External BIAS VBG=800mV VBIAS=900mV)

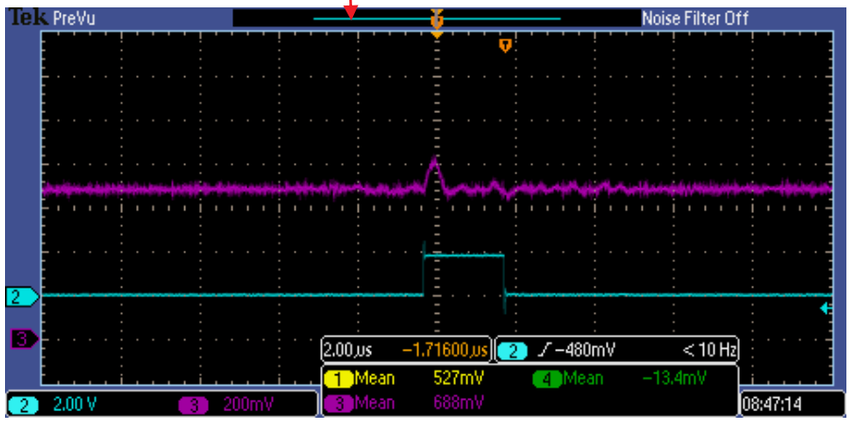
Bias	IBIAS	ITHR	IDB	VCLIP	VCASP	VCASN	VCASN2	VRESET
Design value	440 nA	4.5 nA	1 μA	0/0.2 V	0.6 V	0.55 V	0.5 V	1.4 V
Config. value	440nA	3.5nA	1uA	0.043V	0.64V	0.57V	0.68V	1.71V

Table 2 (Chip2 External BIAS VBG=800mV VBIAS=900mV)

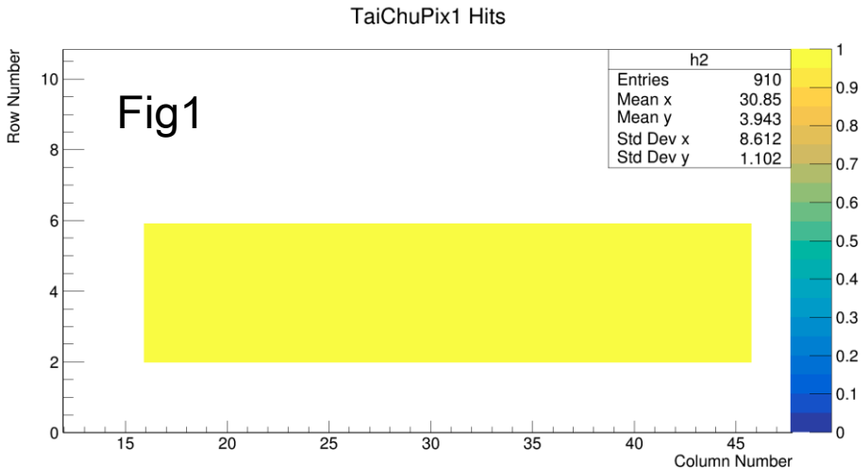
Bias	IBIAS	ITHR	IDB	VCLIP	VCASP	VCASN	VCASN2	VRESET
Design value	440 nA	4.5 nA	1 μA	0/0.2 V	0.6 V	0.55 V	0.5 V	1.4 V
Config. value	440nA	4.5nA	1uA	0.043V	0.6V	0.55V	0.5V	1.71V

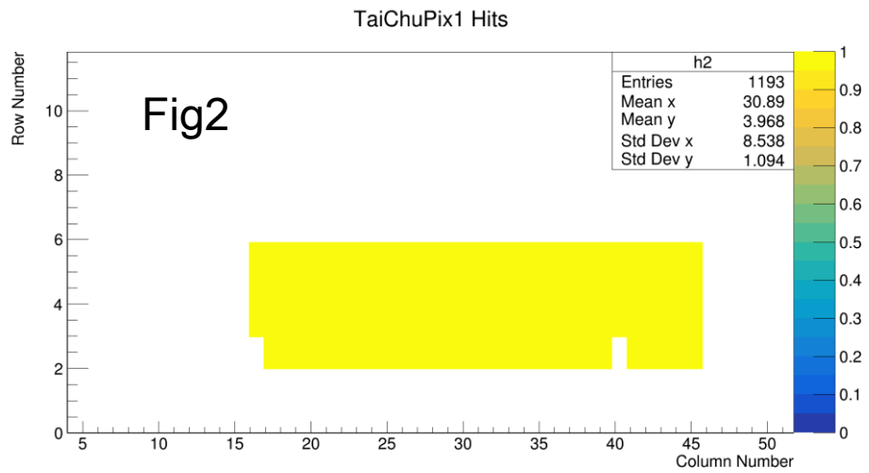


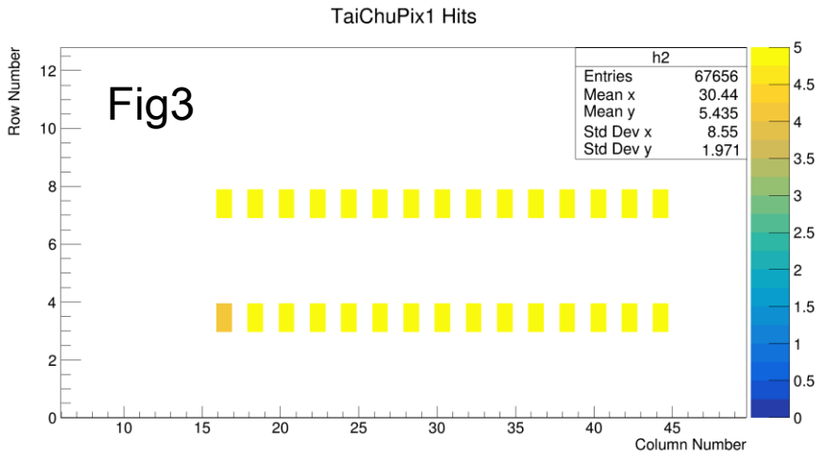


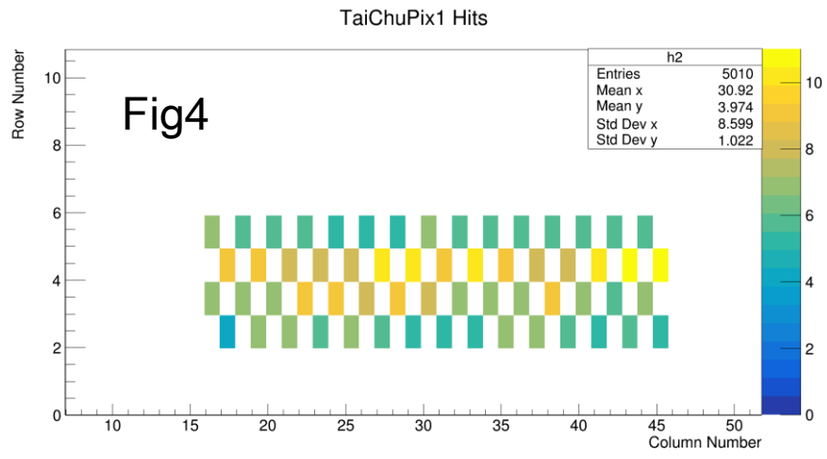


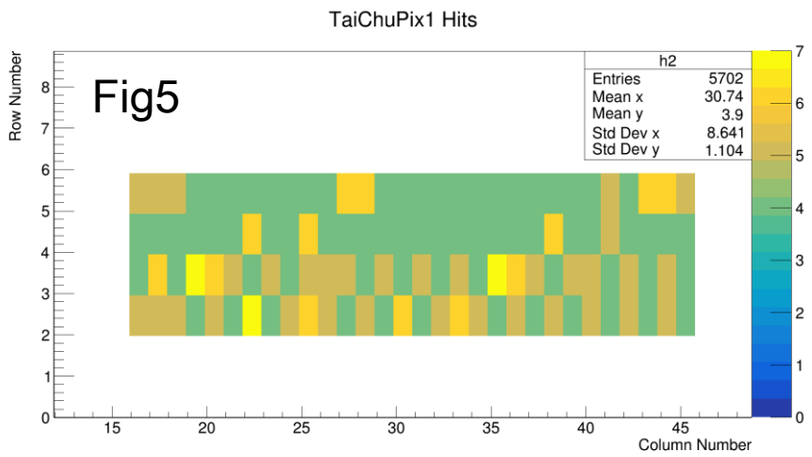
Turn on the external BIAS to DAC

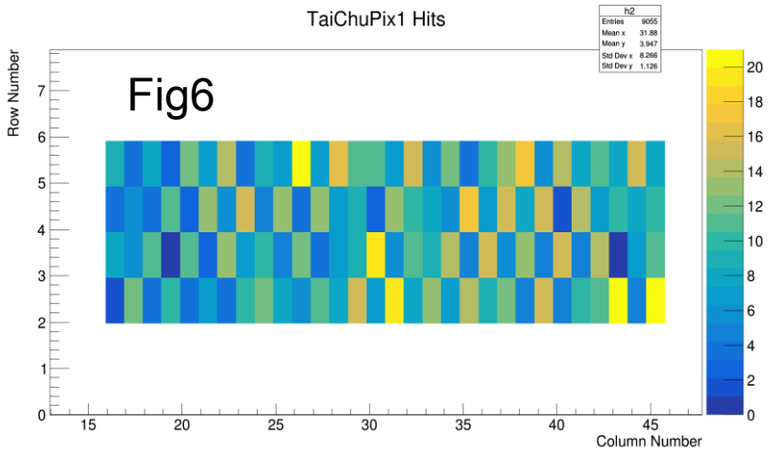






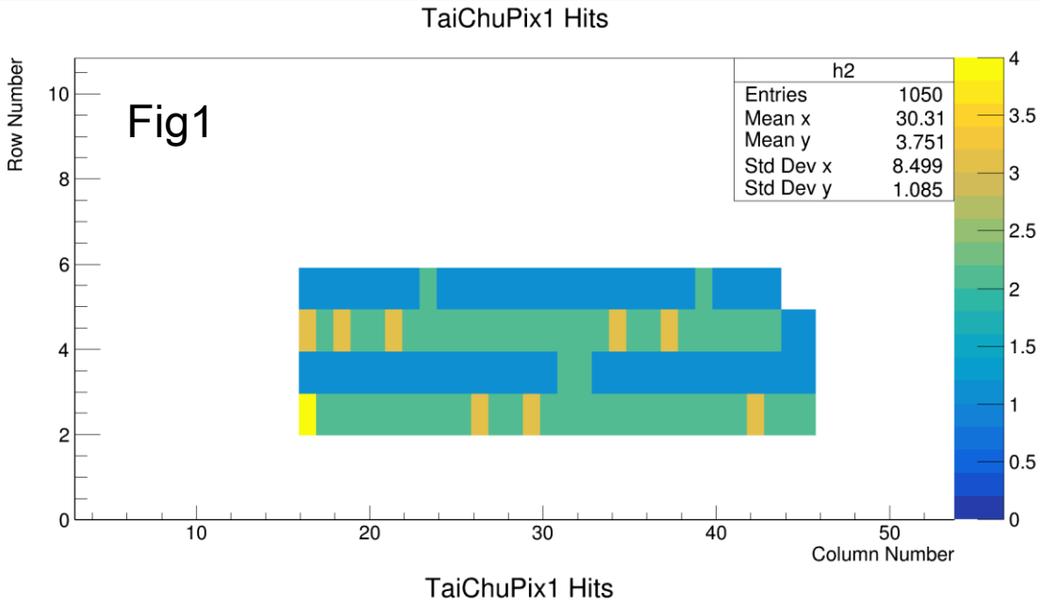


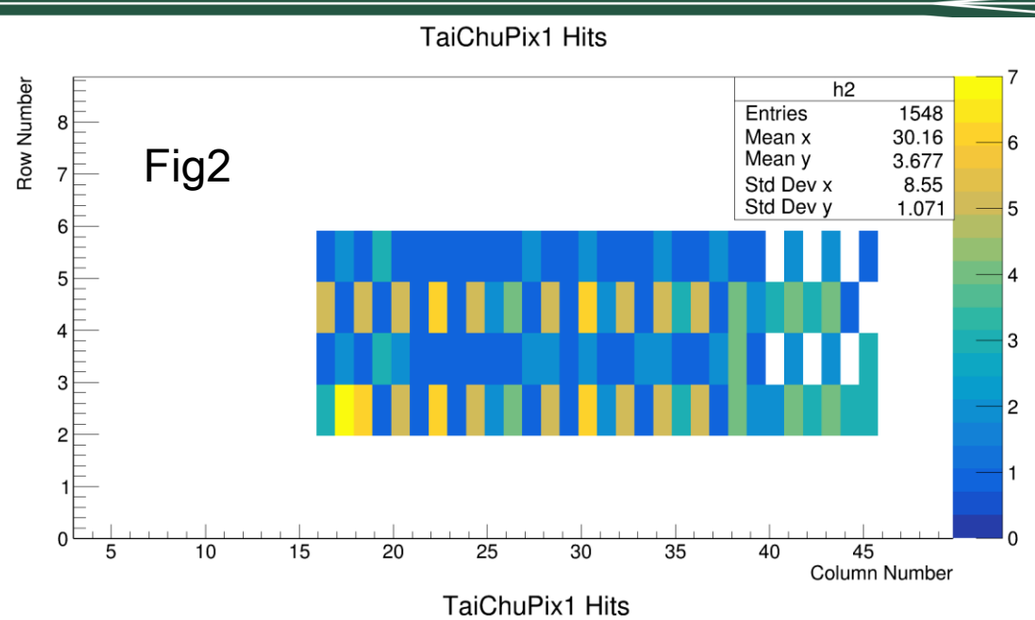


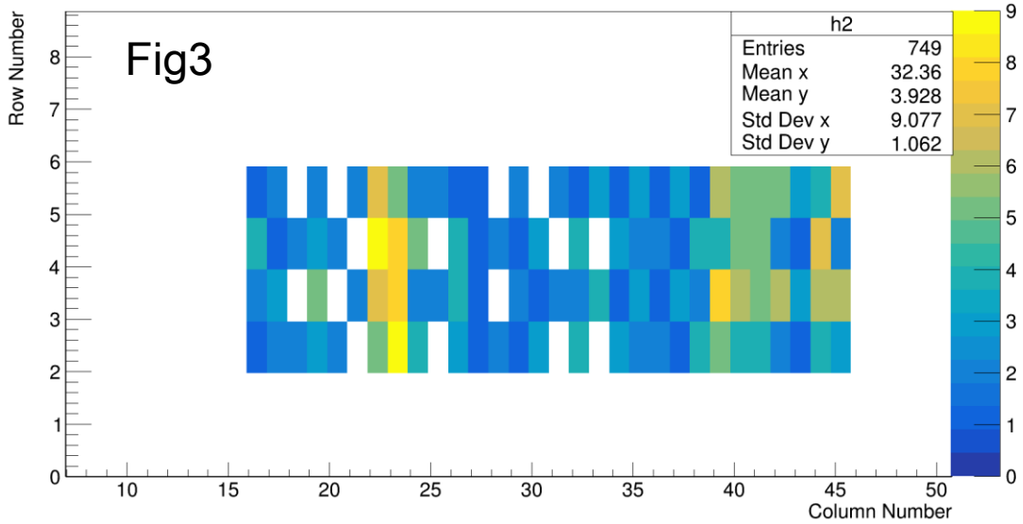


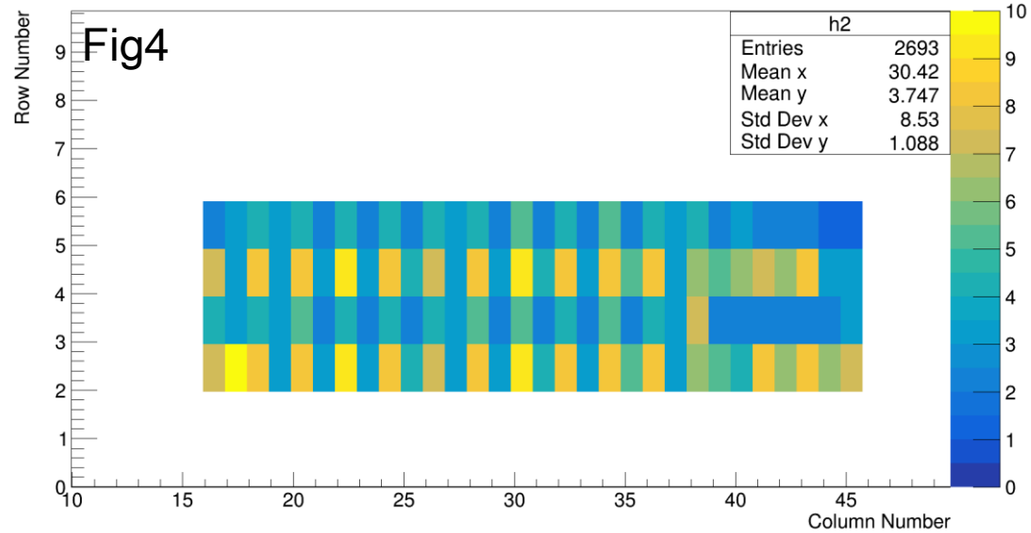
- These plots are from triggerless mode.
- Specify a paticular region with a 4x30 array
- Fig1 to Fig 4 show the different shapes of the particular region.
- Fig1 and Fig2 are the results from one run.
- Fig3 and Fig4 are the multiple results with different timestamp.
- Fig5 and Fig6 are the results of multiple cases.

Turn on the external BIAS to DAC



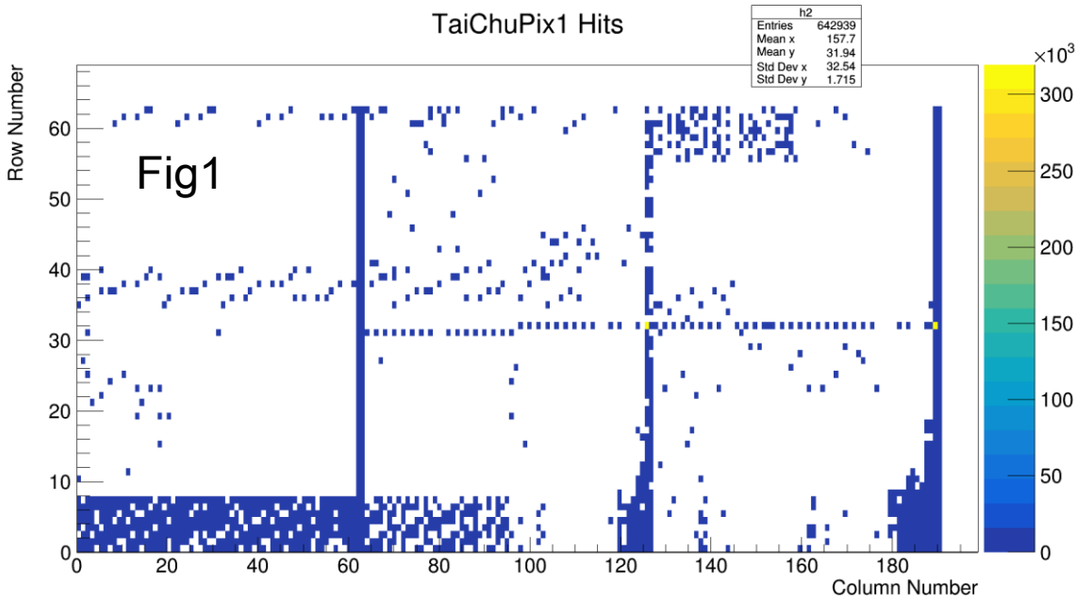


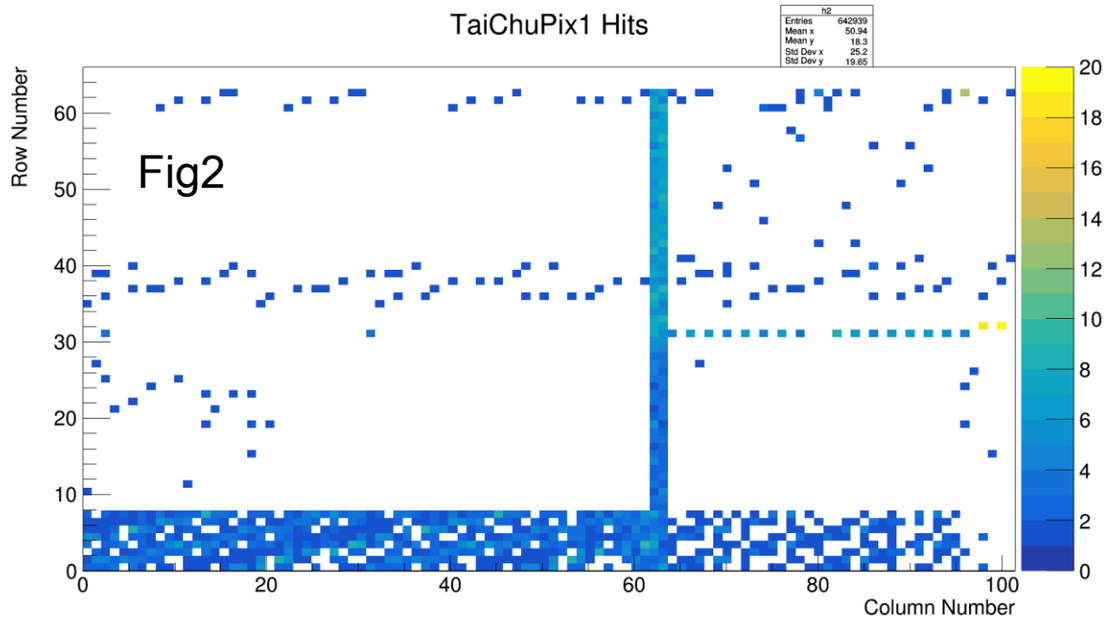


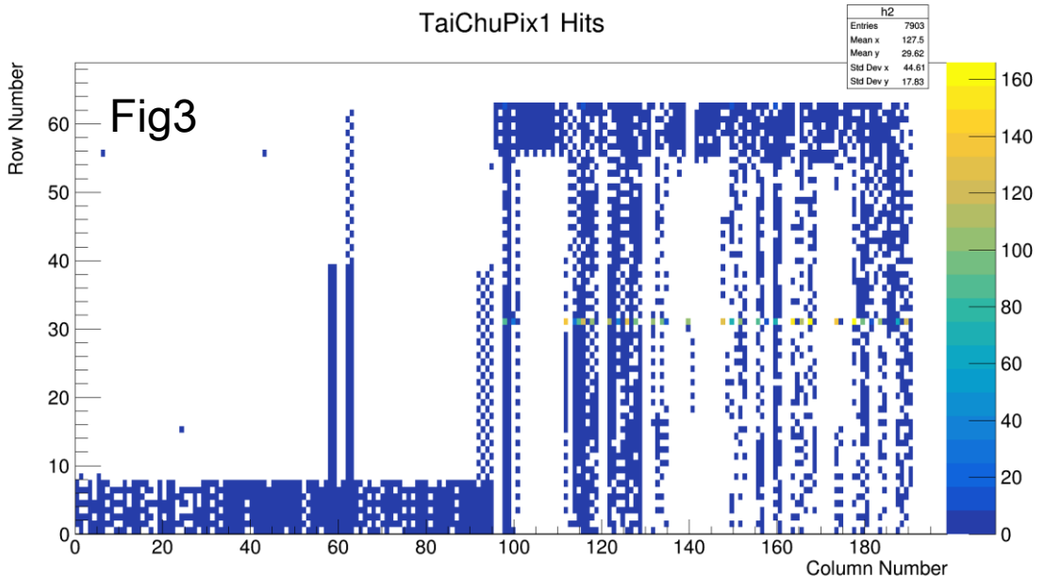


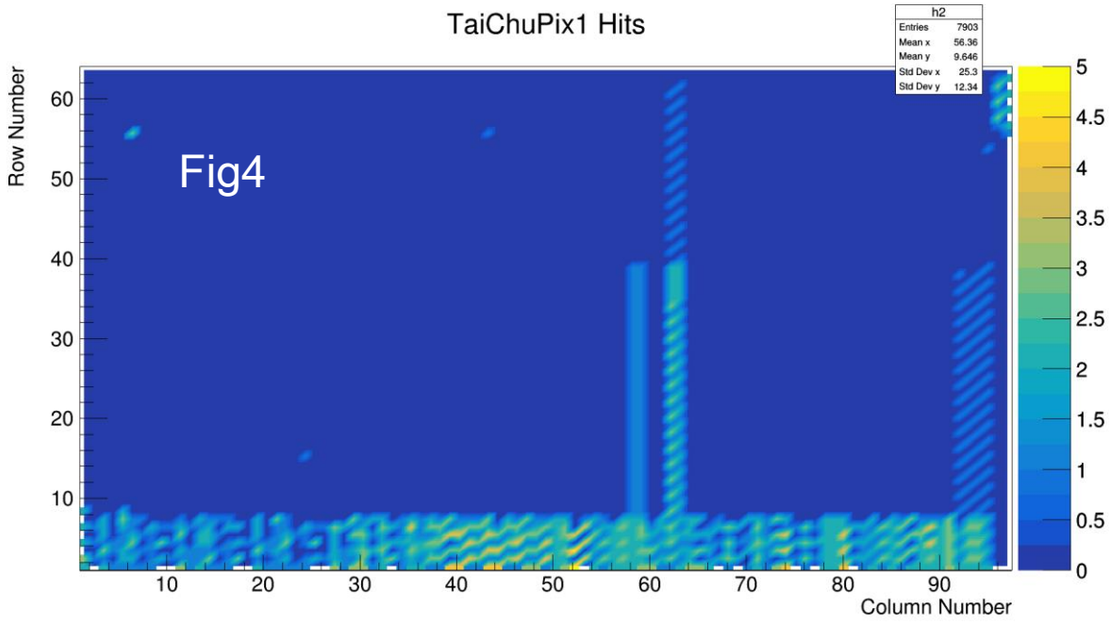
- These plots are from trigger mode.
- Specify a paticular region with a 4x30 array
- Fig1 and Fig 2 show the different shapes may appear in each run of the chip.
- Fig3 show the chip is running with extra lamp light injection.
- Fig4 is the plot which integrates several times of the results.

Turn on the external BIAS to DAC



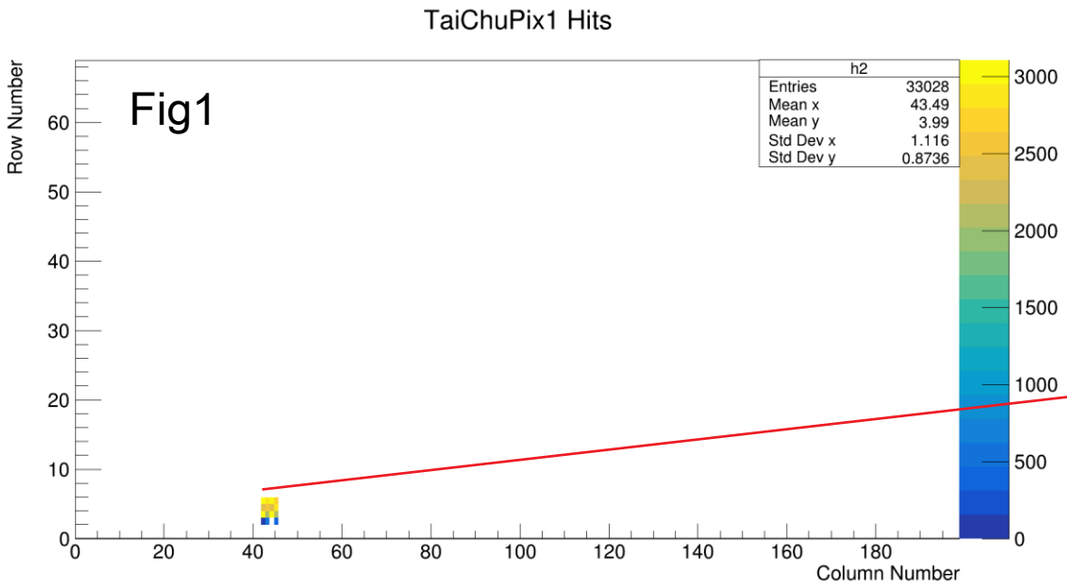


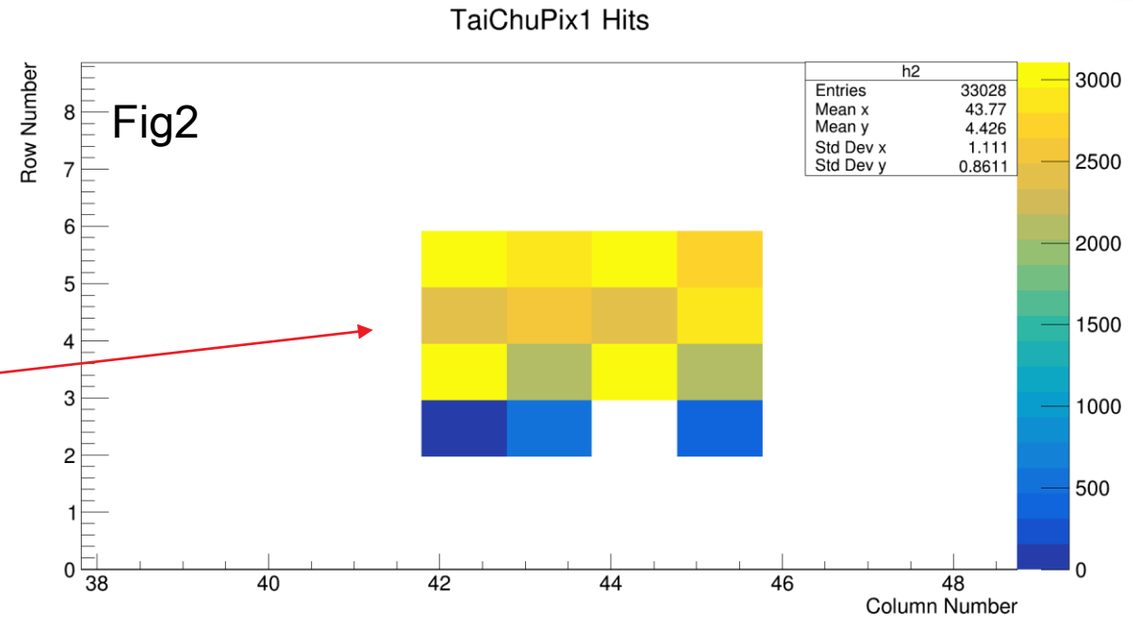


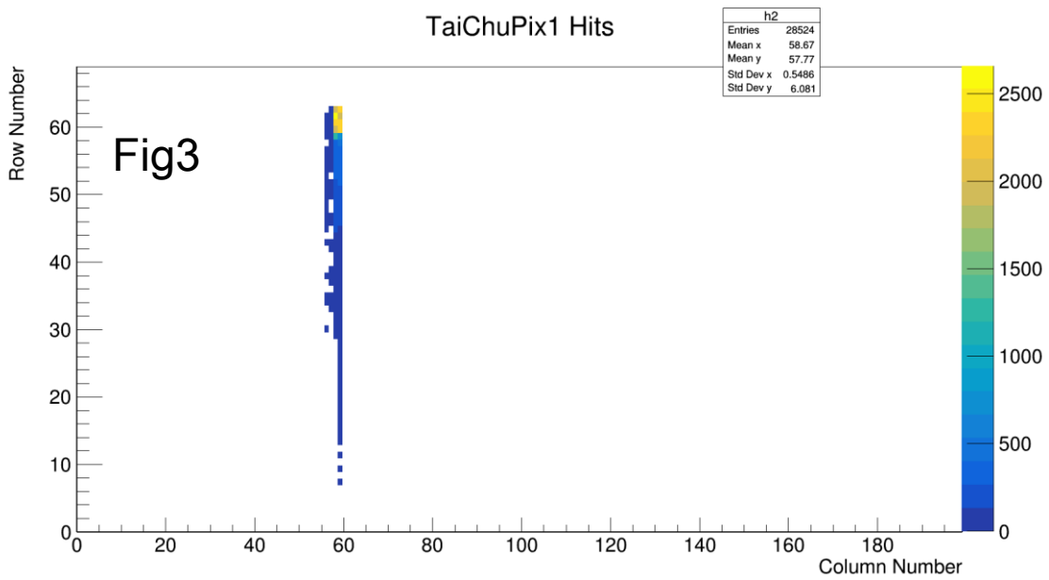


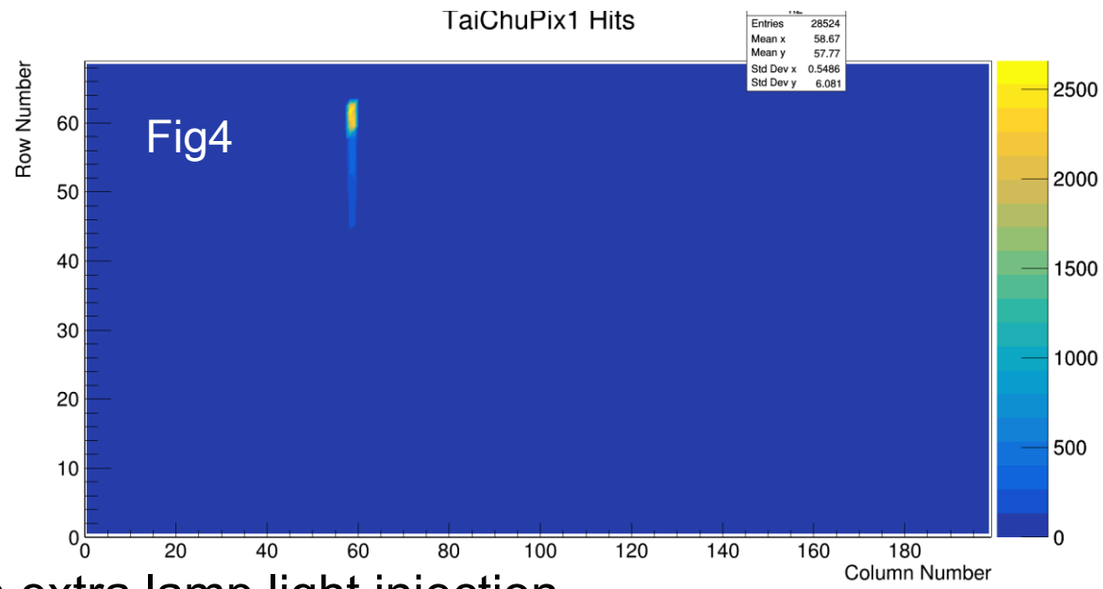
- Fig1 and Fig2 are from triggerless mode while the Fig3 and Fig4 are from trigger mode.
- These results are turning on the entire array of the the chip with light injection.
- Fig2 is the enlarged view of Fig1 left part(FE-I3 like scheme).
- Fig4 is the contour of the left part of Fig3.

Turn on the external BIAS to DAC





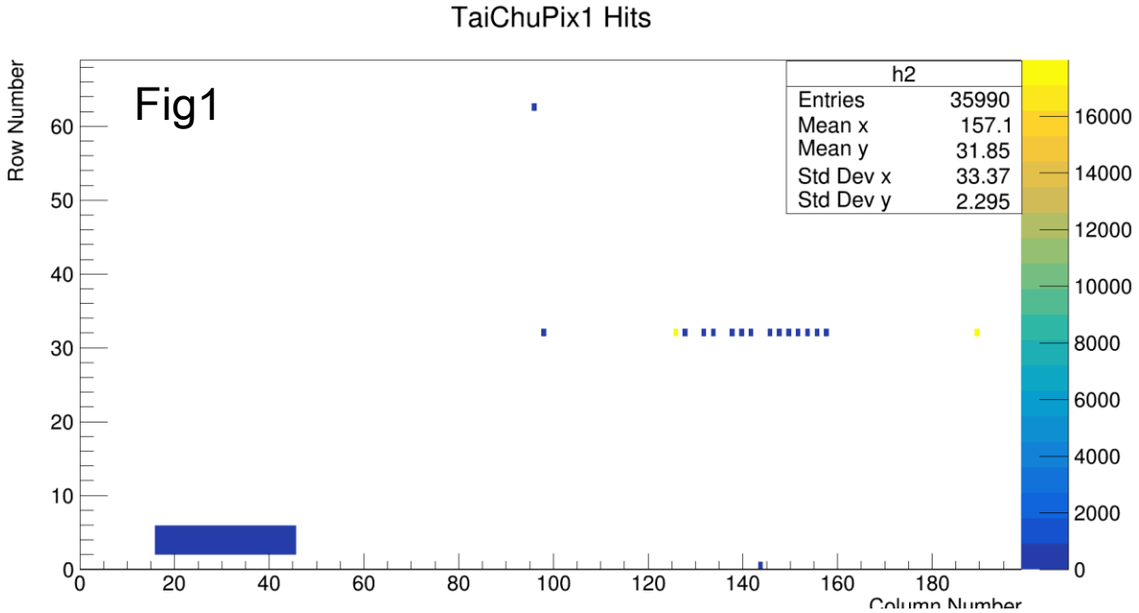


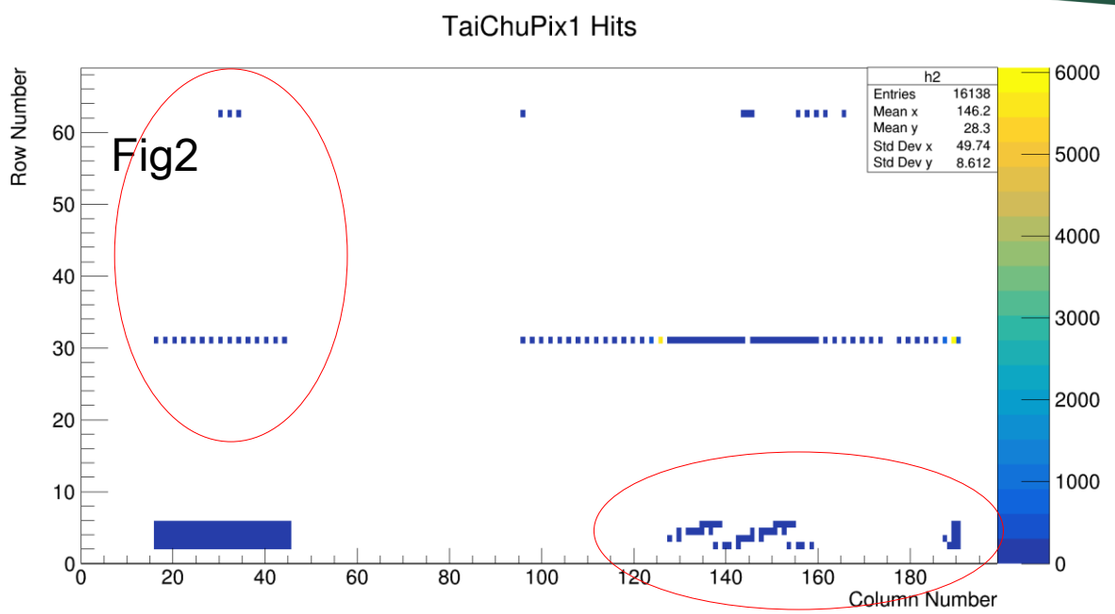


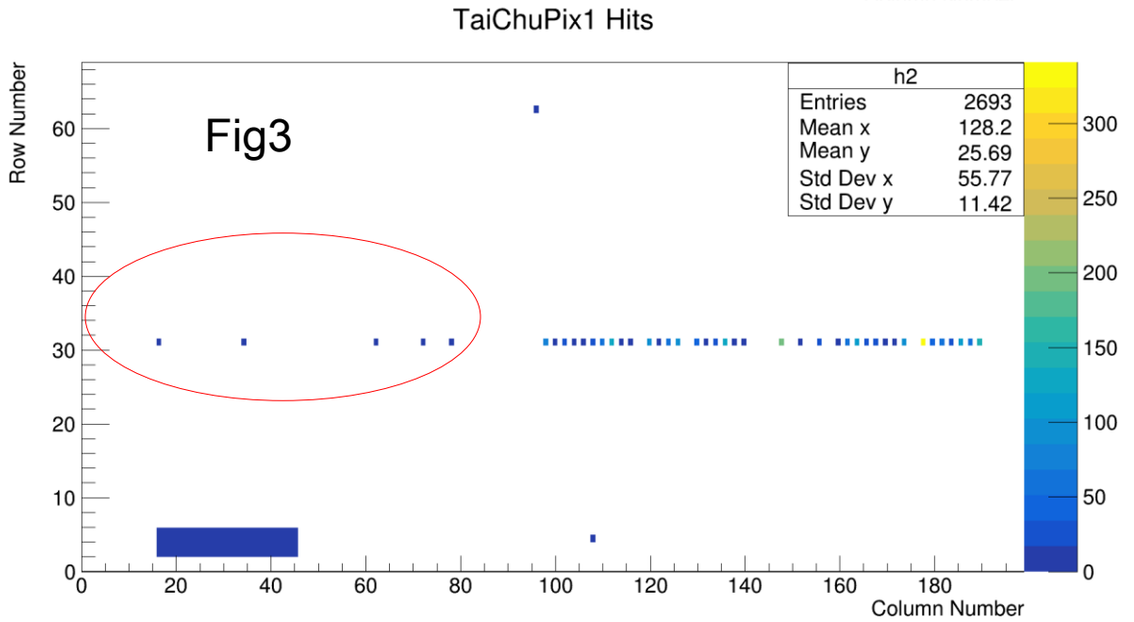
- These plots are from triggerless mode. And with an extra lamp light injection.
- Fig2 is zoomed in from Fig1, and Fig4 is the contour of Fig3.
- Fig1 turned on a specific region with 4x30 pixels, but only part of them was recorded.
- Fig3 turned on the entire pixels, the highest priority pixels is read out many times.

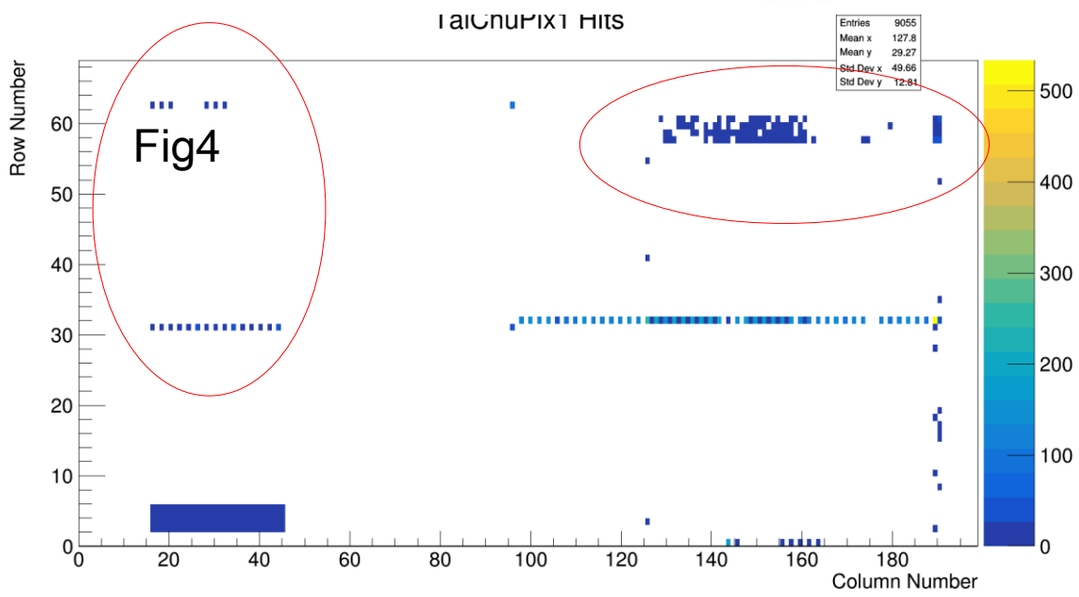
It is important to note that when there is a source of valid data, there will be no noisy points

Some issues from one bit shifting chain









- These plots are from triggerless mode. And run many times of the data acquisition.
- Specify a paticular region with a 4x30 array
- Fig1 is what we are expect, only the right part will generate noisy points and row is 64 or 32.
- But the latch of the shifting chain may not stop at the correct moment. Sometimes it will load the wrong masking information. As it is show in Fig2 and Fig4.

Thanks for your attention.