TaichuPix1 Measurement

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Further test with full chip

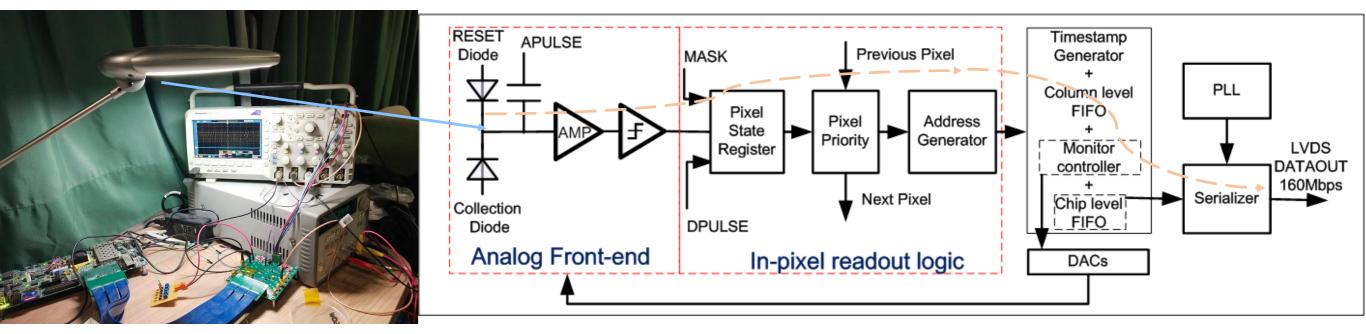


Fig1 test platform for TaichuPix1

- Fig2 shows the hit map of desk lamp shines to the chip.
- It is working at triggerless mode
- Do a loop data acquisition via Ethernet.
- It throws away the repeating data.
- It shields col62~191 with the MASKING and turn on col0~61.(matrix of 192x64)

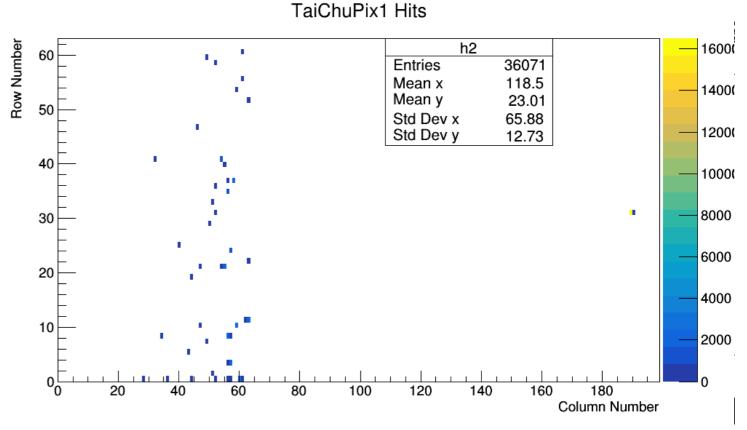
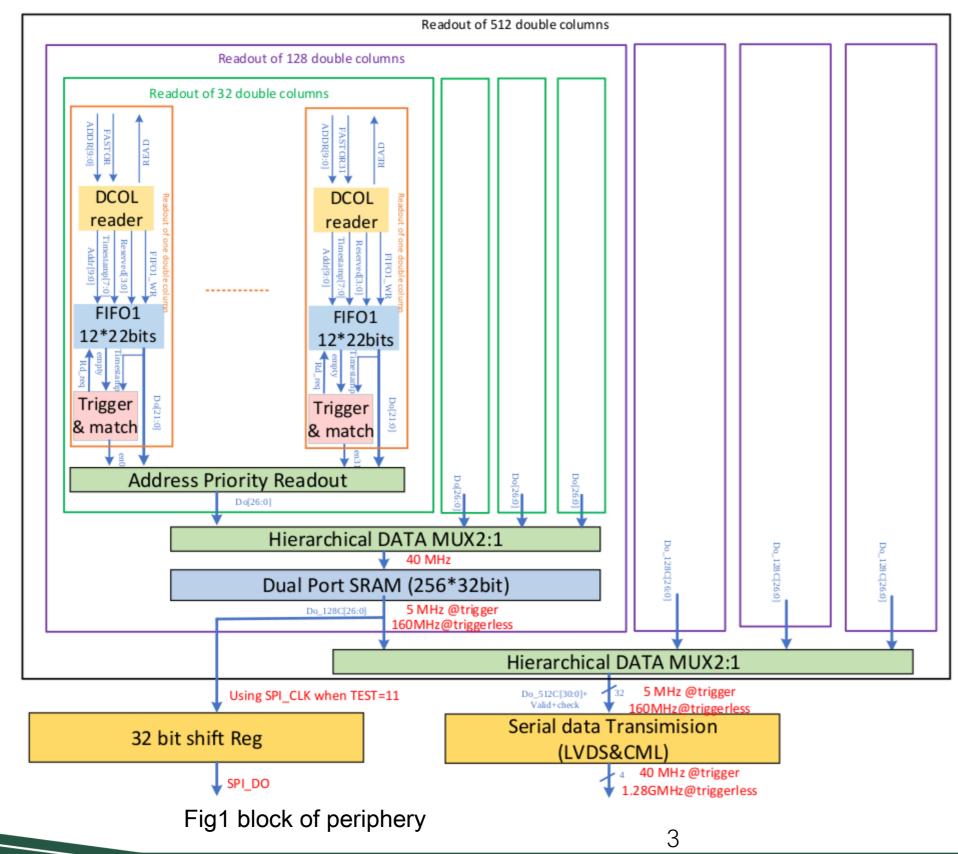


Fig2 LVDS DATA from exposure to desk lamp.



The principle of operation of periphery



- It supports two readout modes: Trigger and Triggerless
- The full speed of Trigger mode is 160Mbps. And for triggerless mode is 4Gbps
- For triggerless mode, it is supposed to read out all the events happens from injection.
- For trigger mode, you could set up a maxium 175ns window to capture the data where you want to record.
- At this moment,LVDS output is at the speed of 160MHz, so that the trigger mode will be better.
- When the output speed is mismatch with the input. It will throw away the rest of data directly.



Strategy to process the raw data

| Open ▼ 🖪 | db26K.t ~/soket/datatest/d | | Save = | | 00 | |
|--|---|--|---|--|--|--|
| 160680a0 160680a0 | Open 🔻 🖪 | cycle_output1.txt ~/soket/datatest/data_process | | Sa | ave 🔳 | |
| 160680a0 ff1b07e0 ff1b07e1 cd0a8140 cd0680a1 cd0680a0 1a87e193 0680a193 1a87e191 1a87e193 0a814193 1a87e192 0a814193 1a87e191 1a87e193 | 010000000101100000110100000 0100000001011000001101000000 | <pre>~/soket/datatest/data_process valid=0 ts=160 valid=0 ts=160 valid=1 ts=224 valid=1 ts=225 valid=1 ts=64 valid=0 ts=161 valid=0 ts=160 valid=1 ts=147 valid=1 ts=147 valid=1 ts=147 valid=1 ts=147 valid=1 ts=147 valid=1 ts=146</pre> | col=44 r col=126 r col=26 r col=26 r col=26 r col=53 r | ow=52 ow=52 ow=88 ow=88 ow=84 ow=52 ow=52 ow=63 ow=63 ow=63 ow=10 ow=63 | pat=0 pat=0 pat=3 pat=3 pat=0 pat=0 pat=0 pat=0 pat=0 pat=0 pat=0 pat=0 pat=0 pat=0 | |
| 0a814193 1a87e191 0a814193 1a87e191 1a87e193 931a87e1 931a87e1 920a8141 931a87e1 | 110010011000010101000000011100000 1100100010 | valid=1 ts=147 valid=1 ts=145 valid=1 ts=147 valid=1 ts=147 valid=1 ts=147 valid=1 ts=145 valid=1 ts=145 valid=1 ts=145 valid=1 ts=225 valid=1 ts=225 | <pre>col=53 r col=53 r col=53 r col=21 r col=53 r col=21 r col=53 r col=53 r col=53 r col=53 r col=53 r</pre> | ow=10 ow=63 ow=63 ow=10 ow=63 ow=10 ow=63 ow=63 ow=63 ow=84 ow=84 | pat=0 pat=0 pat=0 pat=0 pat=0 pat=0 pat=0 pat=0 pat=3 pat=3 | |
| 910a8141 930a8141 931a87e1 931a87e1 931a87e1 931a87e1 931a87e1 910a8141 920a8141 931a87e1 | 101100000110010010000010101000001 10100000110010010000010101000000 11110000110010011000010101000001 10100000110010001000010101000000 1010000011001001000010101000000 10100000110010011000010101000000 11110000110010011000010101000000 11110000110010011000010101000000 111100001100100110000101010000011 11110000110010011000011010000011 11110000110010011000011010000011 11110000110010011000011010000011 10100001100100110000110100000011 | valid=1 ts=65 | <pre>col=36 r col=38 r col=38 r col=34 r col=38 r col=38 r col=38 r col=38 r col=38 r col=38 r</pre> | ow=84 ow=84 ow=84 ow=84 ow=84 | pat=3 pat=3 pat=3 pat=0 pat=0 pat=3 pat=3 pat=3 pat=3 pat=3 pat=0 | |
| 931a87e1 931a87e1 910a8141 910680a1 931a87e1 931a87e1 930a8141 | $\begin{array}{c} 10100000110010000010101000000\\ 10100000110010010000010101000000\\ 11110000110010011000110101000011\\ 111100001100100110001101010000011\\ 111100001100100100010$ | valid=1 ts=65 valid=1 ts=225 valid=1 ts=225 valid=1 ts=225 valid=1 ts=225 valid=1 ts=65 valid=0 ts=161 valid=1 ts=225 valid=1 ts=225 valid=1 ts=65 | <pre>col=36 r col=38 r col=38 r col=38 r col=38 r col=34 r col=34 r col=38 r col=38 r col=38 r</pre> | ow=84 ow=84 ow=84 ow=84 ow=84 ow=84 ow=84 ow=52 ow=84 ow=84 ow=84 | pat=0 pat=3 pat=3 pat=3 pat=3 pat=0 pat=0 pat=3 pat=3 pat=3 pat=0 | |

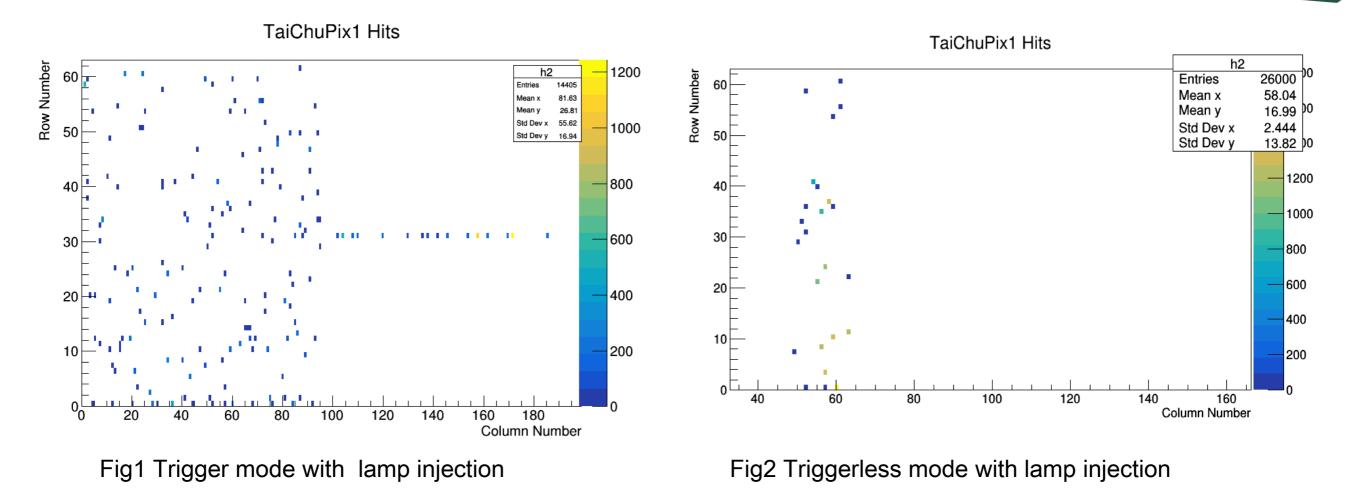
• Here is the example to show how I process the data.

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- a)I received the 32bits raw data via Ethernet.(Here is a 5.8M file with 650K data)
- b)Then try to find pattern(1111110000).
- c) Because there is no frame header of LVDS output, and the order of 32 bits data will shift from time to time. As it shows here,the upper half is different the lower half.
- d) Then shift the proper bits for all the data.(here raw data shift 23bits to the left)
- e)Then keep the data with valid==1 and pattern==0
- f) To improve the accuracy,add an extra condition with Timestamp=147, so that I could throw away most of garbage data.



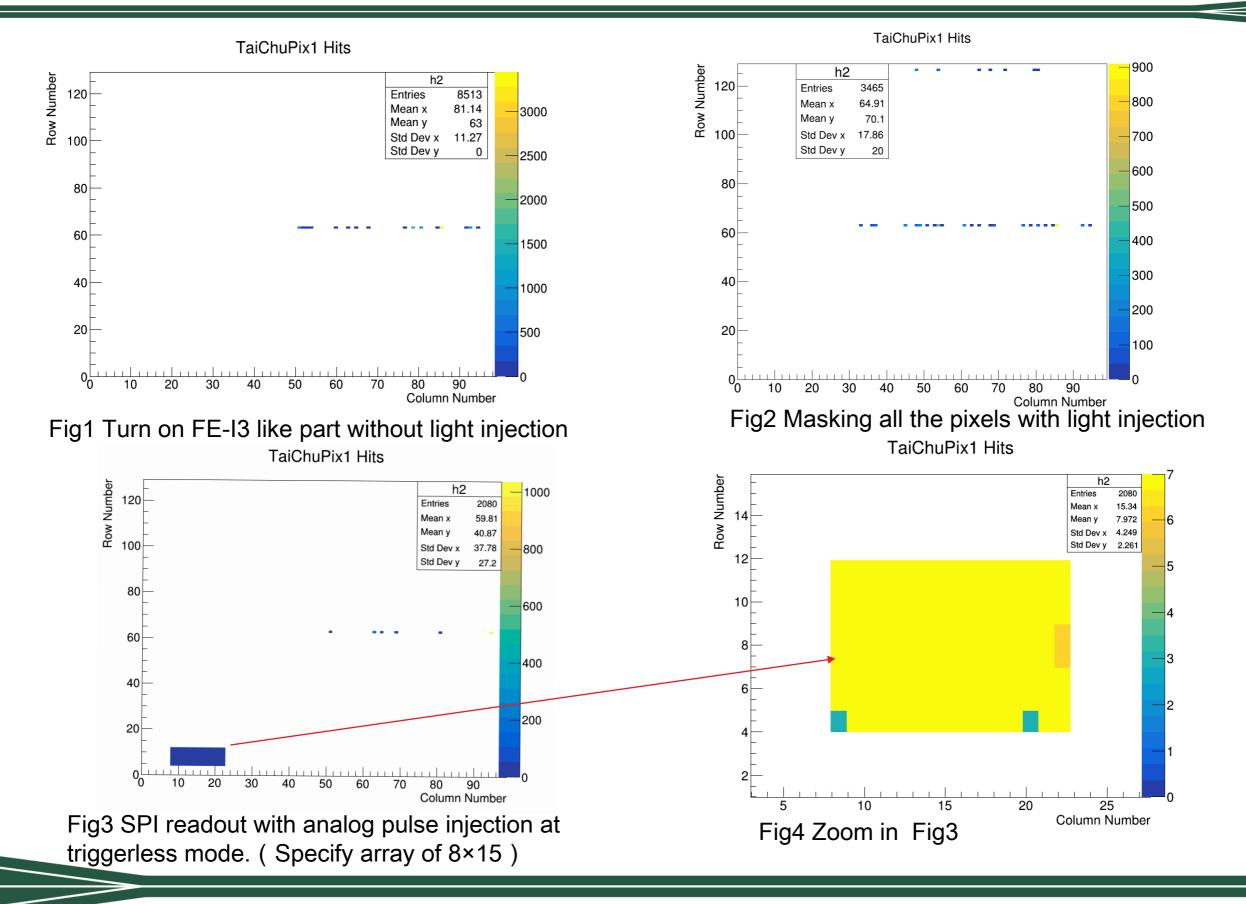
Further test with full chip (Internal DAC)



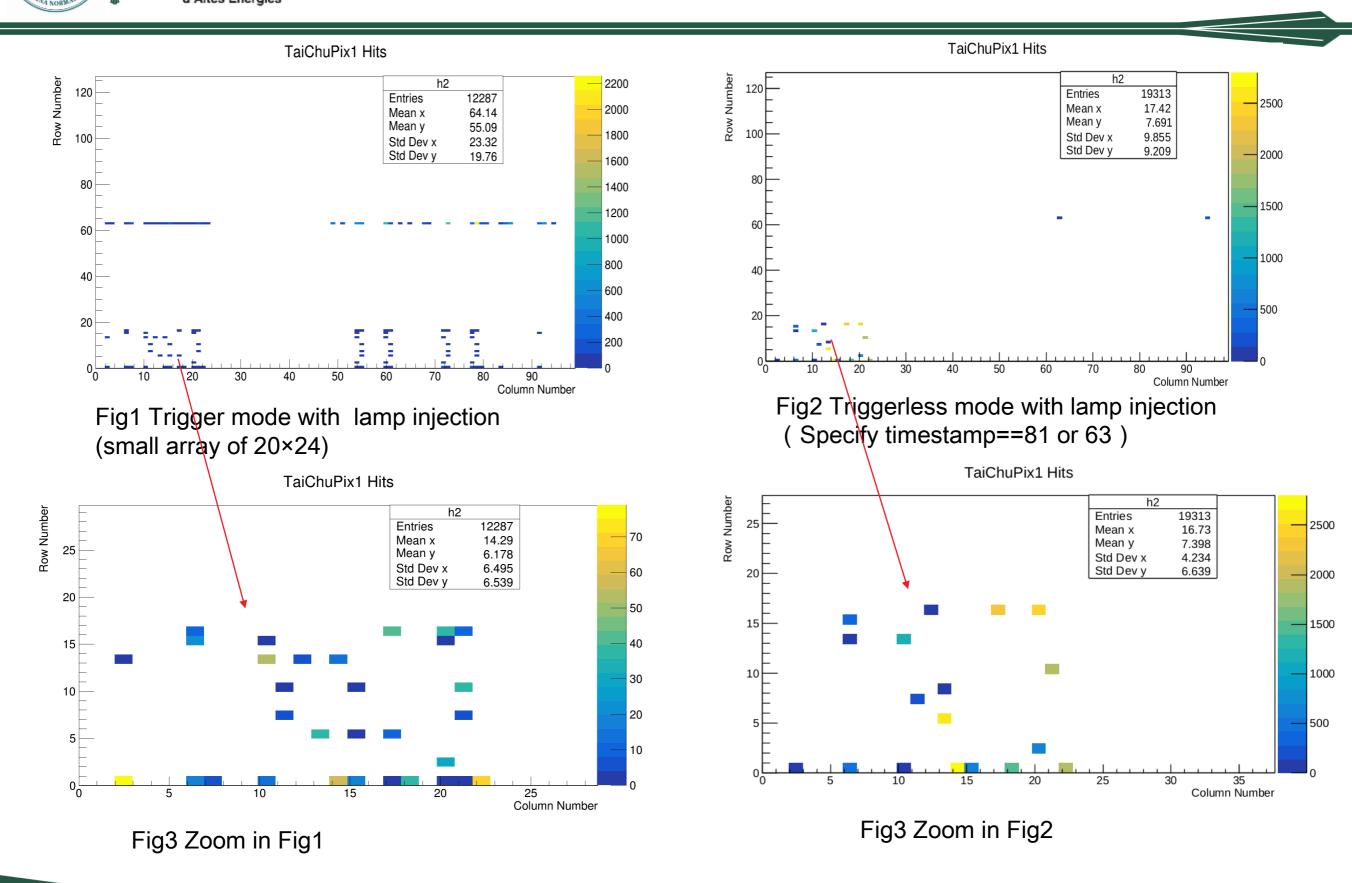
- In same condition of the test platform with different readout mode setup.
- Only left half of FE-I3 like part turns on.
- Trigger mode could show up a larger scale of hits region.
- Triggerless mode could only readout a small range of data due to the readout speed
- The plot results was from internal DAC bias to analog front end.



Baseline of the TaichuPix1 chip



Further test with a particular region





DATA Analysis(COL0~COL95)

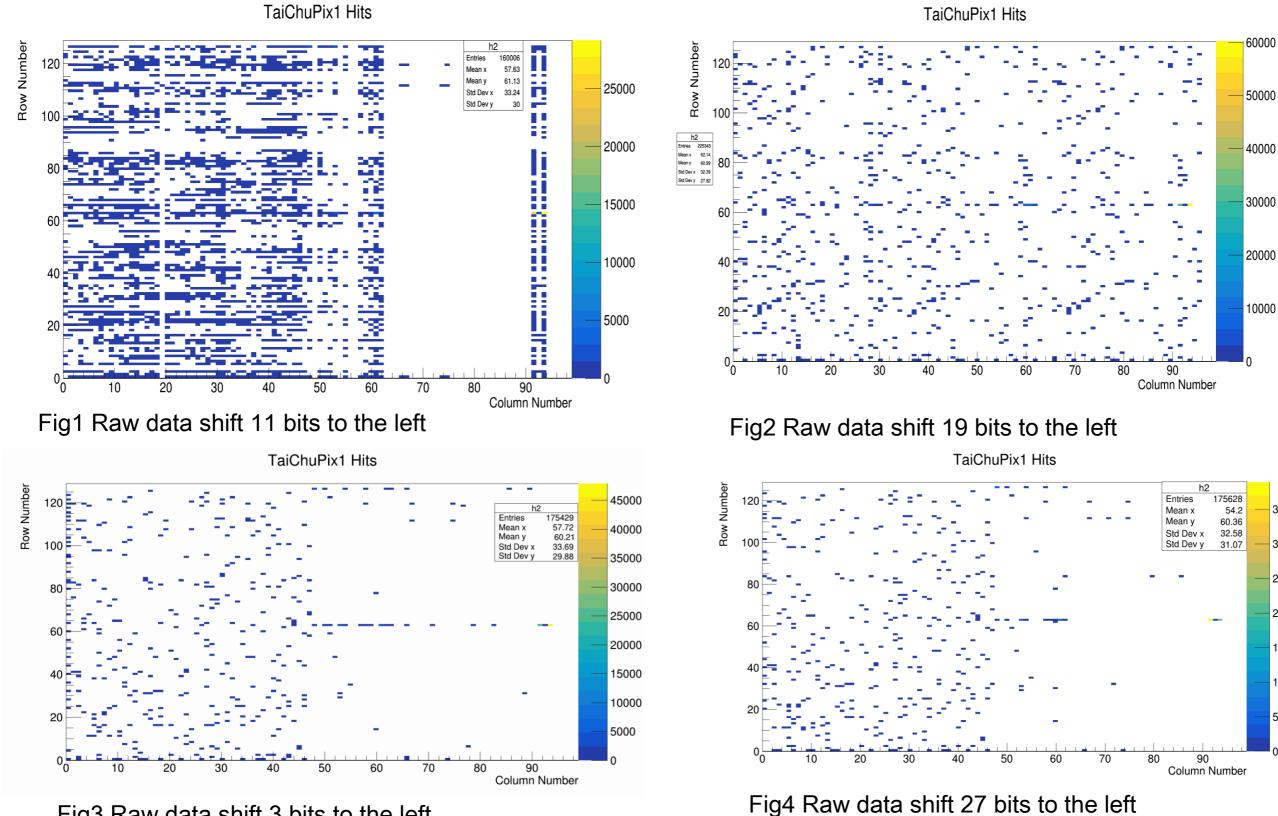


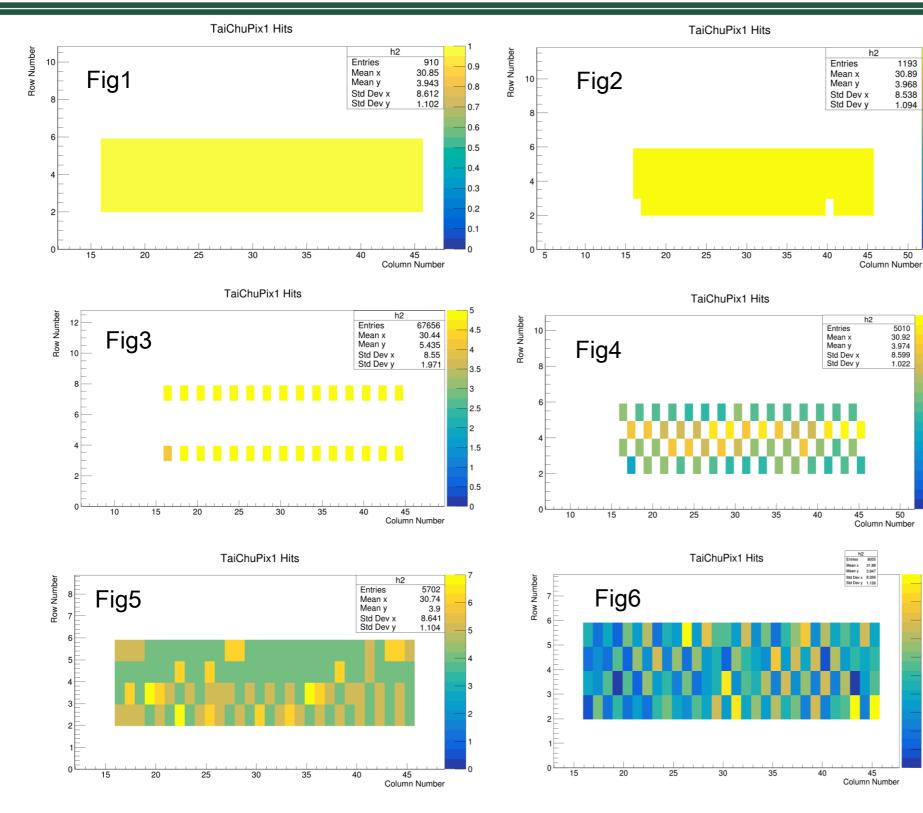
Fig3 Raw data shift 3 bits to the left



Analog front end parameter

| - | E | Bias | IE | BIAS | ITH | R | IDB | V | CLIP | VCA | SP | VCA | SN | VCA | SN2 | VRE | SET | | | |
|------------------------|-----|----------------|-------------|------------------|---------|----------|------|--------|-----------------------------------|-----------------------------------|--------|-------------------|---------------|------------------|------|---------|--|-----|------------------------------|--------|
| Table 1 (Chip2 | | esign alue | 44 | 10 nA | 4.5 r | nA ´ | 1 µA | 0/0 | 0.2 V | 0.6 | V | 0.5 | 5 V | 0.5 | 5 V | 1.4 | I V | | | |
| Internal DAC) | | onfig. alue | 44(|)nA | A 1.5nA | | uA | 0.068V | | 0.6 | SV 0.5 | | 5V 0.5 | | V | 1.71V | | | | |
| Table O | _ | Bias | | IBIAS | | ITHR | | DB | VC | | | SP | VCASN | | VCAS | SN2 VRE | | | | |
| Table 2 (Chip2 | | Desię valu | | 440 n/ | 4 4 | 4.5 nA | 1 | μA | 0/0. | 2 V | 0.6 | 5 V | 0.5 | 5 V | 0.5 | V | 1.4 | V | $\left(\circ \circ \right)$ | |
| External BIAS | | Confi valu | g. | 440nA | . 3. | .5nA | 1u | A | 0.04 | 3V | 0.6 | 4V | 0.5 | 7V | 0.68 | 3V | 1.7 | 1V | | |
| VBIAS=900mV |) _ | | | | | | | | | | | | | | | | | | _ | |
| Table 2 | | Bi | as | IBIA | S | ITHR | | IDB | V | CLIP | VC | CASP | VC | ASN | VC | ASN2 | VRE | SET | _ | |
| (Chip2 External Bl/ | ١S | | sign ue | 440 | пA | 4.5 nA | | 1 µA | 0/ | 0.2 V | 0 | .6 V | 0. | 55 V | 0. | 5 V | 1.4 | 4 V | | |
| VBG=800m VBIAS=900m | V | | nfig. ue | 440 | nA | 4.5nA | • | 1uA | 0. | 043∨ | ′ 0 |).6V | 0. | 55V | 0.5 | 5V | 1.7 | 1∨ | _ | |
| Tak tra | , | ÷ | | Noise Filter Off | | Tek Stop | | | | | _ | Noise Filter Off | i | Tek PreVu | | | <u> </u> | | – Noise Filte | er Off |
| | | | had a | <10Hz -40.2mV | | | 3 20 | | 00,us -1.33 Mean 51 Mean 7; | 100.us) (2) / 35mV (4) 20mV | ***** | <10 H2 -19.0mV | çet ayet in A | | | | 2.00,us -1.716 1 Mean 52 3 Mean 68 | | -480mV <10 Mean -13.4mV | |





- These plots are from
- triggerless mode.

0.9

0.8

0.7

0.6

0.5

0.4

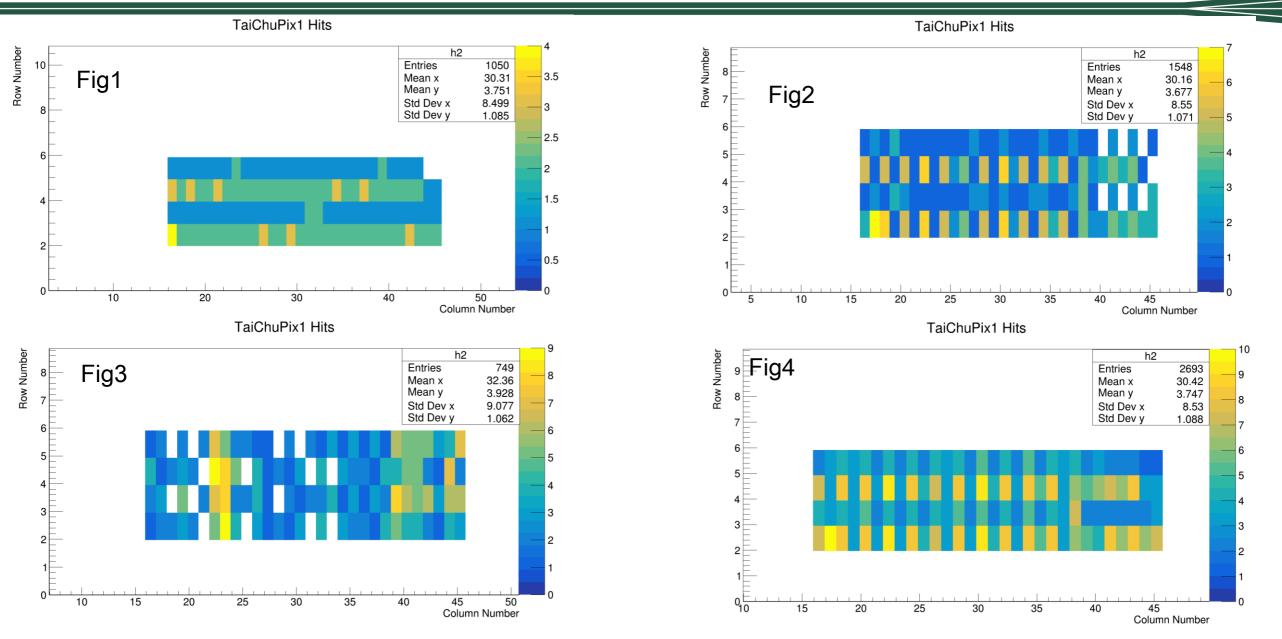
0.2

0.1

20

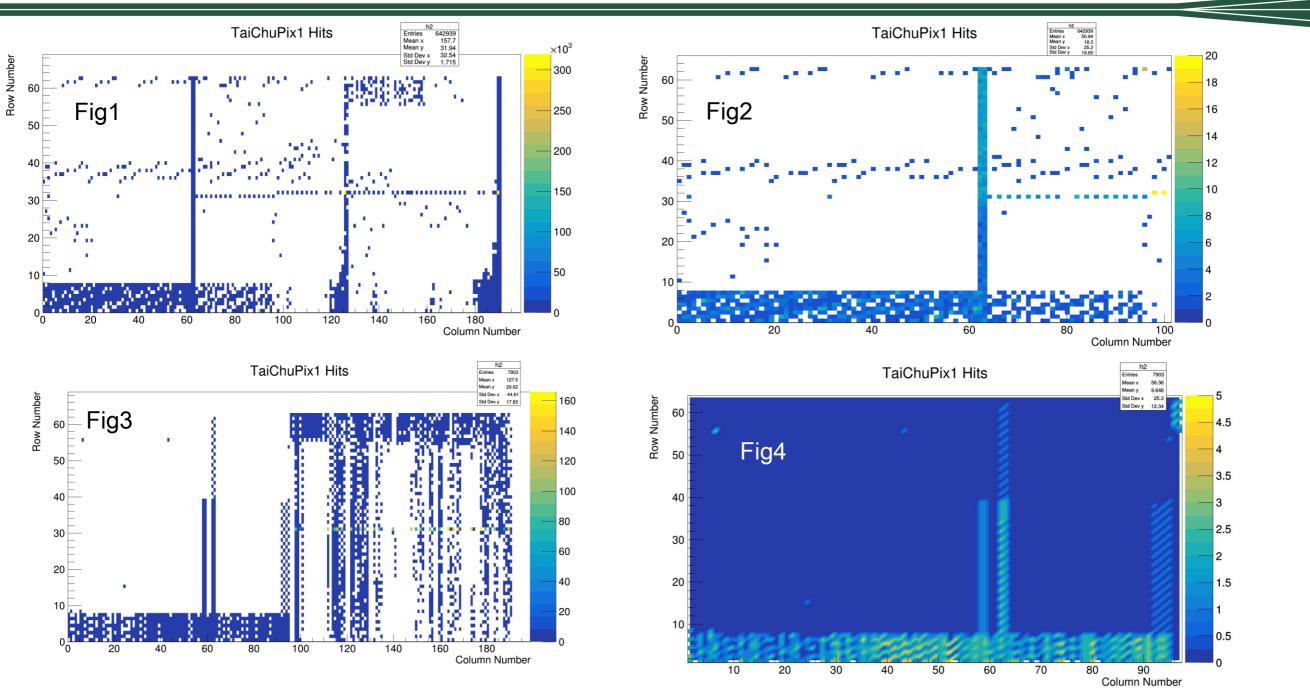
- Specify a paticular region with a 4x30 array
- Fig1 to Fig 4 show the different shapes of the particular region.
- Fig1 and Fig2 are the results from one run.
- Fig3 and Fig4 are the multiple results with different timestamp.
- Fig5 and Fig6 are the results of multiple cases.





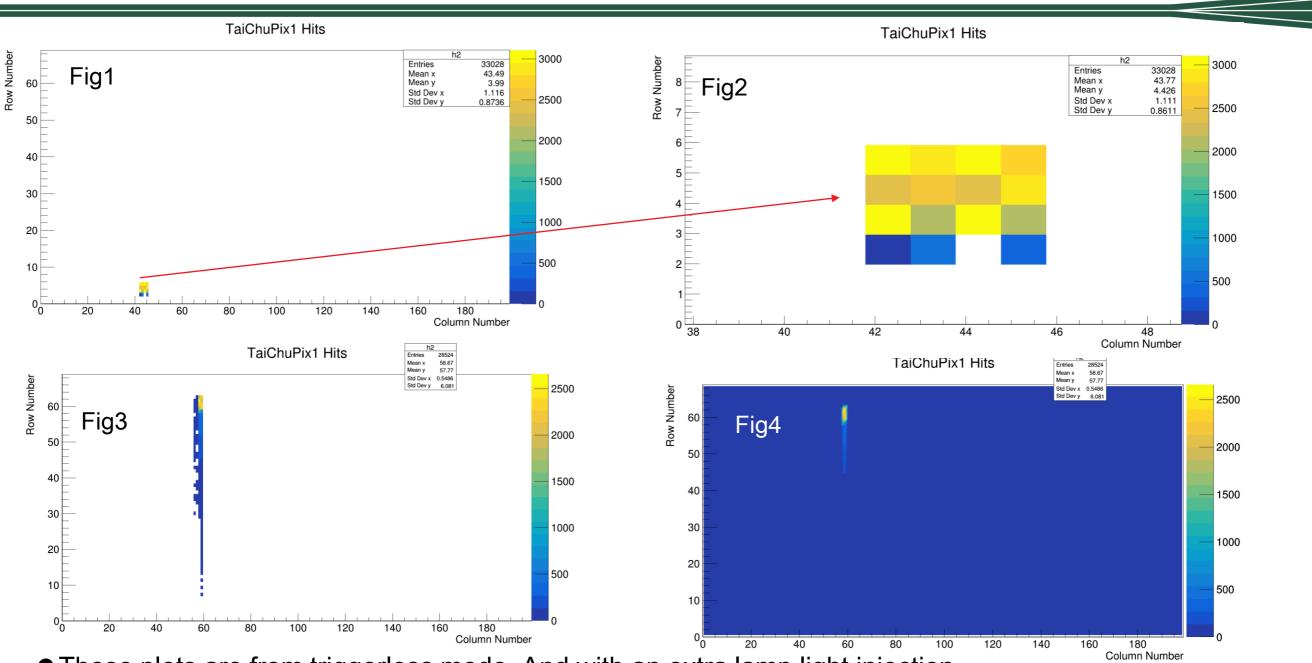
- These plots are from trigger mode.
- Specify a paticular region with a 4x30 array
- Fig1 and Fig 2 show the different shapes may appear in each run of the chip.
- Fig3 show the chip is running with extra lamp light injection.
- Fig4 is the plot which integrates several times of the results.





- Fig1 and Fig2 are from triggerless mode while the Fig3 and Fig4 are from trigger mode.
- These results are turning on the entire array of the the chip with light injection.
- Fig2 is the enlarged view of Fig1 left part(FE-I3 like scheme).
- Fig4 is the contour of the left part of Fig3.



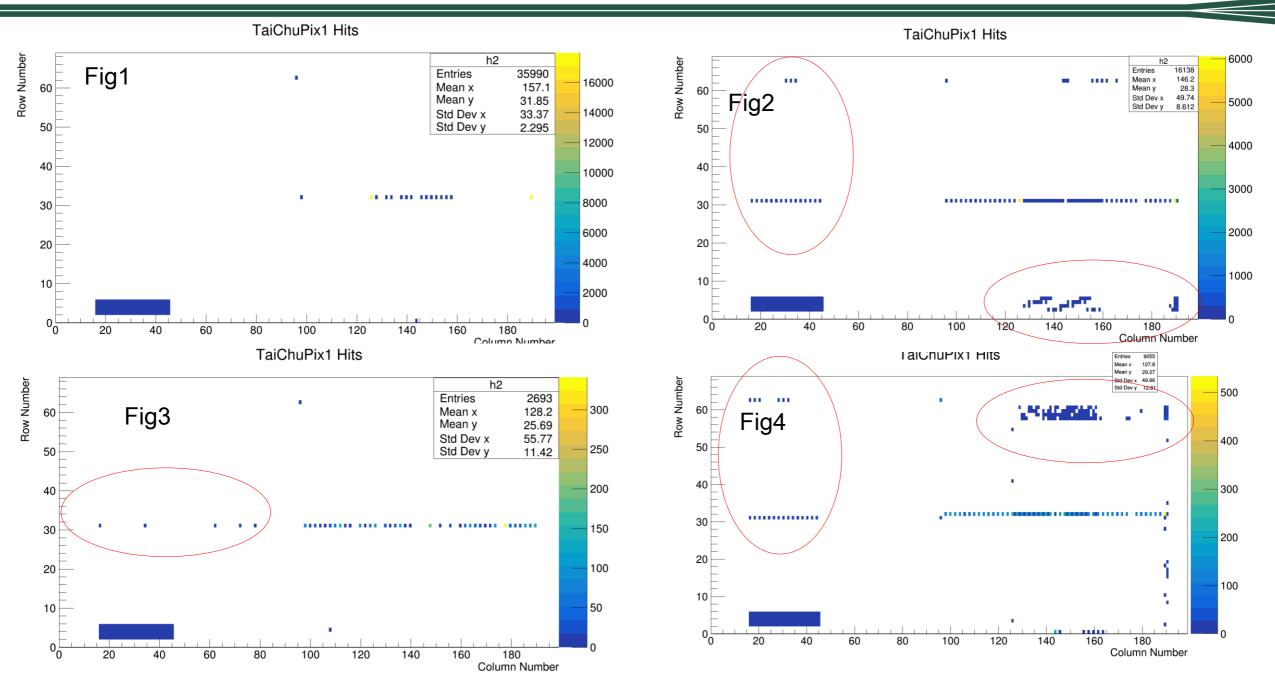


- These plots are from triggerless mode. And with an extra lamp light injection.
- Fig2 is zoomed in from Fig1, and Fig4 is the contour of Fig3.
- Fig1 turned on a specific region with 4x30 pixels, but only part of them was recorded.
- Fig3 turned on the entire pixels, the highest priority pixels is read out many times.

It is important to note that when there is a source of valid data, there will be no noisy points



Some issues from one bit shifting chain



- These plots are from triggerless mode. And run many times of the data acquisition.
- Specify a paticular region with a 4x30 array
- Fig1 is what we are expect, only the right part will generate noisy points and row is 64 or 32.
- But the latch of the shifting chain may not stop at the correct moment. Sometimes it will load the wrong masking information. As it is show in Fig2 and Fig4.



Thanks for your attention.

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