Optical links for future high energy applications

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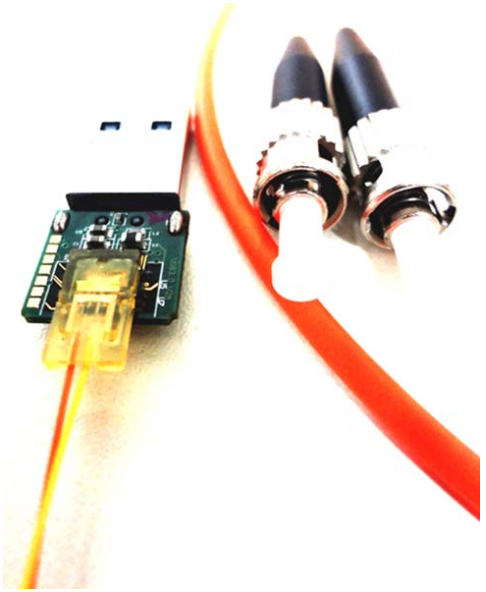
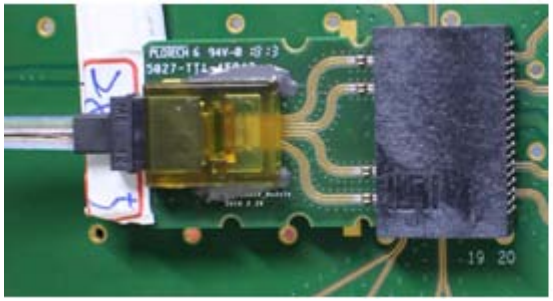




CEPC 2020.12.02
https://indico.ihep.ac.cn/event/13347/

Why Optical links

- Low Mass
  - Optical fiber versus copper wires
  - Radiation hardness sustains with chosen types of fibers
  - OM4 type fibers transmit 25 Gbps
- Long distance data transmission
  - Copper wires can not do > 10 Gbps over 5 m
  - Optical links with 850 nm VCSEL, Multi-mode fiber for ~200 m
- Optical Transceiver R&D issues
  - *FEB output: requires rad-hard EO/OE transceiver*
  - *Counting room: may use commercial high bandwidth OE receiver*
  - *Transceiver assembly in the industry*

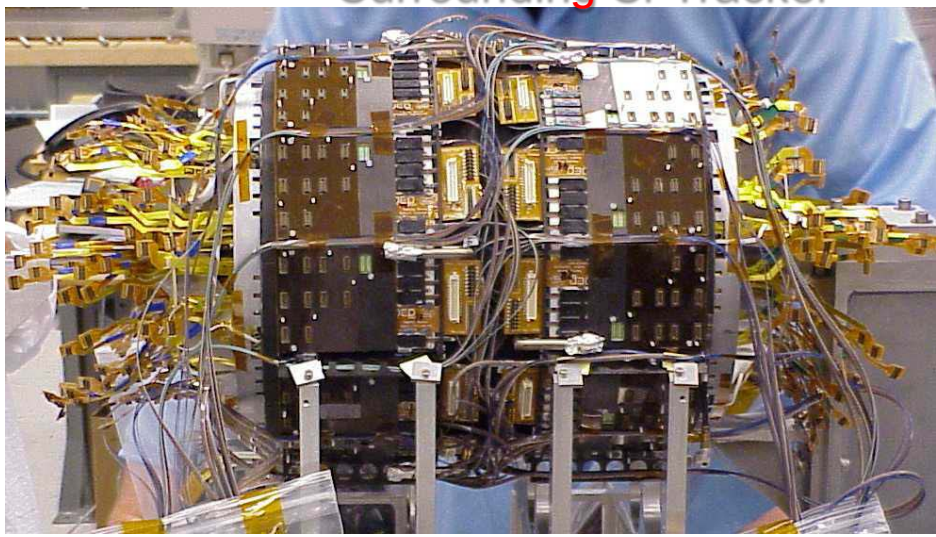
  Choices of VCSEL/PD to fiber coupling

  Customized connectors for compactness
  - *CMOS laser driver , PD TIA*

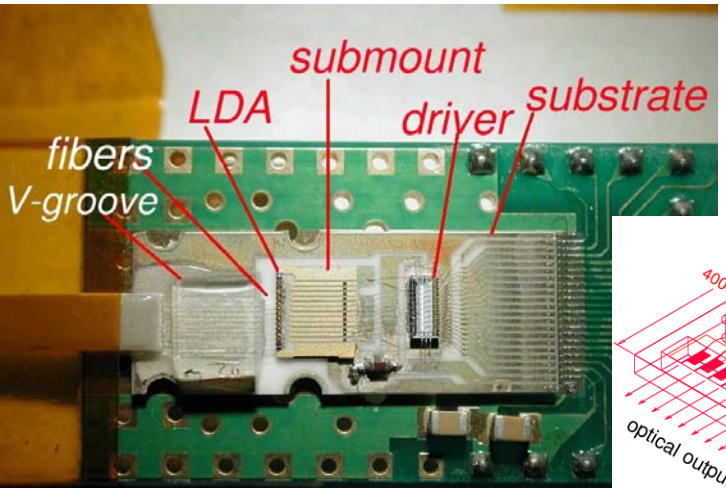
  Requires Custom design for Rad-hard and protocol

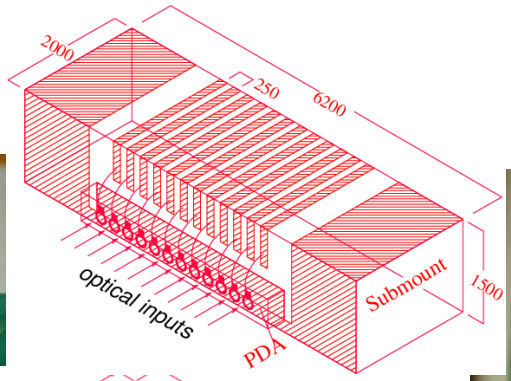
CDF has the first HEP optical link

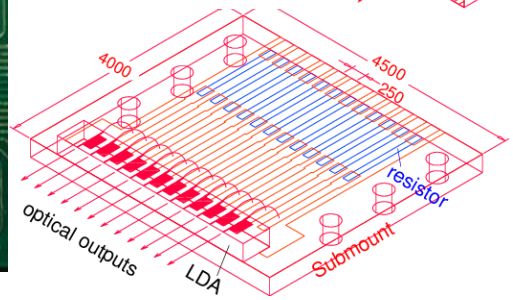
PortCard with transmitters
Surrounding Si-Tracker

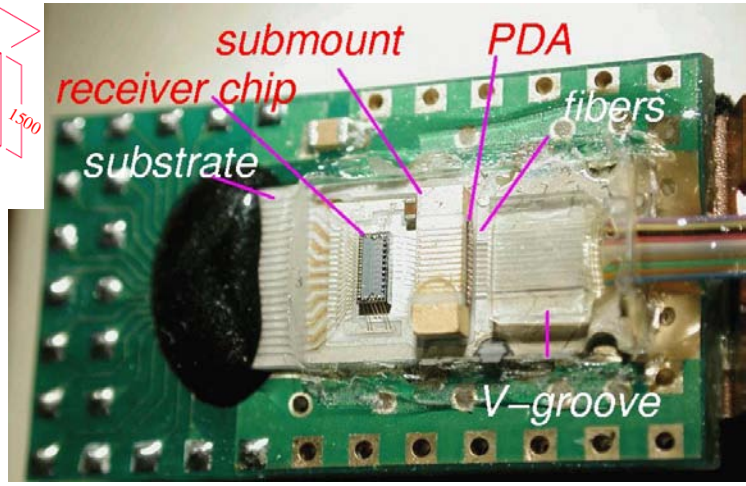


- Edge emitting 1550 nm laser
  - Customized 12-ch laser diode
  - V-groove coupling fibers to Lasers
  - Customized Laser E-O driver
- Alignment, production yield
  - Laser window coupling to fiber
  - Poor uniformity on light power
- Light coupling
  - 90^{o} turn, fiber to PD

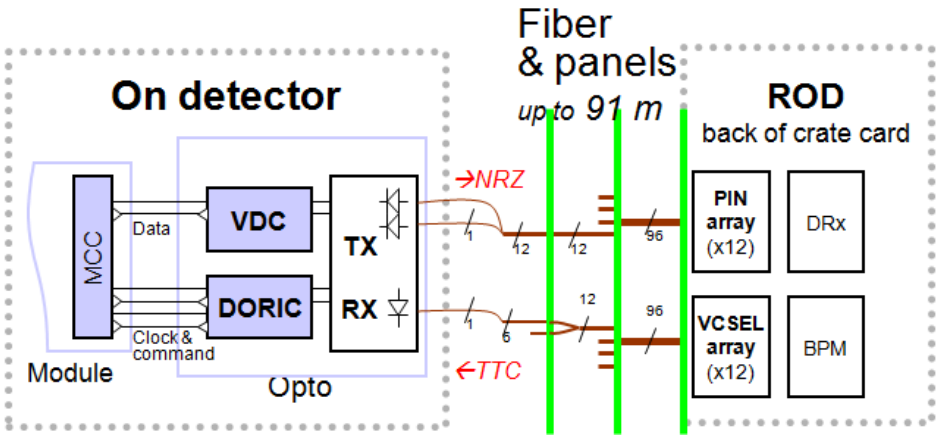


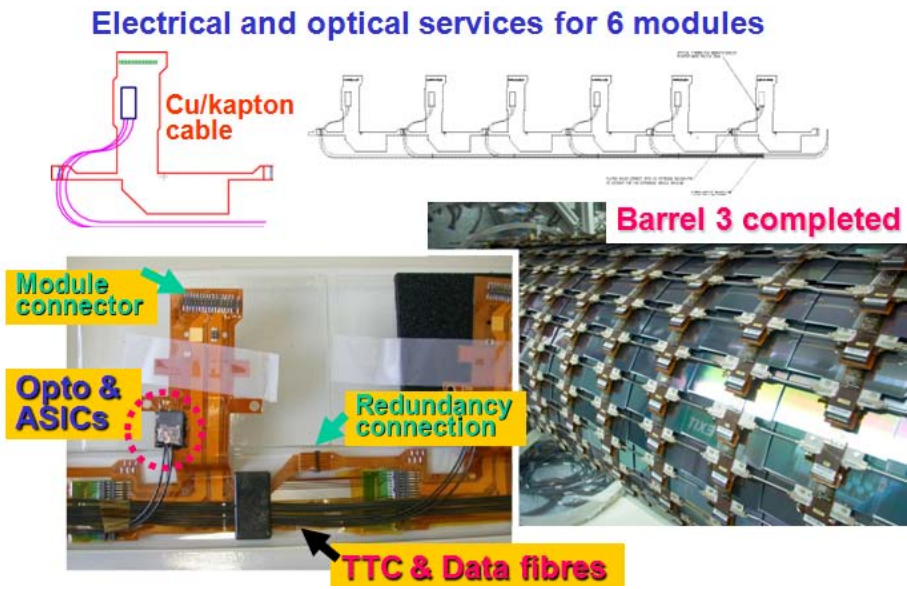






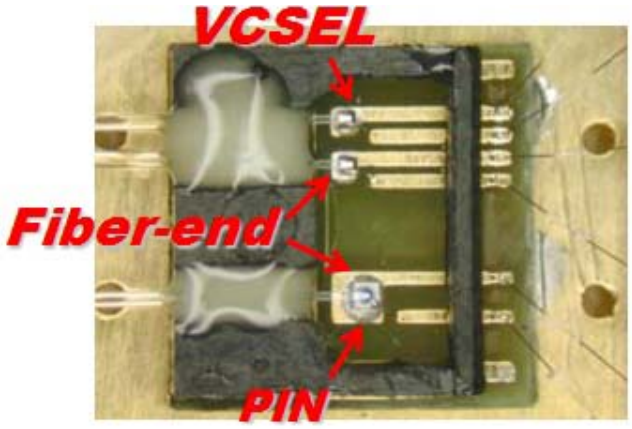
ATLAS silicon tracker Optical link

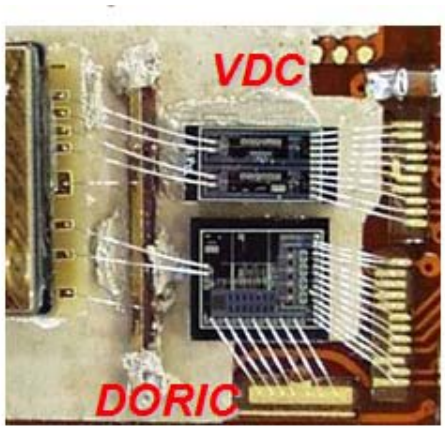


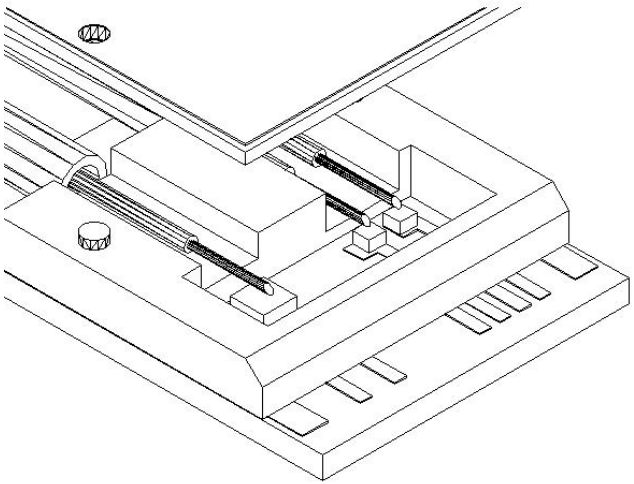


Transceiver module

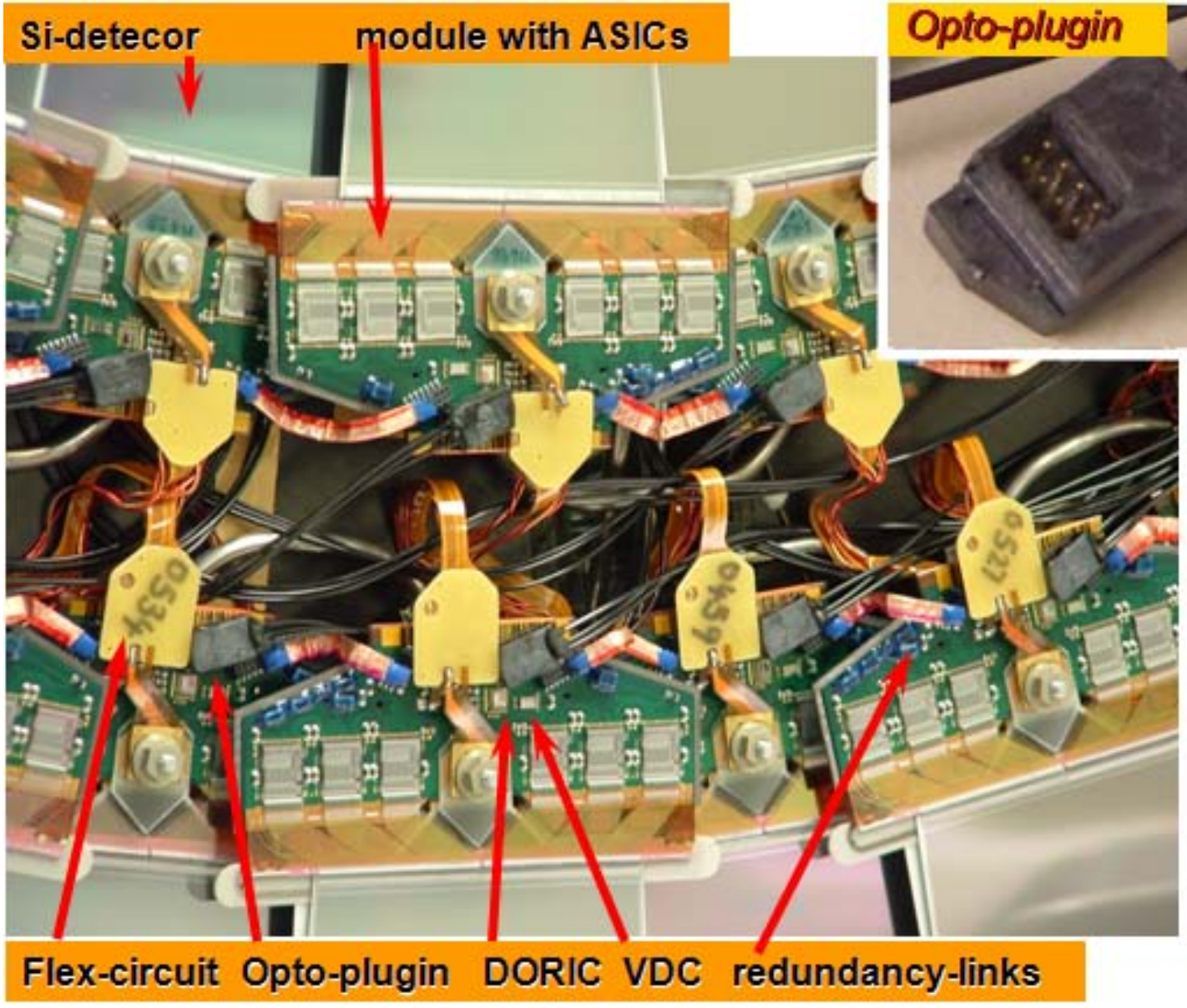
- 1 RX PIN + DORIC for clock+ctl
- 2 TX VCSEL + VDC for data
- 45^{o} fibre end, mirror to VCSEL, PIN





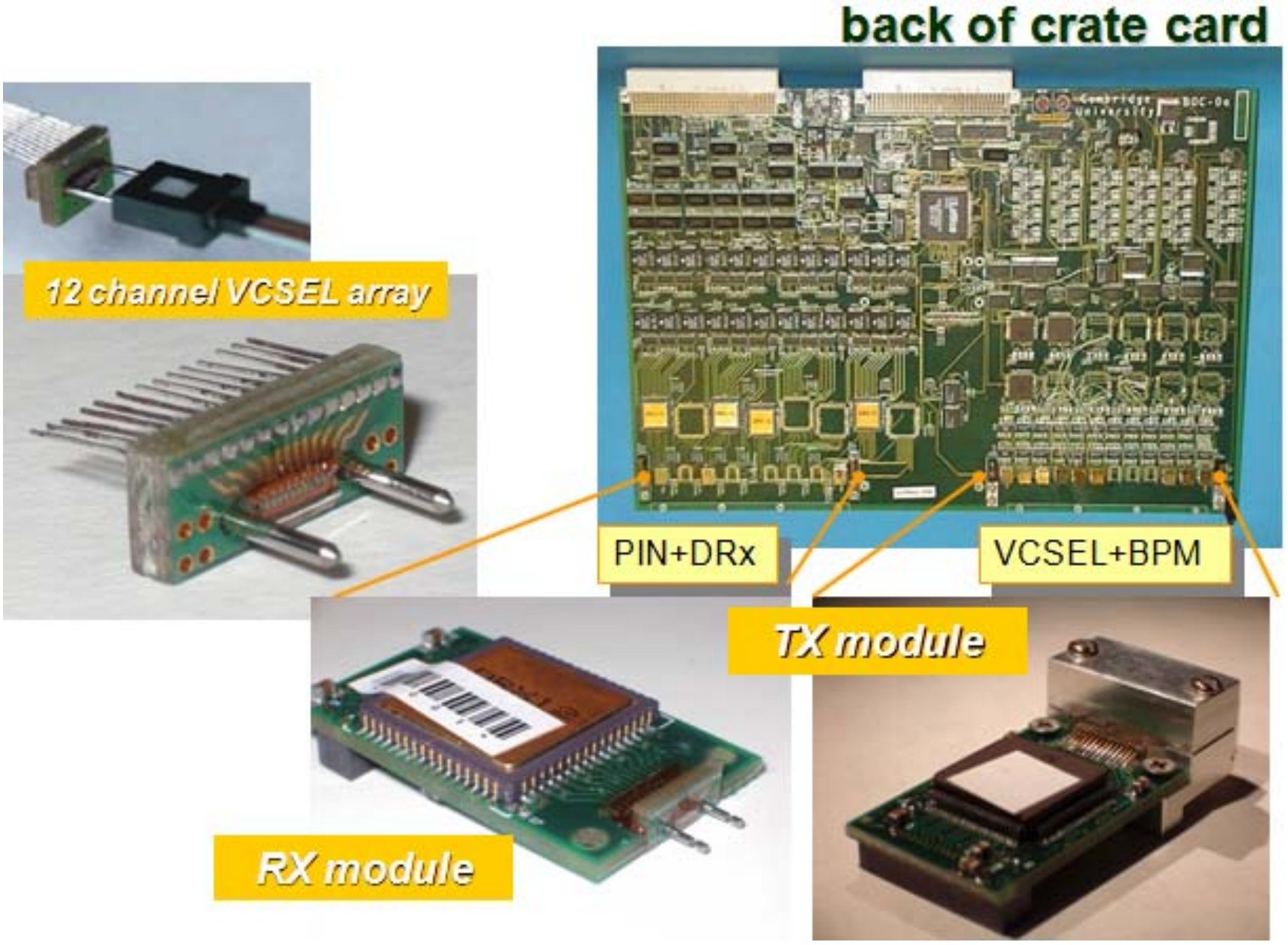


ATLAS silicon tracker end-cap optical plug-in



Endcap hardness
with
6 opto-packages

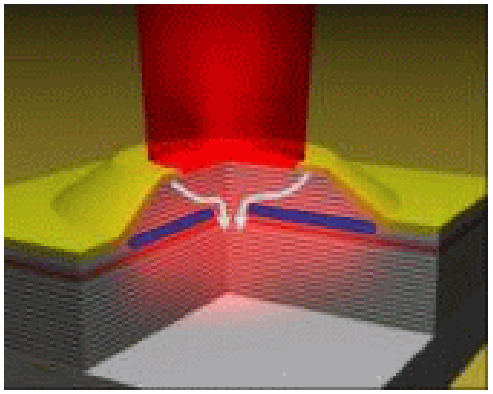
ATLAS silicon tracker off-detector



VCSEL reliability

- VCSEL 850 nm → Si PIN diodes.
- ***Very radiation hard***
- ***ESD damage***
- ***Humidity are protected (ATLAS had suffered)***

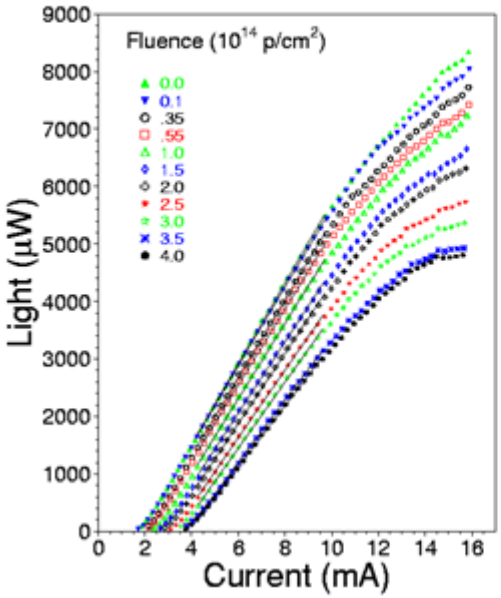
VCSEL
active layer ~ 10 μm
Aperture ~8 μm

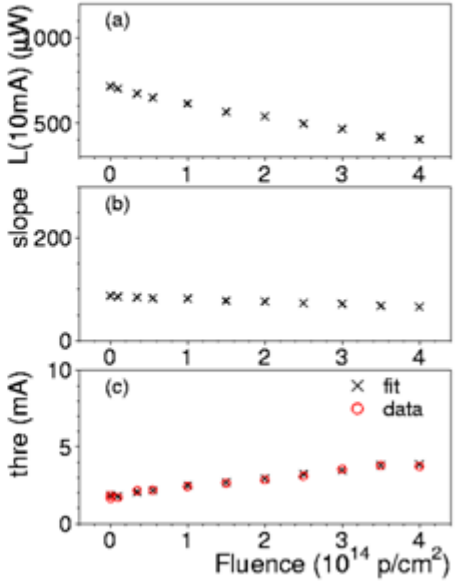


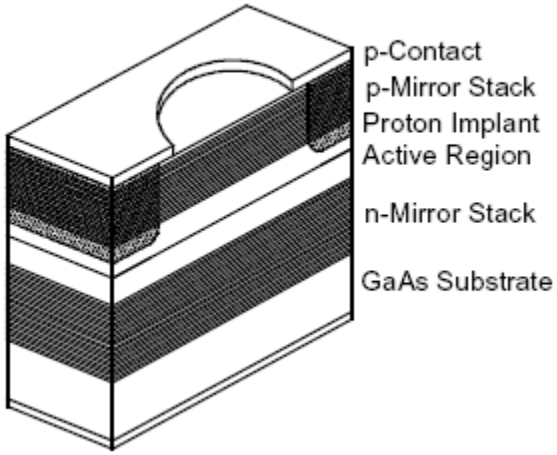
- **VCSEL damage is linear to fluence**

online observation 4x10^{14} (200 MeV) p/cm^2

Oxide-confined VCSEL







Industrial transceivers are well developed

producing customized HEP modules:

1. we choose industrial assemblies

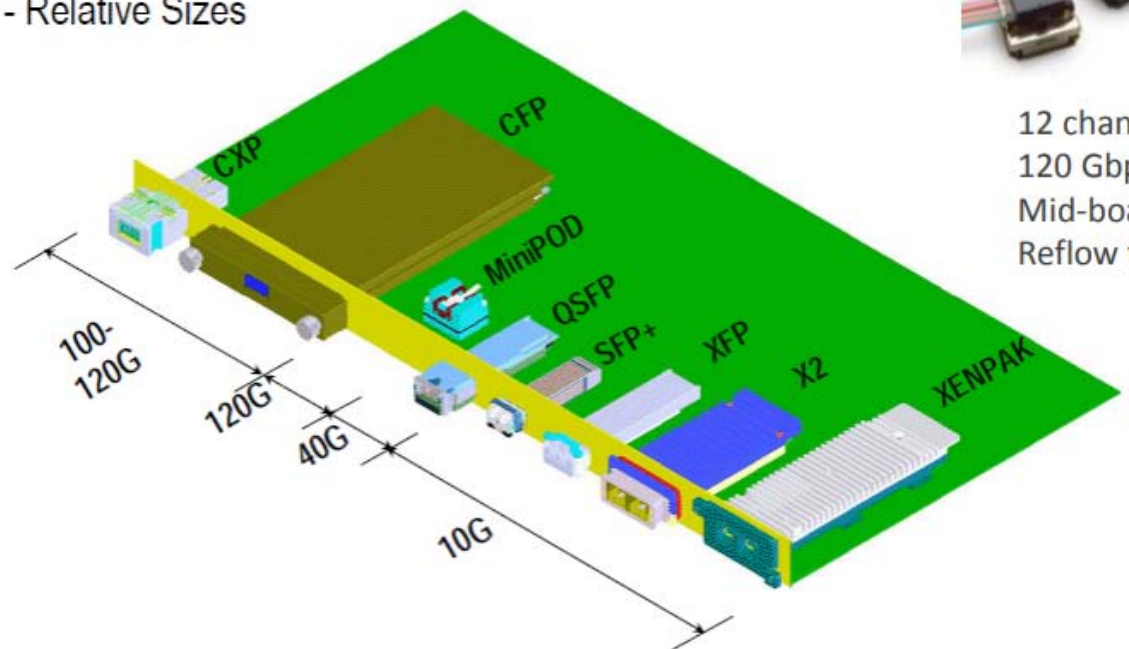
2. we design PCB and IC chips

SFP+ and QSFP are the easiest applicable with LC/MT fiber connectors

HEP needs more compact/low mass connectors

Optical Transceivers

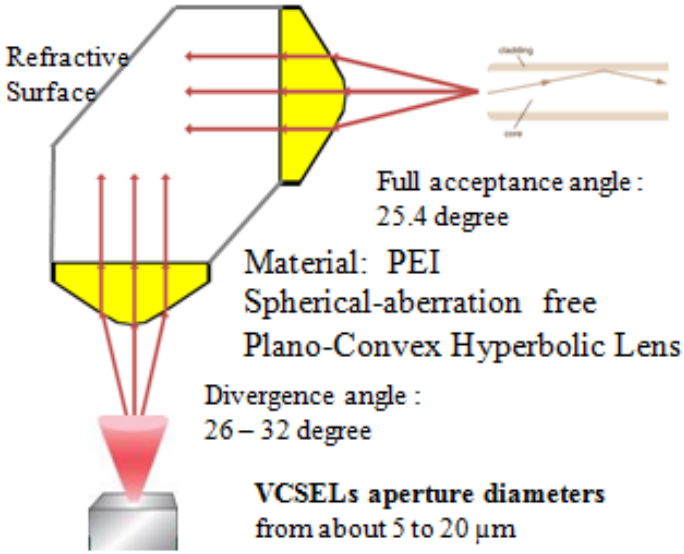
Transceiver Package or Form Factor
- Relative Sizes



12 channel Tx or Rx
120 Gbps (10 Gbps/channel)
Mid-board mountable
Reflow technology

VCSEL light coupling

Mechanism with a Lens Coupling to MM fiber



- ***Industrial off-the-shell***
  many choices of Lens or Mirror
  for VCSEL/PD - fiber coupling
- ***Robotic alignment in assembly***
  precision to ~ 1 μm
  VCSEL emits wider at higher currents

e.g. device at 8 mA
differentiate wave length

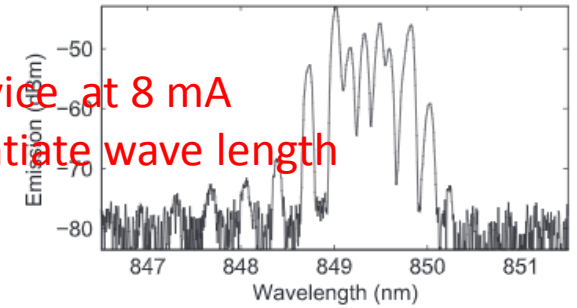


Fig. 2. A typical emission spectrum of a multitransverse mode VCSEL at a bias current of 8 mA.

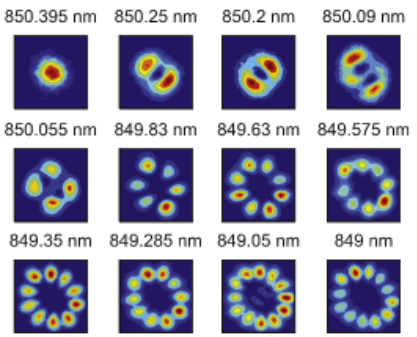
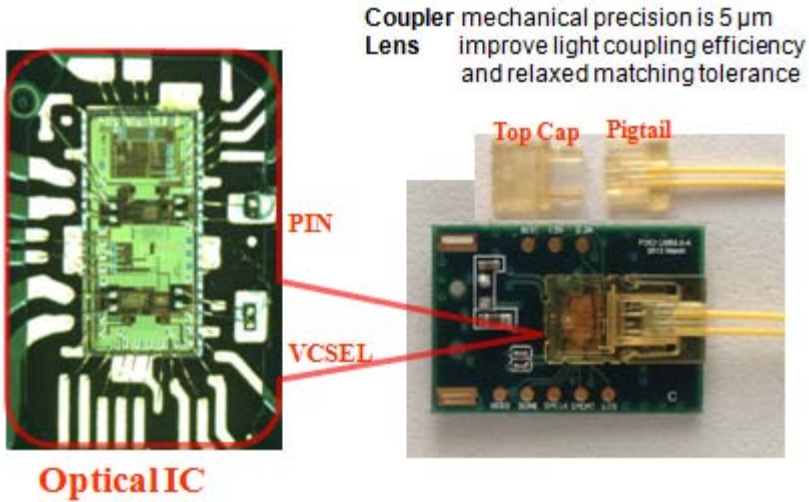


Fig. 3. The spatial-spectrally resolved VCSEL's transverse mode at bias current 8.0 mA.

Optics Comm. 285 (2012) 4117

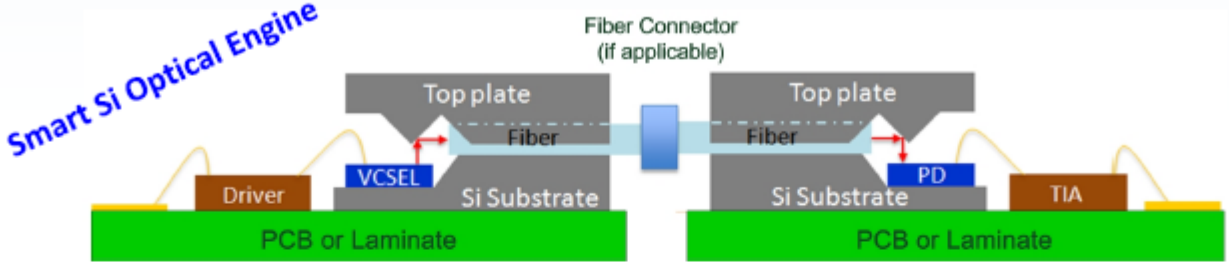
FOCI commercial USB3 transceiver



Centera solution

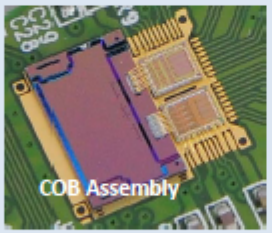
Expensive and protective collaboration not established

Si MEMS Platform as Parallel Optical Engine

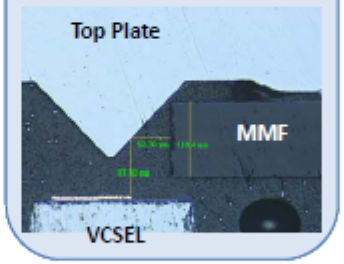


Active Part of SiOB

Circuit Integration



Cross-Section

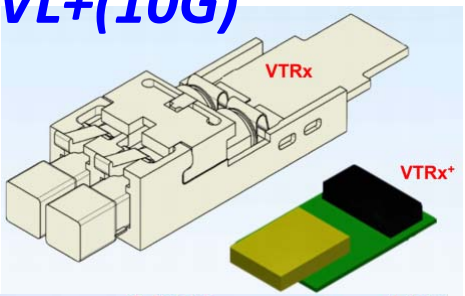


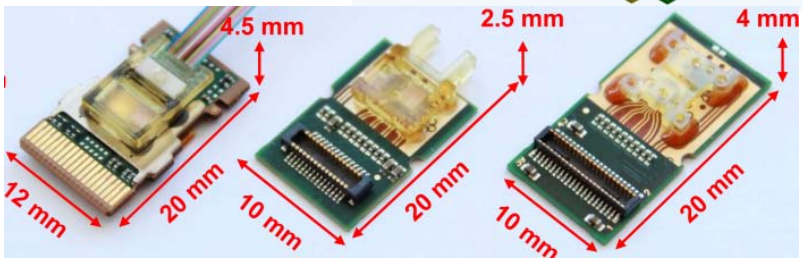
25-Gbps Eye

- SiOB Optical Engine as **common platform** for versatile **SR interconnect** applications.
  - → Easy replace of components, Faster cycle time of high-accuracy die bonding, Easy supply chain management.
  - → Full IP Proprietary

HEP transceivers in development

CERN VL(5G)/VL+(10G) for Phase I/II



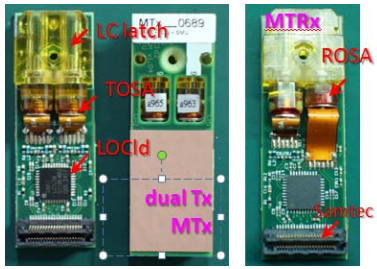


R&D CCNU

55 nm 12ch- Laser driver

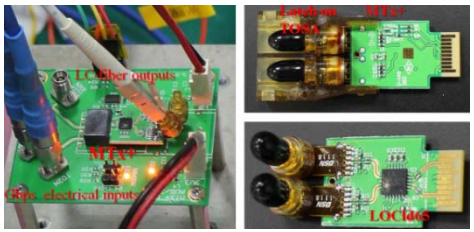
SMU.AS.NJU ATLAS Phase-I LAr NSW

LOCld chip SOS process
TOSA/ROSA assembly
10 Gbps qualified

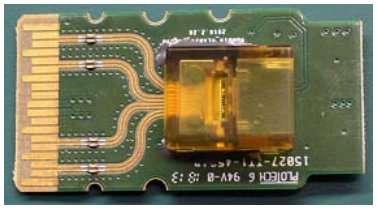


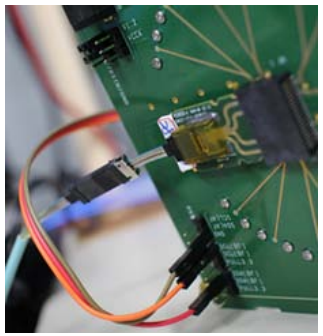
R&D SMU.AS with APAC corp.

LOCld65 TSMC 65nm
25 Gbps qualified

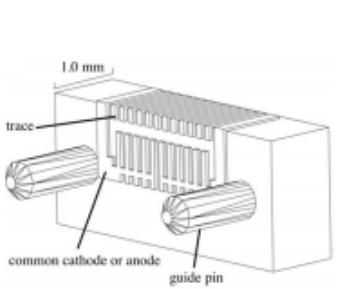


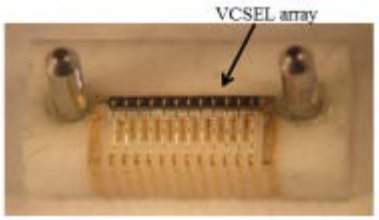
65nm 4ch array
VLAD, cpVLAD, TIA

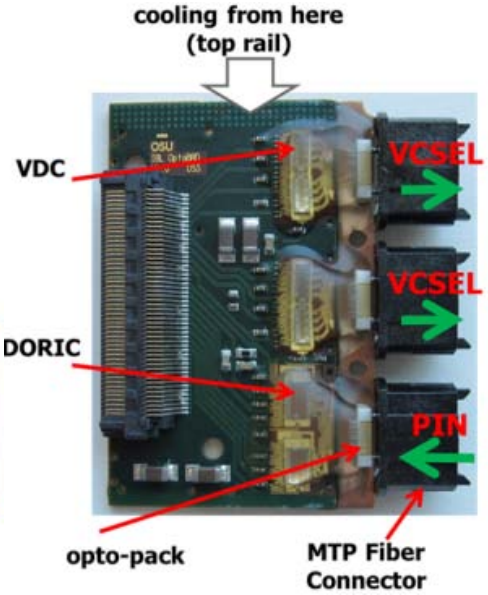




Ohio ATLAS Pixel Phase I







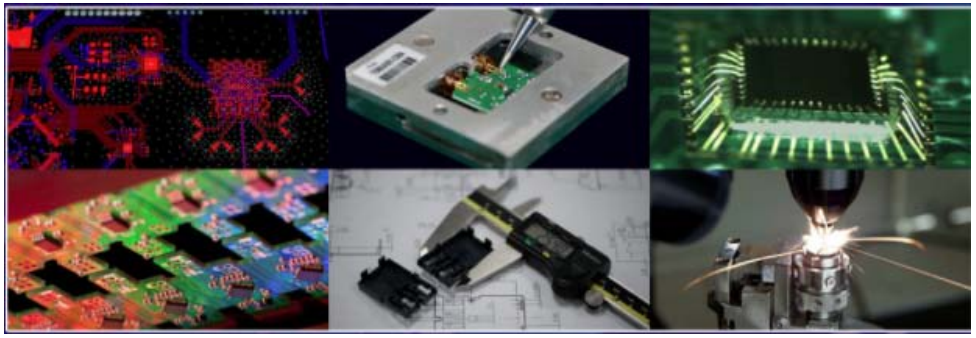
SMU.AS.NJU collab. w. APAC

SMU on chip design, AS+APAC on assembly, NJU on mechanics
Compatible w. VTR+ (4TX 1RX), targeting 25 Gbps/ch
same foot print & more variety of up to 4TX 4RX

- **APAC** has engineers, SMT line, assembly line
  specialized and equipped for 25 Gbps opto-electronics
  - high speed Gerber layout
  - PCB material: Panasonic M6 etc
  - Access to 25G VCSEL/PD provider
  - TOSA/ROSA assembly
  - COB opto assembly
- **Institute Lab** capacity
  only equipped for 10 Gbps
  debugging with probes on optical table

APAC Opto

Service
Customized Transceiver
Die Bond/Wire Bond/COB
Customized Extender



Prototypes in line for >10 Gbps (1)

SMU share-wafer chips, TSMC 65nm

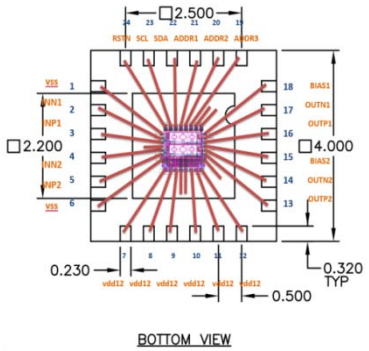
APAC assembly with PCB (M6), VCSEL/PD specified for 25 Gbps

- ***LOCld65*** a dual TX, made in SFP+ type transmitter,

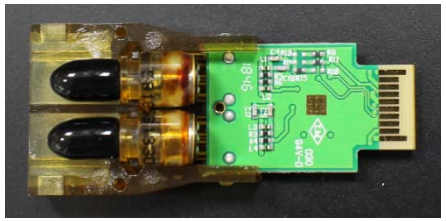
  Univ. Lab to 14 Gbps, JINST 14 C05021

  APAC upgraded to **25 Gbps** HSTD12, NIMA, arXiv:2006.11728

LOCld65

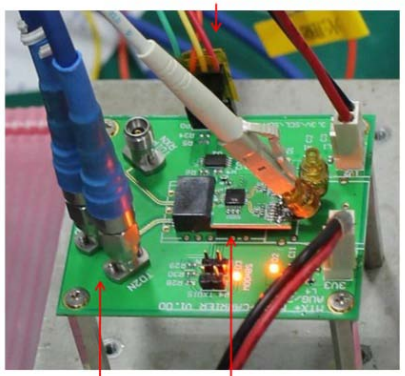


Megatron6 version
tested to 25 Gbps

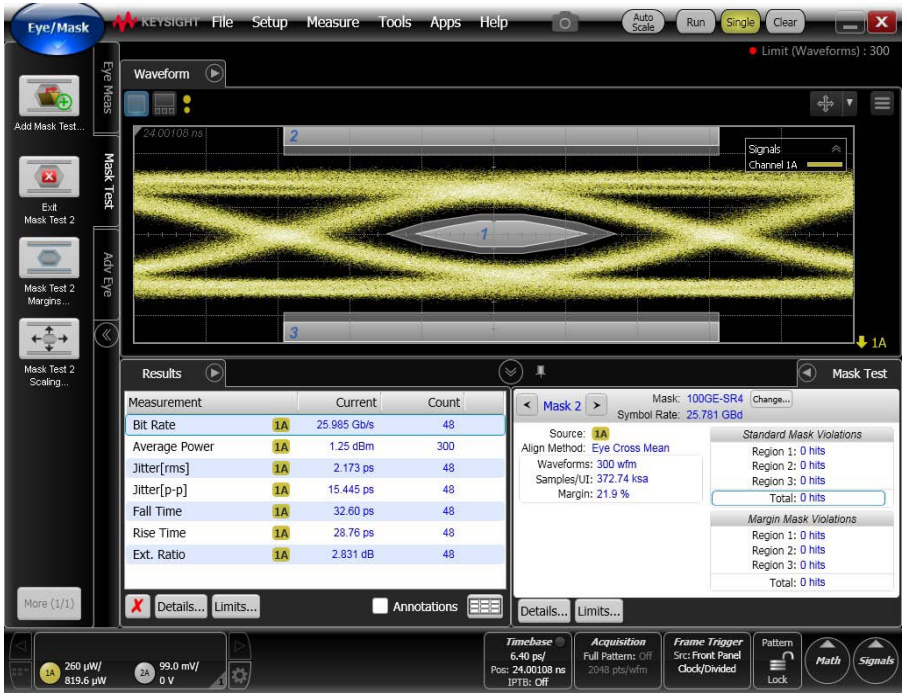


FR4 version
tested to 14 Gbps

I²C to USB interface to LabView

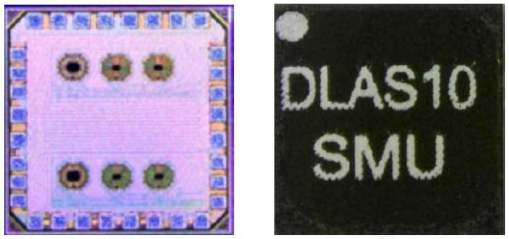


25 Gbps Eye-diagrams, margin 20%



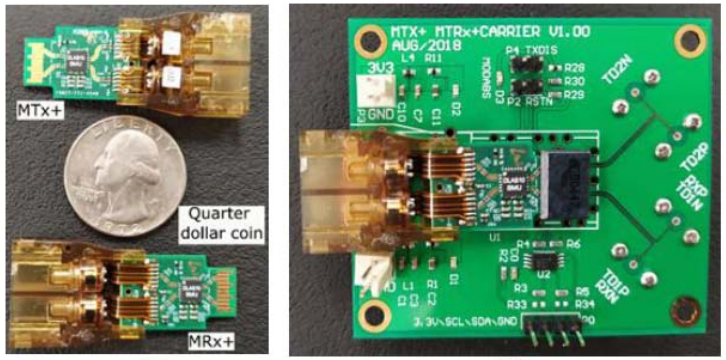
Prototypes in line for >10Gbps (2)

- ***DLAS10*** a LOCld65+ for dual ch. Transceiver (2TX or 2RX or TX+RX)
  Univ. Lab to 10 Gbps TWEPP2019, arXiv:2010.16069
  APAC 25 Gbps study soon



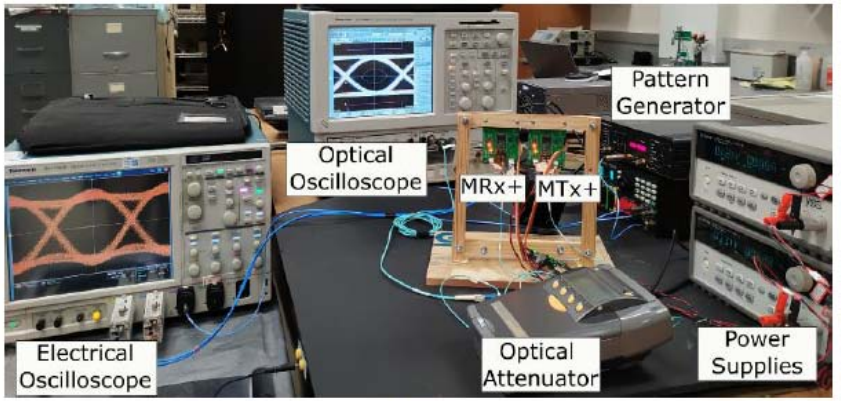
(a) (b)

Fig. 5. (a) Microphotograph of the die; (b) picture of the packaged chip.



(a) (b)

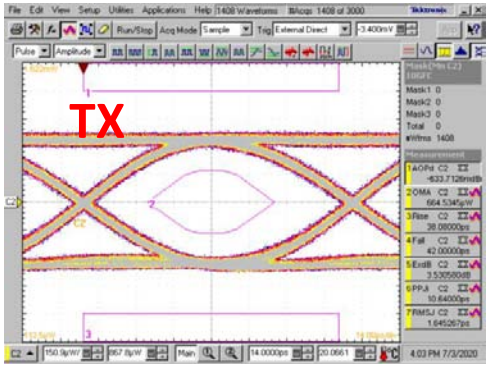
Fig. 6. (a) Photos of MTx+ and MRx+ compared with a quarter dollar coin; (b) the carrier board with an MRx+ mounted.

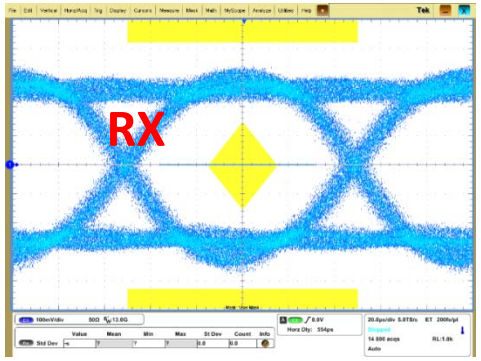


(c)

Fig. 7. (a) and (b) Test block diagrams of MTx+ and MRx+, (c) photo of the test.

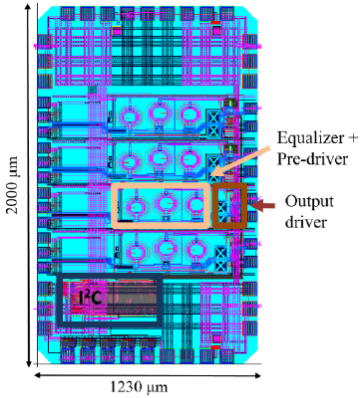
10 Gbps Eye-diagrams, margin 20%



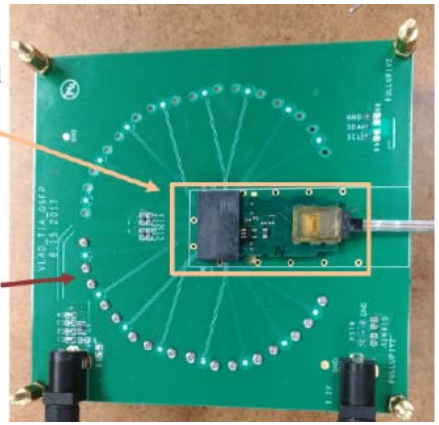


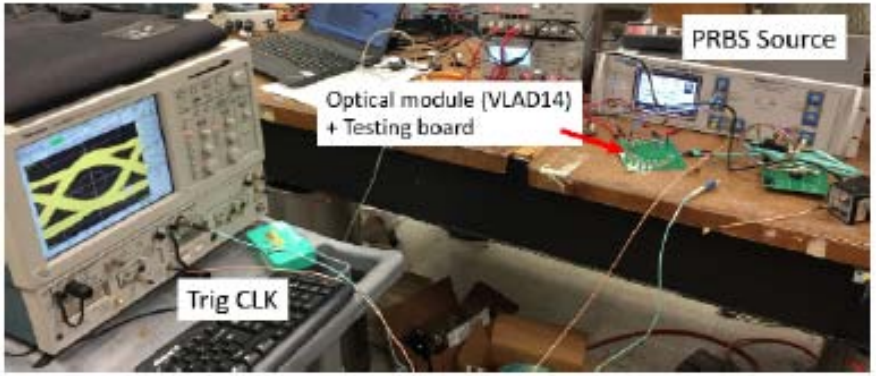
Prototypes in line for >10Gbps (3)

- ***VLAD14, VLAD28*** 4TX array QSFP transmitter
  Univ. Lab to 14 Gbps *JINST* 14 (2019) 05, C05016
  APAC tested 22 Gbps



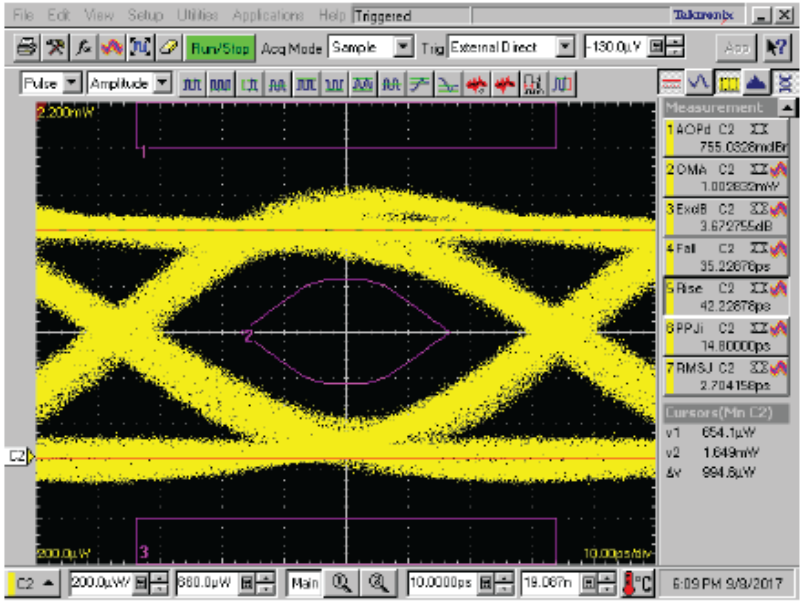
(a) VLAD14 chip layout





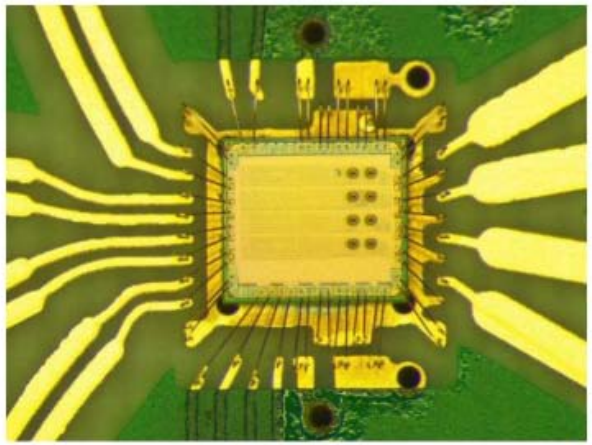
(b) VLAD14 testing picture

14 Gbps Eye-diagrams,

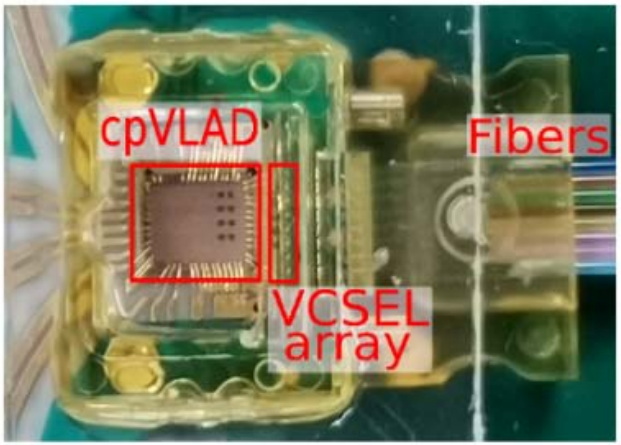

(b) 14 Gpbs optical eye diagram

Prototypes in line for >10Gbps (4)

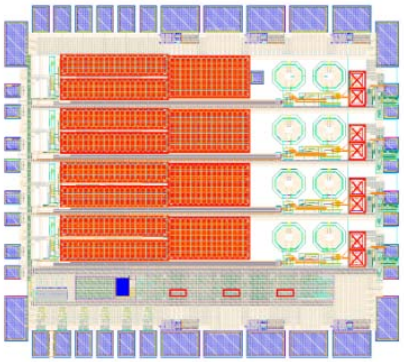
- ***cpVLAD*** 4TX array QSFP transmitter
  Univ. Lab 10 Gbps test, TWEPP2019 arXiv:2009.07121

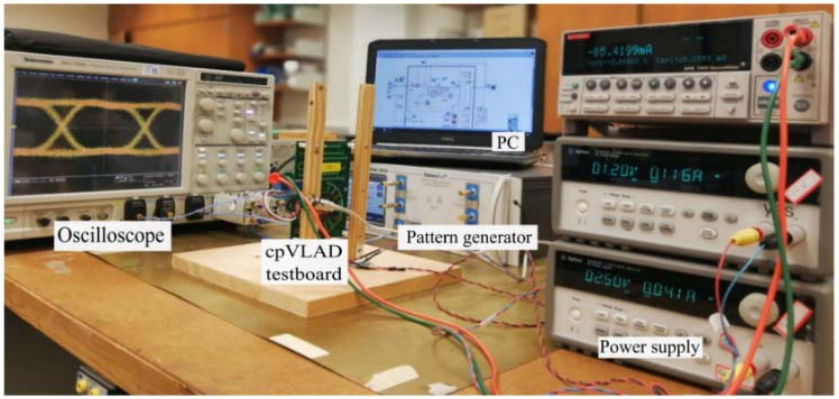


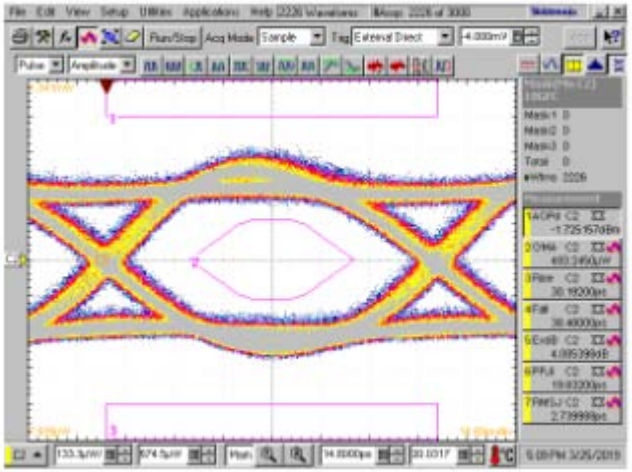
Electrical test boards



optical test boards







Optical

New prototypes and CMOS share-wafer (5)

- Prototypes in line for tests
  TIAS10 single ch. TIA for PD
  Lab 10 Gbps tested,
  made in ROSA, COB assembly waiting for test

APAC assembly
PD + TIAS10

- TSMC 65nm submission in Dec. 2020:
  - ***QTIA***, 2 mm x 2 mm 4ch TIA for RX
  - ***QLDD***, 2 mm x 2 mm 4ch Laser driver
    a cpVLAD+ aims for 25 Gbps/ch
  - ***GBS20v1***, 2 mm x 2 mm 1ch serializer + LD
    a PAM4 laser driver designed
    serializer for 16 electrical inputs @1.25 Gbps/ch
    output 2x10 Gbps

Discussion

- Optical links are industrialized to 25 Gbps
  collab. with manufacturer is good to all partners
  with APAC, we got 25 Gbps/ch transmitter for HEP

- MM 850 nm VCSEL could be topped at 25 Gbps/ch
  PAM4 is a upgrade to 50 Gbps/ch
  the GBS chip is attempted

- Fiber, Opto-electronics, Assembly are all mature
  CMOS shall be customized for our needs