Application of SOI-3D in the Vertex detector

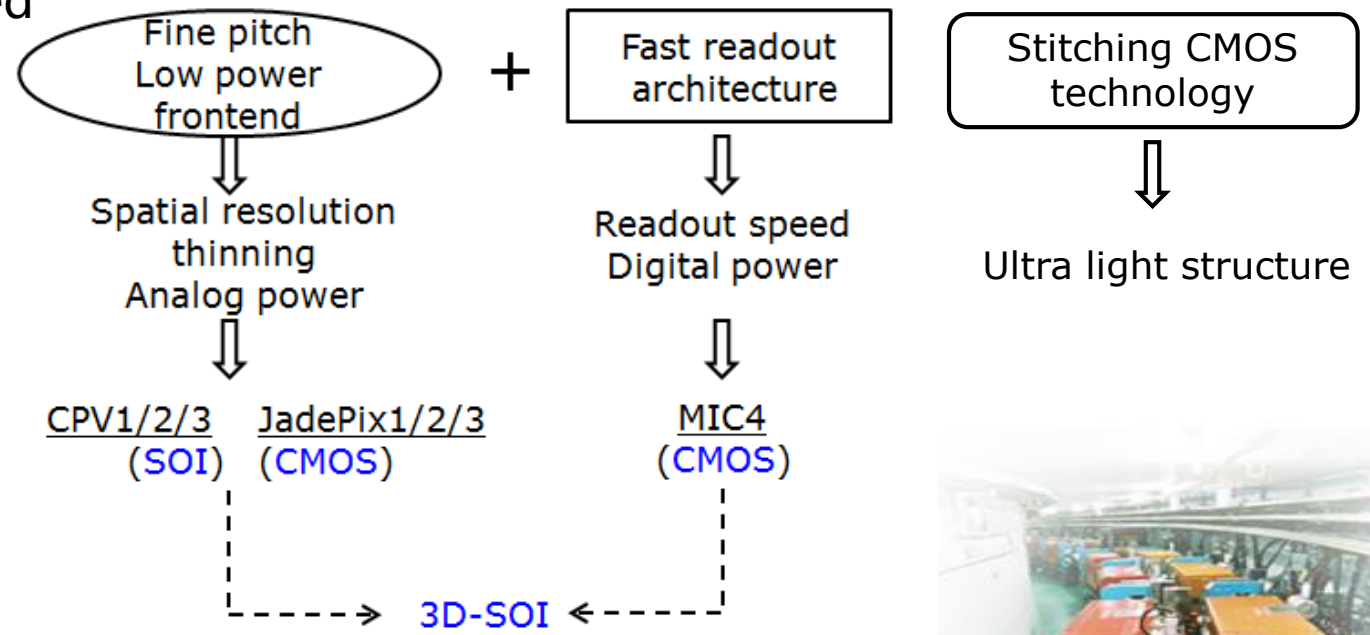
Yang Zhou and Yunpeng Lu

on behalf the SOI-3D team

CEPC DAY (December 28, 2020)

Overview of pixel sensor R&D

- CMOS and SOI development in synergy
  - Following the same roadmap
  - Using the same readout system
- JadePix3 and CPV3 tests in parallel
- CPV4-3D design is done
  - Similar design scheme considered for the JadePix4
- Stitching CMOS technology is being explored



Progress of last 6 months: SOI-3D

Update on CMOS/MOST1 and SOI pixel R&D

Yunpeng Lu and Qun Ouyang

IHEP

On behalf of the study group

CEPC Day / June 15, 2020

Outline:

- Introduction
- Update on JadePix3 and CPV3
- Perspective for next 5 years

SOI-3D

CMOS-Stitching

* contents will be reported: "Development of high resolution low power silicon pixel sensors for the CEPC vertex detector", ICHEP2020, ID #394

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Contents

- Two topics are covered in this report
  - Introduction of SOI-3D: why it is suitable for the Vertex detector
  - First experience: practical aspects of the CPV4-3D design
- Discussion and comments are welcome any time

Specification of Vertex detector

- high spatial resolution, low material budget and fast readout required by the flavor tagging
  - Pixel sensor, the core part to construct a vertex detector

Impact parameter resolution

$$\sigma_{r\phi} = 5\mu m \oplus \frac{10}{p(GeV)\sin^{3/2}\theta}\mu m$$

Vertex detector specs → Pixel sensor specs

$\sigma_{s.p.}$ ~ 2.8um → **Small pixel** ~ 16um

Material budget ~ 0.15% X_0/layer → **Thinning to** ~ 50um

→ **low power** ~ 50mW/cm^2

r of Inner most layer ~ 16mm → **fast readout** ~ 1us

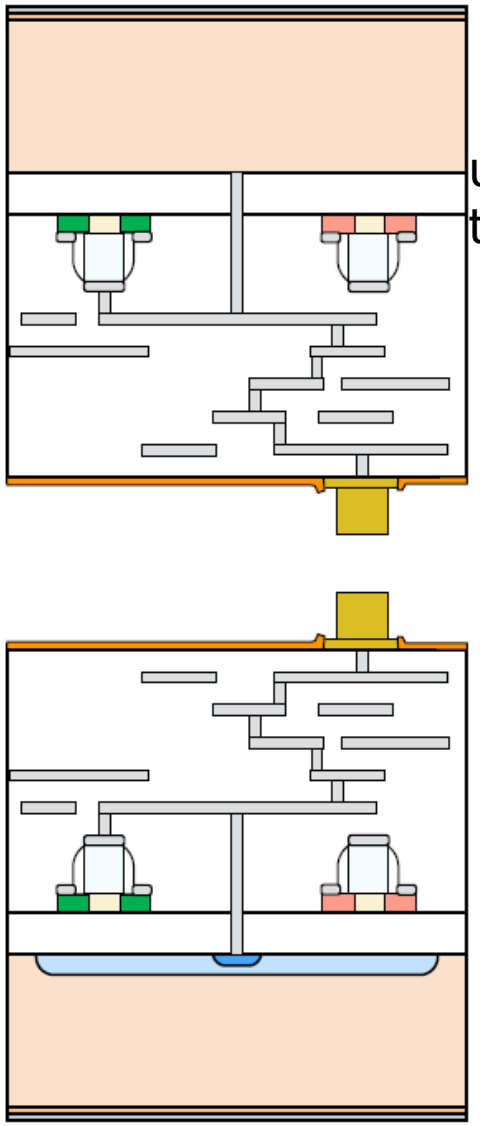
→ **radiation tolerance** ~

$\leq 3.4\ Mrad/year$

$\leq 6.2\times10^{12} n_{eq}/(cm^2\,year)$

- Two options to pursue:
  - Option #1: implement the specs in two **complementary** design (CDR baseline scheme)
  - Option #2: **explore new technology**, promote the performance (advanced scheme)

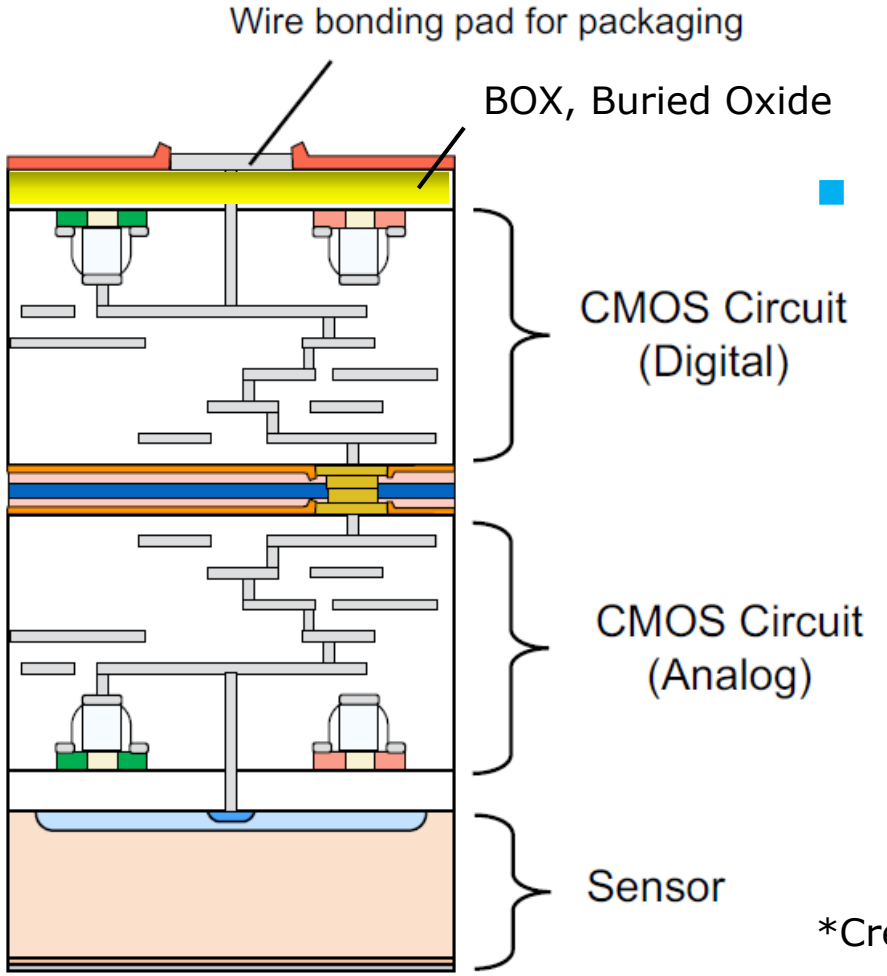
Introduction of SOI-3D: design resources



- Shrinking pixel size always pushed to the physical limit
  - 0.35um process: ~10 transistors and 6 metal layers, pixel size ~ 20*20 um^2
  - 0.18um process: ~100 transistors and 6 metal layers, pixel size ~ 26*28 um^2
- 0.2um SOI-3D process: ~100 transistors and 5 metal layers **in each tier**
  - lower tier: sensing diode and analog front-end
  - upper tier: digital readout
  - Pixel size can be cut half without compromise of functionality

*Credit of the conceptual drawing: Miho Yamada

A minimum increase of material in SOI-3D

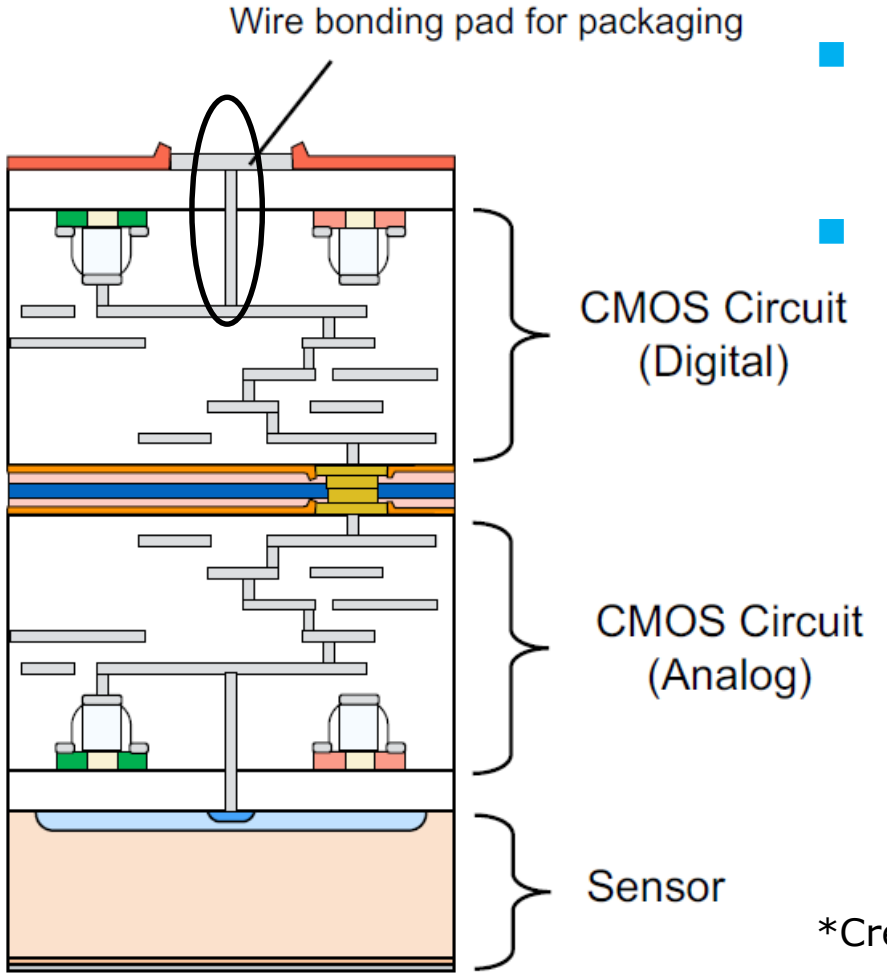


- The bulk of upper tier is **removed by wet-etching**
  - 260 um → 10 um thick
  - Wet-etching stopped by the box layer automatically, which makes SOI quite compatible with 3D integration
- Lower tier can be thinned as a conventional sensor
  - 75 um in SOI case and 50 um in CMOS case (lower tier not necessarily an SOI sensor)

* Currently SOI-3D demonstrated on a lower tier of 260 um thick

*Credit of the conceptual drawing: Miho Yamada

Backside connections



- Backside connection is Through Box Via (TBV)
  - Not the Through Silicon Via (TSV)
- 0.32 um hole which implemented already in the SOI process
  - Smaller than TSV hole by a factor of 10
- Additional metal layer formed for the bonding pad

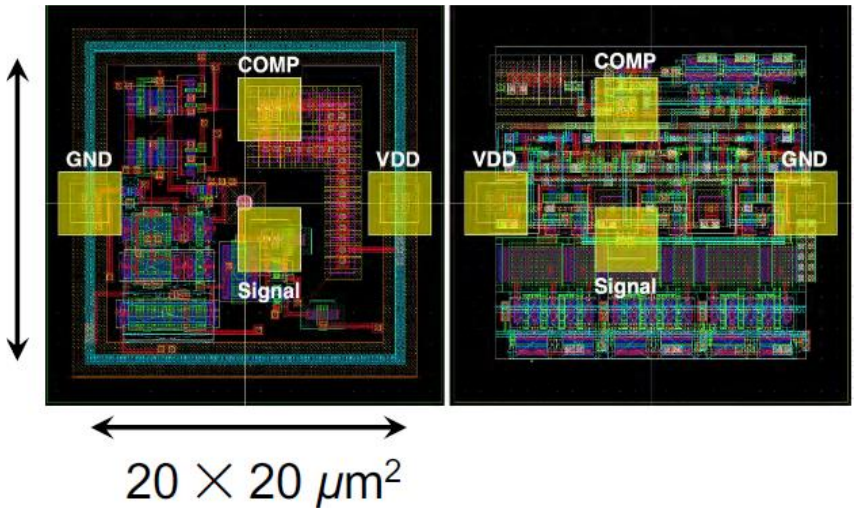
*Credit of the conceptual drawing: Miho Yamada

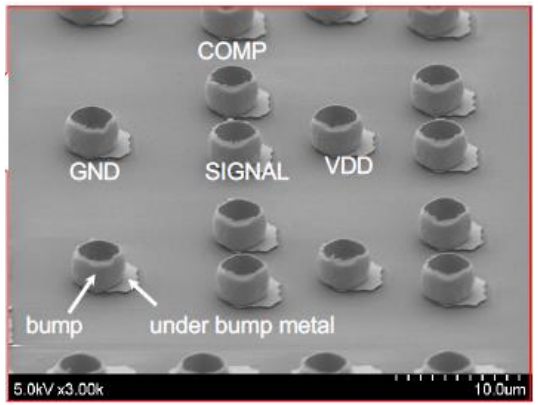
Frontside connections

- 3 um cylindrical Au bump (diameter)
  - Multiple vertical connections per pixel, necessary and feasible

4 connections per pixel: power/ground, analog signal and comparator output in the SOFIST4 by KEK, first demonstration of SOI-3D

lower pixel upper pixel Au bumps



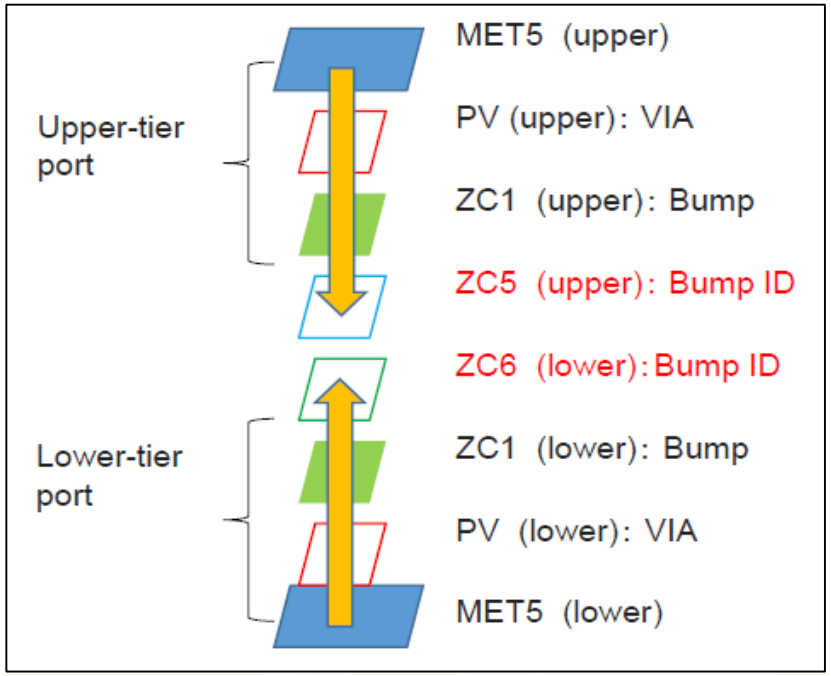


SEM image

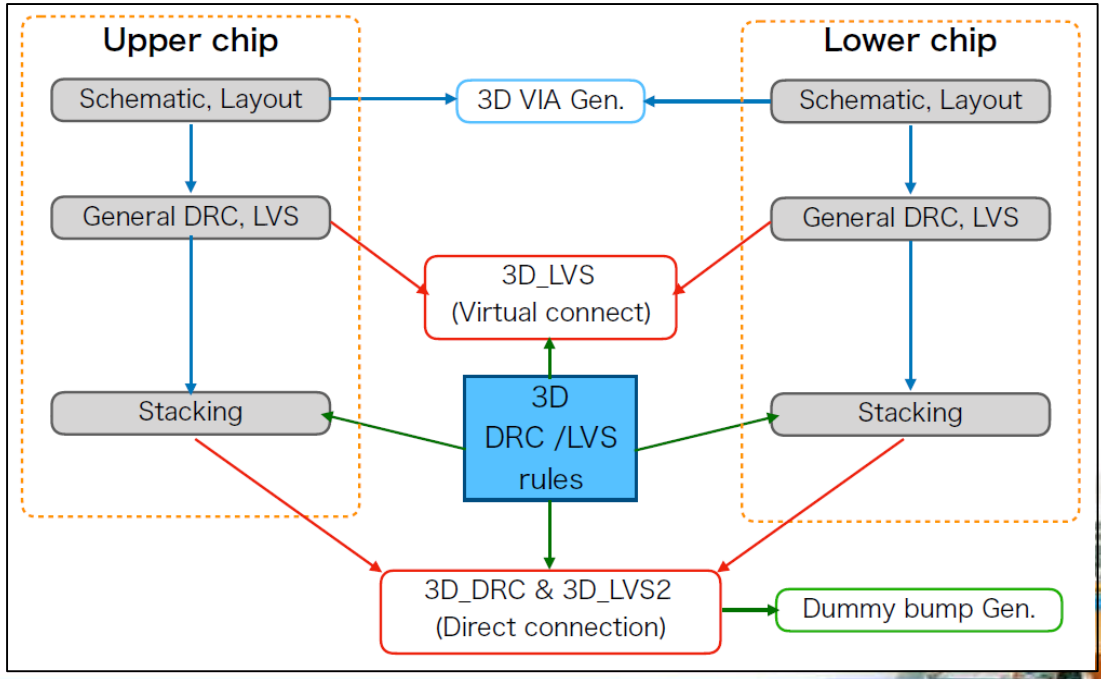
Design flow established

- Conventional SOI tape-out plus a special 3D add-on process
  - Upper and lower chips manufactured with the LAPIS 0.2um process
  - Chip-to-chip 3D integration implemented by T-Micro originated in Tohoku-U.
  - **Driven rules** of 3D design and verification integrated into the EDA tools

stack-up of 3D layers

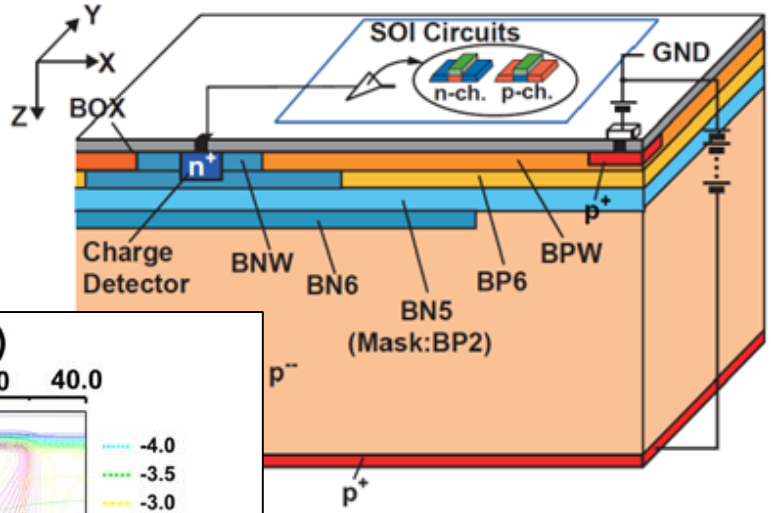


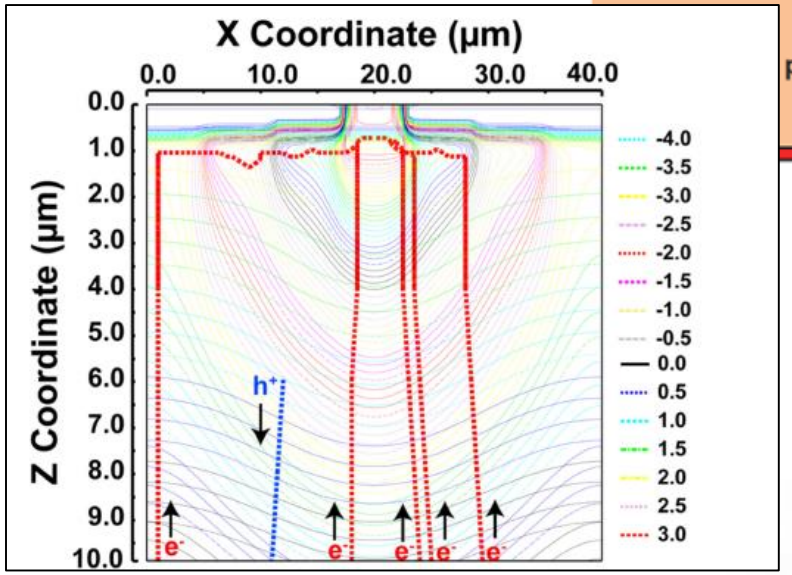
flow chart of SOI-3D design



PDD sensing diode system

- Not 3D-specific, but the most active part of study in SOI pixel **sensor** technology
  - Evolution of years' development: BPW, Nested-wells, Double SOI, and PDD (Pinned Depleted Diode)
- **All-in-one solution** in the sensor part:
  - Control back-gate of transistors
  - Maximize charge collection efficiency
  - Suppress leakage current of Si-SiO_2 interface
  - Minimize the capacitance of electrode (Cd)
  - Shield the capacitive coupling between the sensor and pixel circuit



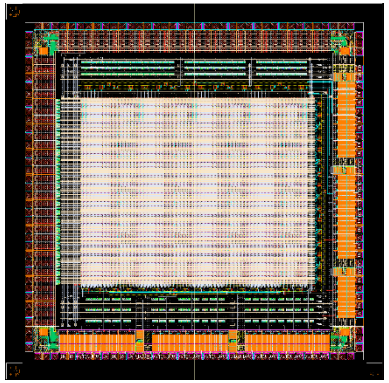


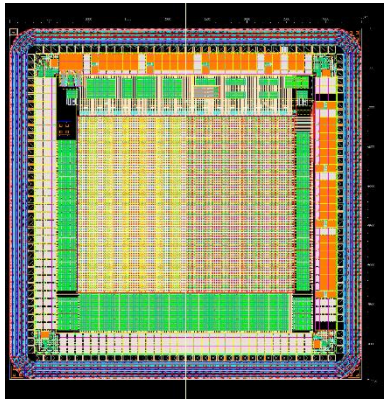
Electric field and e- transportation simulation in PDD structure:
Ref: doi:10.3390/s18010027 by Shoji Kawahito

CPV4-3D design

- Transition from technology to design
  - Two proficient designers spending 90 work days

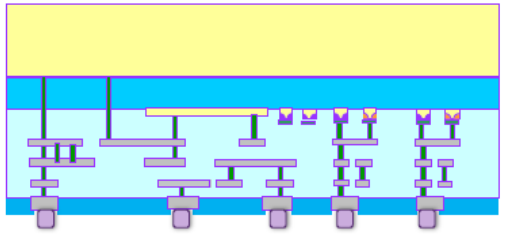
CPV4_U (Yang Zhou)

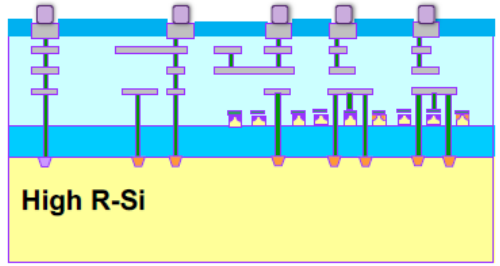




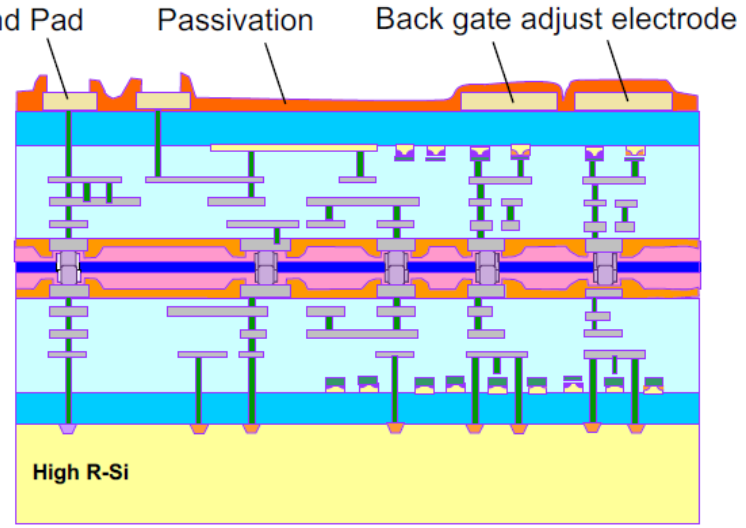
CPV4_L (Yunpeng Lu)

Upper Chip





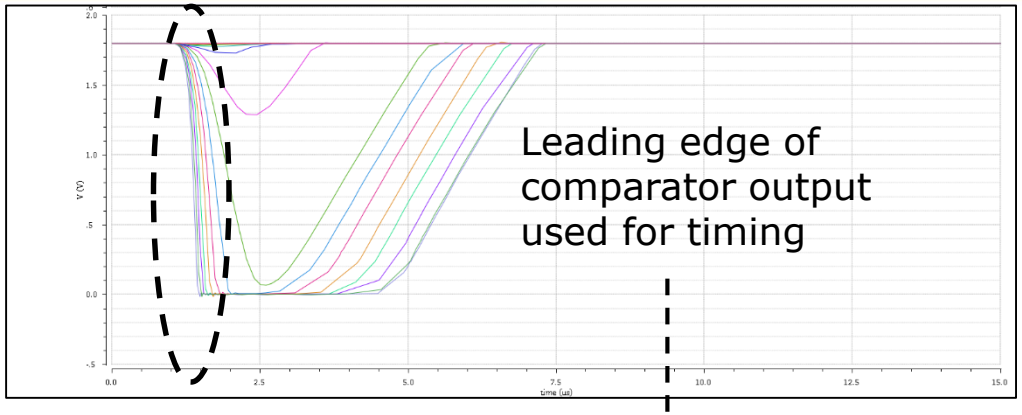
Lower Chip

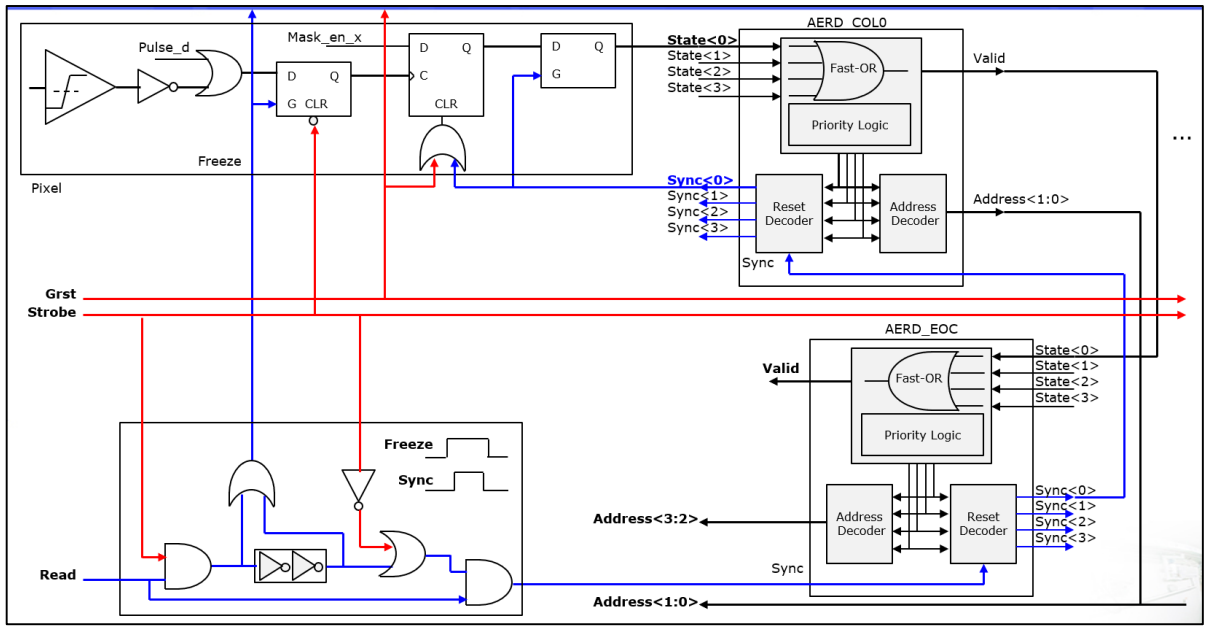


CPV4 design scheme

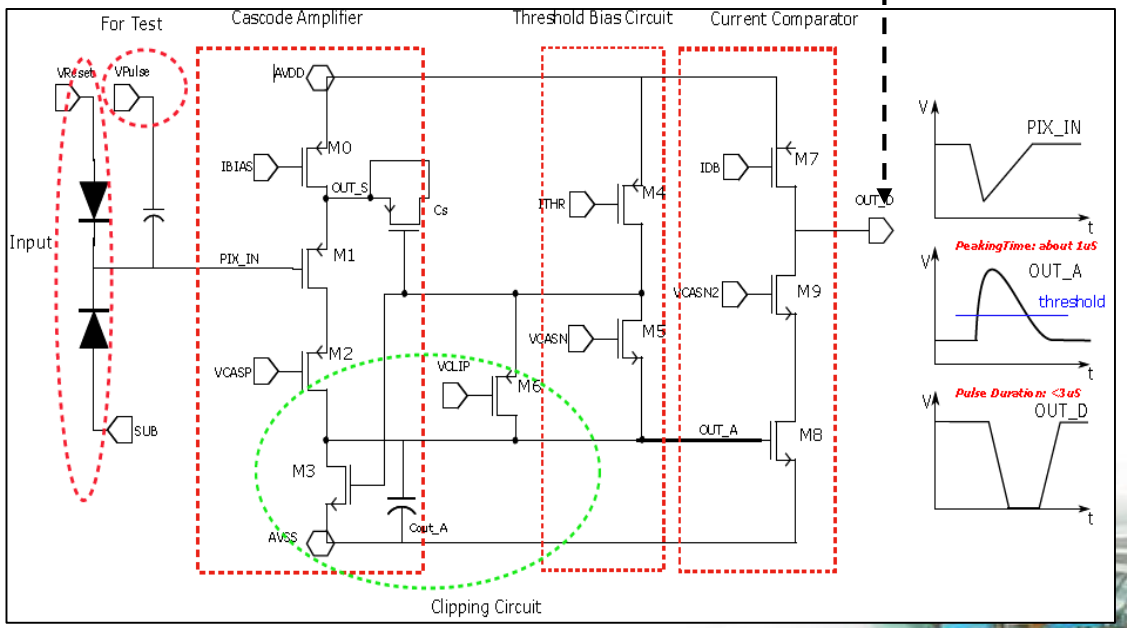
- **Low power** front-end: amplifier and comparator
  - Using its leading edge for timing < 1us
- Data-driven readout (Asynchronous Encode Reset Decode*)
  - **Two readout modes**: continuous and triggered
- Power consumption ~ 50mW/cm^2

*Ping Yang, NIMA 785 (2015) 61-69





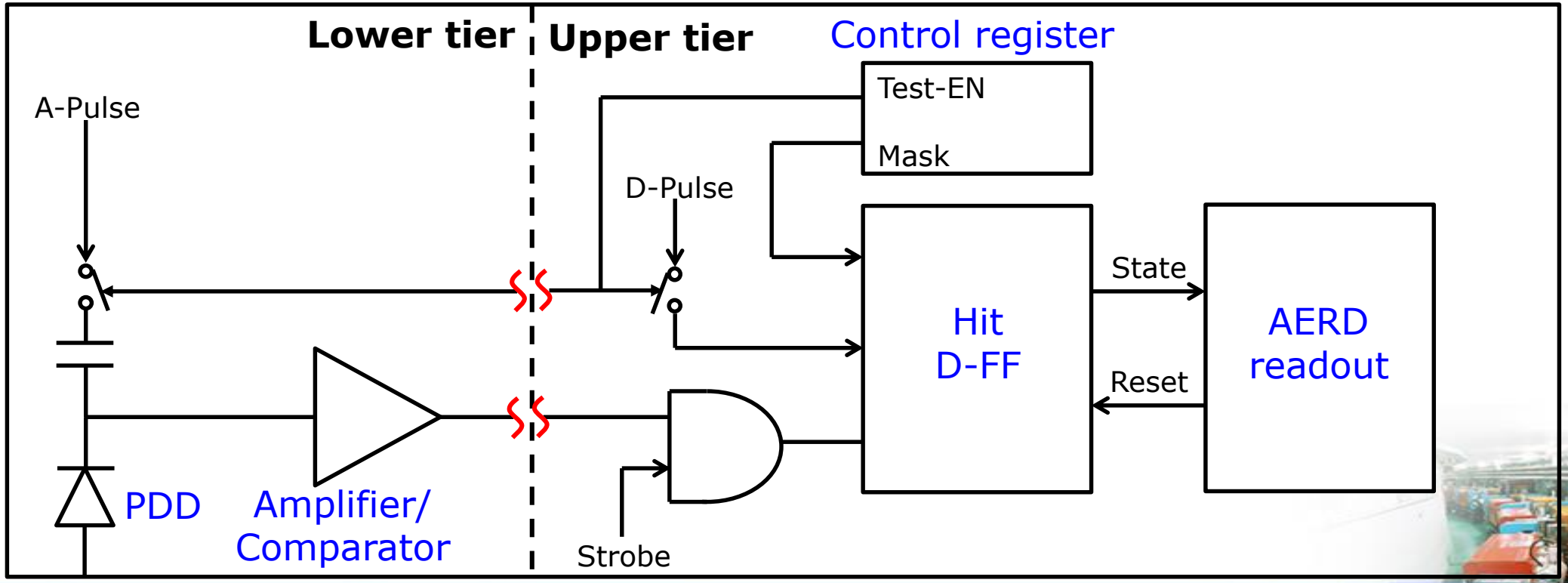
Explanatory diagram of CPV4 design scheme



amplifier and comparator

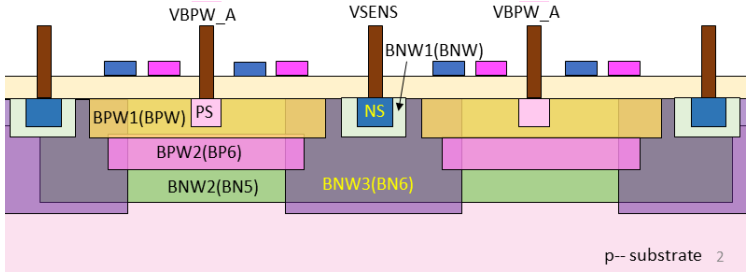
Division of upper and lower functionality

- Lower tier: PDD sensing diode + amplifier/comparator
- Upper tier: Hit D-Flipflop + Control register + AERD readout
- **2 vertical connections** in each pixel: comparator output and test switch
  - Analog and Digital power/ground separated, a common practice in mixed-signal design

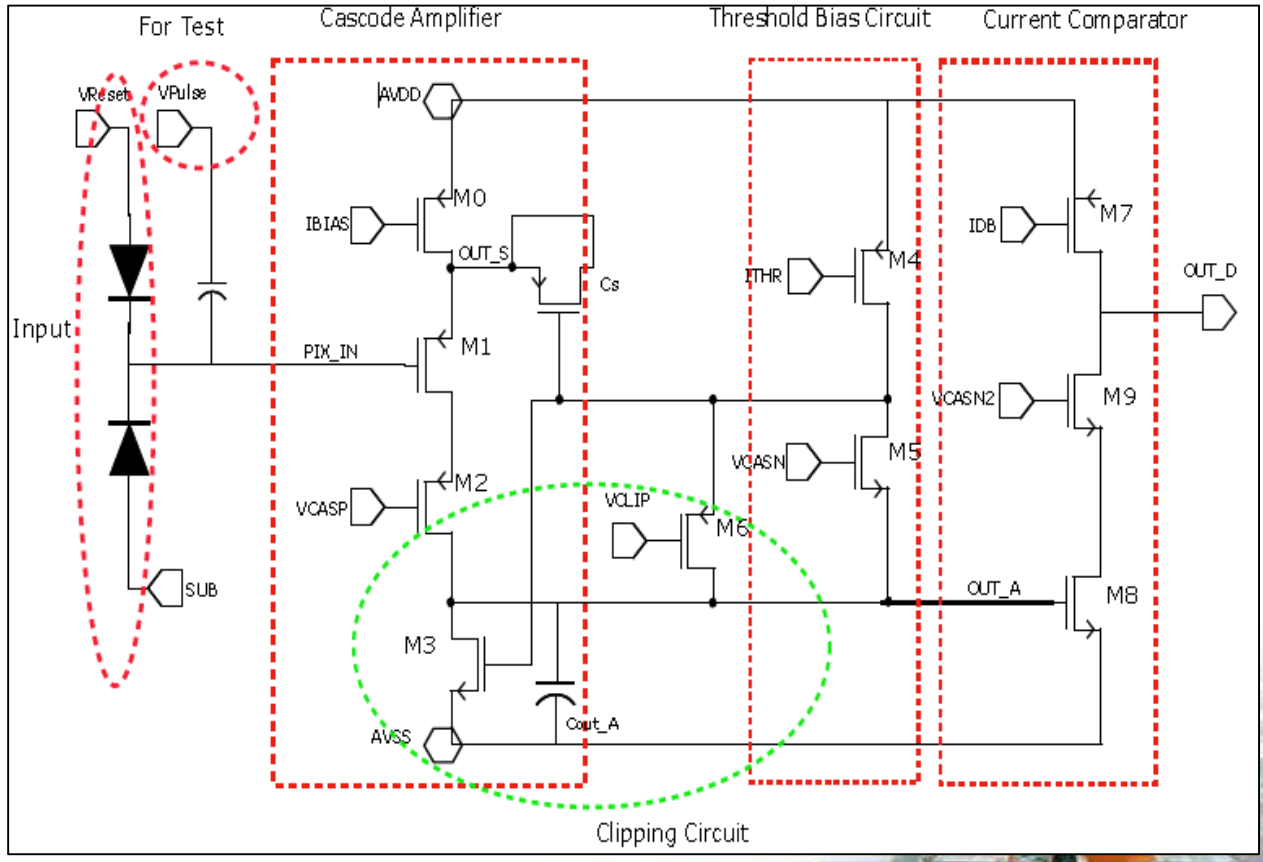


Management of Vth shift

- -4V on the **back-gate** of MOS transistors required (BPW shown below) in order to minimize electrode capacitance Cd.
  - Vth decreased 70 mV for PMOS and increased 50 mV for NMOS
  - Characterized and modeled in HSPICE by KEK
- Influence on the front-end assessed
  - Current mirror matched and placed in a -4V N-well (Counter-part branch of M0, M4, M7)
  - The other transistors compensated by proper offset on their bias voltage (VCASN e.g.)
  - **Confirmed by circuit simulation**



PDD requires -4V applied on BPW



Pixel design

- **Transistor size** selected roughly according to ALPIDE design* to minimize FPN as a first order approximation
  - Statistical parameters of SOI process is not sufficient to perform a reliable MC simulation

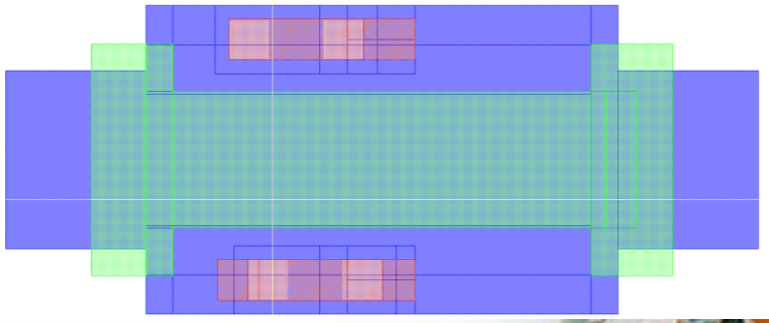
Transistor	M0	M1	M2	M3	M4	M5	M6	M7	M8	M9
W/L	1.8/8.5	1/0.4	1/0.4	1/5	2/8.05	0.63/4.94	0.63/3	1/5	1/0.4	1/1

- Simulation results of **threshold and noise**

	Threshold	Gain@Thr	Vnoise@Thr	ENC
Pre-layout	75 e^-	32mV/10e^-	4.33 mV	1.34 e^-
Post-layout	**125 e^-**	8.6mv/10e^-	2.92 mV	**4 e^-**

- TID radiation enhancement
  - H-gate transistors used for M5 in test pixels for TID
  - Compensation of TID-induced Vth shift to be applied on the BPW layer

H-gate NMOS layout



*Ref: D. Kim et al., 2016 JINST 11 C02042

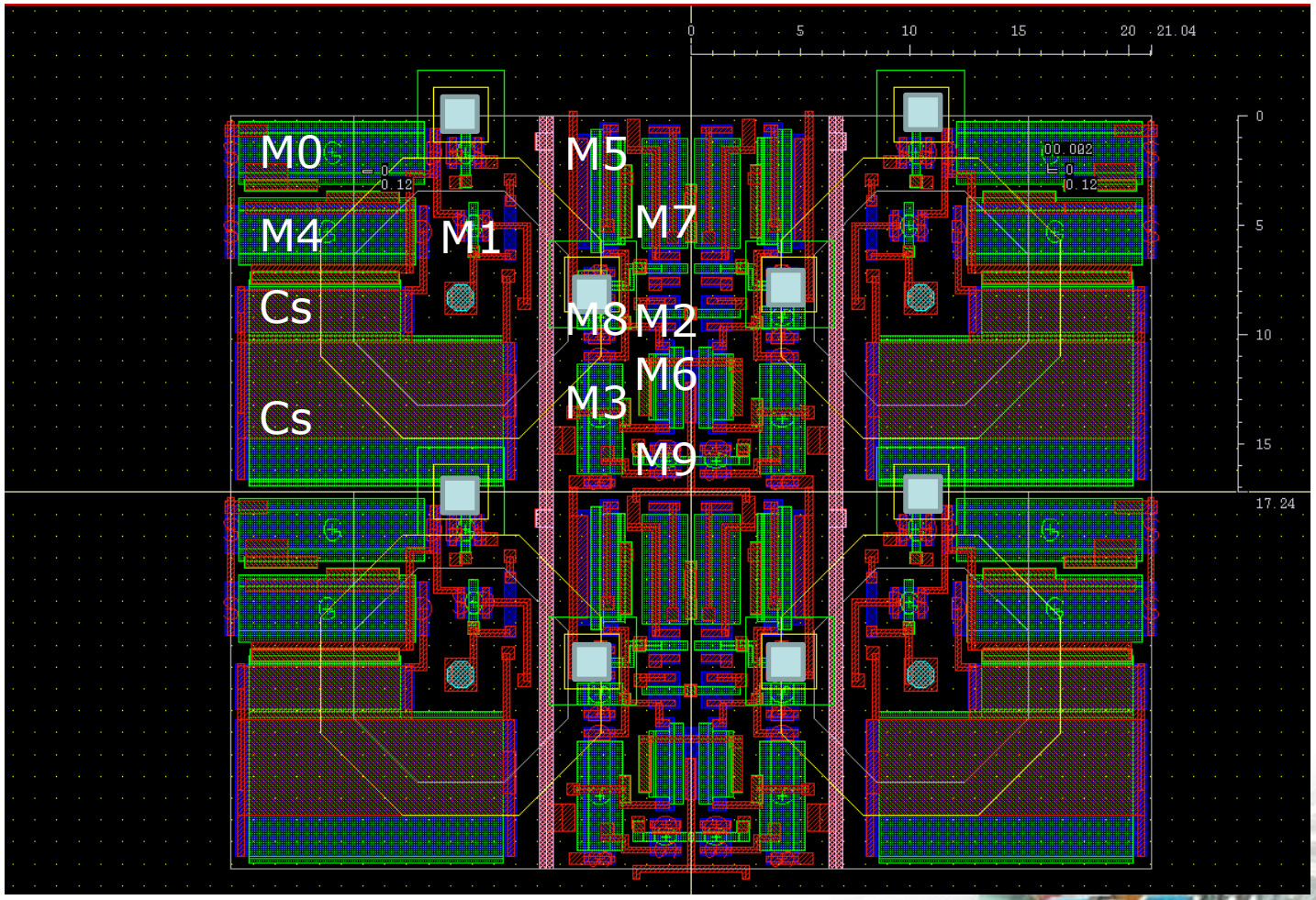
Pixel layout

- A lot of efforts to minimize the layout size
  - 21.04 um * 17.24 um
- Y-axis mirrored, **sensitive input node**

protected against the output node

- To minimize the crosstalk

3D bumps marked with

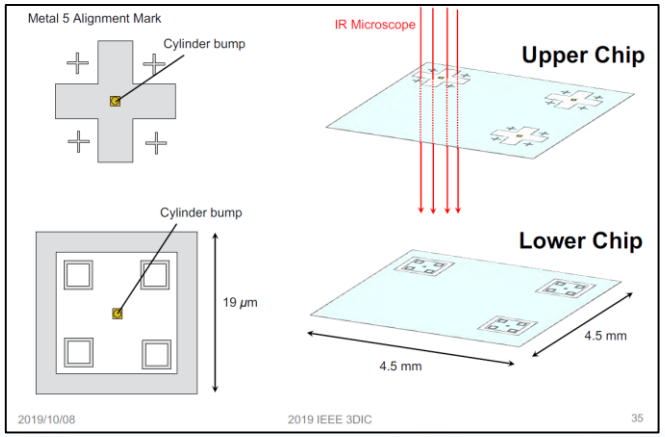


4 pixels arranged in two columns

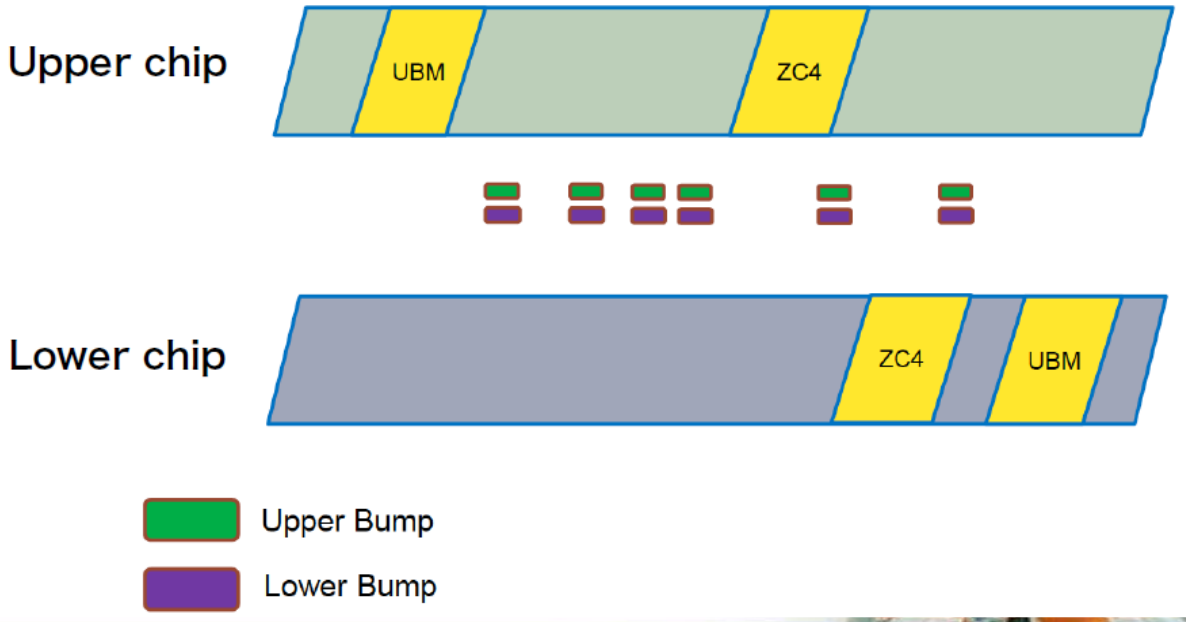
Dummy 3D bumps

- Dummy 3D bumps, to **relieve the mechanical stress** of upper tier
- Generated automatically in the user-designated area
- Excluded area for the dummy 3D bumps
  - The pixel matrix
  - The p-stop of guard ring
  - The alignment marks

Alignment marks



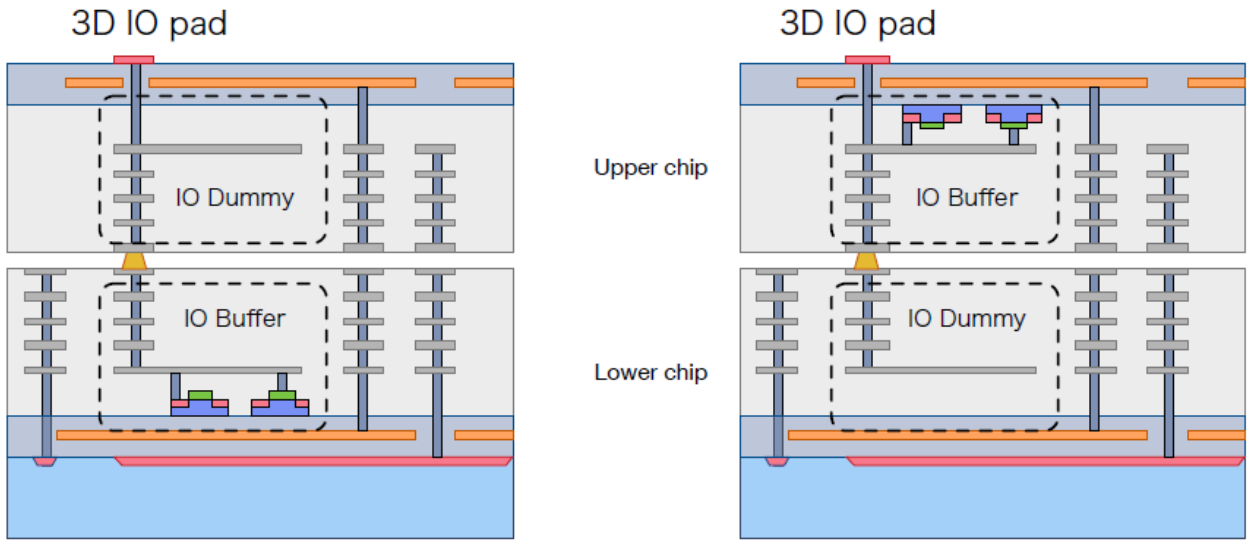
dummy 3D bumps avoids UBM and Masking ZC4



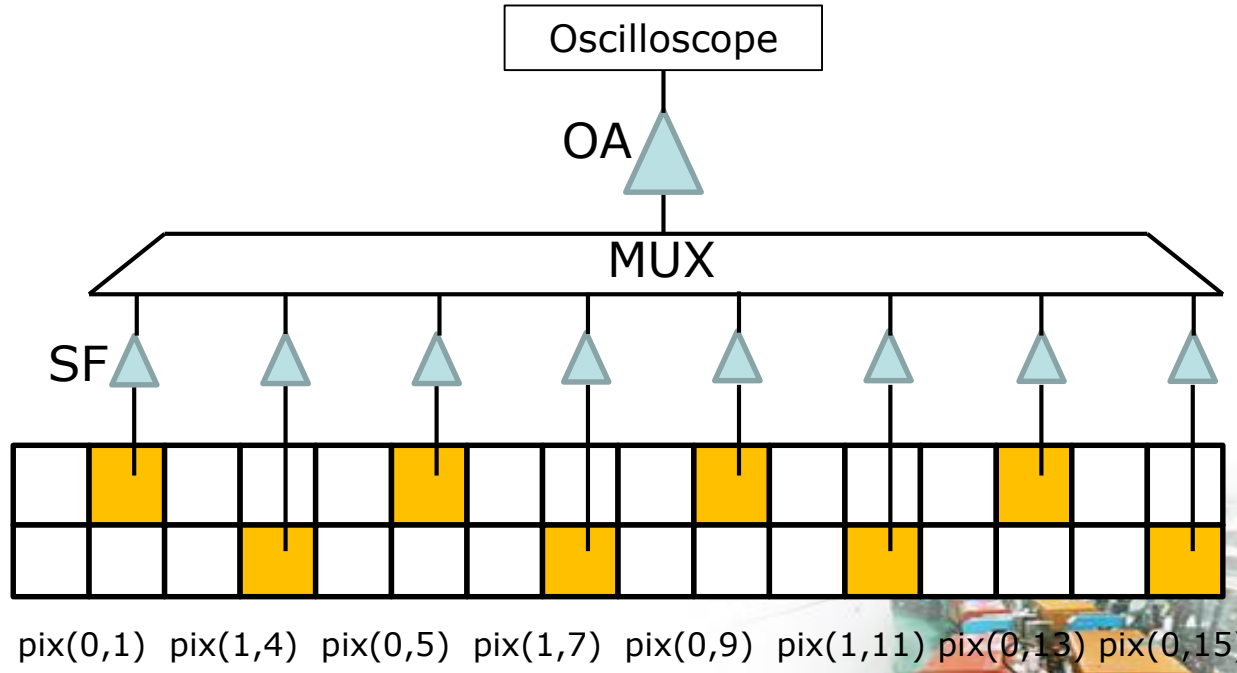
Design for test

- Signal and power access to the chips
  - Conventional IO pad equipped on both lower and upper chips, **accessible before 3D integration**
  - Functional IO always stacked up with dummy IO to avoid conflicts of buffers

Configuration for the signal of lower tier(left) and upper tier(right)



- Internal signal waveform are routed out of test pixels and buffered for oscilloscope observation
  - **Internal node** OUT_A and OUT_D
  - Two-stage buffers: Source-Follower and Operational Amplifier



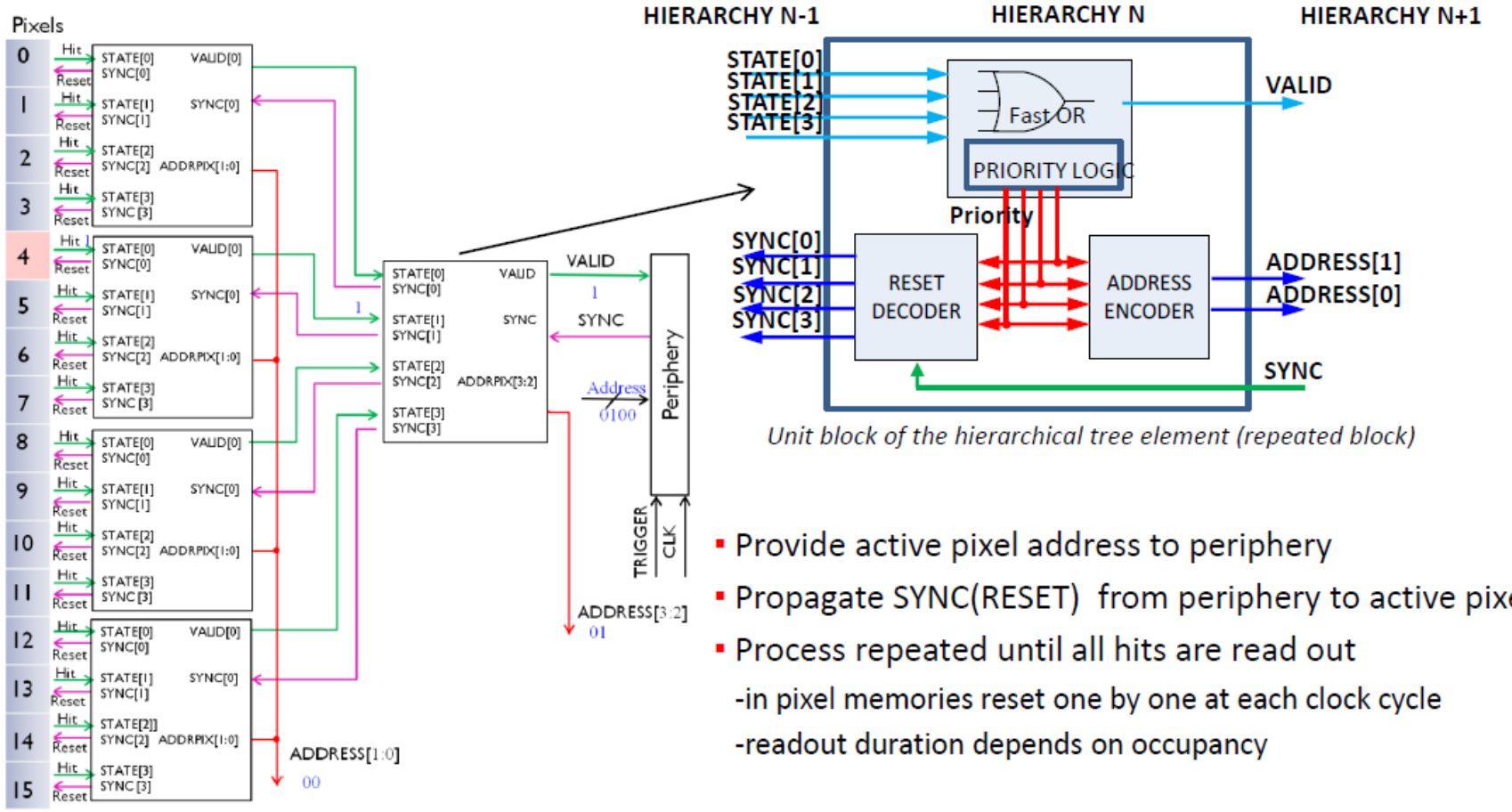
Summary

- Exploration of SOI-3D has started with the first design of CPV4-3D
  - Targeting on the full specs of pixel sensors
  - To examine the scheme, implementation and yield of SOI-3D
  - Expected separate tests in the 1st half of 2021, 3D tests in the 2nd half of 2021
  - 2 ~3 MPW run planned in 5 years
- Update on the JadePix3
  - Sent for wire bonding last Friday
  - Debugging to start in one week
  - Laser test planned before May 2021
  - Interested in the opportunity of electron test at the BSRF
- Update on the CPV3
  - Characterization of PDD structure finished
  - Optimized structure identified for the CPV4-3D design
  - One research article in preparation

Thanks for your time!

Backup slides

Address Encoder Reset Decoder principle

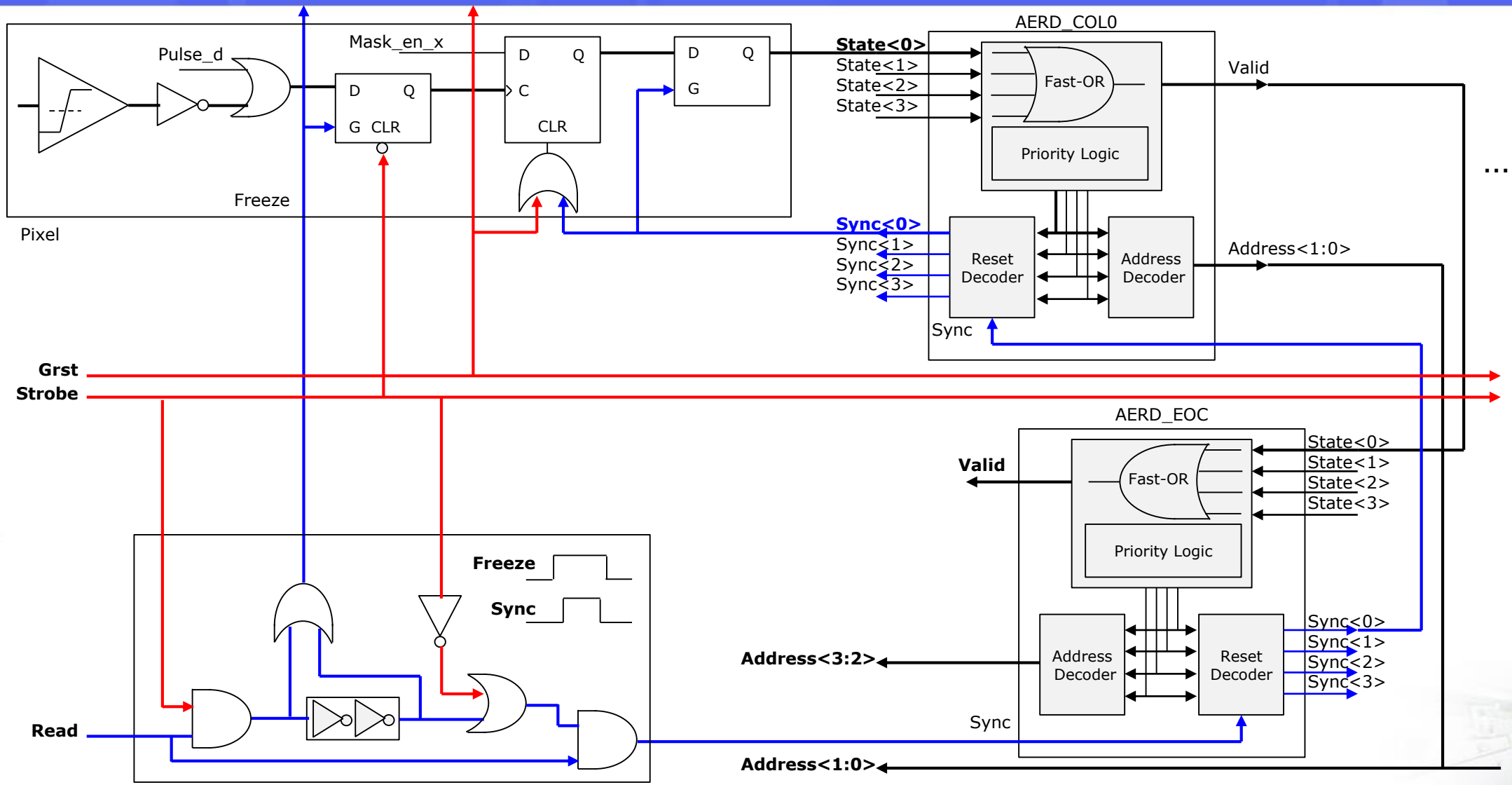


Unit block of the hierarchical tree element (repeated block)

- Provide active pixel address to periphery
- Propagate SYNC(RESET) from periphery to active pixel
- Process repeated until all hits are read out
  -in pixel memories reset one by one at each clock cycle
  -readout duration depends on occupancy

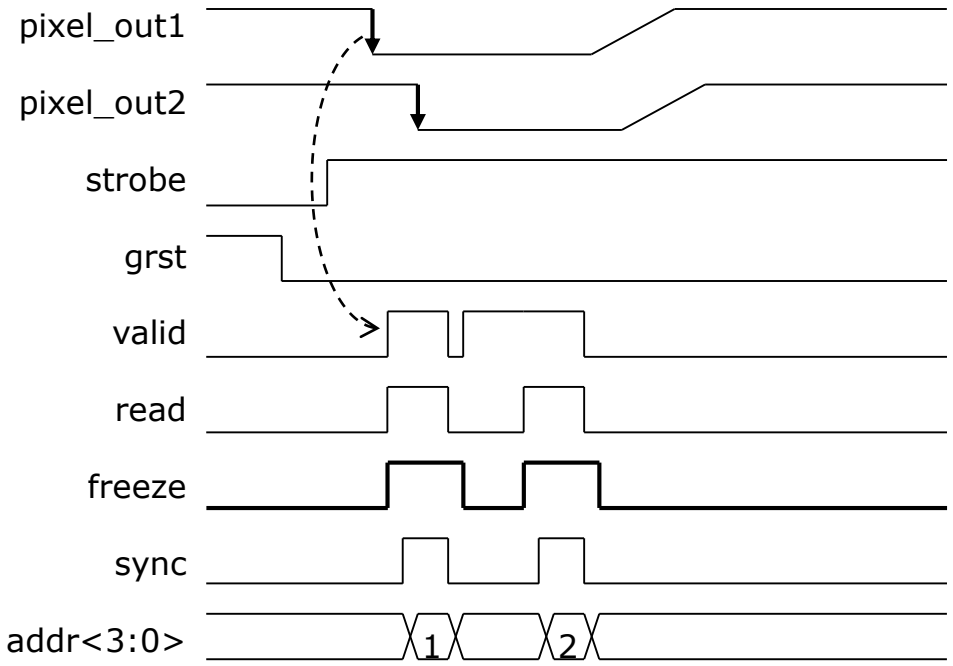
- Hierarchical arbiter tree structure -> reduces loads, 5 hierarchy to encode 1024 pixels
- Fully combinatorial asynchronous circuit without clock propagating into the matrix
  -reduction of power & noise

Readout Architecture



Readout mode

- Continuous mode
  - Valid asserted by the falling edge of pixel_out1
  - Pixel_out2 froze before pixel_out1 is done
  - Timing resolution of falling edge < 1us



- Triggered mode
  - Strobe as the gate control
  - Readout after trigger (strobe)
  - Timing resolution of pulse width < 10us