



Jadepix3 Test System

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Tuesday, March 9, 2021

Updates on Software and Firmware

V1.0.0

DAC70004, SPI, pixel configuration (MASK/PULSE), control logic, global shutter.

V1.1.0

Implement S-Curve mode. Improve the method of the pixel configuration. The configuration time is decreased **from 2min to 2s**.

V1.2.0

Fix bug: the maximum value of the valid counter was not set correctly. It was set to 14, should be 16. So we can only read only 42 column of 48 in total for one sector.

V1.3.0

Fix bug: row 512 can be readout. This bug is caused by the timing issue of the readout logic.

V1.4.0

Improvement: Before this version, we can only read the data of one sector, and change the sector manually by software. Now we can read one whole column data, and sector can be switched automatically by the firmware.

New Issue

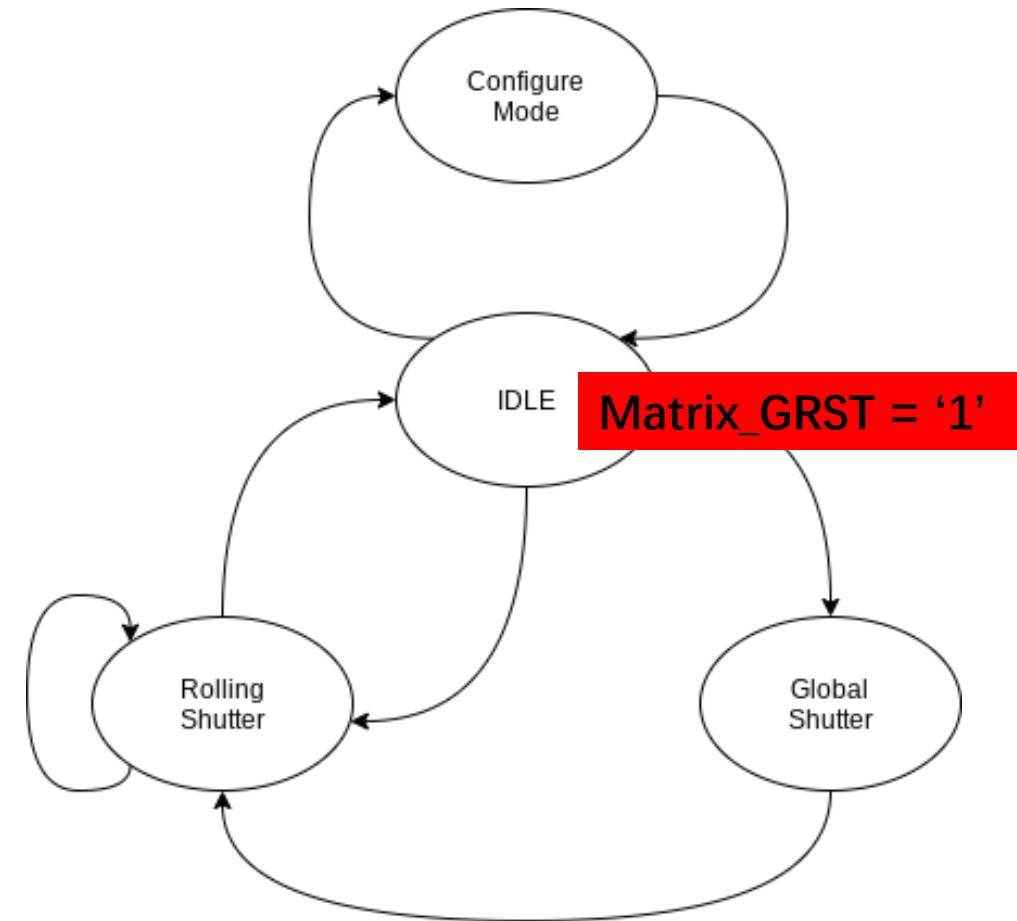
Lose data at the last row (512) of the last frame. 6/16 in one block can be readout at most.

- The reason

The reset port (Matrix_GRST) is assert immediately after rolling shutter control logic finished and the FSM return to IDLE state, while the data of row 512 haven't be fully readout.

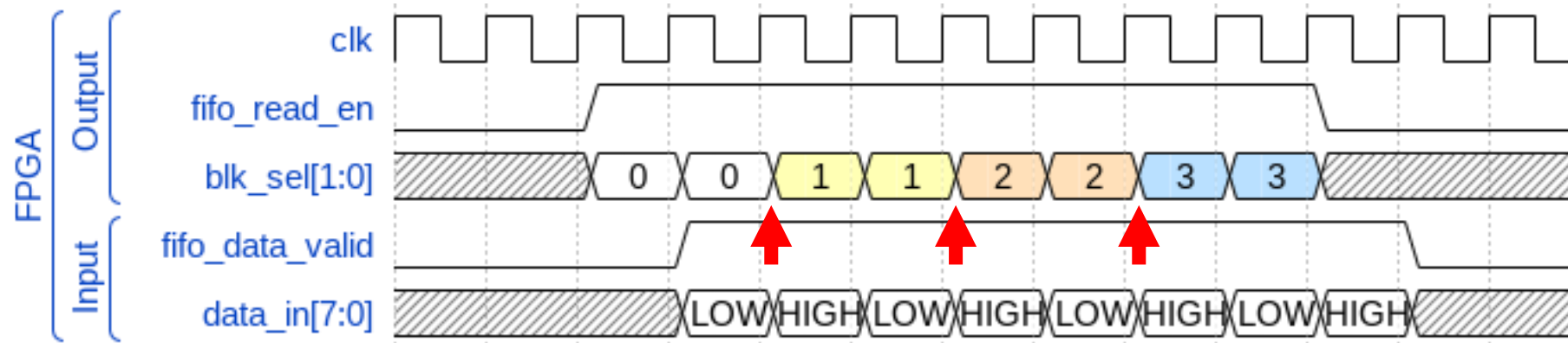
- Fix it or keep it?

This issue can be fixed by firmware easily. We think it's a chip design issue, and we prefer to keep it.



Jadepix3 Control FSM

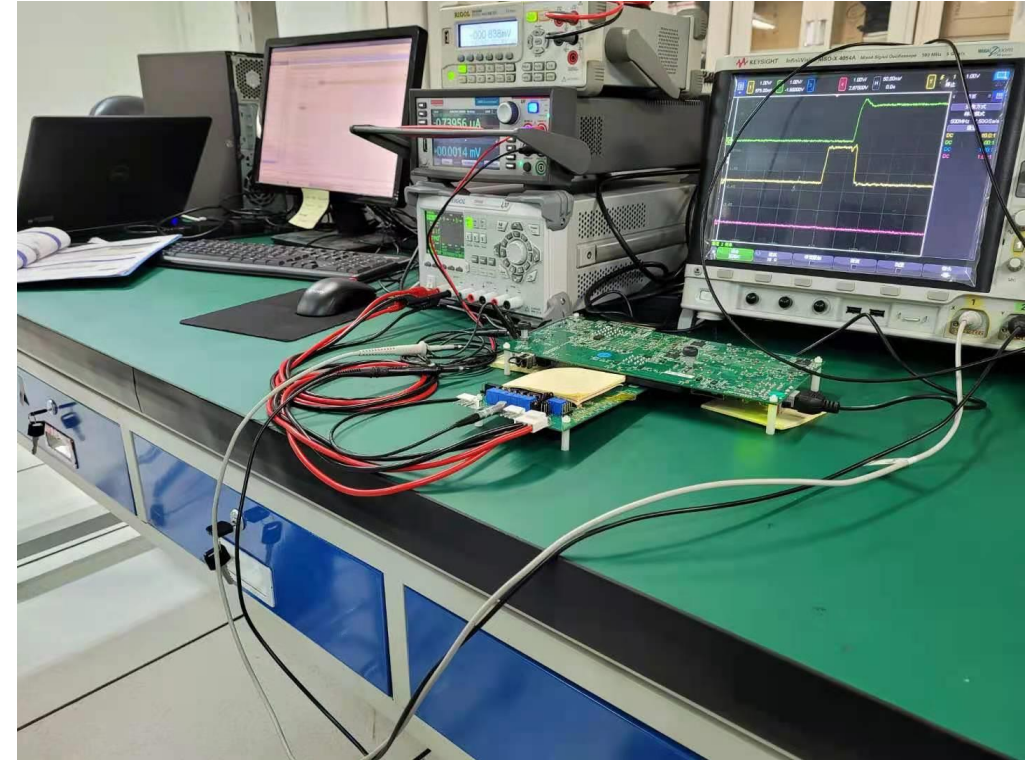
The timing of the readout logic



- We found data timing issue when switch block.
- Though the chip function simulation and ILA testing, we think signal 'blk_sel' is delayed for uncertain reason.
- Solution:
 - Use IODELAY to adjust IO timing
 - **Before switching block, insert one clock period to set signal 'blk_sel'.**

The test setup @CCNU

- 4 daughterboards works well. (002, 004, 005, 008)
 - 2 chips are replaced. (002, 004)
 - Soldering issue.
 - PSUB current issue.
- Each part of the board should be tested before testing chip
 - DAC70004
 - SPI
 - Bandgap voltage



In future

Release Testing-System v2.0.0

- Rolling shutter mode implement and fully test.
- More testing and more debugging...

Thank you!