@Debugging

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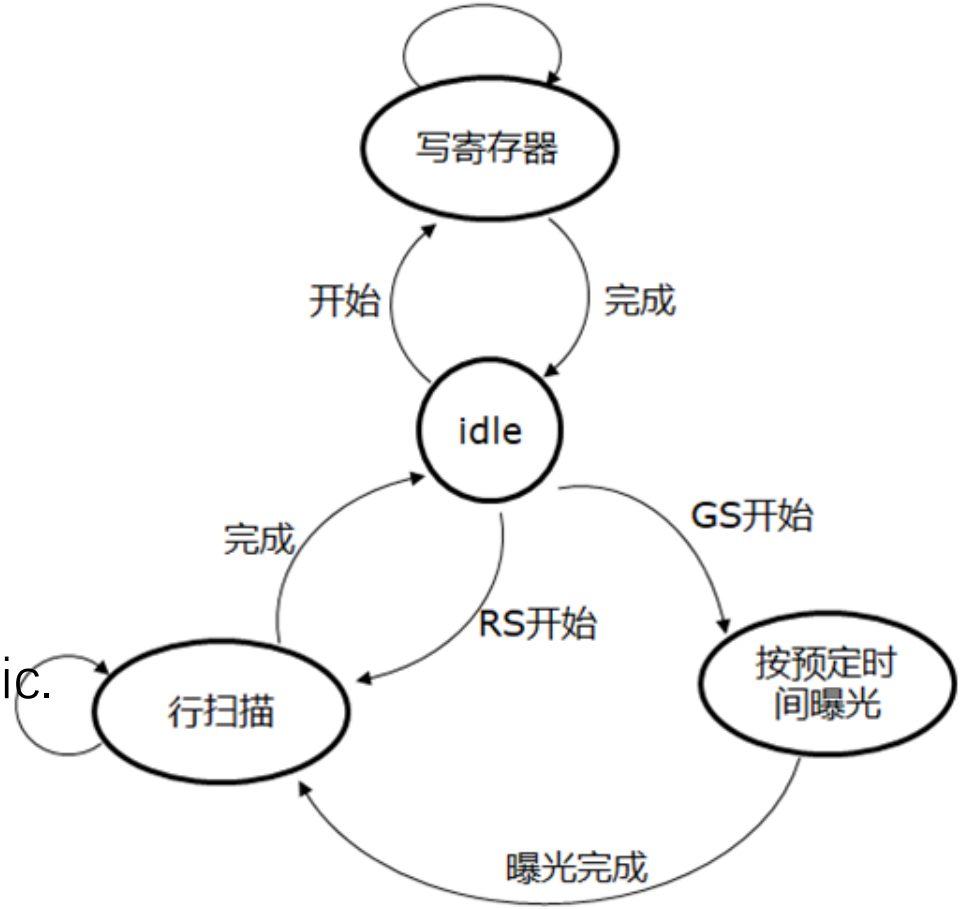
Bugs

- Pixel configuration:
  - FIFO block write failed. Firmware logic stuck at configuration logic.
  - Firmware checkout back to the version register configure mode. (Slow but works).
  - Not fixed yet
- Firmware macro define
  - When we change the system clock from 12ns to 50ns, the state machine stuck at configuration logic.
  - The maximum value of some counters should be defined directly, not based on the system period.
  - Fiexd



Updates

- More signals
  - Hitmap, for testing digital logic
  - INQUIRY, switch DATA_OUT logic
- Debug mode
  - These FPGA output signals are controlled by software and firmware. Add a „debug“ flag to enter debug mode. these signals are controlled only by software.
    - DIGSEL_EN
    - ANASEL_EN
    - APLSE
    - DPLSE
    - GSHUTTER
    - CA
    - CA_EN

Test results – PCB and Control Logic

- DAC70004
  - Working as expected.
- In Chip

  The timing is checed by Vivado ILA, and it's right, but the hitmap_out monitored is wrong.
  - Digital
    - some signals are working. (matrix_grst, mask, gshutter)
  - Analog front-end
    - No change on Aout while using APLSE
    - Manual set VPLSE_HI, We got Aout as expected.
  - SPI
    - Working as expected.
  - DAC
    - 3 channels are modifiable, the other 3 channels are not.

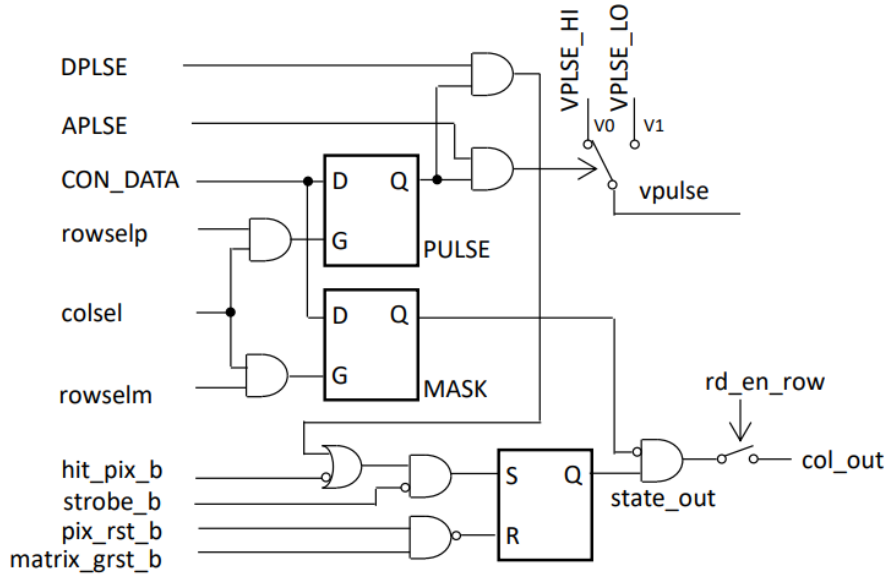


图 3 像素内数字电路 DGT_V0

Test results – Zero Suppression

- INQUIRY
  - 0b00 - K28.5
    - DATAOUT: 0xbc, as it should be.
  - 0b01 - Data
    - We have **first-time** programming condition.
  - 0b10 - FIFO Status
    - not tested yet.
  - 0b11 – RESERVED
- CACHE_CLK
  - Working as expected
- CACHE_BIT_SET
  - 0b0000
    - Data should be 0x0000
    - **first-time** programming condition.
      - Sec 1 and sec 4 output 0
      - Sec 2 and sec 3 output 1
  - 0b0001
    - Same as 0b0000

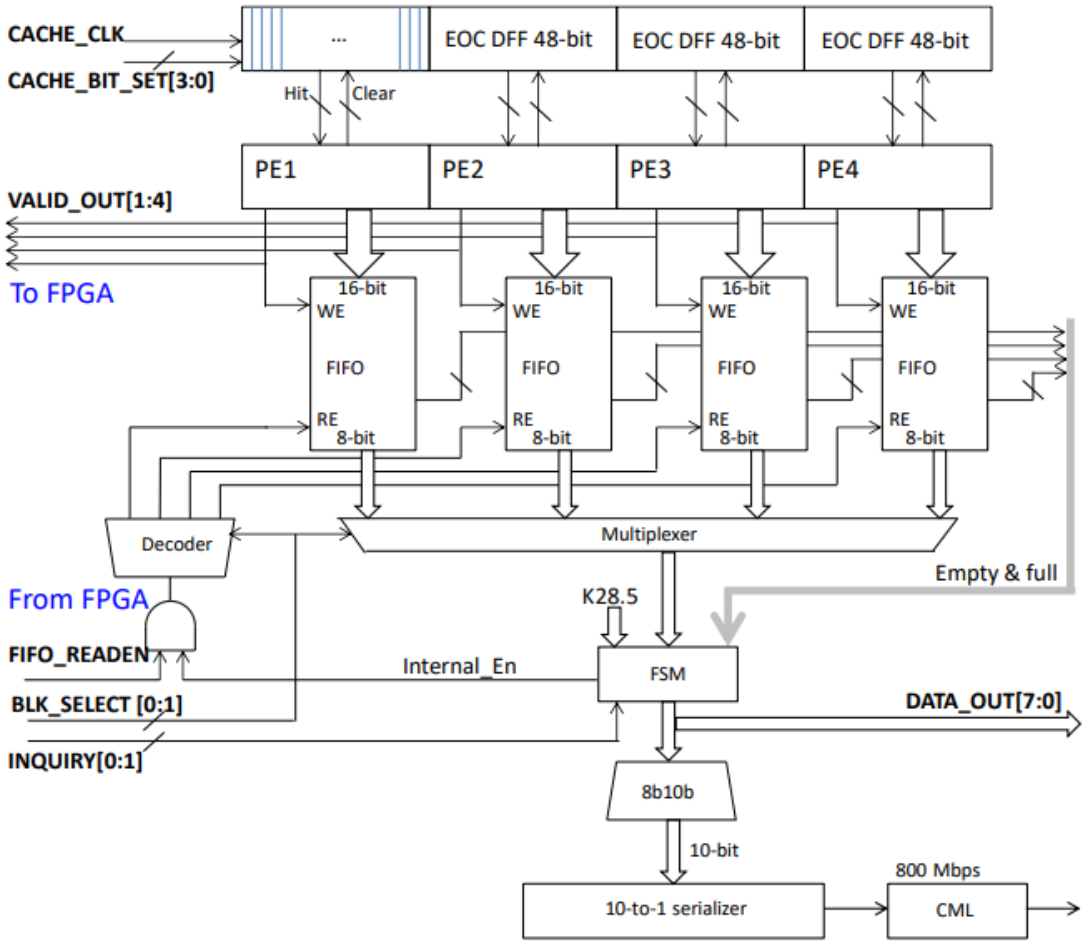


图 9 零压缩和数据缓存电路框图

Thank you for your attention.