

Jadepix3 Testing @IHEP

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Test Setup

- IPbus small-scale system.
 - KC705: 192.168.3.18/24
 - PC: 192.168.3.100(8)/24
- Firmware (debug branch active):
 - https://github.com/habrade/JadePix3_Firmware/tree/debug
- Software (debug branch active):
 - https://github.com/habrade/JadePix3_Software
- Update the software environment @IHEP

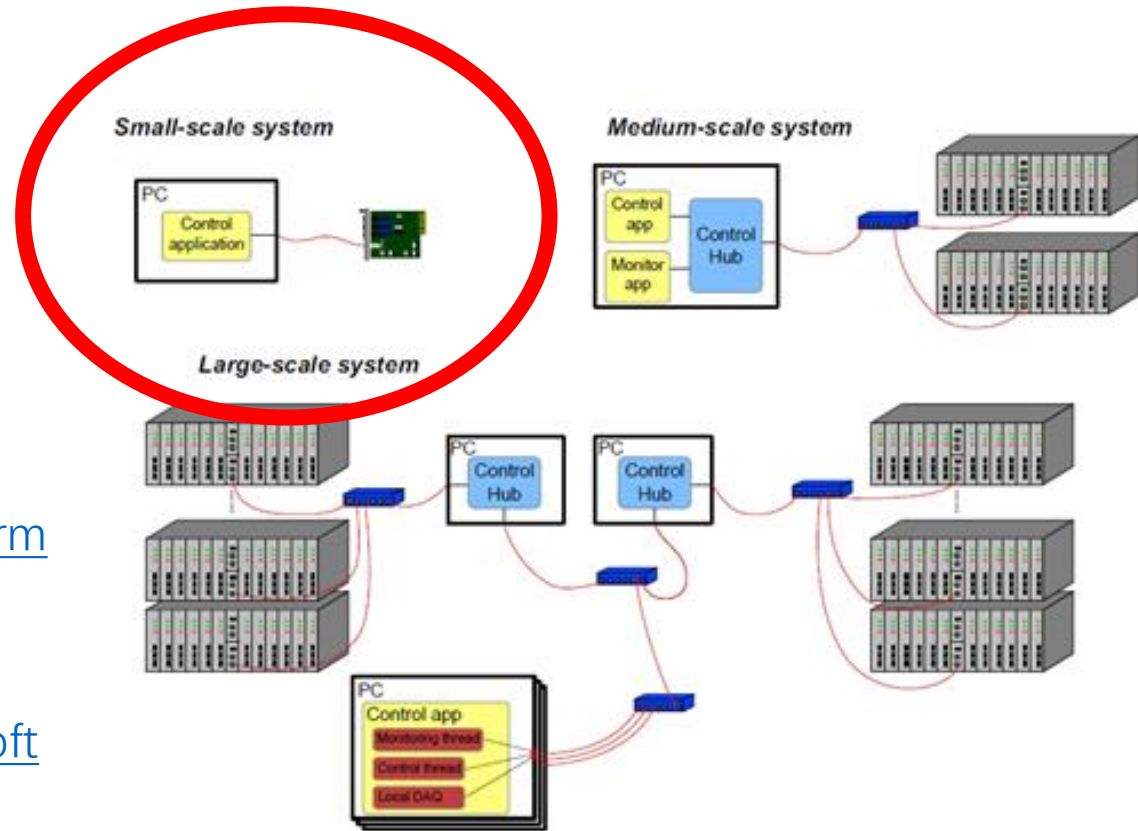
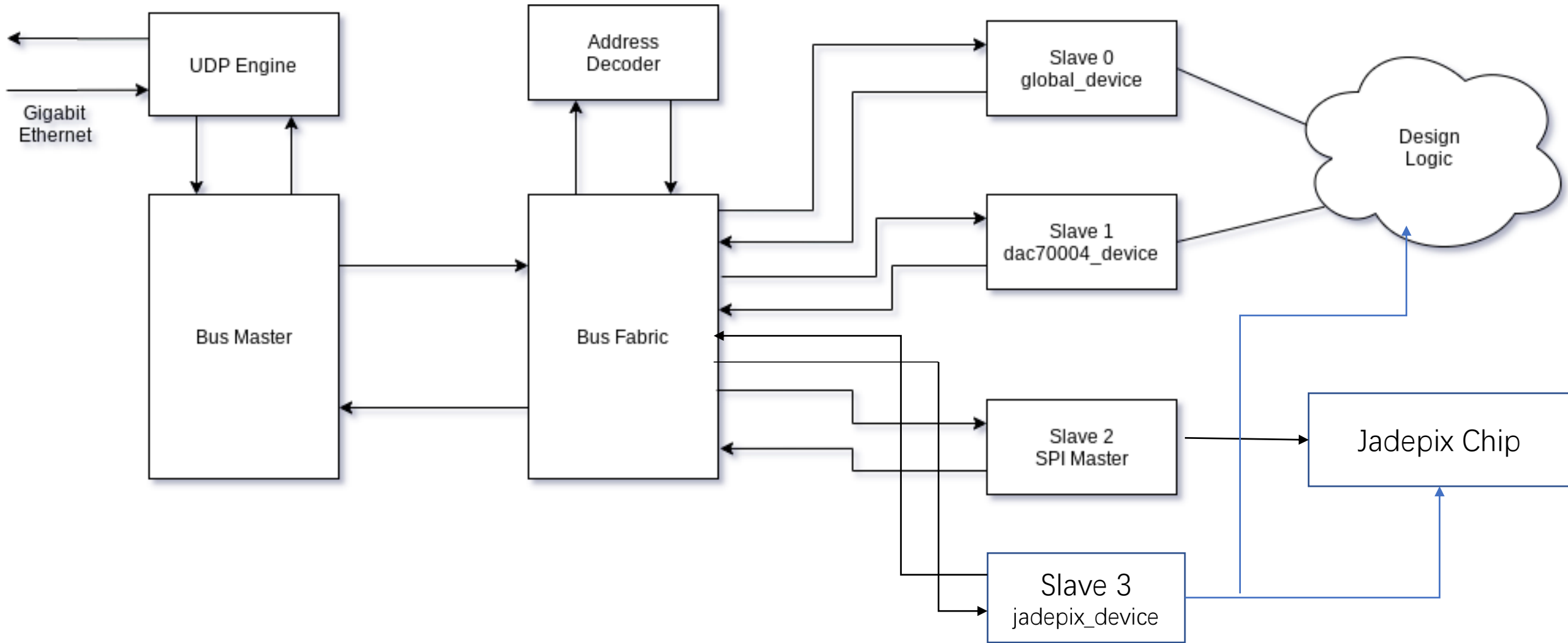


Figure 1. Example topologies of IPbus control systems involving μ TCA hardware, from small to large scale.

Firmware structure



The logic

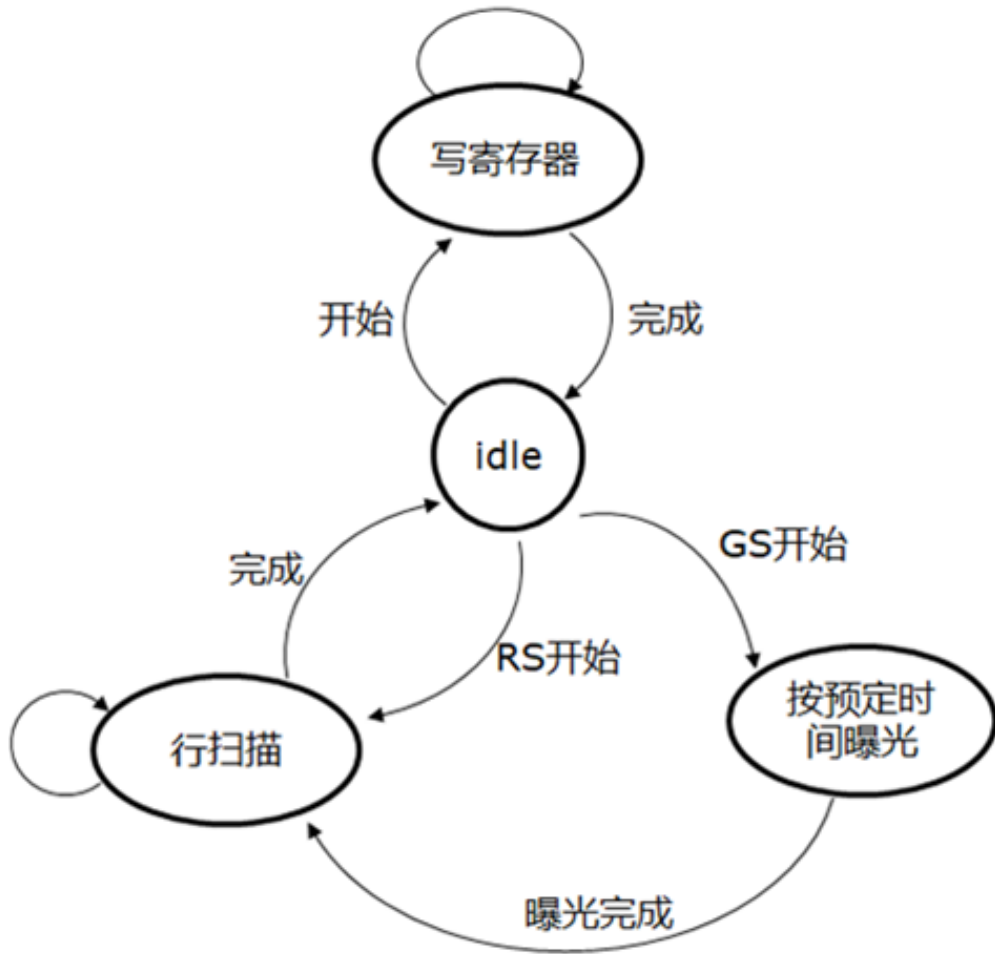


Figure from YunPeng Lu

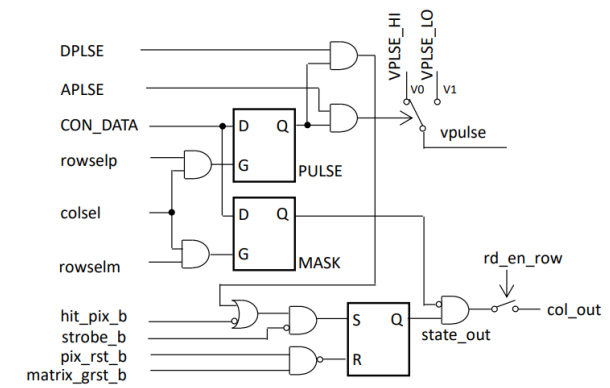


图 3 像素内数字电路 DGT_V0

Pixel configuration:

FIFO block write failed. Firmware logic stuck at configuration logic.

Firmware checkout back to the version register configure mode. (Slow but works).

Not fixed yet

Global Shutter:

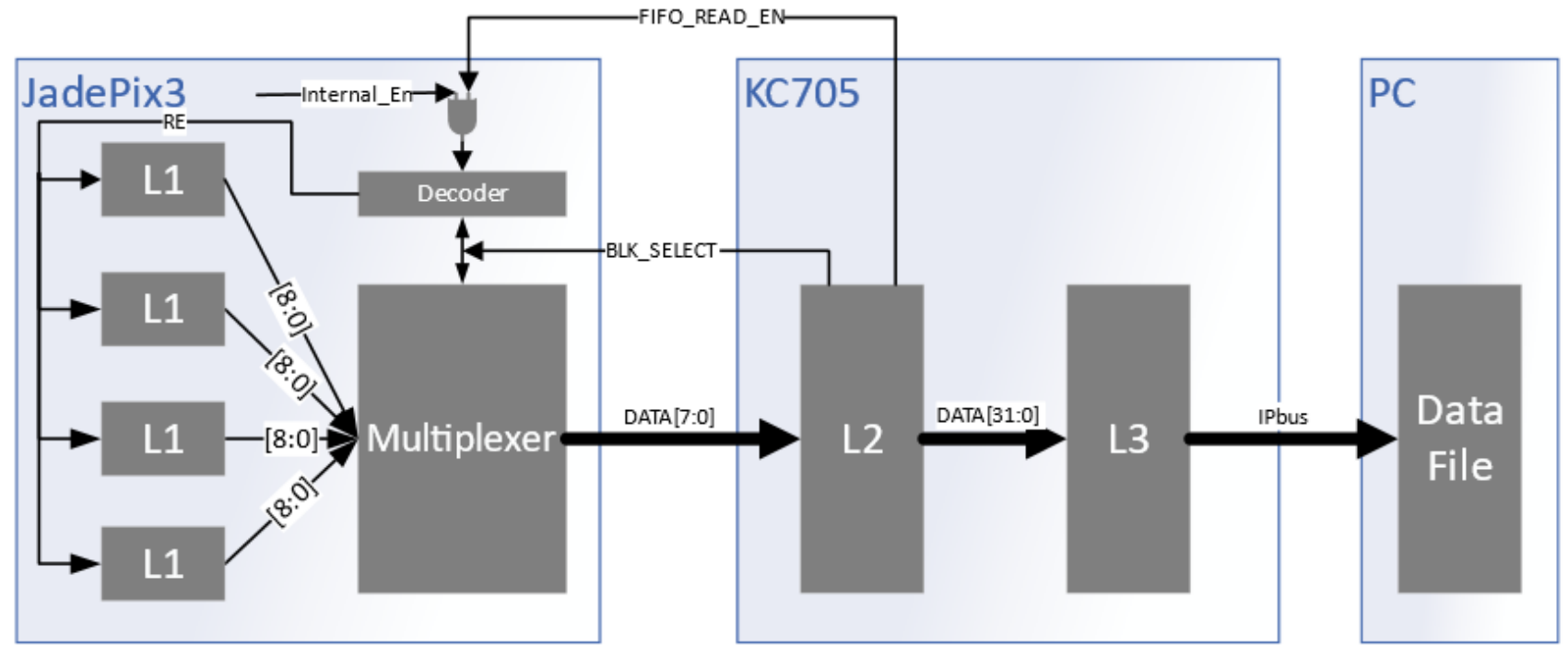
Working after fixing the bugs and the logic in the software and the firmware.

The default value of *blk_select* should be change manually each time. (Timing issue)

Rolling Shutter:

Not tested yet.

Data Loss Discussion



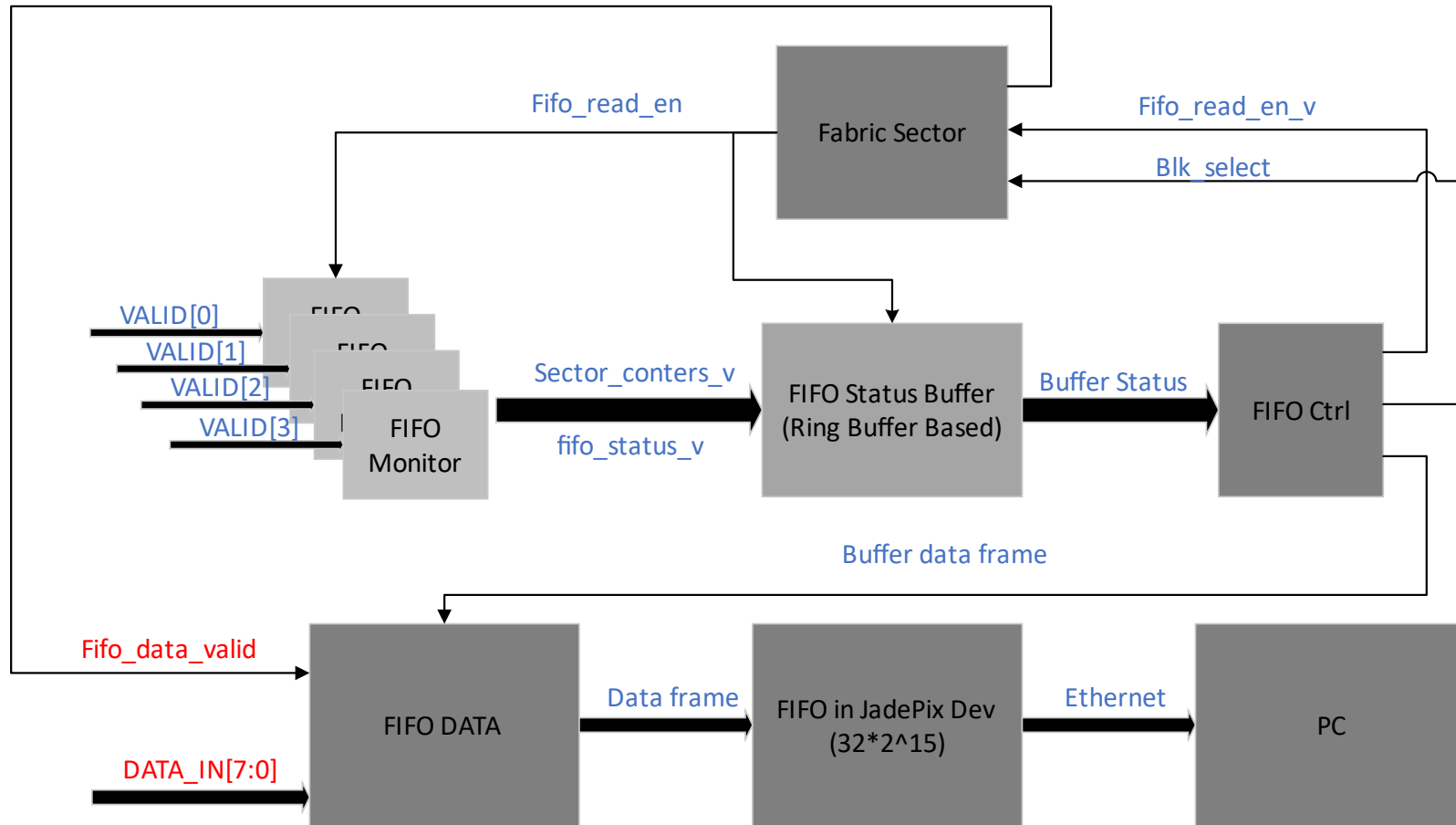
- Three Level Caches
 - L1: the cache FIFO in the chip, size=48*16 bits
 - L2: the ring buffer in the FPGA, size=192*86 bits
 - L3: the IPbus data FIFO in the FPGA, size= $2^{17} * 32$ bits
- Since the FIFO in the chip is a synchronous FIFO, the readout speed is same as the write speed. We have 4 FIFOs input and 1 selected output. In principle, the readout speed should be 4x than the write speed. So the caches will be overflow soon if we have plenty of input data, then the data lost.
- L1 low speed readout -> L1 and L2 overflow
- PC software low speed readout -> L3 overflow

Conclusion

- Jadepix3 Chip is alive and working.
- Timing issue in the firmware need to be test.
- Data readout path is clean @ low speed and small scale.
- X curve and Rolling shutter mode have not tested.

Backup

Jadepix Data Readout



FIFO type: Standard or First Word Fall Through?

fifo_data_valid: one clock period after signal `fifo_read_en` ?

There are WFIFO and RFIFO slaves in Jadepix device, so we can read DATA in RFIFO Periodically.

Need to test how fast the data should be read, and the number of data for one block read.

