Status of TaichuPix chips

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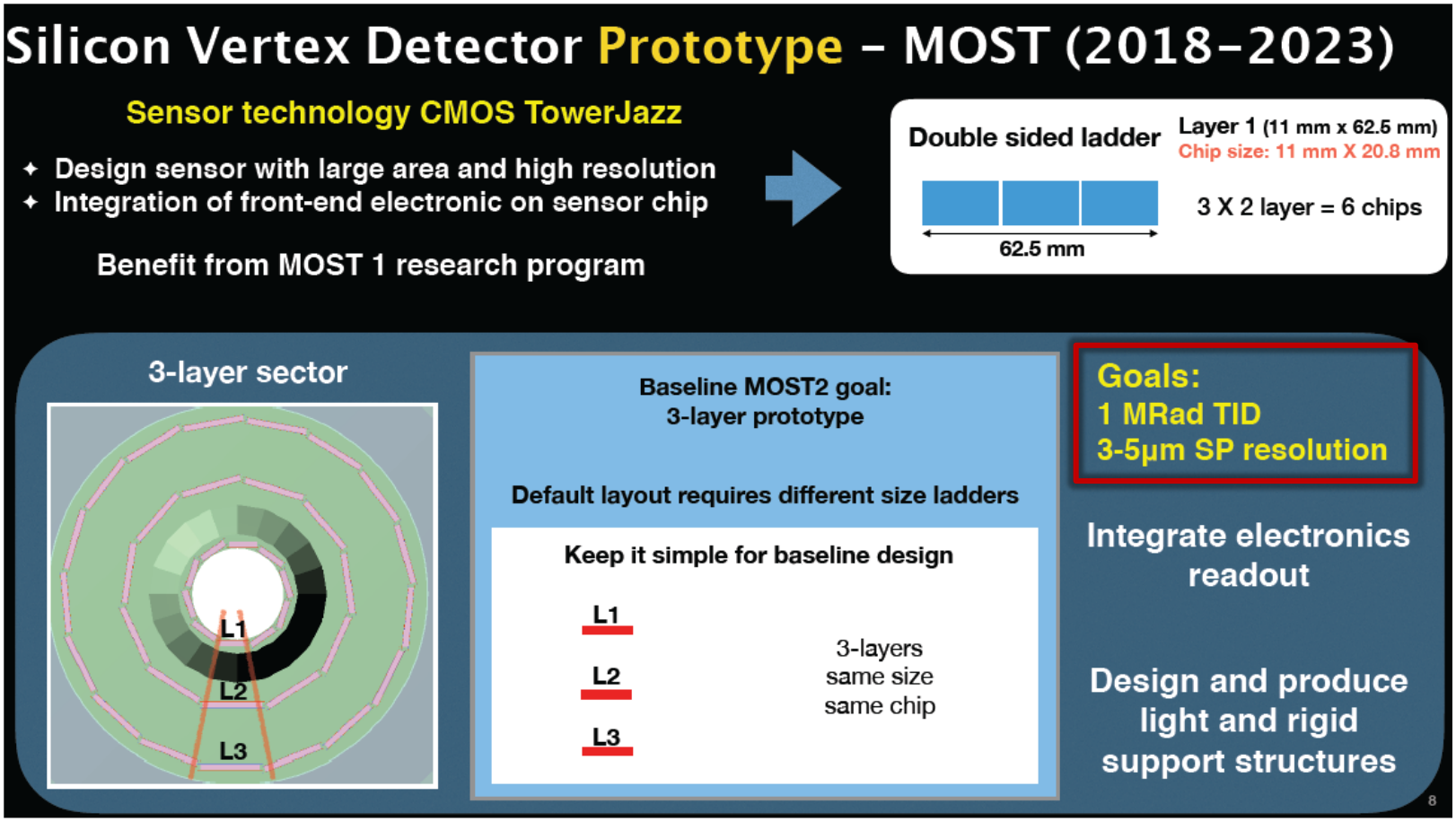
On behalf of the CEPC MOST2 Vertex detector design team

2021-1-22

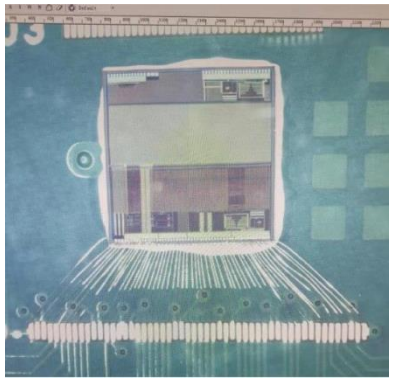
MOST2 project requirements on pixel chip



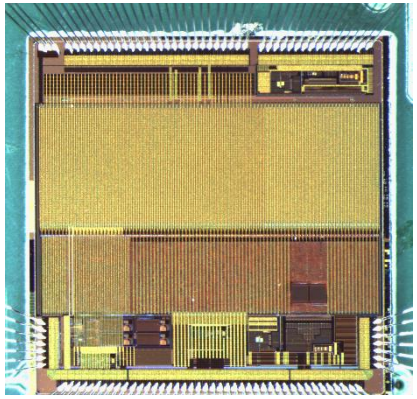
- **Motivation for TaichuPix chip design**
  - Large-scale & full functionality pixel chip
  - Fit to be assembled on ladders with backend Elec. & DAQ

Ref: Introduction to the Pixel MOST2 Project, Joao Costa, 2018.6

TaichuPix chips overview



TaichuPix-1
Chip size：5 mm × 5 mm
Pixel size：25 μm × 25 μm

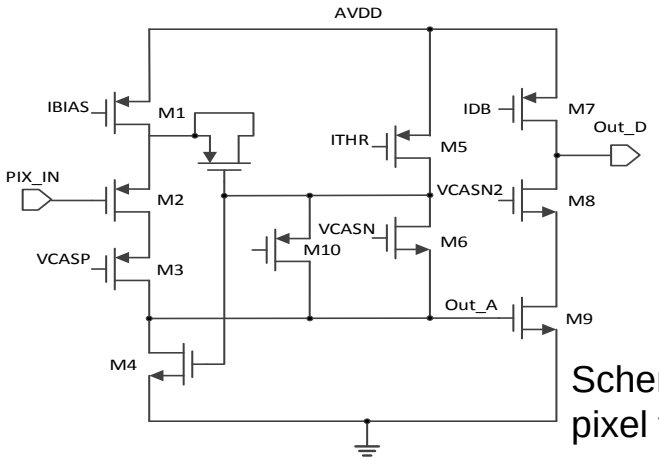


TaichuPix-2
Chip size：5 mm × 5 mm
Pixel size：25 μm × 25/24 μm

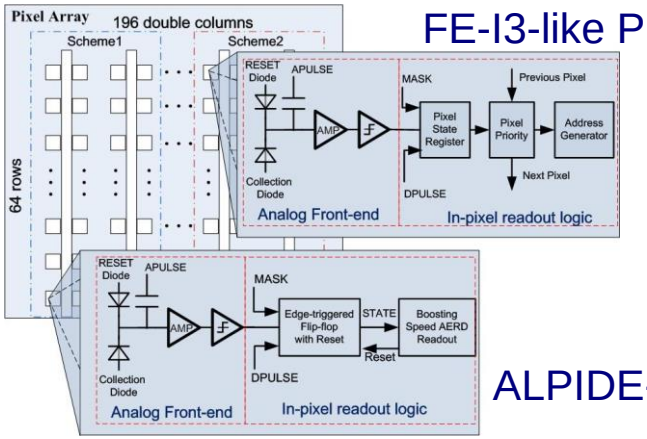
- **Two MPW chips were fabricated and verified**
  - TaichuPix-1: 2019.06~2019.11
  - TaichuPix-2: 2020.02~2020.06
- **Chip size 5 mm×5 mm with standalone features**
  - In-pixel circuitry:
    - Continuously active front-end
    - Two digital schemes, with masking & testing config. logics
  - A full functional pixel array (64×192 pixels)
  - Periphery logics
    - Fully integrated logics for the data-driven readout
    - Fully digital control of the chip configuration
  - Auxiliary blocks for standalone operation
    - High speed data interface up to 4 Gbps
    - On-chip bias generation
    - Power management with LDOs
    - IO placement in the final ladder manner
      - Multiple chip interconnection features included

Design variations of pixel array in TaichuPix-2

Sector	Pixel front-end	Pixel digital	Pixel size
S1	Same as S1 of TC1, reference design	FEI3-like	25 μm × 25 μm
S2	M6 with guard-ring, PMOS in independent nwell	FEI3-like	25 μm × 25 μm
S3	M6 in enclosed layout, PMOS in independent nwell	FEI3-like	25 μm × 24 μm
S4	Increasing M3, M4, M9. M6 in enclosed layout, PMOS in independent nwell	FEI3-like	25 μm × 25 μm
S5	Same FE as S2, with smaller sensor	ALPIDE-like	25 μm × 25 μm
S6	Same FE as S1	ALPIDE-like	25 μm × 25 μm



Schematic of in-pixel front-end

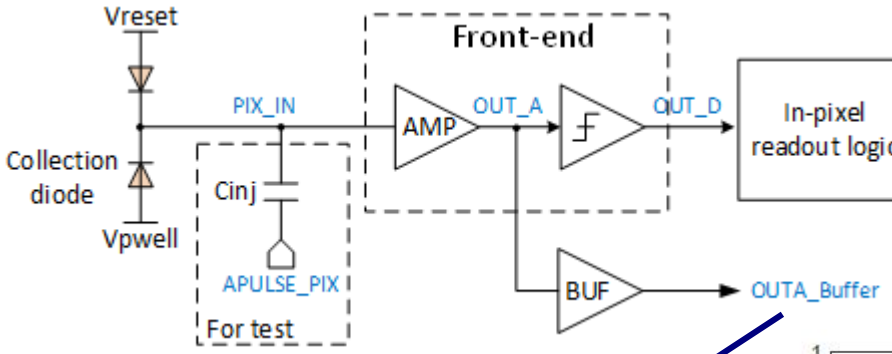


FE-I3-like Pixel

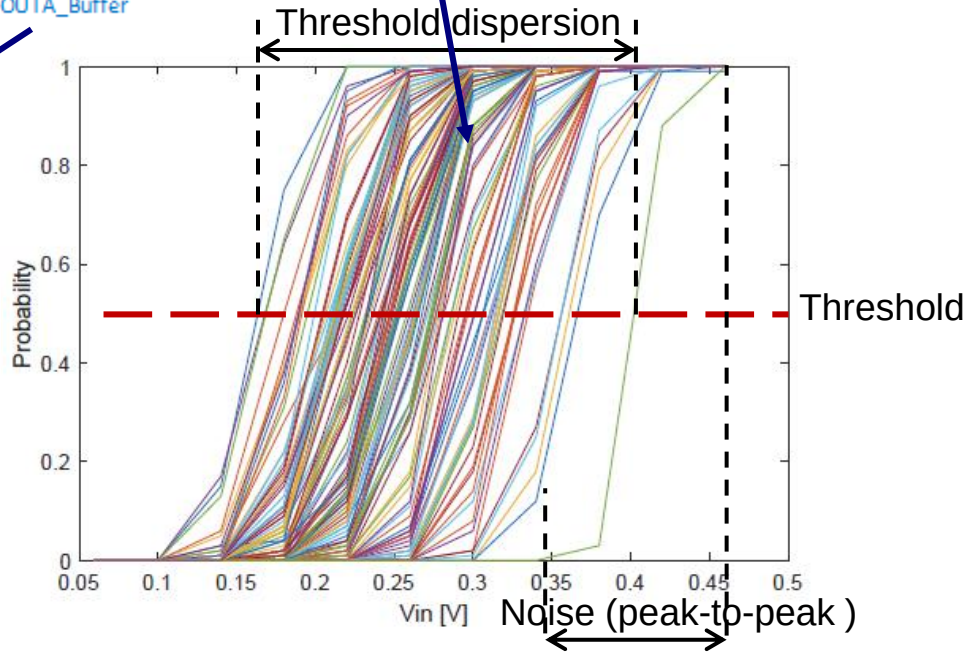
ALPIDE-like Pixel

Electrical test

- **Electrical performance verified by injecting external voltage pulses into pixel front-end**



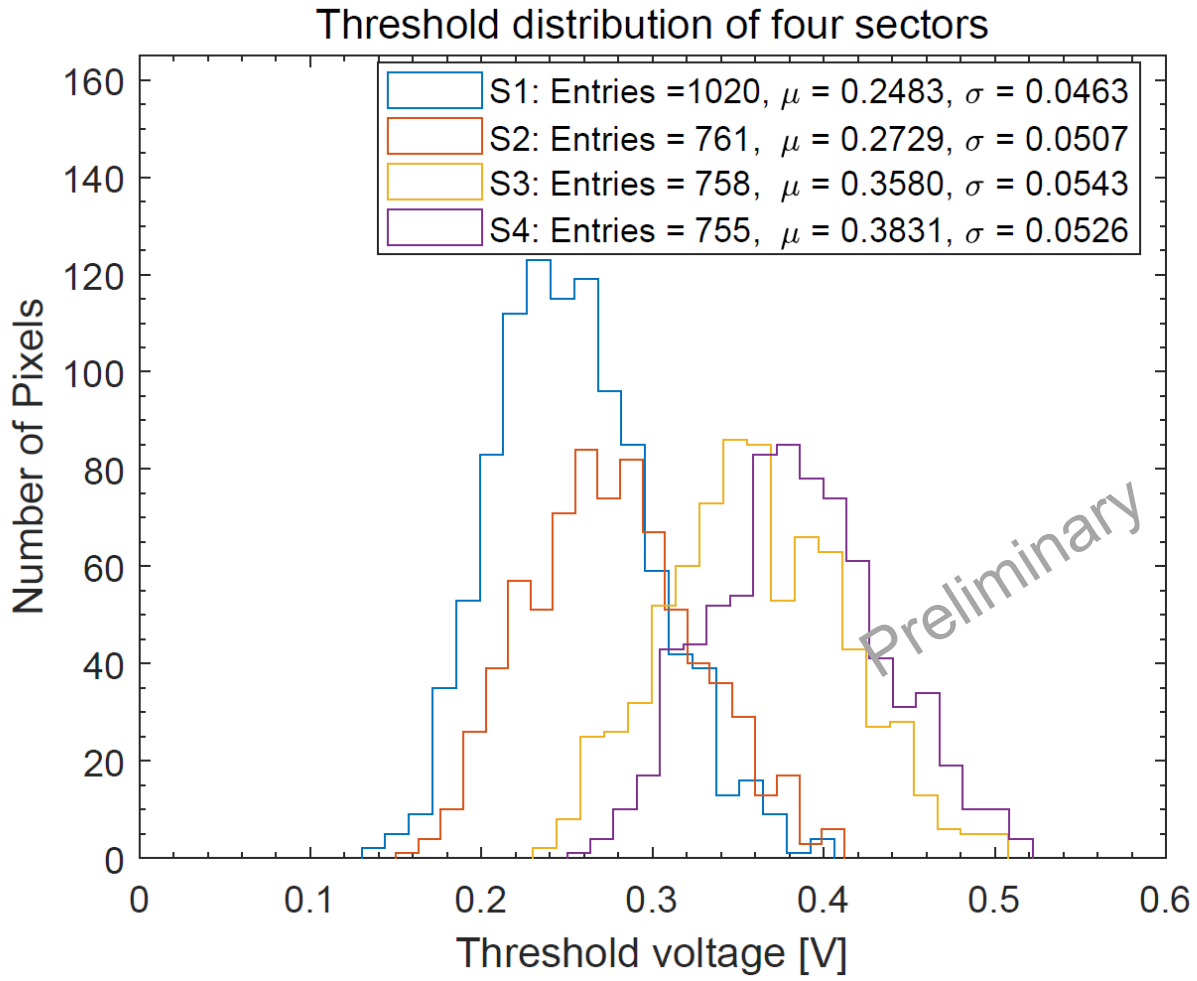
Analog output of a pixel @ Vin = 0.9 V



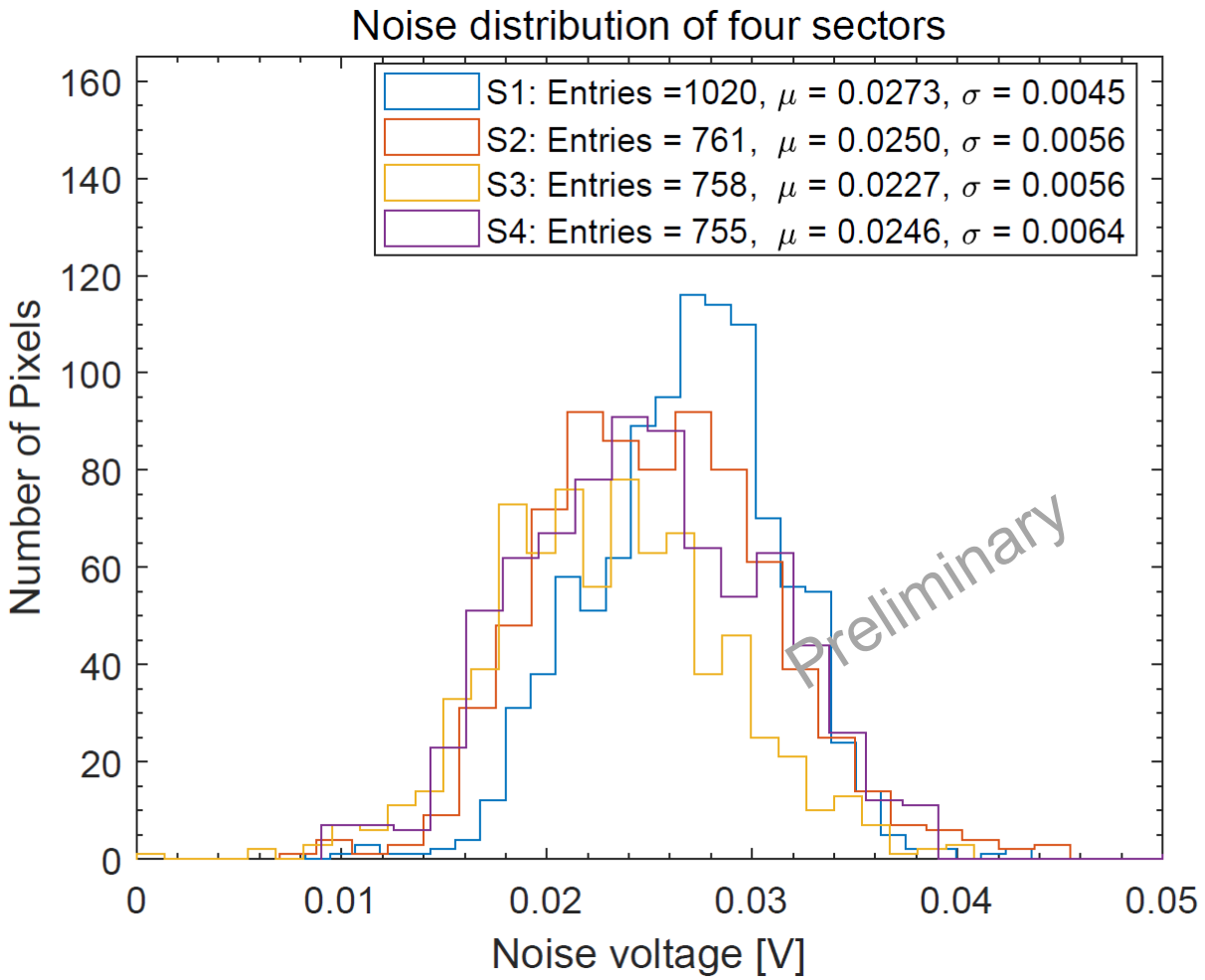
Measured “S-curve” for 128 pixels

Threshold distribution measured on S1-S4

- **Based on the same bias setting for pixel analog, S-curves measured for S1-S4 (with different pixel analog designs)**



Noise distribution measured on S1-S4



The measured threshold and noise variations between different sectors agree with design qualitatively.

Comparison of sectors

- **Threshold and noise performance summary**

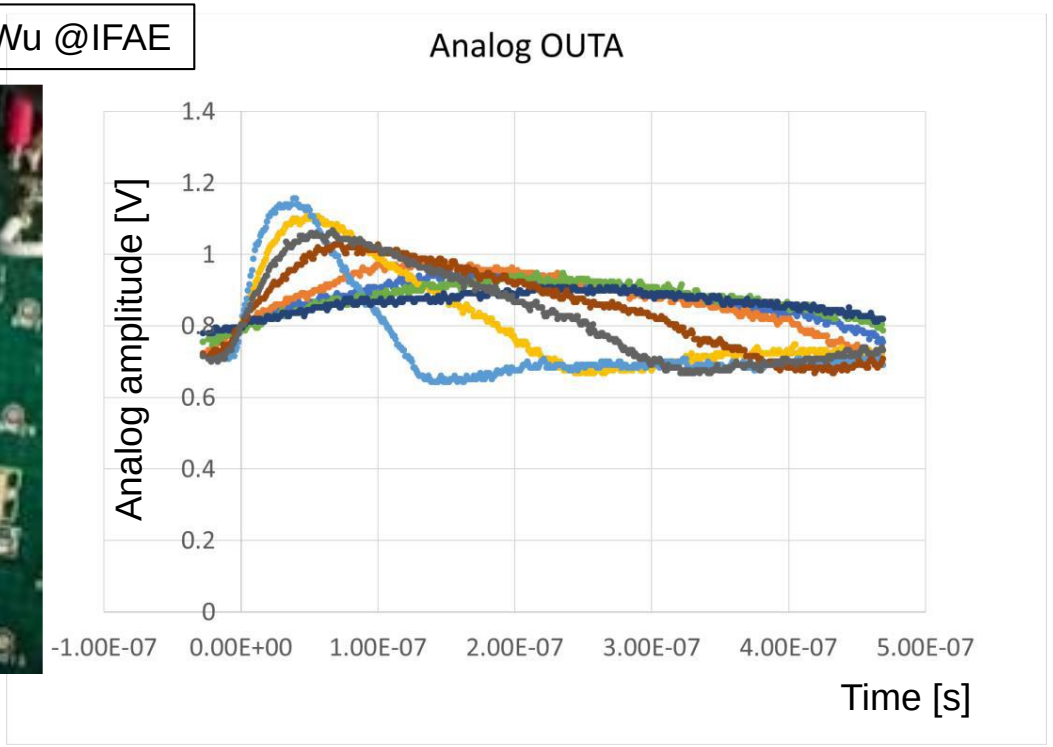
Preliminary

	Threshold Mean (mV)	Threshold rms (mV)	Random noise (mV)	Total noise (mV)
S1	248.3	46.3	27.3	53.8
S2	272.9	50.7	25.0	56.5
S3	358.0	54.3	22.7	58.9
S4	383.1	52.6	24.6	58.1

- **Four sectors with FEI3-like digital logic works well, and show similar noise performance. S1 shows the lowest threshold.**
  - Need testing more chips to verify performance variations
- **Analog front-end in S5 & S6 (with ALPIDE-like digital) proved to works normally, but unfortunately no digital signal output observed when input an analog/digital test pulse. Need further investigation.**

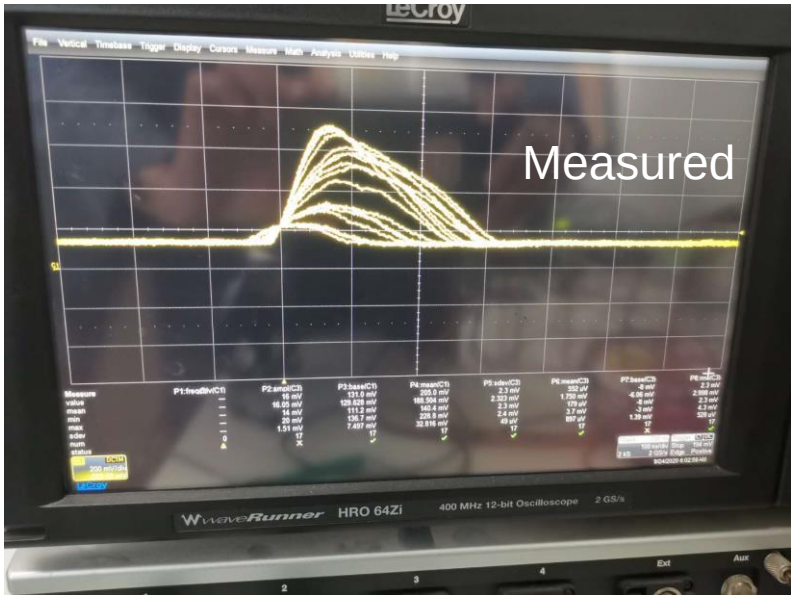
TaichuPix-1 response to ^{90}Sr

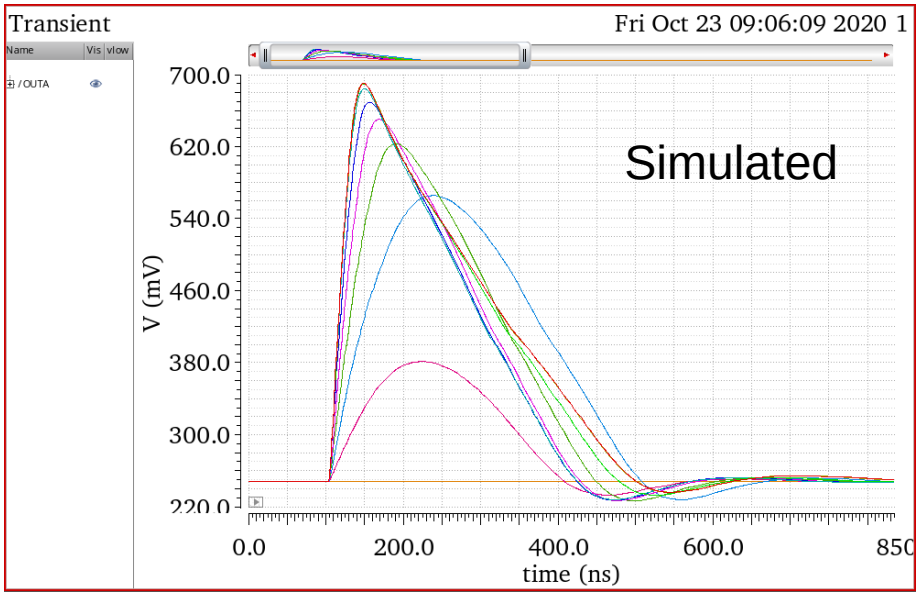
By T. Wu @IFAE



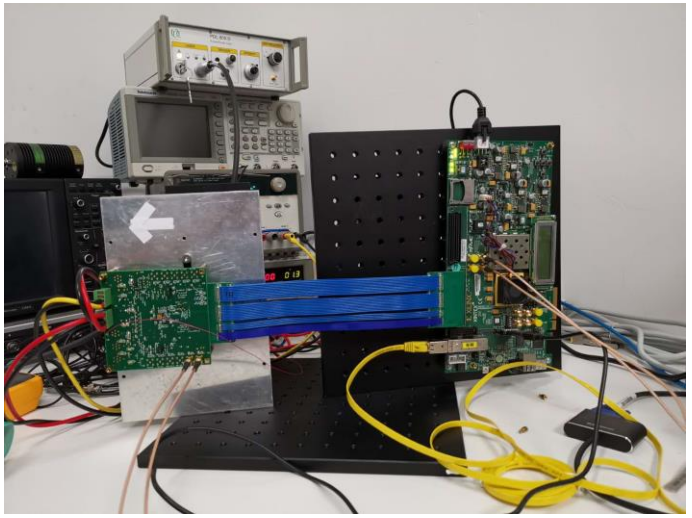
- **Analog signals of a pixel were captured with oscilloscope.**
- **Larger signal having smaller peak time and pulse duration, agrees with simulation**
- **TaichuPix-2 will be tested with ^{90}Sr soon**

Preliminary verification with X-rays

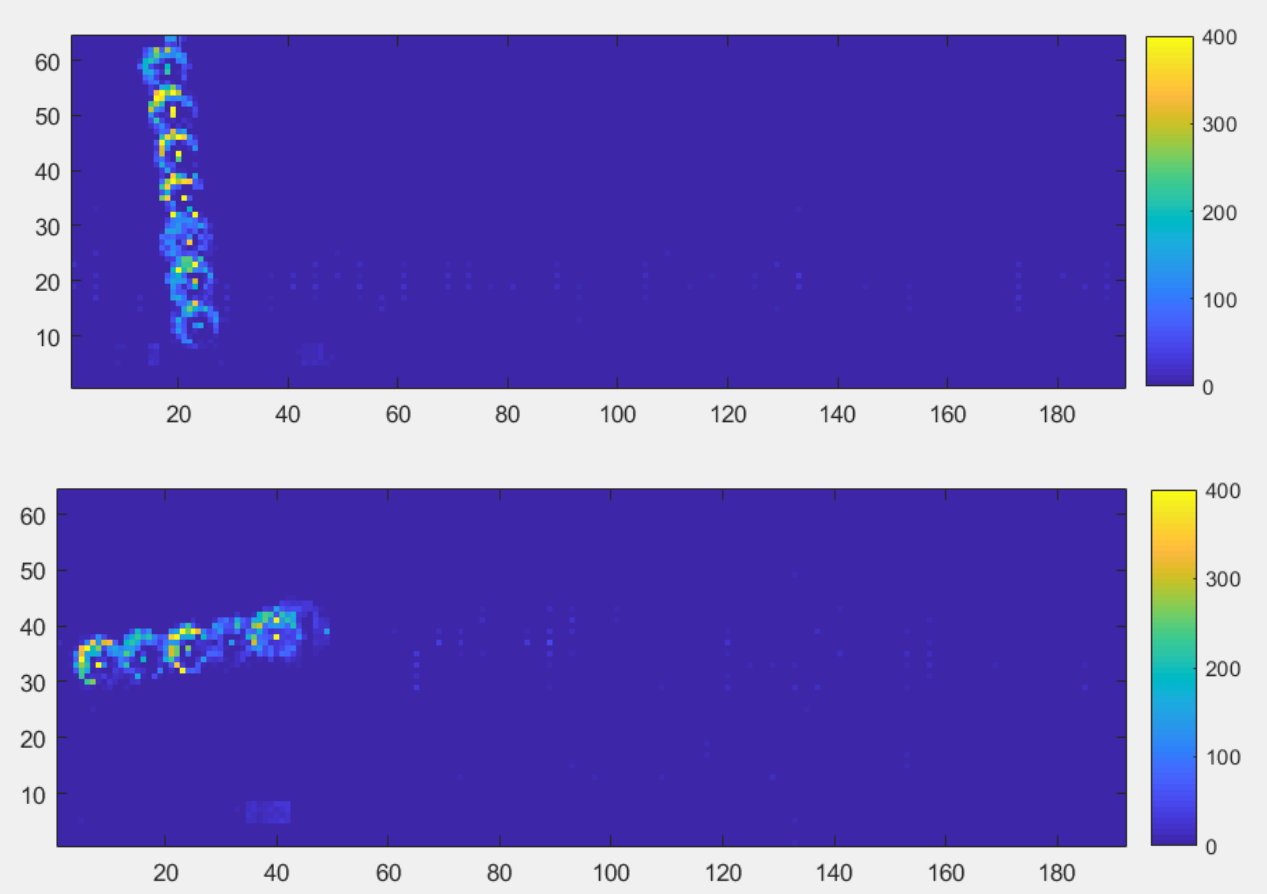


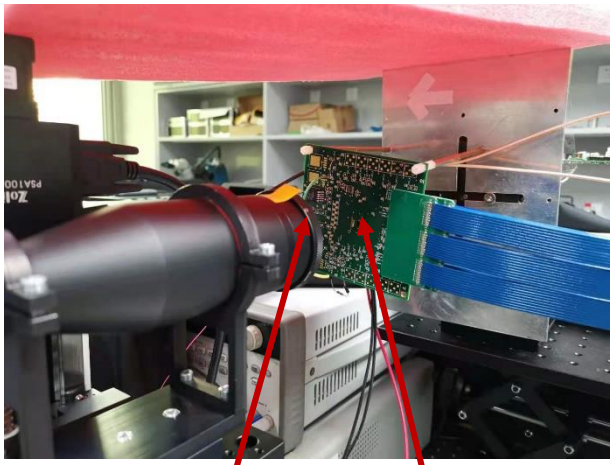


- **Analog output waveform agreed with the simulation when tested by X-rays**
  - eg. signal amplitude, signal width, edge speed
- **Note: for the small signal, the S/N ratio was also good, inferred that the noise performance was also good**



Pixel dimension test (Preliminary)





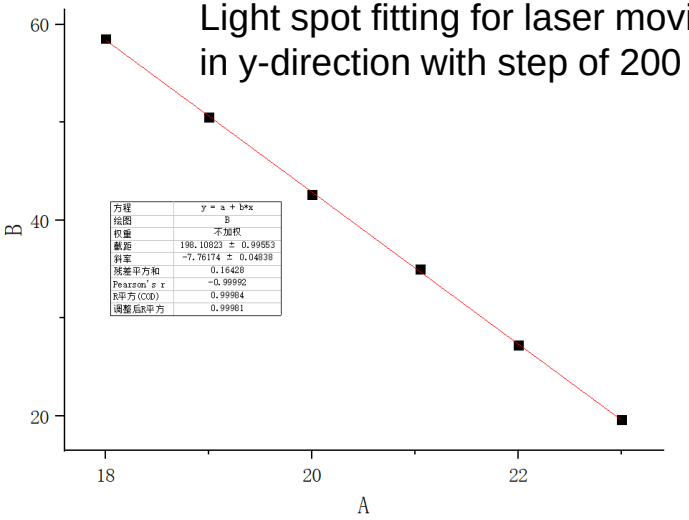
Laser (1064 nm)

TaichuPix-2

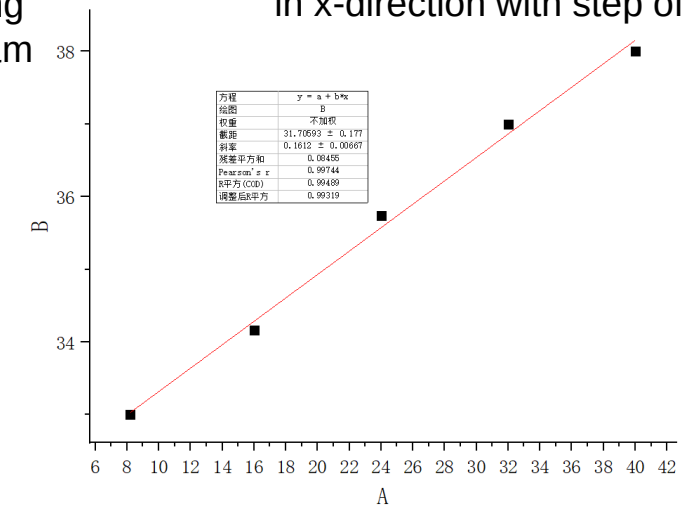
- **Laser was moved every 200 μm in X/Y direction , the center of the light spot was used for position**
- **Linear fit was done with interpolation if the center was found at 2 pixels**

Pixel dimension test (Preliminary)

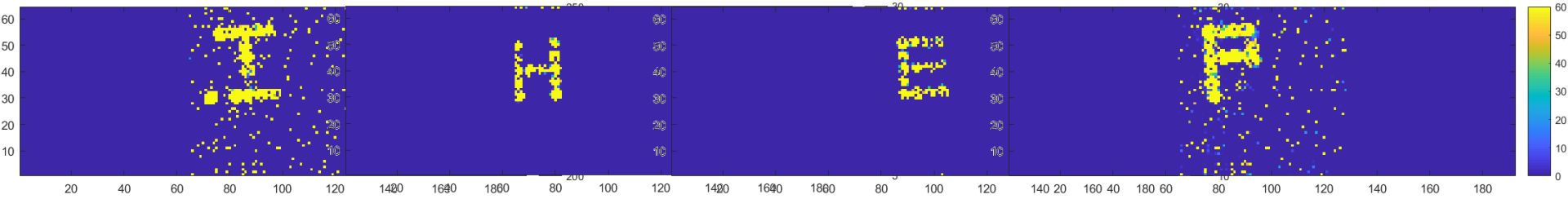
Light spot fitting for laser moving in y-direction with step of 200 μm



Light spot fitting for laser moving in x-direction with step of 200 μm

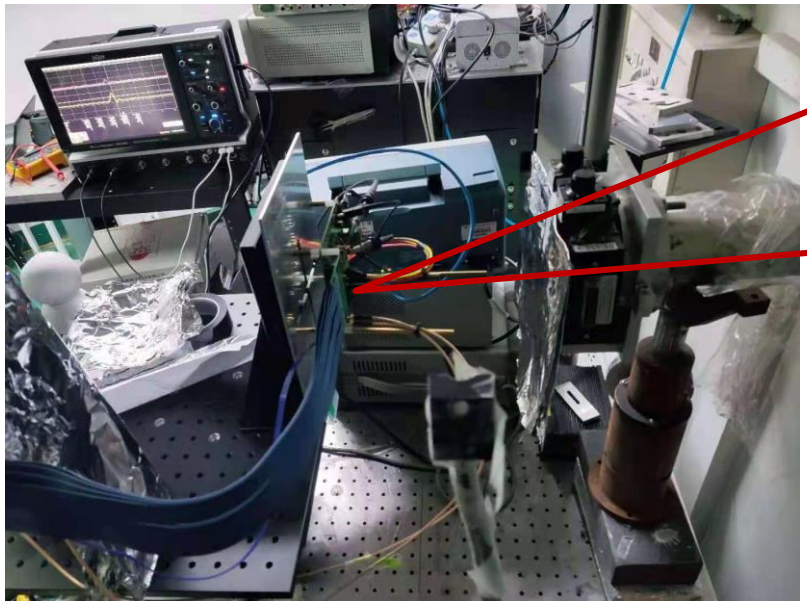


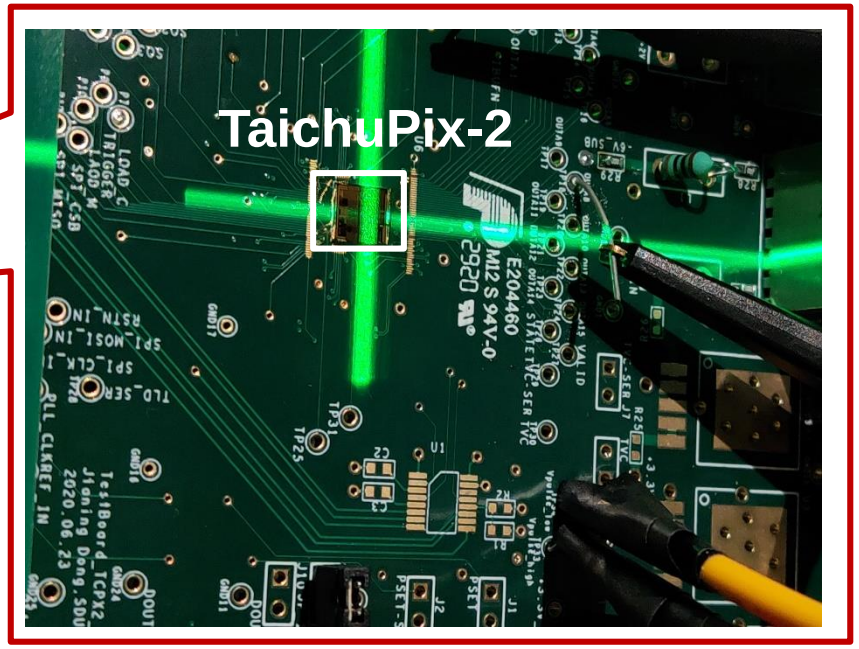
- **-7.762±0.05 & 1/(0.162±0.007) were found as the fitted pixels per 200 μm, while theoretical moving step were 8-pixel**
- **Linearity in x-direc. worse than in the Y-direc., because the test board surface was not fixed vertically to the platform, due to the heavy extension cable of the KC705**



Some letter scanning experiments

TID test setup

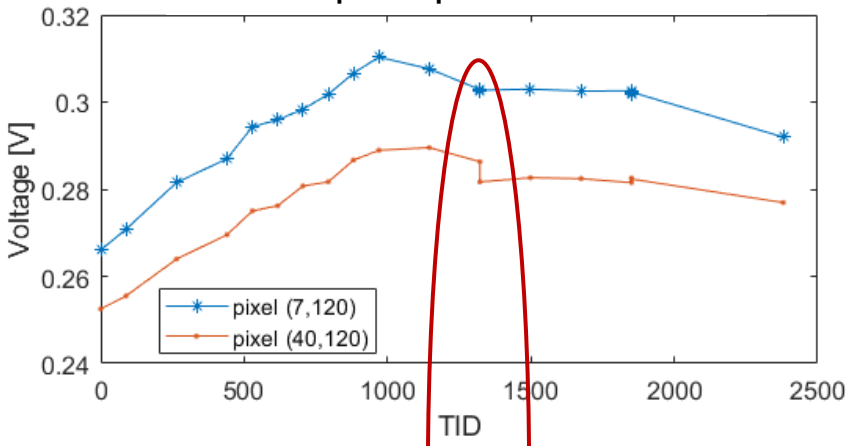




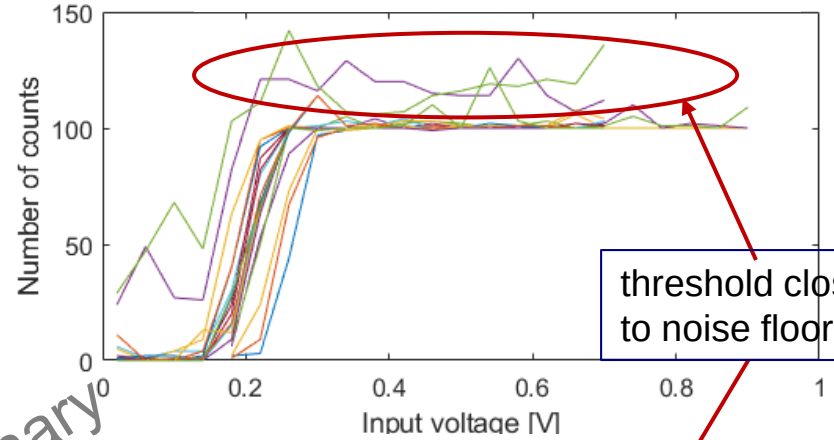
- **TaichuPix-2 irradiated at BSRF 1W2B beamline (6 keV X-ray)**
- **Dose rate ~17.63 krad/min for the first 2.5 Mrad, then 211.56 krad/min for 51 min, then 1.24 Mrad/min for 15 min**
  - Dose rates were calibrated with an ion chamber before test
- **Chip was exposed with full working condition: bias, clk, …**
  - All pixels in working mode, but only two columns (from S1&S3) were enabled to read out
- **Test procedure: chip exposed 5-10 min → close X-ray → electrical test on chip**

TID results within 2.5 Mrad, increased linearly

Probed pixel pedestal vs. TID

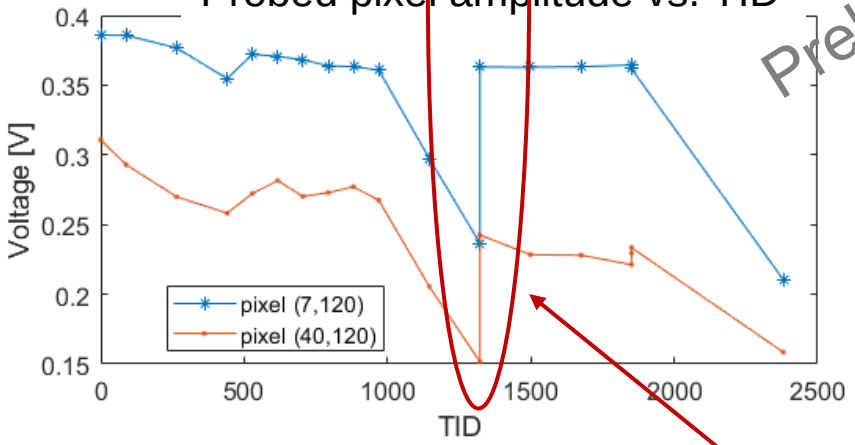


S-curve of pixel (7, 120) in S1

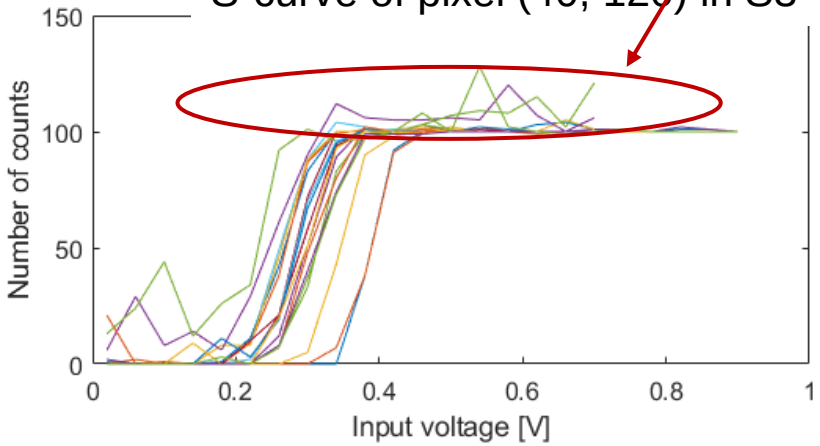


threshold close to noise floor

Probed pixel amplitude vs. TID



S-curve of pixel (40, 120) in S3

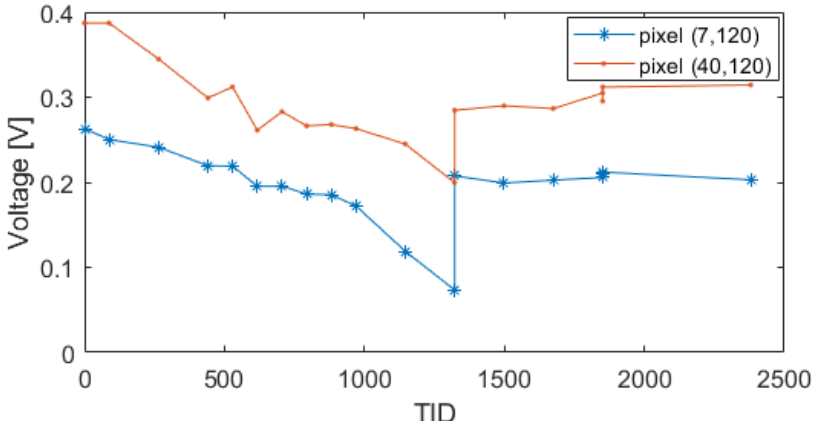


Preliminary

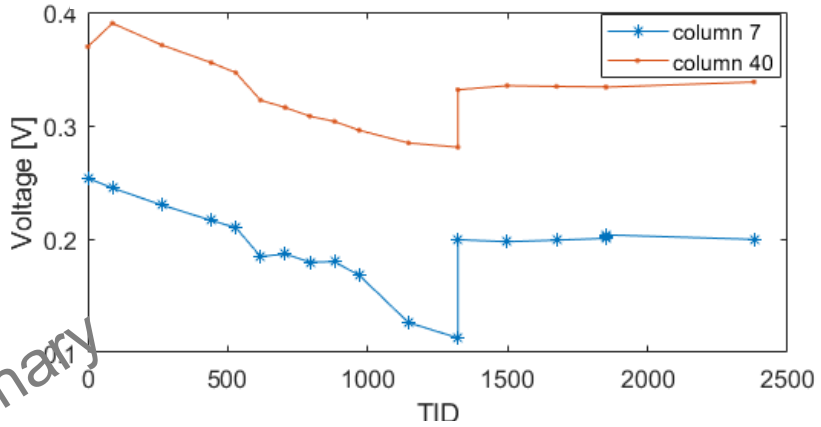
The threshold was initially set at the minimum level. After ~1 Mrad, the pedestal level was shifted to see noise floor in S-curves, so the threshold level was set higher.

TID results within 2.5 Mrad, increased linearly

pixel threshold vs. TID

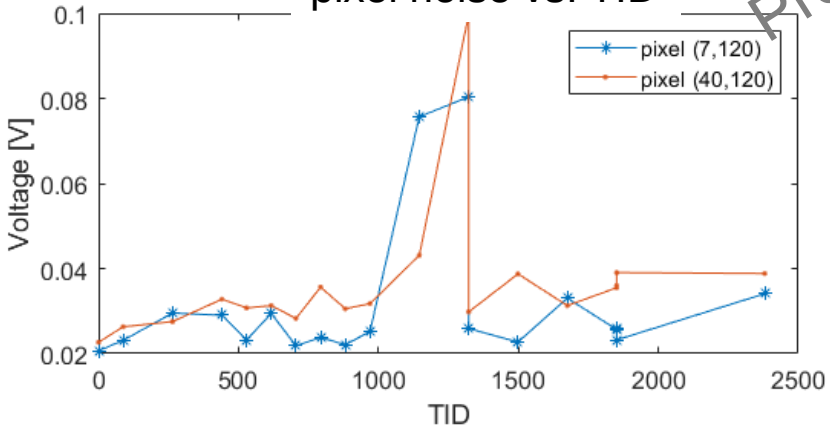


Mean threshold of a column vs. TID

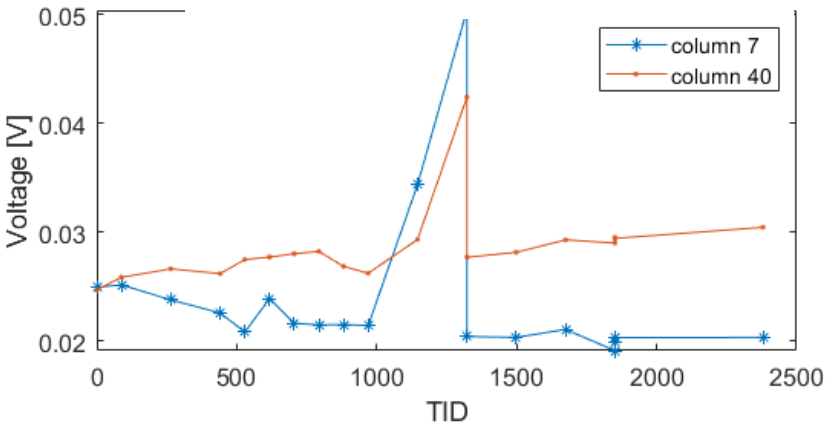


Preliminary

pixel noise vs. TID



Mean noise of column vs. TID



Good chip function and noise performance proved to 2.5 Mrad, and no deterioration observed when TID up to 30 Mrad.

Summary of chip characterization status (1)

- **Pixel analog (✓)**
  - Noise & non-uniformity tested and verified, S-curve scanned, works stable
  - Good S/N, reasonable noise and non-uniformity (However, needs energy calibration)
  - Found some resonance/crosstalk effect during the multiple pixels calibration, however, this will not affect the normal operation of chip
- **Pixel digital (✓)**
  - FE-I3 approach fully verified (proved since Tcpx1), works stable (✓)
  - ALPIDE approach was problematic since Tcpx1, tends to abandon this approach
- **Periphery (✓)**
  - Proved since Tcpx1
  - Fully verified, works stable (✓)
  - Pixel array configuration found slow, however, will not affect the real chip operation after power on configuration
- **DAC (✓？)**
  - Major bug solved from Tcpx1, works stable in Tcpx2 (✓)
  - Minor bug detected: min bias for the threshold still too high, believed can be solved in the next version

Summary of chip characterization status (2)

- **PLL & Data link (✓)**
  - Proved since Tcpx1, further improved in Tcpx2 and works stable(✓)
  - Now always run @160Mbps, more reasonable at the ladder level
  - 4Gbps only tested at block level, found 2Gbps is more stable, meaning too much expense and pressure for the backend electronics
- **LDO & Power (?)**
  - IO ring problem in TCPX1 had solved
  - LDO was problematic since Tcpx1, still waiting a conclusion from the test in Tcpx2
  - Without LDO, the ladder can still be designed, but needs wider power rail for less IR drop
- **Negative substrate power supply**
  - TCPX2 work functionally for VSUB of -1 V~ -5 V, need more test for performance evalu.
- **The chip and the full test-readout system was proved by laser test and X-ray test, works stable**
  - Test board needs to be improved
- **Preliminary test demonstrate TCPX2 satisfies the TID requirement**

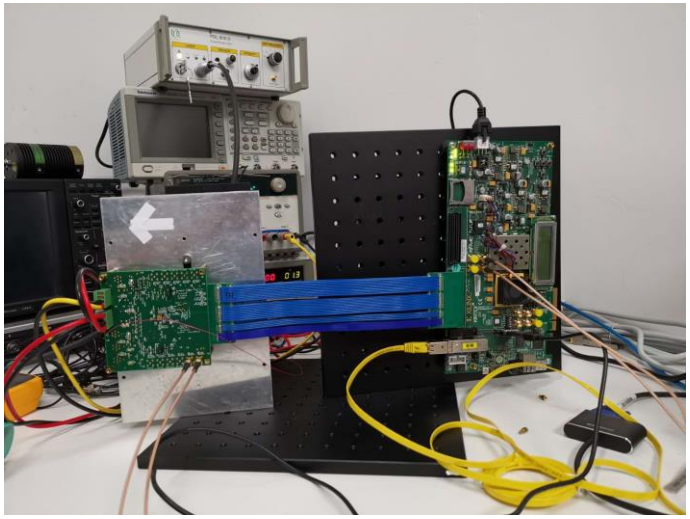
All the key blocks were proved and ready for the full size verification, minor bugs will be fixed in the next version

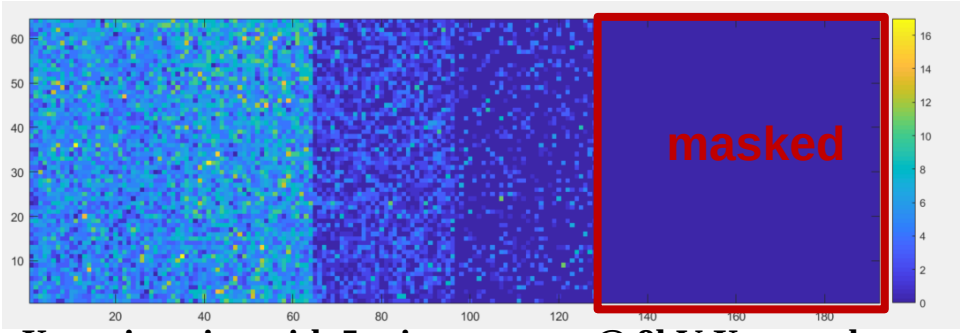
Next submission and schedule

- **Proposed to submit a engineering run in April**
  - To verify full size prototype, including a 1024*512 pixel matrix
  - Pixel analog solution, one of S1-S4, decide after further tests
  - Pixel digital solution: FEI3-like scheme
- **Recent schedule**
  - January: define the final scheme for the full size chip
    - Pixel array digital part finalization
    - Periphery modification & finalization
    - DAC modification scheme
    - LDO's solution
  - 2.1-3.15 (vacation for 2 weeks)
    - Design rescaling & layout
  - 3.15-4.1
    - Layout integration
  - In parallel (January-3.15)
    - Beta source test & beam test to define the final pixel analog solution (threshold)
    - More TID tests to verify chip variations

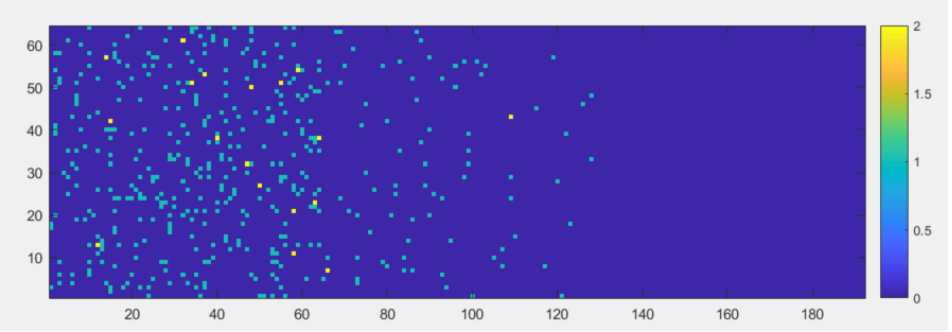
Backup

X-ray imaging





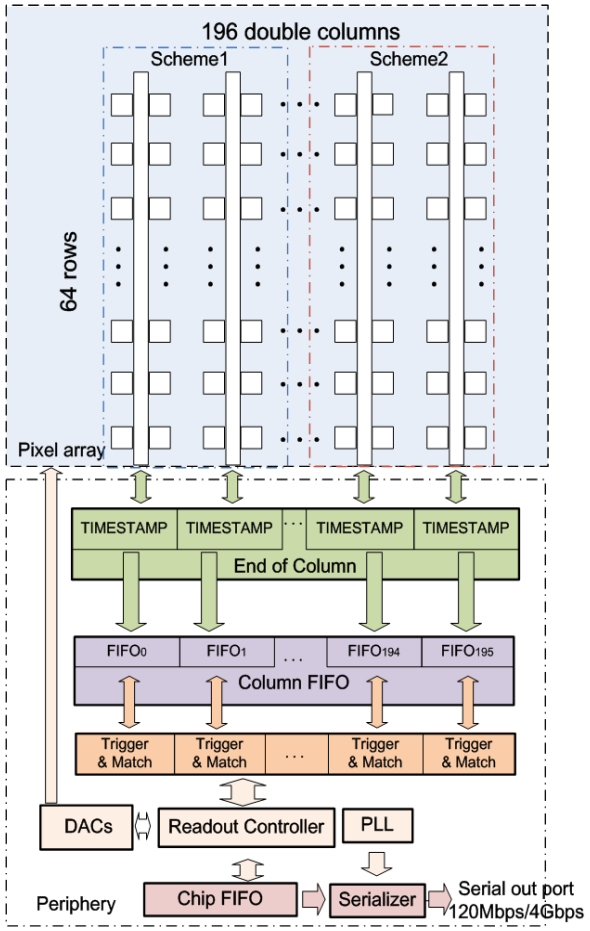
X-ray imaging with 5 min exposure @ 8kV X-ray tube



“single frame” X-ray imaging with 10s exposure @ 8kV X-ray tube

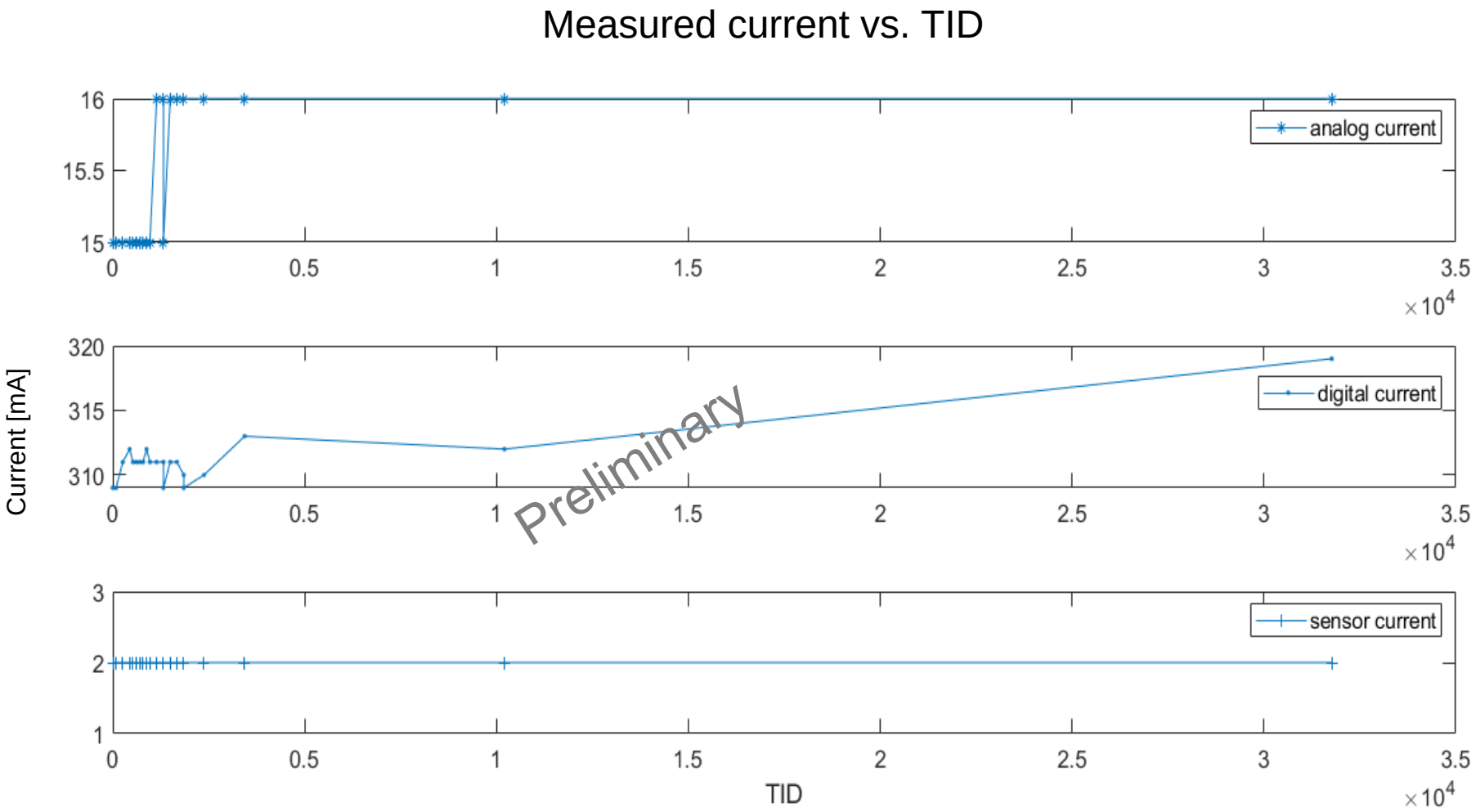
- **“DAQ” system established for the test system, with continuous data acquisition**
- **Triggerless readout @160 Mbps LVDS were applied at the current stage**
- **The full signal chain (pixel analog-digital-periphery-data interface) was proved by both X-ray and laser imaging**
  - Full array/sector was sensitive
  - “Single frame” imaging showing no crosstalk detected between clusters (good S/N ratio)
- **X-ray imaging with 5 min exposure showed clearly the different sectors of the pixel array (2 sectors were masked)**

TaichuPix architecture

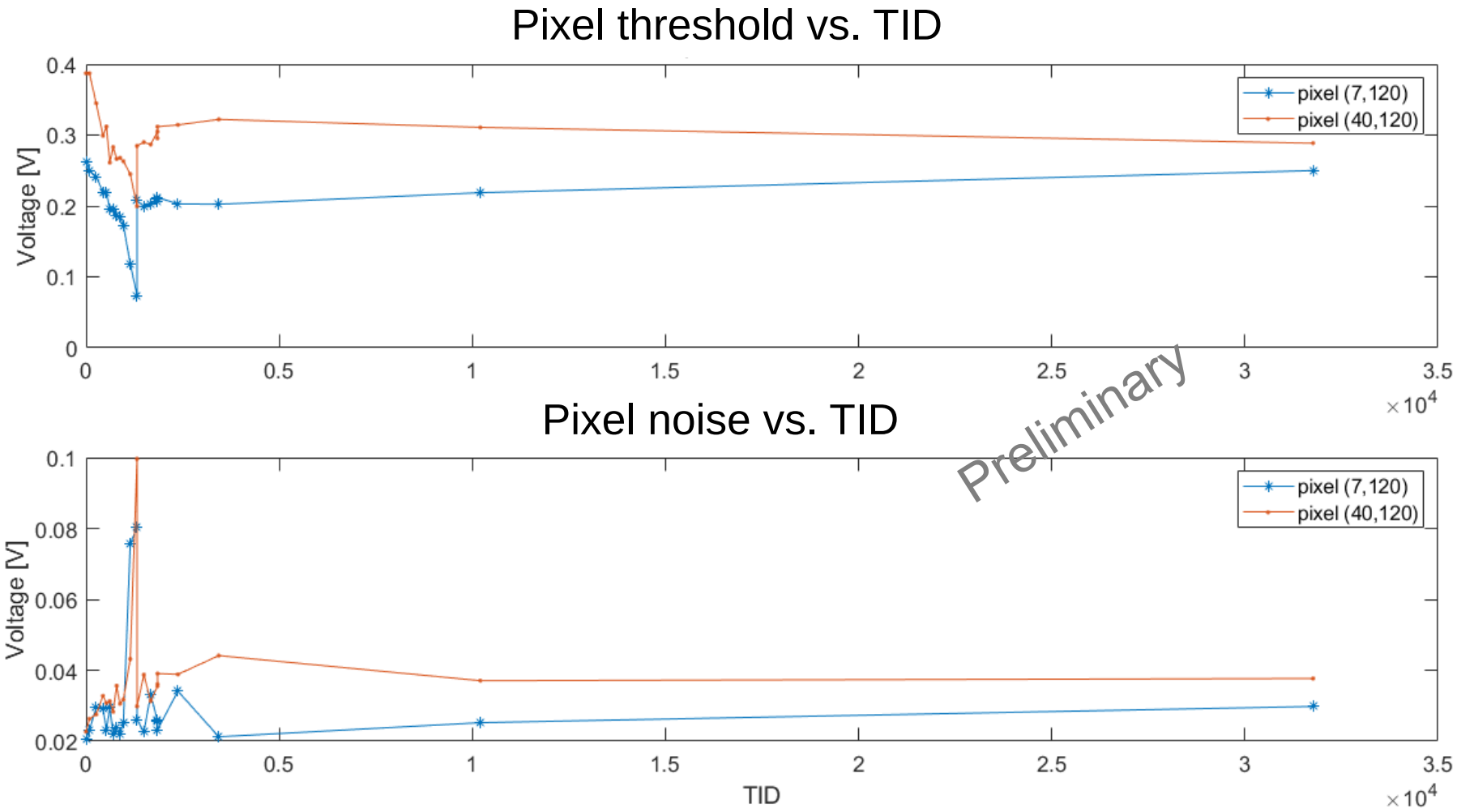


- **Similar to the ATLAS ITK readout architecture: "column-drain" readout**
  - Priority based data driven readout, zero-suppression intrinsically
  - Modification: time stamp is added at EOC whenever a new fast-or busy signal is received
  - Dead time: 2 clk for each pixel (50 ns @40MHz clk)
- **Two parallel pixel digital schemes**
  - ALPIDE-like: Readout speed was enhanced for 40MHz BX
  - FE-I3-like: Fully customized layout of digital cells and address decoder for smaller area
- **2-level FIFO architecture**
  - L1 FIFO: In column level, to de-randomize the injecting charge
  - L2 FIFO: Chip level, to match the in/out data rate between the core and interface
- **Trigger readout**
  - Make the data rate in a reasonable range
  - Data coincidence by time stamp, only matched event will be readout

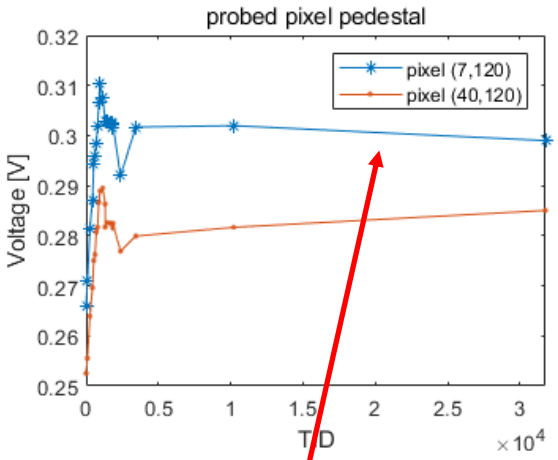
TID results till 30 Mrad

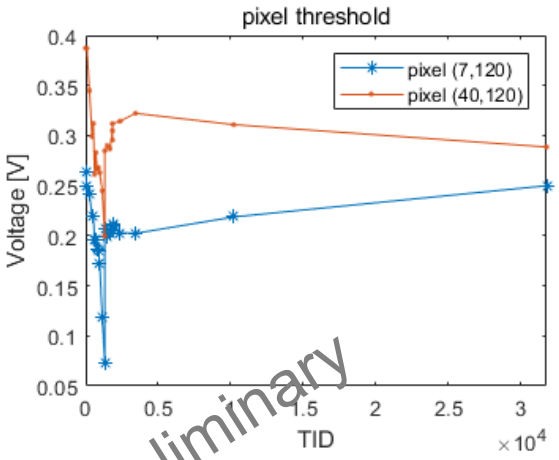


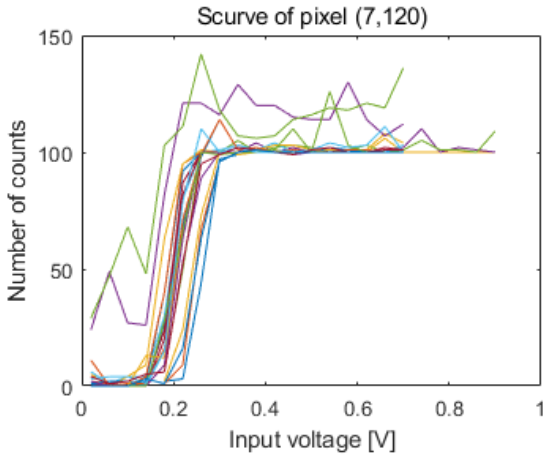
TID results till 30 Mrad

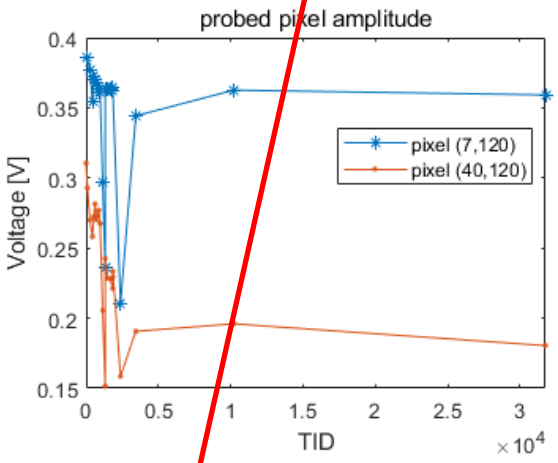


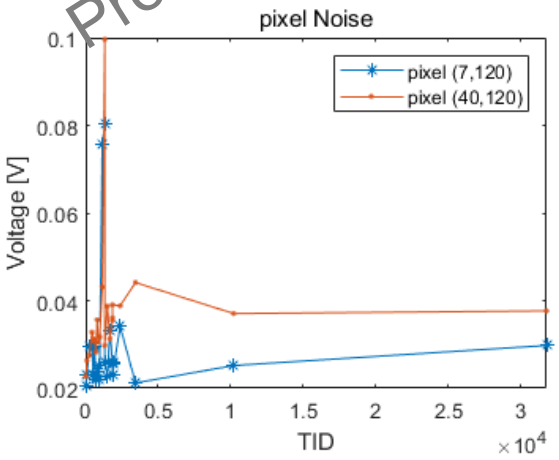
TID results till 30 Mrad

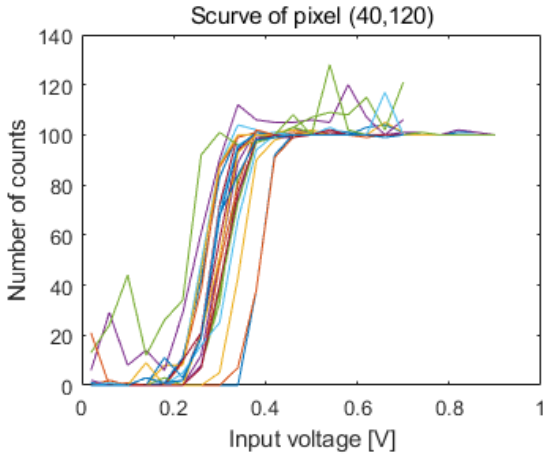










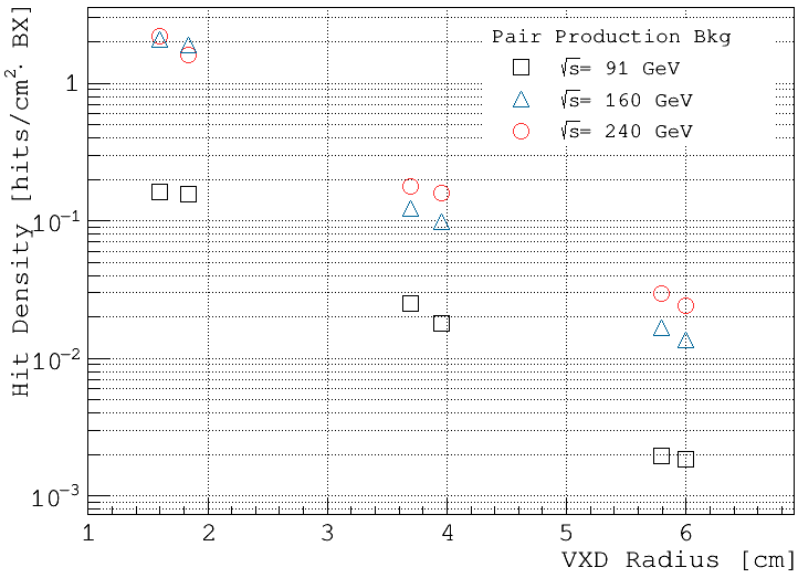


Dose rate was changed from 211 krad/min to 1.24 Mrad/min somewhere, However, no data before taking the action to reveal the effect, unfortunately

Main specs of the full size chip for high rate vertex detector

- **Bunch spacing**
  - Higgs: 680 ns; W: 210 ns; Z: 25 ns
  - Meaning 40M/s bunches (same as the ATLAS Vertex)
- **Hit density**
  - 2.5 hits/bunch/cm^2 for Higgs/W; 0.2 hits/bunch/cm^2 for Z
- **Cluster size: 3pixels/hit**
  - Epi-layer thickness：~18 μm
  - Pixel size：25 μm × 25 μm

From the CDR of CEPC



For Vertex	Specs	For High rate Vertex	Specs	For Ladder Prototype	Specs
Pixel pitch	<25 μm	Hit rate	120 MHz/chip	Pixel array	512 row × 1024 col
TID	>1 Mrad	Date rate	3.84 Gbps --triggerless ~110 Mbps --trigger	Power Density	< 200 mW/cm^2 (air cooling)
		Dead time	<500 ns --for 98% efficiency	Chip size	~1.4 cm×2.56 cm