CEPC Detector R&D Project

2.2 Silicon Tracker Prototype

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Change history

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| **Revision** | **When** | **What changed and why** |
| 1 | 28/12/2019 | First draft |
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Readme first

1. Please do not delete or modify this section or its structure.
2. Only change text enclosed by (and including) angled brackets “< … >”.
3. Don’t change field directly, instead modify the document options, under File🡪 Properties (or similar)
   * Enter name of person that wrote the document in Document:Summary: Author
   * The project ID number, should follow the rules provided to you earlier. The number should be changed in Document:Custom: PBS.
   * The project name should be changed in Document:Summary: Subject.
4. In Section [*Project Objectives*](#ProjectObjectives) provide a brief description of the project goals, i.e. why and what is being produced, for PBS item **1.1** **Vertex Prototype**. If this project includes identifiable sub-projects you can indicate them in the [*Sub-projects Description*](#SubprojectsDescription) Section, otherwise submit a separate document for each of them. The sub-project IDs are free for you to define.
5. Finally, remember to update the [*Change History*](#ChangeHistory).

2.2 Silicon Tracker Prototype: Project Objectives

The project objective is to define a Silicon Tracker that fits the detector requirements outlined by the CDR document, in particular the detector resolution, timing and material budget.

2.2 Silicon Tracker Prototype: Sub-projects Description

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| **Project ID** | **Title** | **Description** |
| 2.2.1 | CMOS pixel sensor and strip sensors | Full size CMOS pixel sensor with full functionality to be used in a silicon tracker detector |
| 2.2.2 | Readout electronics & DAQ | Data throughput and 680ns / 25ns readout of the detector |
| 2.2.3 | Low-mass staves | Low-mass support and cooling structure for sensors |
| 2.2.4 | Mechanical structure | Low-mass mechanical support structure |
| 2.2.5 | Module building | Pick and Place options for automatic building |
| 2.2.6 | Detector simulation | Investigate the overall detector design based on physics benchmark processes. |
| 2.2.7 | System test | Test of full system, including beam tests |
| 2.2.8 | System integration | Integration of all systems into a complete detector |

We envisage a number of prototypes to study electrical/DAQ, mechanical and thermal properties. Mechanical properties need to be studied for short staves, long staves and the support structure. For the overall design, one will also need to consider the interplay between vertex detector and tracker barrels and disks.

**2.2.1 CMOS pixel sensor**. Given the aggressive time scale there is little time for the development of new sensor technology. Thus a monolithic silicon CMOS sensor based on already existing technology is selected as baseline, with adaptations to CEPC and improvements being developed.

2.2.1.1 ATLASPix3/ARCADIA/FCEPCPix1. A working baseline sensor is ATLASPix3 with a pixel size of 50 x 150 μm and 25 ns readout. This sensor achieves the required spatial resolution and efficiency (> 99%) with a state-of-the-art power consumption. Another sensor fulfilling the requirements as well is for example MuPix.

Another candidate sensor is the ARCADIA chip which implements 25 x 25 μm pixels with peripheral readout, achieving an extremely low power consumption. This sensor concept and the associated foundry allow for stitching of sensors, high-resistive wafers and back-side processing.

Characterisation of considered sensors have included laser measurements, radioactive sources and beam tests. Further tests will include small-spot laser measurements, irradiation programmes and further beam tests in addition to further lab measurements. Lancaster, IHEP, Bristol, KIT, Como, Milano and Torino are interested in evaluating bulk sensor properties.

There will be an engineering run of an updated sensor design in April 2020 (FCEPCPix1), evolving ATLASPix3 in order to accommodate data aggregation (to reduce the number of data links required), optimise the pixel geometry to 25 x 200 – 300 μm improving pT resolution by halving the r-phi pitch, and test improved dE/dx capabilities. Similarly ARCADIA is being developed further, in particular an engineering run with full pixel matrix is planned.

KIT, Liverpool and Torino are chip design institutes working on sensor designs and the related chip testing.

2.2.1.2 FCEPC40Pix. It is desirable to be able to produce the monolithic CMOS tracker sensor in China. Therefore the possibility of a port of a relevant chip design to a Chinese fab (e.g. SMIC or HHGrace) will be explored. Processes with smaller feature sizes will also be investigated as they could offer both smaller pixels (better resolution) and lower power consumption. Based on development and testing cycles any significant new development and port to a new process could take up to 6 years. KIT, IHEP, NWPU and HITWH are interested in this development.

2.2.1.3 Pixel sensor development. Some sensor developments should be evaluated in addition to the baseline efforts, e.g. SUPix, which is a sensor developed at Shandong University that will be pursued as a first-principles generic CEPC sensor (rather than a sensor adapted to CEPC). NWPU is another institute that has experience with both, MAPS and Chinese foundries.

2.2.1.4 The silicon strip option is based on the possibility to use a reduced set of masks from a commercial CMOS process to implant strip diodes and top-level metal lines for readout on commercially available high-resistivity substrates used for RF application. The reticle size for commercial CMOS processes is limited to about 20x30 mm2 area, but large are detectors can be achieved by stitching the reticle. This production process may be competitive with the traditional processing of a wafer-size mask on detector-grade silicon substrate, for which it is difficult to find reliable manufacturers for large size production. Some strip detectors are being produced by LFoundry as a byproduct of a larger production of passive pixel detector by the ATLAS Collaboration. They use the 150 nm process and will be available in January 2020. Besides the possibility to achieve a large production size at reasonable costs, using a CMOS process may allow both the integration of further features, like a multiplication layer aiming at achieving good timing resolution, or integrating the readout electronics, providing monolithic strip sensors. Como and Milano in particular are interested in developing this option.

2.2.1.4 Sensor powering. Any chip technology needs to adopt either serial powering or DC-DC conversion as part of its powering scheme to reduce the material budget otherwise necessary to accommodate the massive low voltage supply currents.

**2.2.2** **Readout Electronics & DAQ.** For the purposes of the CMOS tracker, the readout electronics/DAQ comprises the data and power bus cable (often envisaged to be a flexible PCB (“flex”), an opto-conversion (and aggregation) stage at the end-of-stave/structure and a prototype DAQ system that will evolve into a counting room design.

2.2.2.1 Stave Flex. There is an existing “module flex” design effort for ATLASPix3, based on a 2×2 sensor matrix (quad module) produced by Milano and using industry standard copper-on-Kapton technology. This will be used for an electrical prototype testing the readout. USTC, RAL, Liverpool, Edinburgh and Milano are interested in the flex design.

2.2.2.2 GECCO/YARR/CaRIBou. The powerful and scalable RD53 YARR readout system is based on cost-efficient off-the-shelf PC components and will be used to test individual chips and quad modules, and can be scaled up to read out full stave prototypes. Thanks to its modular nature, its suitability for the final off-detector DAQ will be studied with the upgraded version. This is the baseline option and Lancaster and Edinburgh are interested in developing the YARR readout. In the short term the GECCO readout system used by KIT is available for sensor testing. The CaRIBou readout system has been developed for various sensor developments and has implemented ATLASPix3. It can also use FELIX as a backend. We will investigate all three readout options. Almost all participating institutes are interested in developing the readout and hosting a system on site.

2.2.2.3 FELIX. There is also experience in various groups in China and the UK, such as USTC and RAL, with the FELIX readout system, which is the envisaged ATLAS DAQ system for the whole detector based on high-end custom FPGA-PCIe-cards.

2.2.2.5 End-of-stave electronics. Depending on the chip that is being used, data will be aggregated at the end of the stave. In either case there will be an opto-conversion for a low mass single connection to the readout. (USTC & SJTU, RAL)

**2.2.3 Low Mass Staves.** Both ATLAS and ALICE use a carbon fibre truss structure for support of the flex and sensors, with ALICE having the lower material budget. The driving factor is cooling, where the requirements for ALICE are lower as they do not require 25ns readout. First FEA analyses of a stave with cooling pipes look promising.

2.2.3.1 Ti-Pipes with bi-phase CO2. There is considerable expertise within the UK groups (especially Lancaster, Liverpool, Sheffield and RAL) with Ti-pipes and bi-phase CO2 coolant developed for the ATLAS experiment. This will be pursued as the baseline option.

2.2.3.2 ALICE-style low pressure water-cooling will be investigated as an alternative, in particular with view of the material budget.

2.2.3.3 Micro-channel cooling can provide highly efficient cooling with low material budget. This option will be studied in parallel. Liverpool and Pisa are interested in developing this option.

2.2.3.4 End-of-stave cooling is another option that should be investigated.

2.2.3.5 Air-cooling is one of the options that should be investigated, depending on the overall size of the tracker, the expected power consumption of the sensor and the compactness of the detector layout.

2.2.3.6 The ALICE, ATLAS and CMS truss structures will be evaluated in detail for an updated design to minimise the material requirement. Liverpool, Pisa, Daresbury and Lancaster are interested in the design and prototyping of this structure.

**2.2.4 Mechanical Structure.** We envisage a carbon fibre based support structure for the overall system. In particular Liverpool and Pisa are interested in this investigation.

**2.2.5 Module Building.** Depending on the detector option a Full Silicon Tracker can have an active area of over 100m2. We will be looking into industrial scale building options for detector staves. There is experience in the UK, Italy and China with the ALICIA pick and place robot. Options to extend this to CEPC will be investigated.

**2.2.6 Detector Simulation.** The design of the tracker is driven by physics requirements. In particular the impact of the material budget on benchmark physics processes will be investigated (Edinburgh, Warwick, Lancaster). The usage of dE/dx for particle ID and heavy flavour object tagging will also be studied. The number of layers will be a limiting factor. Whilst it is possible to provide dE/dx with the existing sensor and electronics, a cost/benefit analysis will be performed.

**2.2.7 System Test.** Evaluating a full stave(let) with cooling, a number of sensors, a stave flex/power bus and full speed readout of all modules will be performed on its own, with cosmics and possibly with a beam. Interested institutes are Bristol, Daresbury, RAL, IHEP, Lancaster, Edinburgh and USTC.

**2.2.8 Integration.** Detector integration of staves, support structure, DAQ and services.

2.2 Silicon Tracker Prototype: CEPC Relationship

This project makes heavily use of the ATLAS and ALICE experience in China, Italy and the UK. There is also overlap with the LHCb upgrade R&D in China and the UK. The R&D is useful for any collider with up to 25ns BX timing, but given the proposed timescale the R&D is aimed primarily at the CEPC.

2.2 Silicon Tracker Prototype: Project Schedule

The project schedule depends on the available funding.

November 2020: Evaluate sensor options. Start physics simulations.

November 2020: First prototype stavelet based on ATLASPix3 with quad modules mounted on carbon fibre with established readout.

May 2021: Electrical and mechanical prototypes. One long stave. First simulation results.

December 2021: Physics simulation informs the first overall detector design, prototype with 4 layers, prototype ladder finished.

2.2 Silicon Tracker Prototype: Funding Availability

There is no dedicated CEPC funding available at this time. All activities are funded by group budgets. R&D activities are derived from ATLAS, ALICE or LHCb developments where all sides profit from a parallel development.

Dedicated funding is needed and will be sought, while project approval would be helpful in doing so.

2.2 Silicon Tracker Prototype: Leadership Arrangement

WANG Meng, Shandong University

Harald FOX, Lancaster University

Groups involved:

Hongbo Zhu & Jianchun Wang, IHEP; Xin Chen, Tsinghua; Changqing Feng, USTC; Yann Hu, NWPU; Weihao Wu, SJTU/TD Lee; Chenxu Wang, Harbin Institute of Technology; Yanyan Gao, Edinburgh; Tim Jones, Liverpool; Jaap Velthuis, Bristol; Jens Dopke, RAL; Roy Lemmon, Daresbury; Trevor Vickey, Sheffield; Bill Murray, Warwick; Ivan Peric, KIT (Karlsruhe, Germany); Massimo Caccia, Como; Attilio Andreazza, Milano; Franco Bedeschi, Pisa; Manuel Da Rocha Solo, Torino.

2.2 Silicon Tracker Prototype: Manpower Resources

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| **Type** | **Average FTE Expected** |
| Faculty |  |
| Postdoc |  |
| Students |  |
| Engineers |  |