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# Test results of TaichuPix chips

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On behalf of the CEPC MOST2 Vertex detector design team

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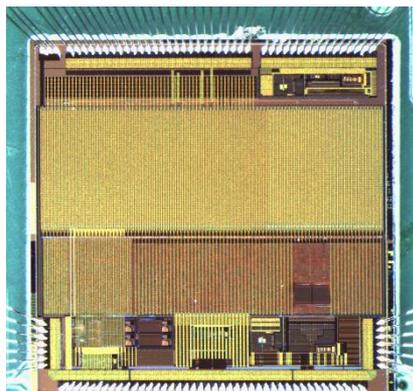
# TaichuPix chips overview



**TaichuPix-1**

**Chip size: 5 mm × 5 mm**

**Pixel size: 25 μm × 25 μm**



**TaichuPix-2**

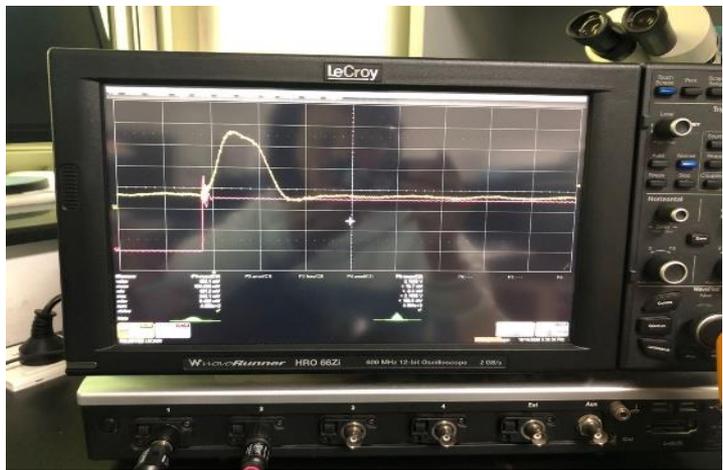
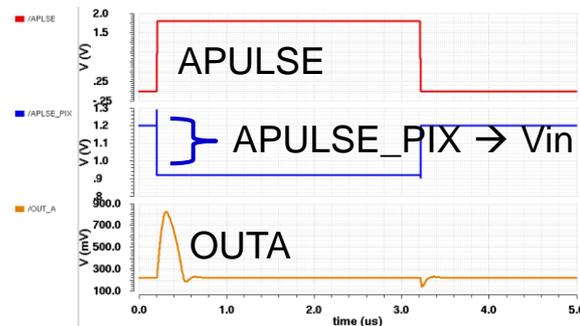
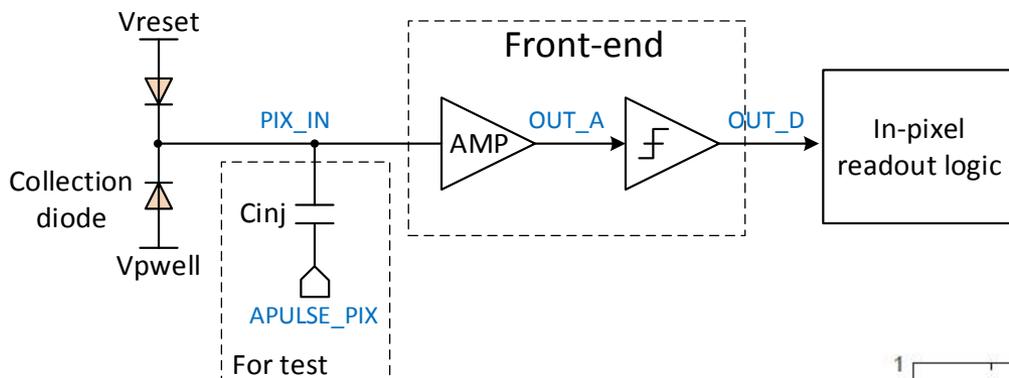
**Chip size: 5 mm × 5 mm**

**Pixel size: 25 μm × 25/24 μm**

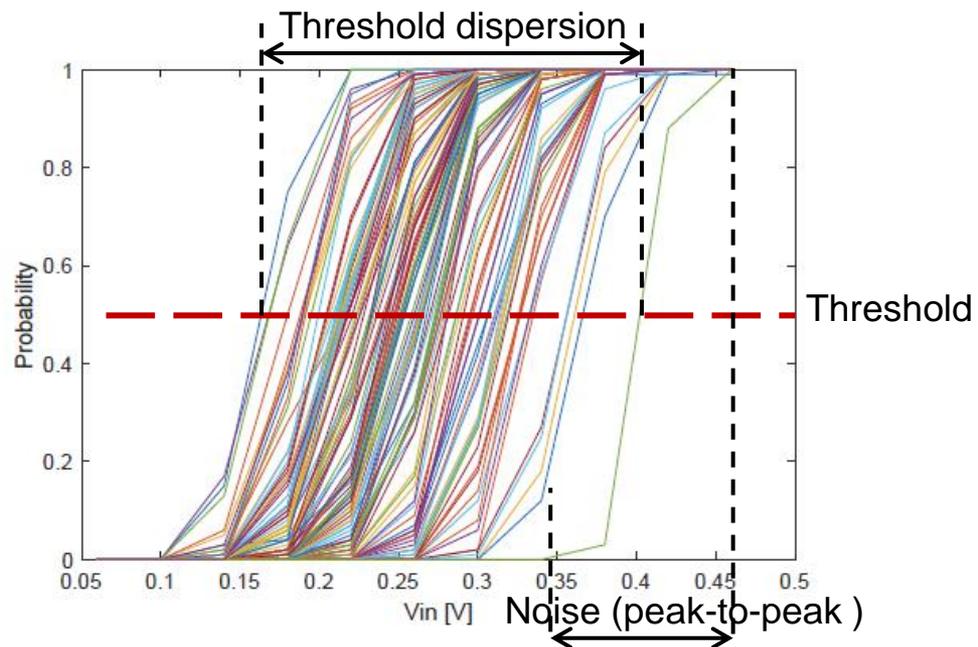
- **Two MPW chips were fabricated and verified**
  - TaichuPix-1: 2019.06~2019.11
  - TaichuPix-2: 2020.02~2020.06
- **Chip size 5 mm×5 mm with standalone features**
  - Pixel size of 25 μm×25 μm (one sector with 25 μm×24 μm pixels in TaichuPix-2)
  - A full functional pixel array (small scale)
    - A 64×192 Pixel array (including 6 pixel variations)
  - Periphery logics
    - Fully integrated logics for the data-driven readout
    - Fully digital control of the chip configuration
  - Auxiliary blocks for standalone operation
    - High speed data interface up to 4Gbps
    - On-chip bias generation
    - Power management with LDOs
    - IO placement in the final ladder manner
      - Multiple chip interconnection features included

# Electrical test

- Electrical performance verified by injecting an external voltage step (charge) into pixel front-end



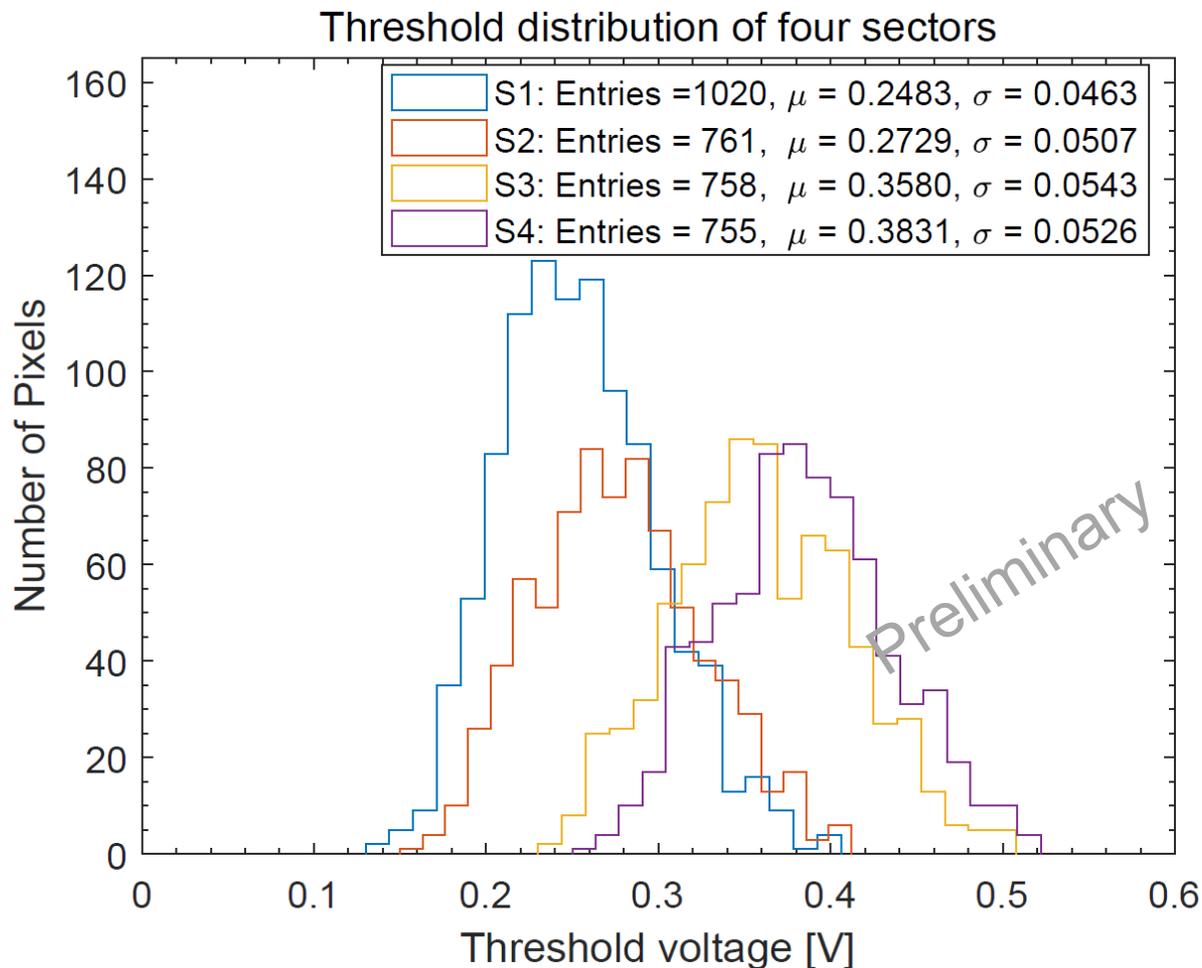
Analog output of a pixel @  $V_{in} = 0.9$  V



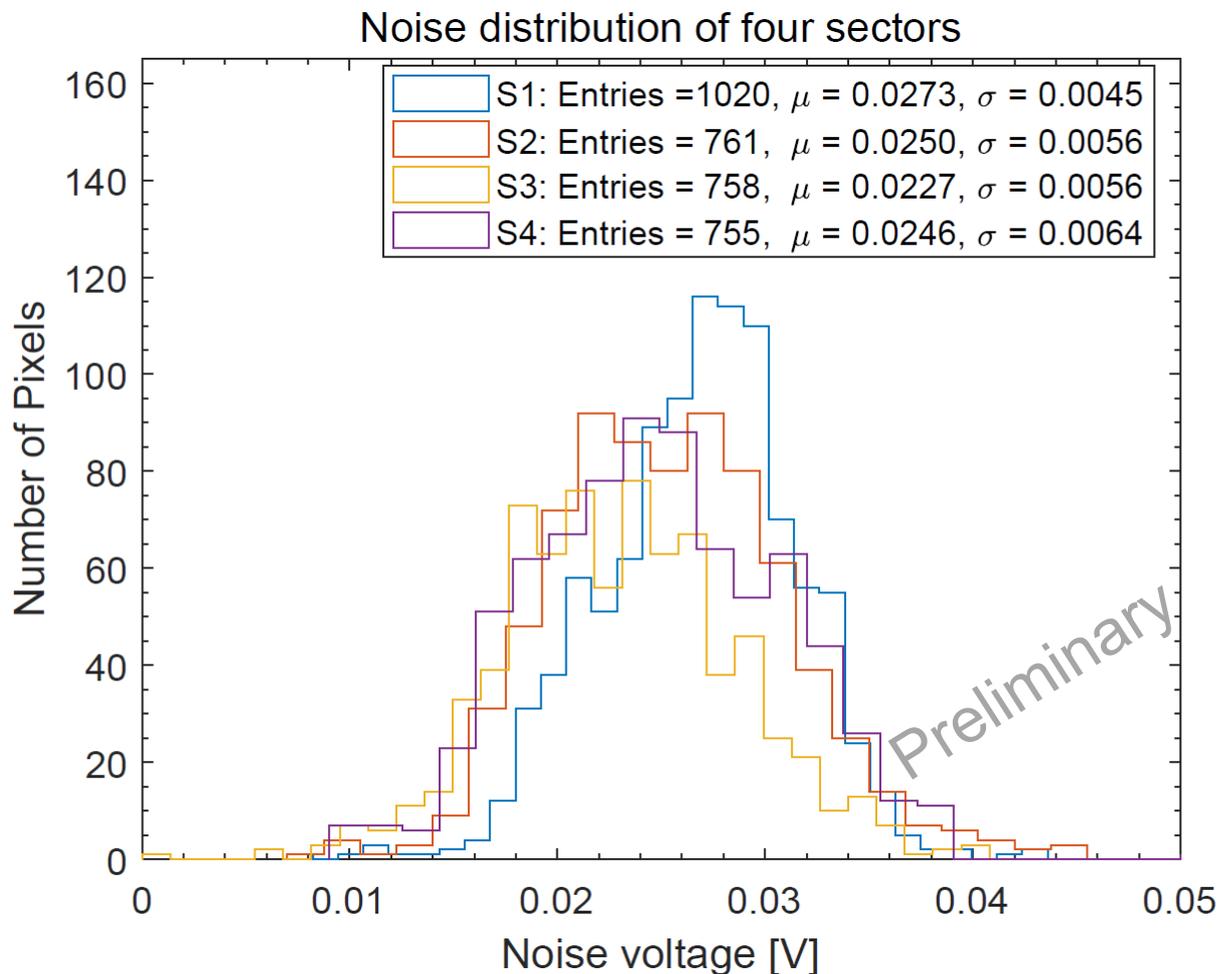
Measured "S-curve" for 128 pixels

# Threshold distribution measured on S1-S4

- Based on the same bias condition for pixel analog, S-curves measured for S1-S4 (with different pixel analog designs)



# Noise distribution measured on S1-S4



The measured threshold and noise difference between different sectors agree with design qualitatively.

# Comparison of ENC and Charge Threshold

- **Converting the noise/threshold voltage to electrons by 0.88 mV/e<sup>-</sup>**
  - Assuming the charge injection capacitance in each pixel is 0.18 fF, which is extracted from layout

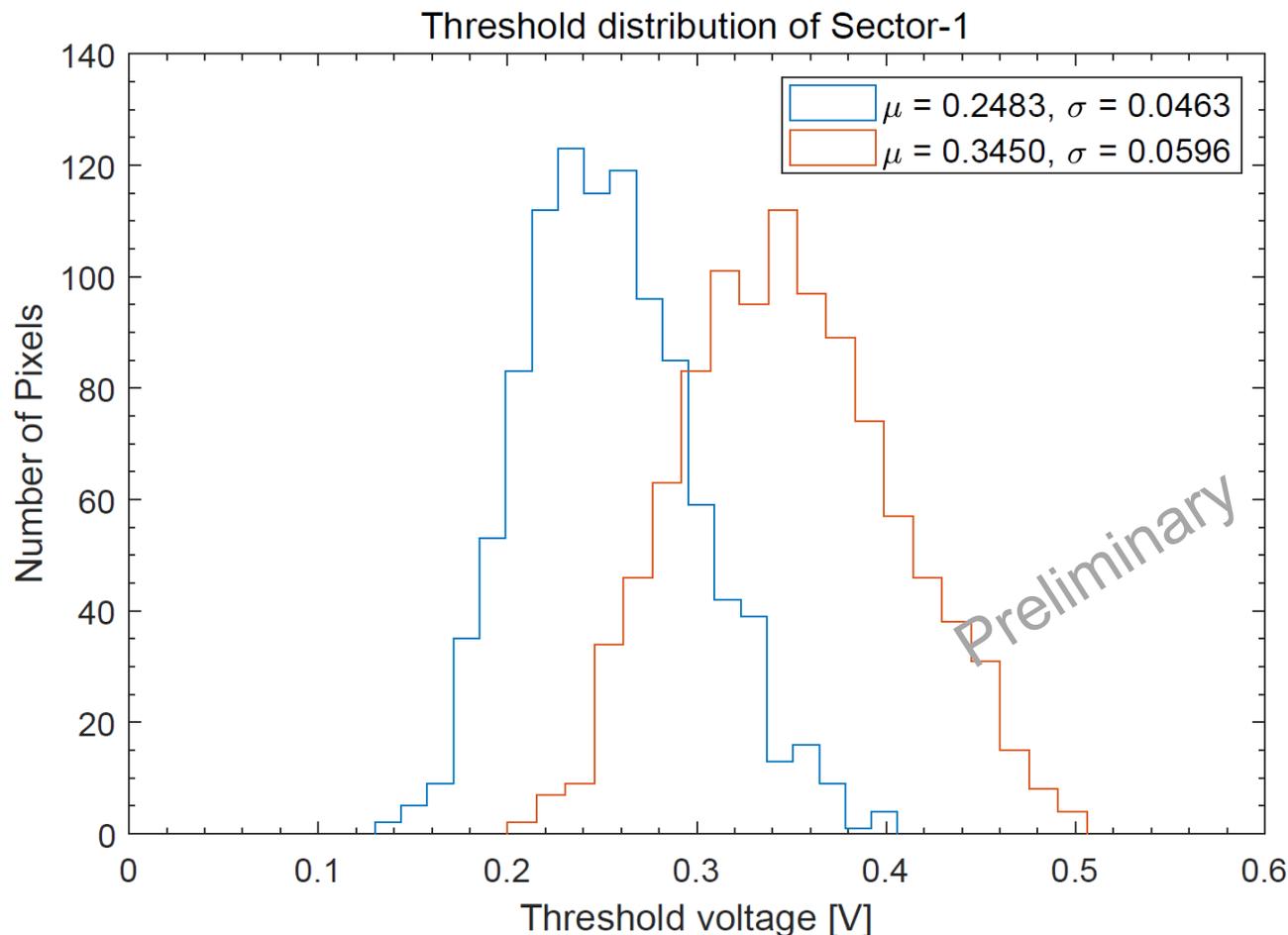
	<b>Threshold Mean</b>	<b>Threshold RMS</b>	<b>ENC</b>	<b>ENC Std. dev</b>
S1	282.1 e <sup>-</sup>	52.7 e <sup>-</sup>	31.0 e <sup>-</sup>	5.1 e <sup>-</sup>
S2	310.1 e <sup>-</sup>	57.6 e <sup>-</sup>	28.4 e <sup>-</sup>	6.4 e <sup>-</sup>
S3	406.8 e <sup>-</sup>	61.7 e <sup>-</sup>	25.8 e <sup>-</sup>	6.3 e <sup>-</sup>
S4	435.3 e <sup>-</sup>	59.8 e <sup>-</sup>	28.0 e <sup>-</sup>	7.3 e <sup>-</sup>

**ENC and charge threshold in this table only for comparison of different sectors, but the absolute value can not used for the sensor assessment**

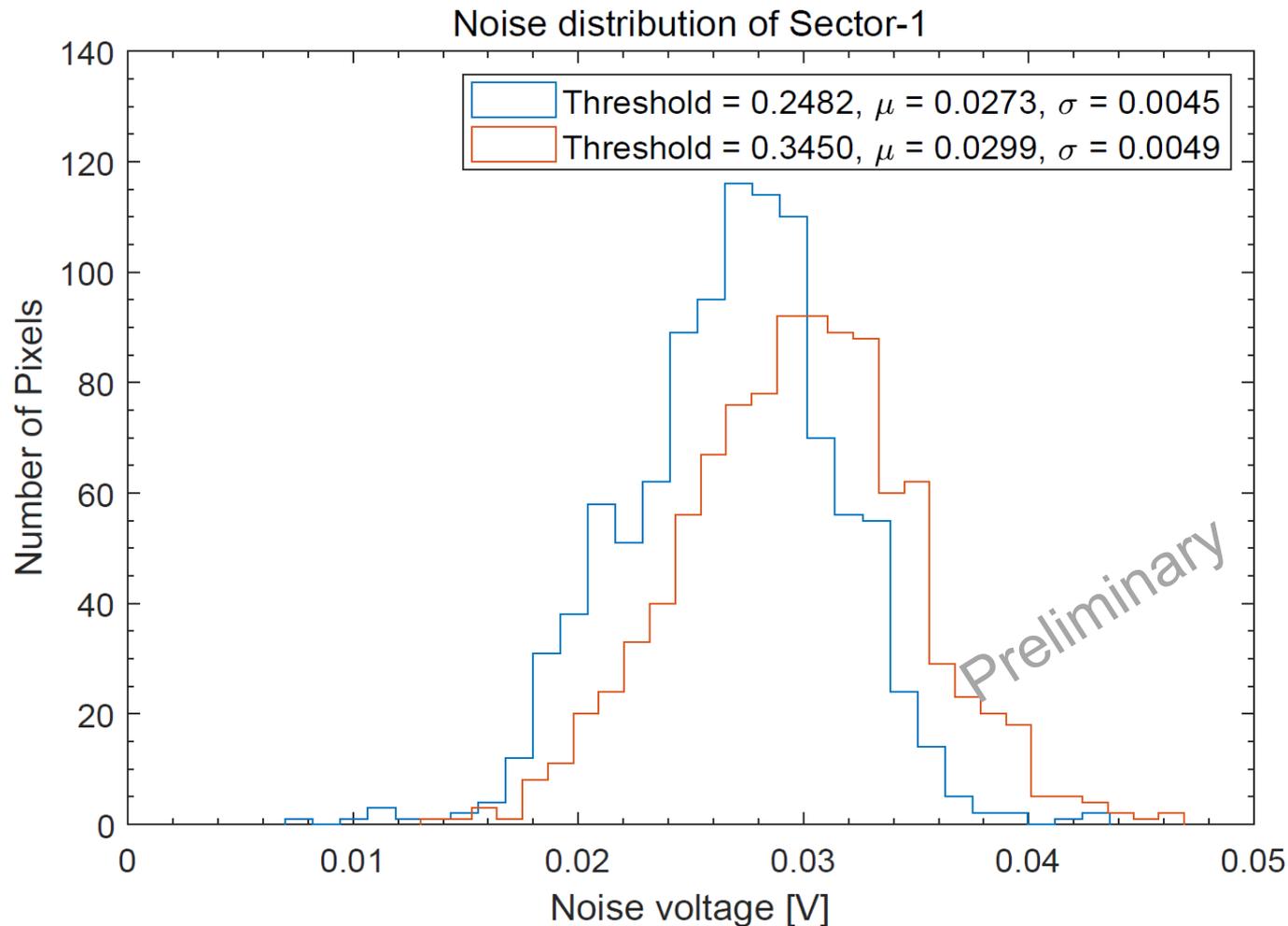
- **Factor of charge to voltage (0.88 mV/e<sup>-</sup> in simulation) need to be calibrated**

# Threshold distribution measured on S1

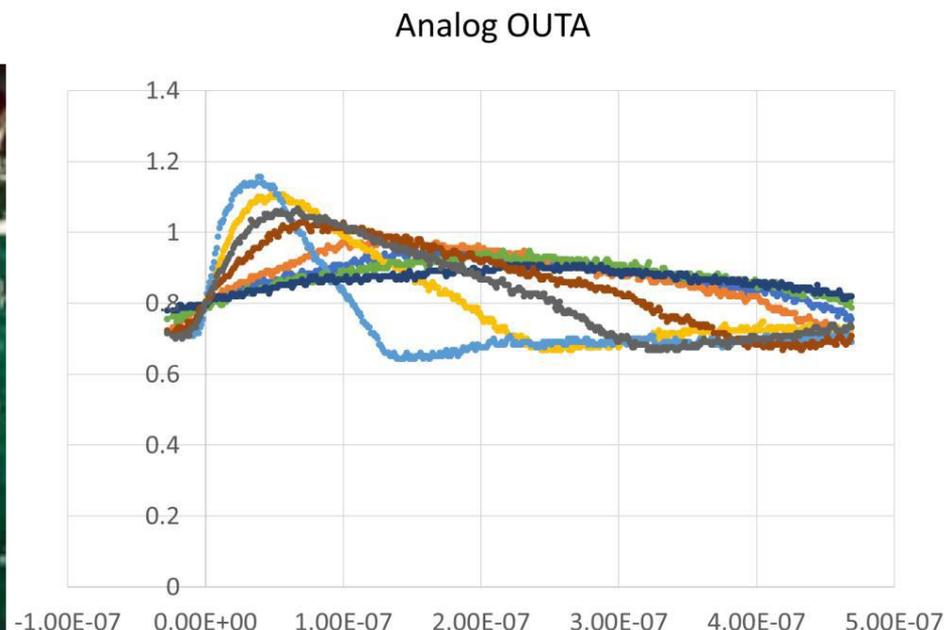
- S-curves measured on different bias conditions of front-end for S1
- The effect of bias condition on threshold coincides with design



# Noise distribution measured on S1

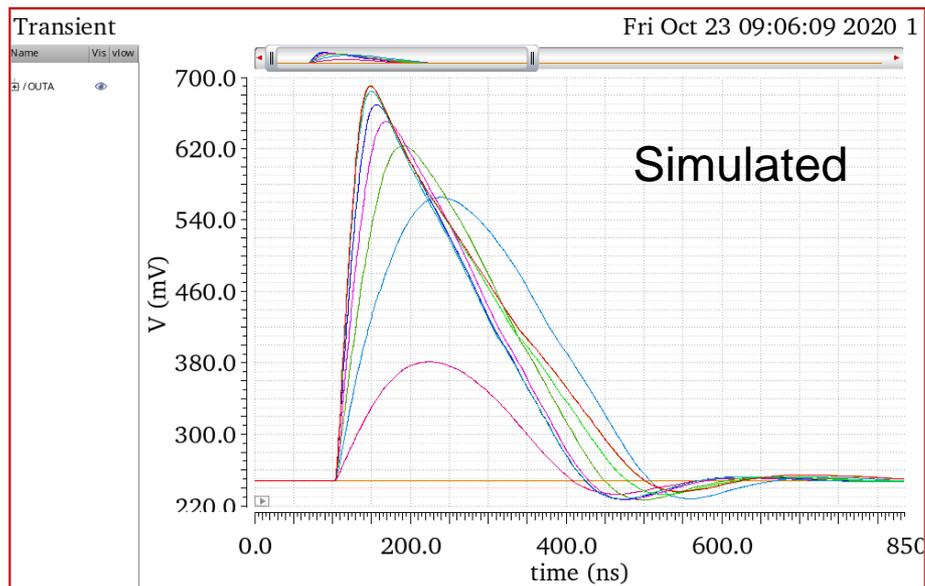
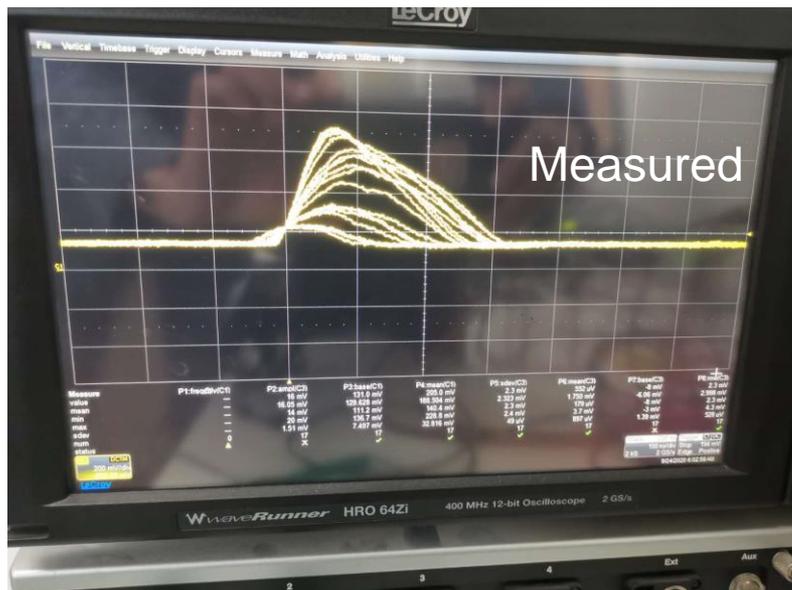


# TaichuPix-1 response to $^{90}\text{Sr}$

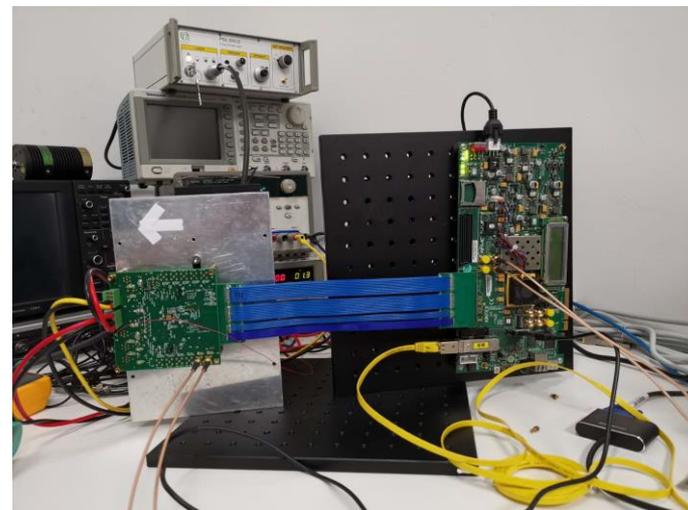


- Analog signals of a pixel were captured with oscilloscope.
- Larger signal having smaller peak time and pulse duration, agrees with simulation
- TaichuPix-2 will be tested with  $^{90}\text{Sr}$  soon

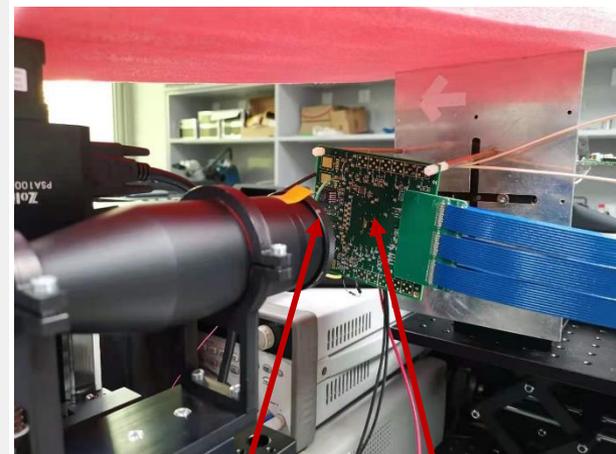
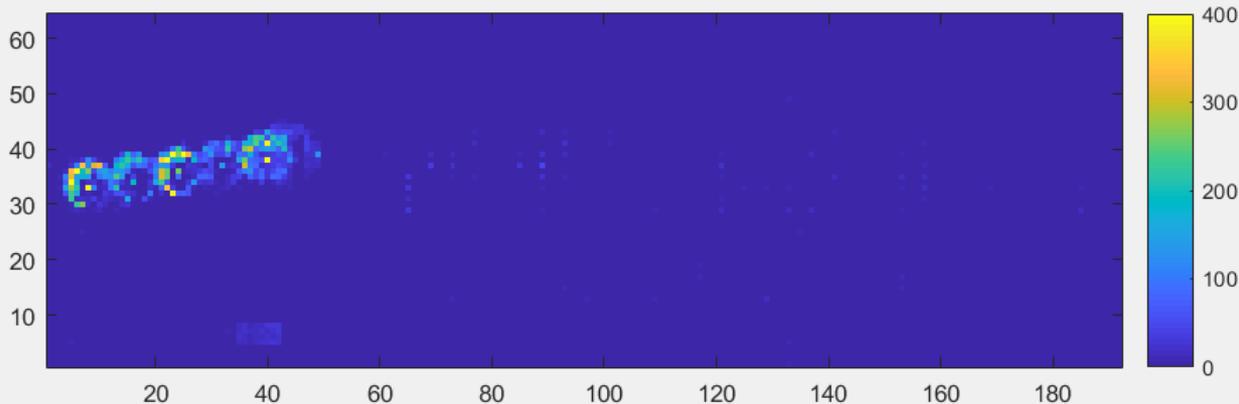
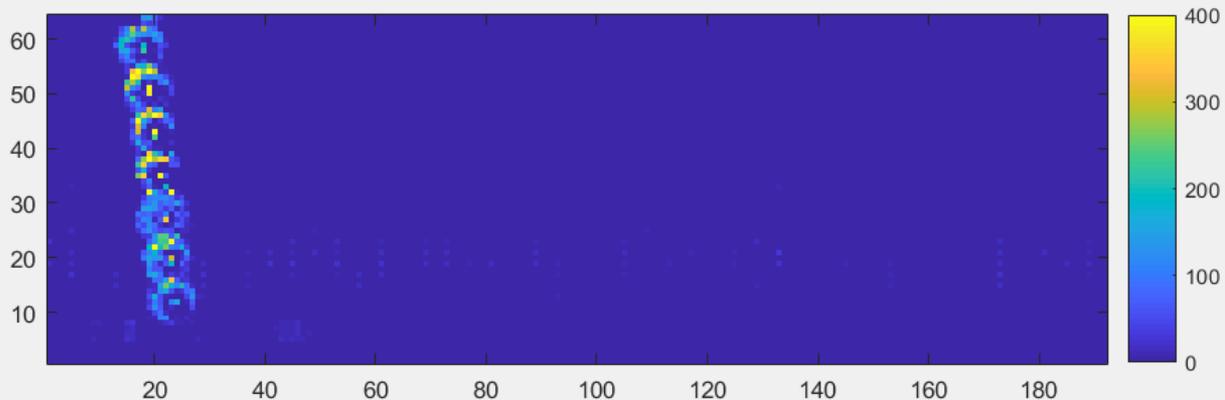
# Preliminary verification with radioactive



- Analog output waveform agreed with the simulation when tested by X-rays
- Signal amplitude, signal width, edge speed...all are almost agreed
- Note: for the small signal, the S/N ratio was also good, inferred that the noise performance was also normal (good)



# Pixel dimension test (Preliminary)

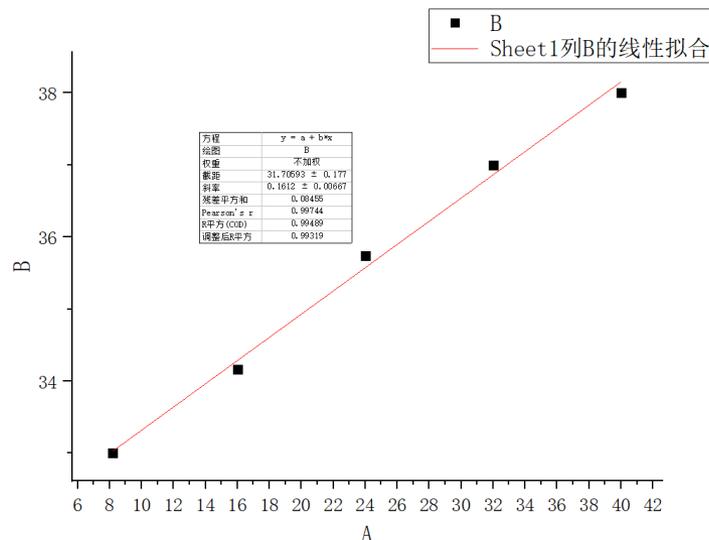
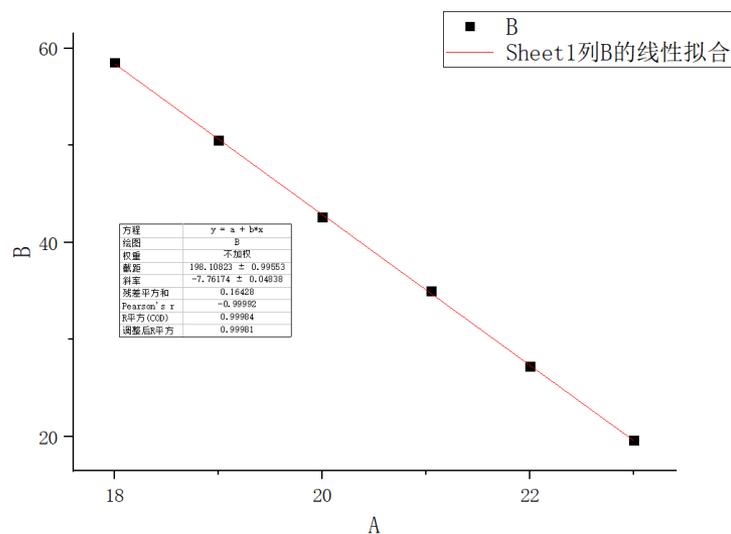


Laser  
(1064 nm)

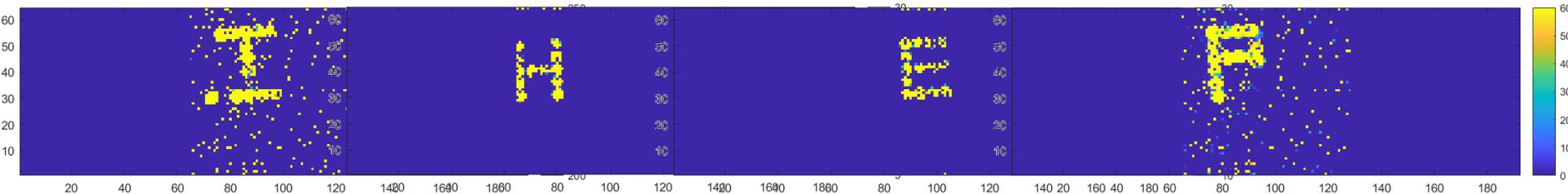
TaichuPix-2

- Laser was moved every 200  $\mu\text{m}$  in X/Y direction , the center of the light spot was used for position
- Linear fit was done with interpolation if the center was found at 2 pixels

# Pixel dimension test (Preliminary)



- $-7.762 \pm 0.05$  &  $1/(0.162 \pm 0.007)$  were found as the fitted pixels per 200um, while estimated pixels were 8
- The reason was the test board surface was not fixed vertically to the platform, due to the heavy extension cable of the KC705



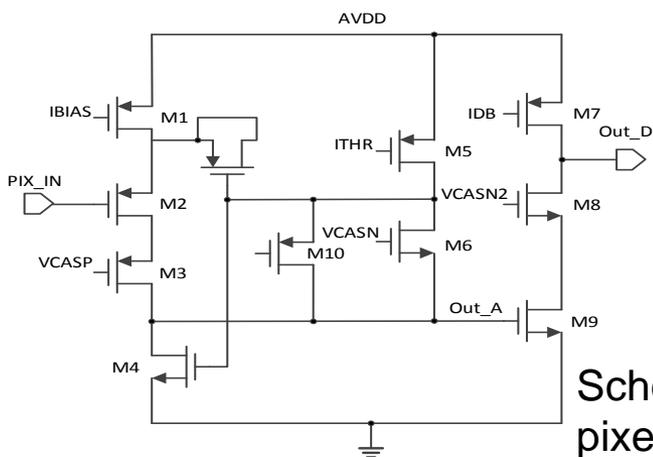
Some letter scanning experiments

## Summary and plan

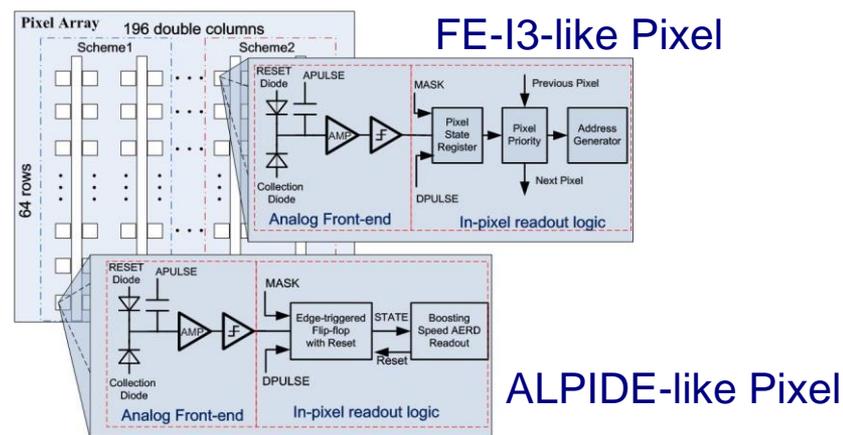
- **Major functionality proved stable by the full readout system**
  - Minor bugs will be fixed in the next version
- **Test with  $^{90}\text{Sr}$  source, TID test, laser test will be done**
- **Preparation for the next version chip**
  - A engineering run is proposed

# Backup

Sector	Pixel front-end	Pixel digital	Pixel size
Sector 1	Same as S1 of TC1, reference design	FEI3-like	25 $\mu\text{m}$ $\times$ 25 $\mu\text{m}$
Sector 2	M6 with guard-ring, PMOS in independent well	FEI3-like	25 $\mu\text{m}$ $\times$ 25 $\mu\text{m}$
Sector 3	M6 in enclosed layout, PMOS in independent well	FEI3-like	25 $\mu\text{m}$ $\times$ 24 $\mu\text{m}$
Sector 4	Increasing M3, M4, M9. M6 in enclosed layout, PMOS in independent well	FEI3-like	25 $\mu\text{m}$ $\times$ 25 $\mu\text{m}$
Sector 5	Same FE as S1, with smaller sensor	ALPIDE-like	25 $\mu\text{m}$ $\times$ 25 $\mu\text{m}$
Sector 6	Same FE as S1	ALPIDE-like	25 $\mu\text{m}$ $\times$ 25 $\mu\text{m}$



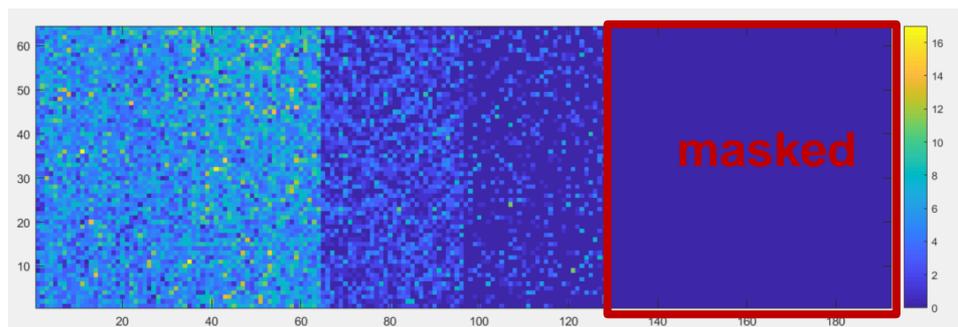
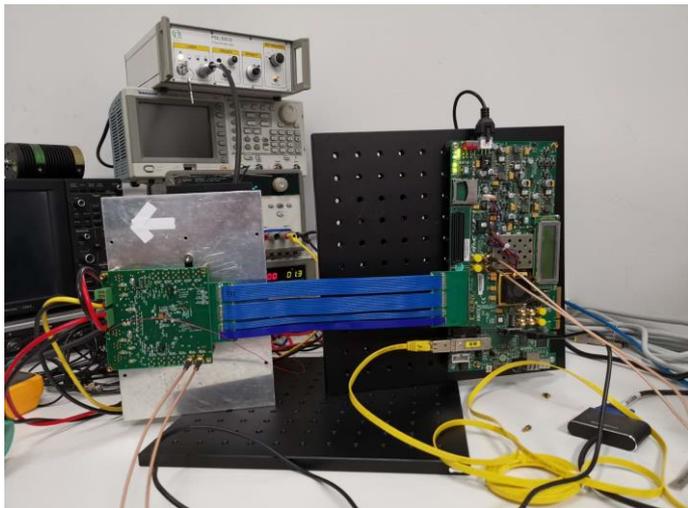
Schematic of in-pixel front-end



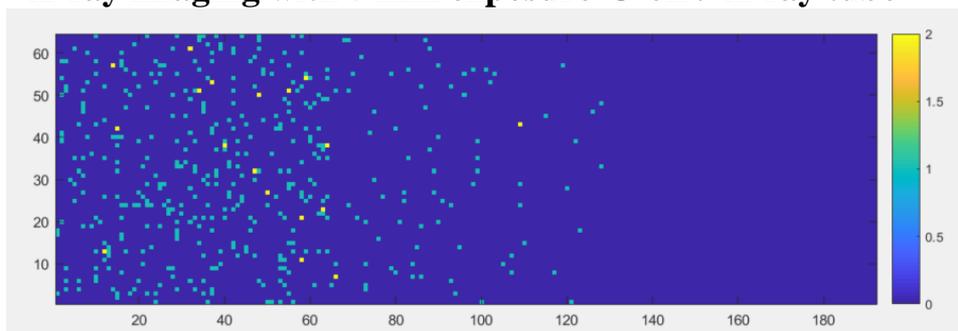
FE-I3-like Pixel

ALPIDE-like Pixel

# X-ray imaging



X-ray imaging with 5 min exposure @ 8kV X-ray tube



“single frame” X-ray imaging with 10s exposure @ 8kV X-ray tube

- “DAQ” system established for the test system, with continuous data acquisition
- Triggerless readout @160Mbps LVDS were applied at the current stage
- The full signal chain (pixel analog-digital-periphery-data interface) was proved by both X-ray and laser imaging
  - Full array/sector was sensitive
  - “Single frame” imaging showing no crosstalk detected between clusters (good S/N ratio)
- X-ray imaging with 5 min exposure showed clearly the different sectors of the pixel array (2 sectors were masked)