R&Ds for Detector Front-end Data Transmission, Present and the Future

Jingbo Ye

Dept. of Physics, SMU

Dallas, Texas, 75275

Content

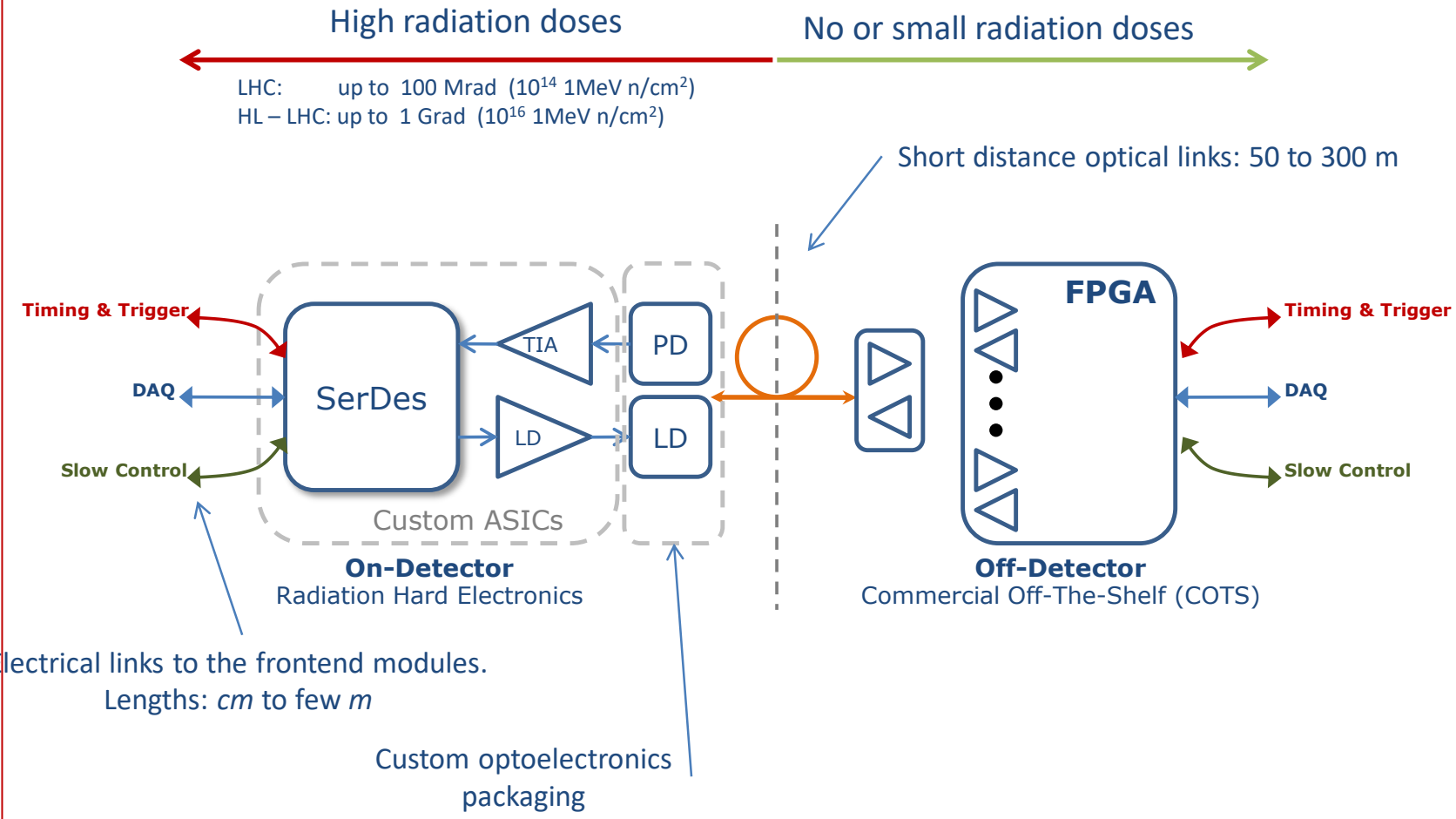
- A very brief overview of ASICs and optical modules we have developed and been using since 2000.
- Going forward what's on the horizon (my understand of it).
- Some R&Ds at SMU (in collaboration with many others, especially IPAS):
  - GBS20 to push to 20 Gbps per fiber.
  - cpVLAD to cope with extreme use conditions, example: inner tracker.
  - QTIA to explore ideas that may mitigate the p-i-n diode degradation in radiation.
- Summary.

Today's typical HEP Link Architecture

Challenges:

- Radiation, in both pp and ee machines
- Reliability, especially the link to the detector, and the radiation induced degradation in photo diode.
- High channel/data density and throughput from detector
- Low power, low mass and small formfactor (of the module)

Not included here is the electric link over low mass FLEX PCBs and cables for data from near the IP. This is a direction in future R&D due to the use of ultra low mass transmission media.



Slide from Paulo Moreira, CERN EP workshop on R&D, 2019/10/24

Looking back two decades, and till now*

	Generation/Speeds		(AS)ICs	OMs (Optical Modules)
Current LHC detectors	1**,	1.6 Gbps	G-Link (the only COTS, bipolar, high power) GOL (0.25 um CMOS, CERN ASIC)	OTx, ORx (COTS based custom modules) SC or ST type of COTS transceiver
For Phase-I upgrades	2,	4.8 Gbps	GBTx, GBLD, GBTIA, LOCx2-130 (130 nm CMOS)	VTRx (CERN common project)
		5.12 Gbps	LOCx2, LOCld (0.25 um SOS)	MTx, MTRx (specially for LAr, 6 mm height)
Some for Phase-II upgrades	3,	5.12 /10.24 Gbps 7*1.28 Gbps	lpGBT, LDQ DLAS10, cpVLAD (65 nm CMOS) GBCR, a cable receiver for electrical transmission over meters	VTRx+ (4 Tx + 1 Rx array), MTx+, MRx+, MTRx+

*, the list is not complete. For example, it does not include link through electric cable.
**, there are custom modules in tens of Mbps developed for inner trackers.

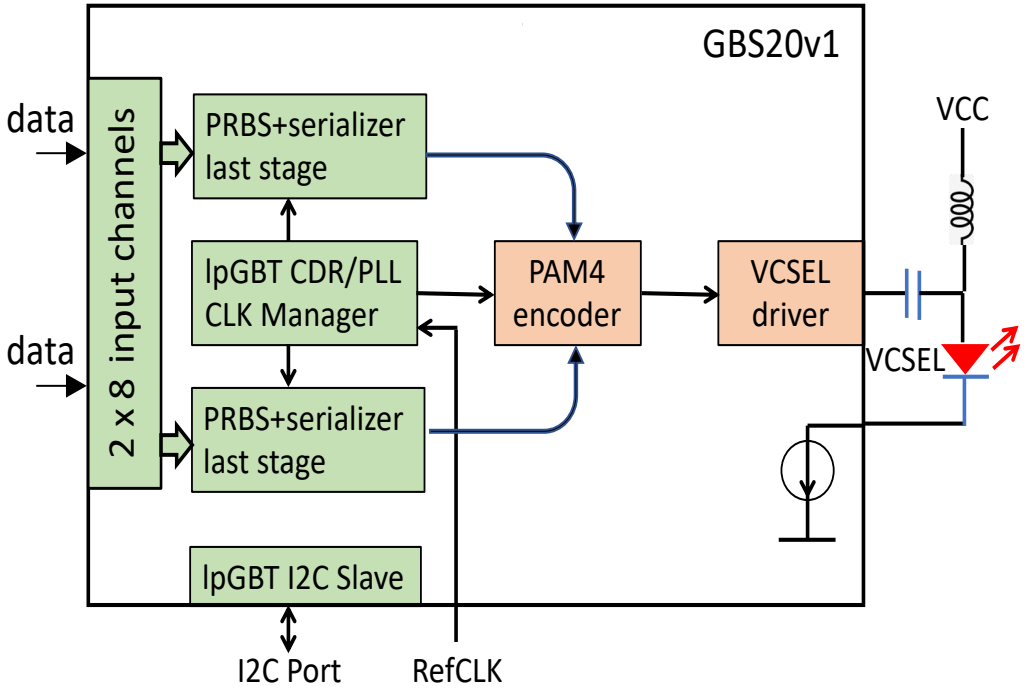
System level studies were carried out by the Versatile Link common project. It is important to point out that current tera-bit-per-second systems need system level specs to ensure reliability.

Looking forward

- Not trying to do any advertisement for CERN, but I would like to point out the following developments that I know:
  - CERN EP R&D program and the WG6 on Fast Links: ASICs on high data rates, optoelectronics drivers and low-mass electrical cable transmission; FPGA-based system testing and emulation; Silicon photonics (chip, packaging and system, and next-generation VCSEL-based optical modules). On ASIC, one goal is 28 nm CMOS based 28 Gbps NRZ and 56 Gbps PAM4 transmitters.
  - Task Force 7 reports (March 25, 2021) in the the ECFA Detector R&D Roadmap Symposia cover ASICs and Links for detector front-end electronics, including data links.
- Some R&Ds on links at SMU.

GBS20

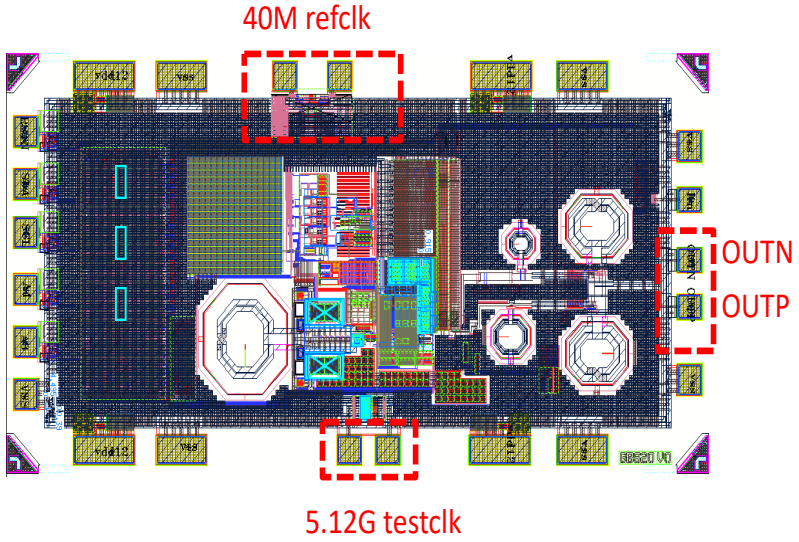
- GBS20 is an ASIC that uses many design blocks from lpGBT (65 nm CMOS), plus a PAM4 encoder + driver, for a data rate at 20.48 Gbps per fiber.
- The diagram is just a prototype of the ASIC.
- The highspeed clock drives the two serializers and the PAM4 encoder, greatly simplifies the link transmitting circuit implementation.
- Staying at 65 nm CMOS and 10 G based offers a practical solution to 20.48 Gbps per fiber applications, already a big step up from 10.24 Gbps.

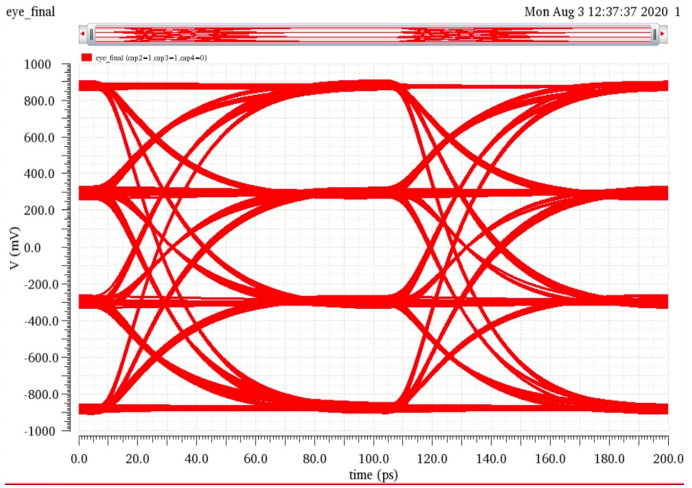


- It will also provide experience in PAM4 + VCSEL for future designs in 28 nm PAM4 which will be a lot more expensive than 65 nm.
- Going to 28 Gbps NRZ or 56 Gbps PAM4 will need more studies on fibers (OM4 and OM5). Fiber must be rad-tol as well.

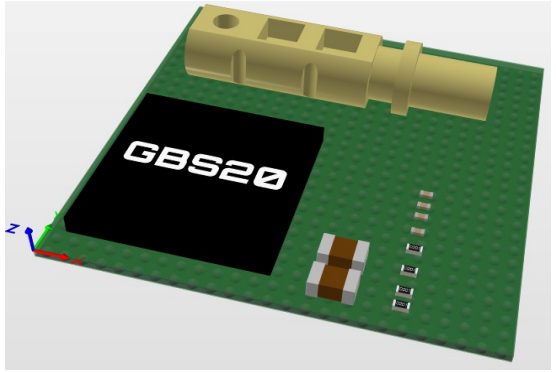
GBS20

- Test results of the first version were reported at RT2020, Tests of the second prototype chips will start next week. Tests provide experience in PAM4 + VCSEL.



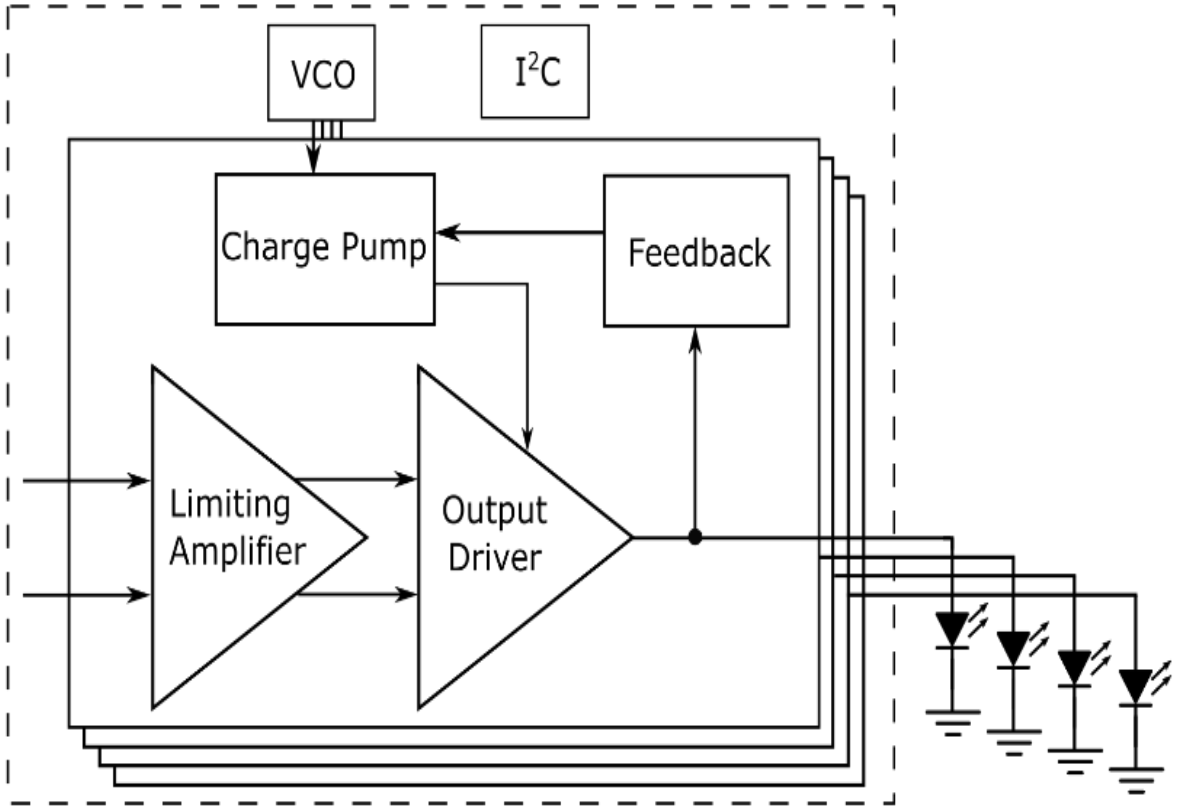


- The final goal is to implement the full lpGBT transmitter (and the link protocol), and to develop the optical transmitter as a mezzanine, to fit into the lpGBT ecosystem, and to spare system developers the trouble of dealing with fast (10G) PCB layout and expensive PCB materials.



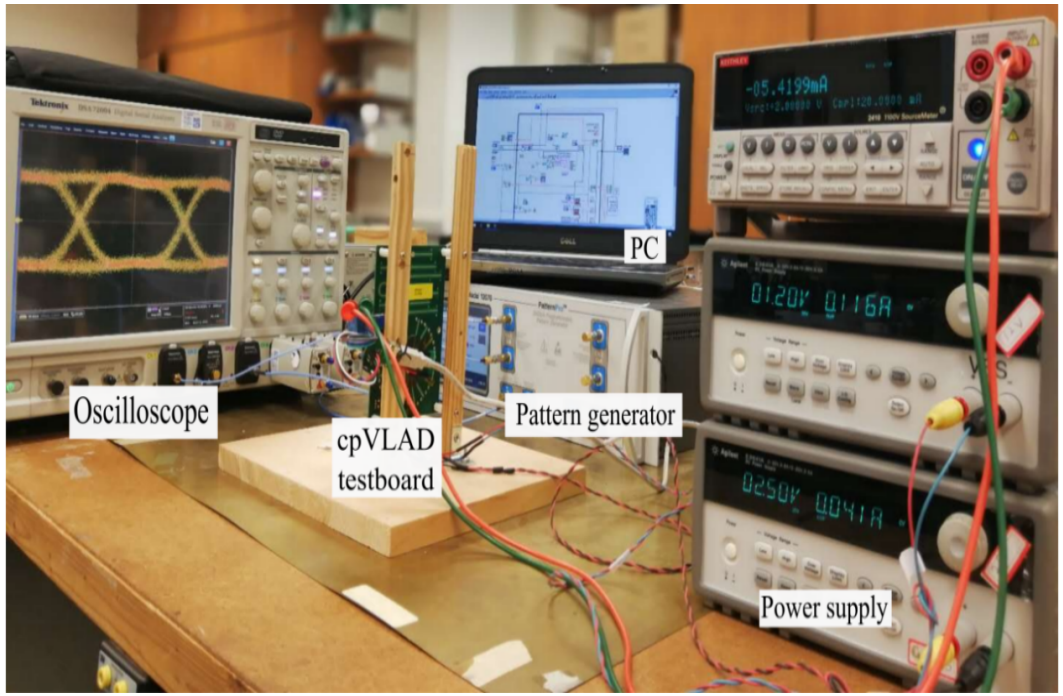
cpVLAD

- cpVLAD is a 4 lane, 10 Gbps each, VCSEL array driver developed to address the issue that VCSEL forward voltage increases under ultra high radiation and low temperature. This increase will cause problem of array optical transmitters in the current 1.2 and 2.5 V powering scheme.

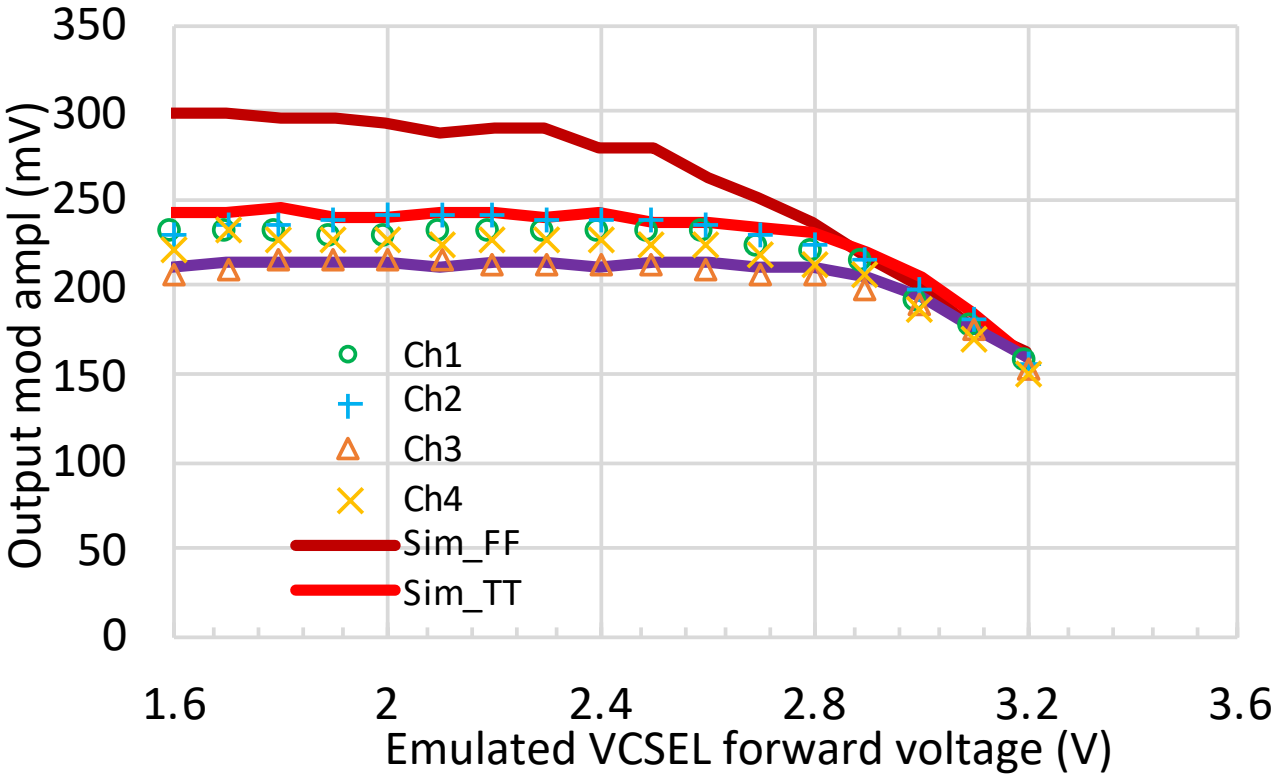


cpVLAD

- This design has been fully tested and reported (TWEPP and JINST). It can be used in future development of array optical transmitters for applications in extreme conditions.

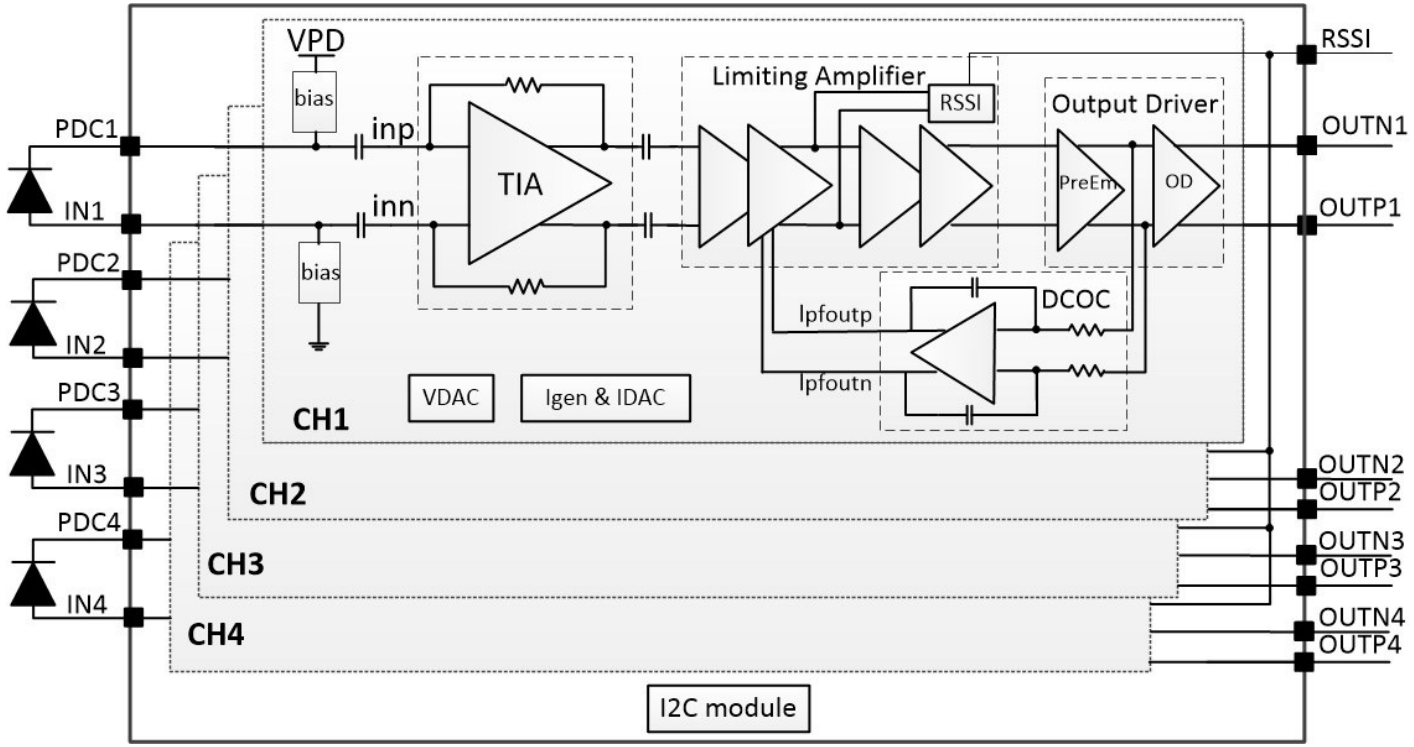


Test in collaboration with CERN



QTIA

- QTIA is a 4 lane array p-i-n diode (GeAs or InGeAs) TIA + LA. The speed is selectable to be 2.56 and 10 Gbps. Different diode biasing schemes, with one that has a charge pump to raise the bias voltage, are designed in the 4 channels to search for mitigation to radiation induced performance degradation of the diodes.

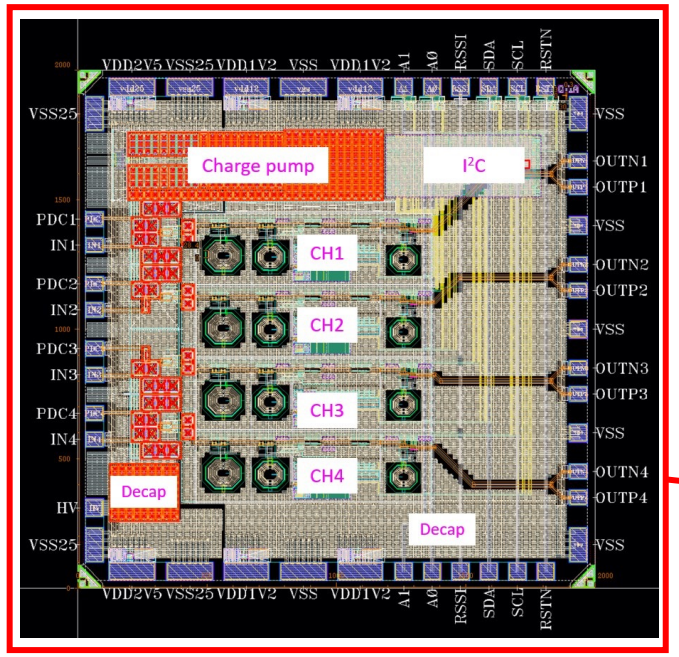


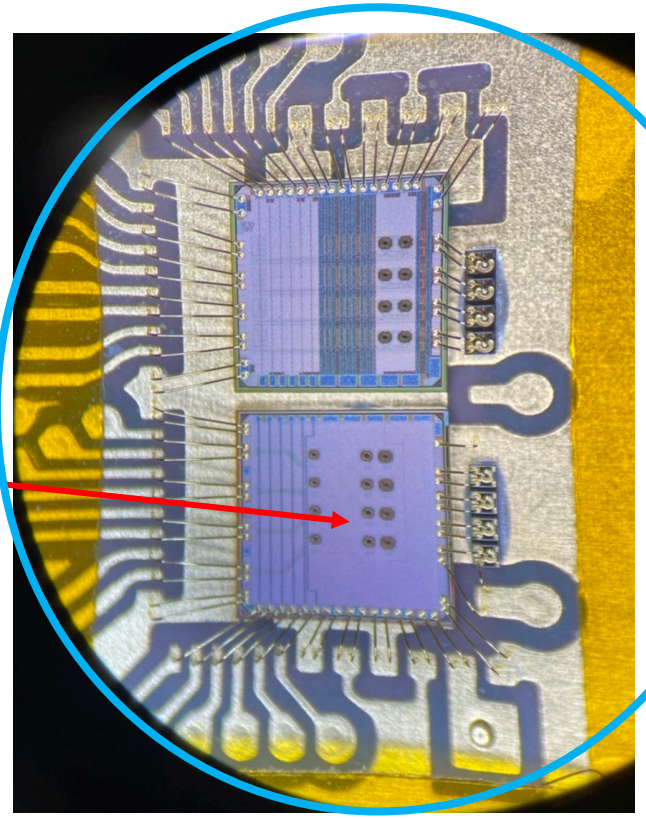
Other than testing the TIA + LA, we will test different biasing condition to the diode to mitigate responsivity loss due to radiation.

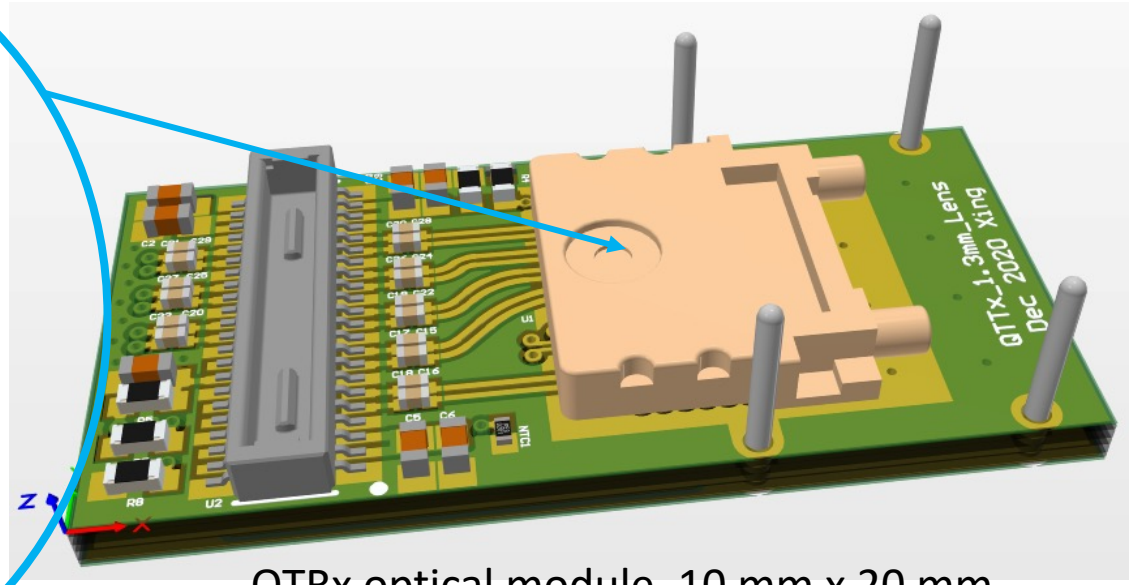
- ❑ CH1: charge pump + PD bias UP & Down
- ❑ CH2: (VDD25) + PD bias UP
- ❑ CH3: (VDD25) + PD bias Down
- ❑ CH4: HV (external) + PD bias UP & Down

QTIA

- Tests of the prototype chips will start next week. The results will be reported to the community in due time.
- The final goal of this ASIC is for the 4Tx+4Rx optical module QTRx, with cpVLAD as the VCSEL driver.







QTRx optical module, 10 mm x 20 mm
4 Tx + 4 Rx, each up to 10 Gbps

Summary

- We progressed from 1 Gbps (15 – 20 yrs ago) to 5 Gbps (now) and are reaching 10 Gbps (to be installed in detectors in a few years) for detector data transmission.
- Many ASICs and Optical Modules have been developed, and the community is adapting to the lpGBT ecosystem (transmission protocol and forward error correction for SEUs).
- While the GBT and lpGBT ecosystems from the common projects are vital for future detector data transmission systems, ASICs may still be needed for applications that have special needs, example: low latency in trigger channels.
- To push the speed further up, there are plans of R&Ds to reach 28 Gbps NRZ and 56 Gbps PAM4, through 28 nm CMOS. This will be expensive.
- In collaborations with IPAS, SMU is carrying out R&Ds on a few ASICs and optical modules (not reported in this talk) to address difficult issues in detector data transmission, and to try to reach 20 Gbps using PAM4 using the 65 nm CMOS.