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TaichuPix-2 test results

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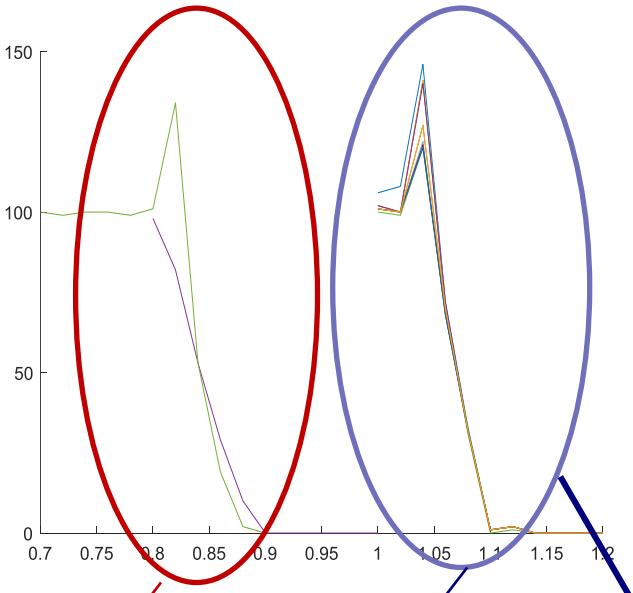
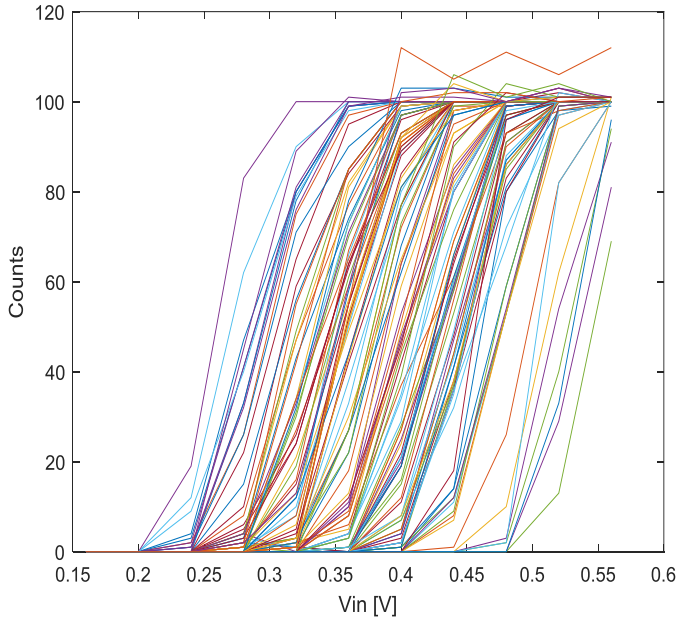
S-curve test

- **In the previous test, when one column of pixels are enable, their s-curves show NO dispersion**
- **In the recent test, when one column of pixels are enable, their s-curves show obvious dispersion**



1/2 pixels unmasked & enabled

128 pixels Unmask & enabled

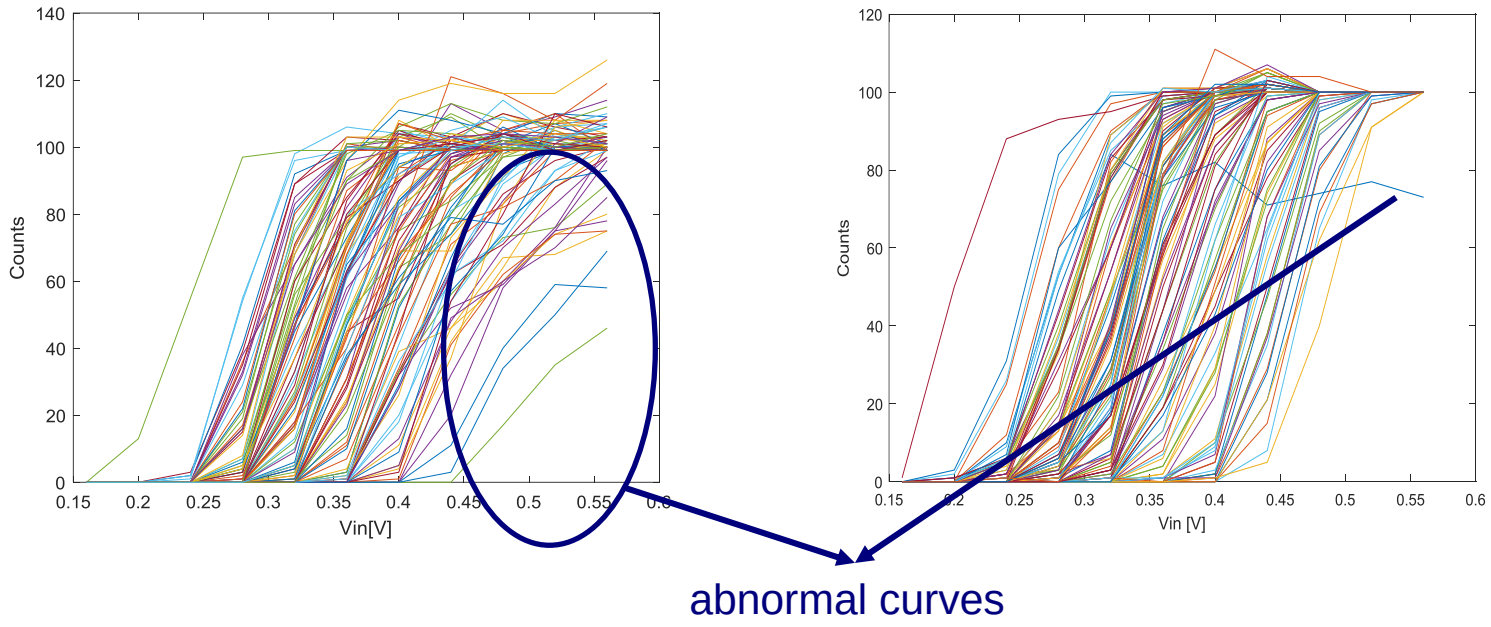


S-curves of column#8 with all pixels enable

This phenomenon NOT reappear any more, with same/different bias condition, even for another chip

S-curves of column#1

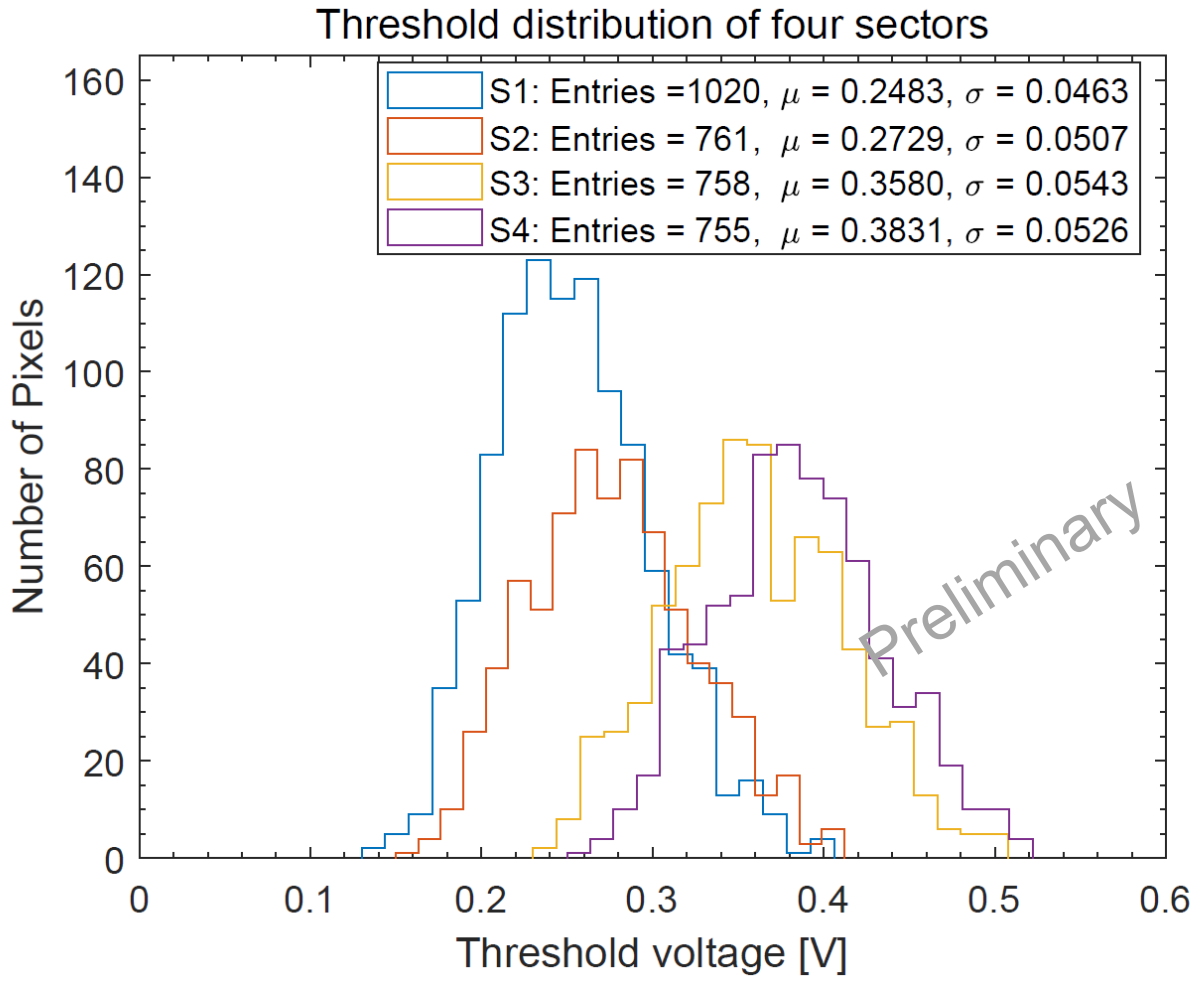
- **Enable one pixel every time**
- **Enable all pixels at one time**



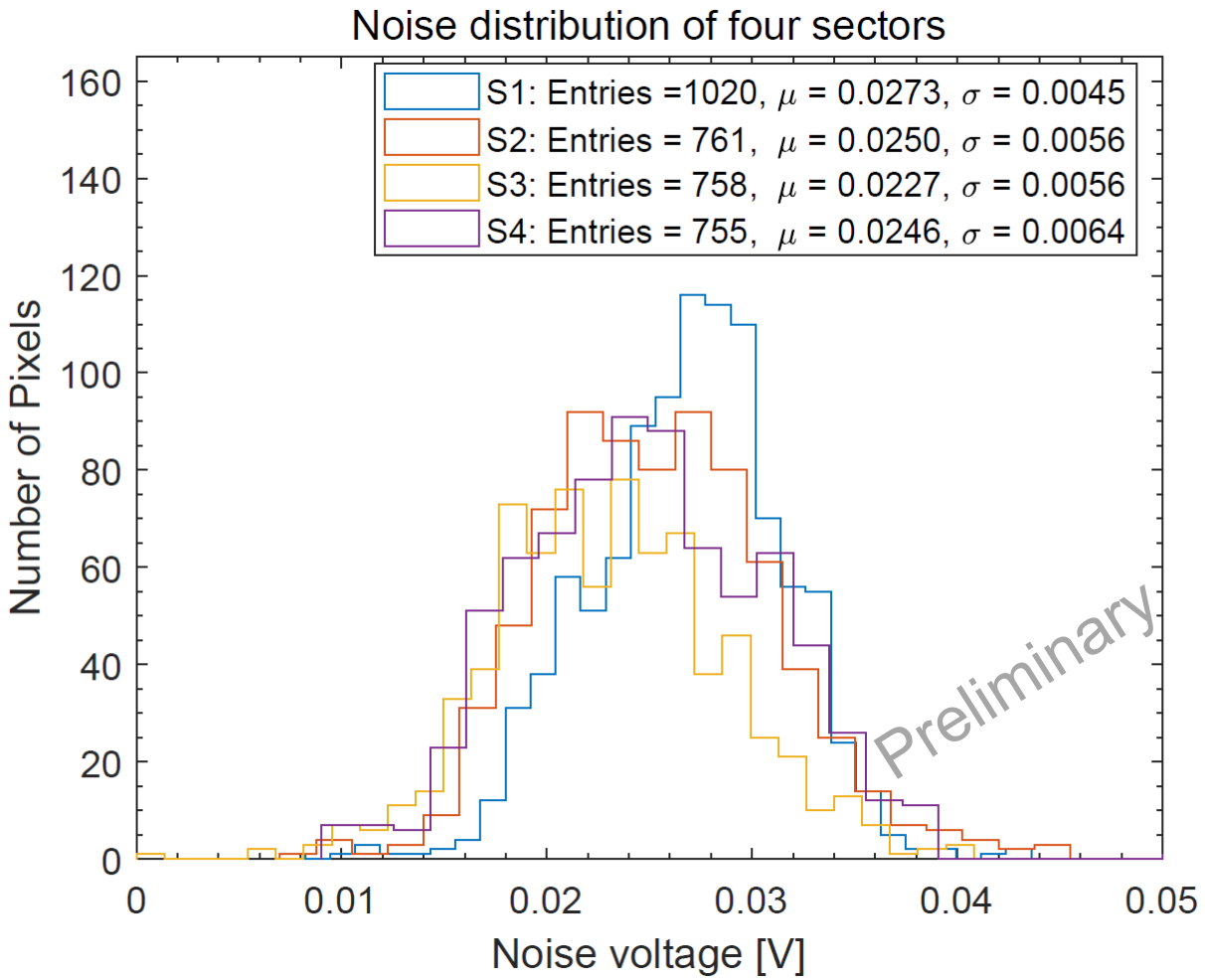
- The two tests show comparable results, and the abnormal curves are due to the order of s-curve scanning. These pixels show normal s-curve if they are scanned alone.
- In the following tests, all s-curves are measured with one column enable at one time.

Threshold distribution measured on S1-S4

- **Based on the same bias condition for pixel analog, S-curves measured for S1-S4 (with different pixel analog designs)**



Noise distribution measured on S1-S4



The measured threshold and noise difference between different sectors agree with design qualitatively.

Comparison of ENC and Charge Threshold

- **Converting the noise/threshold voltage to electrons by 0.88 mV/e$^-$**
  - Assuming the charge injection capacitance in each pixel is 0.18 fF, which is extracted from layout

Preliminary

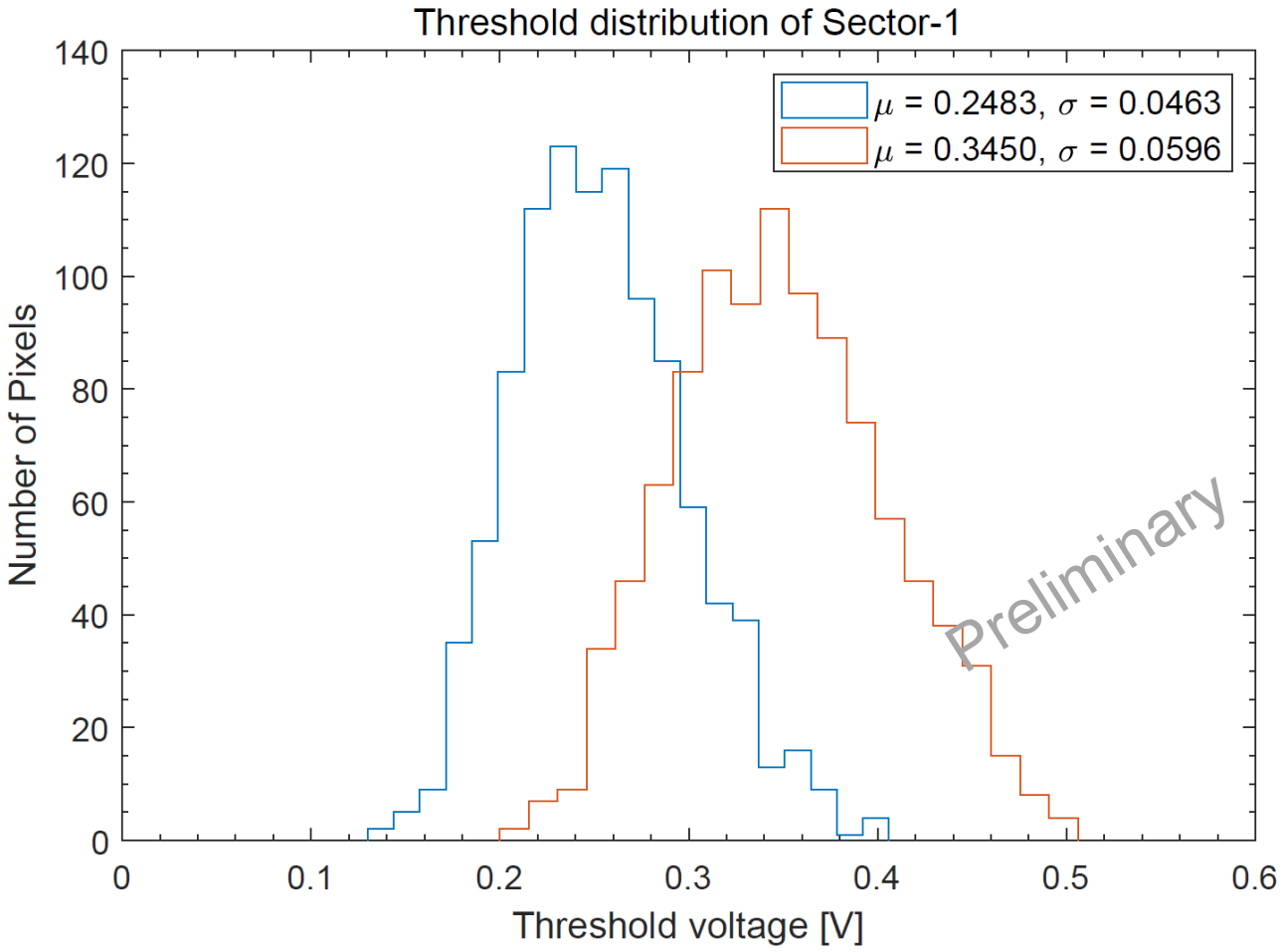
	Threshold Mean	Threshold RMS	ENC	ENC Std. dev
S1	282.1 e$^-$	52.7 e$^-$	31.0 e$^-$	5.1 e$^-$
S2	310.1 e$^-$	57.6 e$^-$	28.4 e$^-$	6.4 e$^-$
S3	406.8 e$^-$	61.7 e$^-$	25.8 e$^-$	6.3 e$^-$
S4	435.3 e$^-$	59.8 e$^-$	28.0 e$^-$	7.3 e$^-$

ENC and charge threshold in this table only for comparison of different sectors, but the absolute value can not used for the sensor assessment

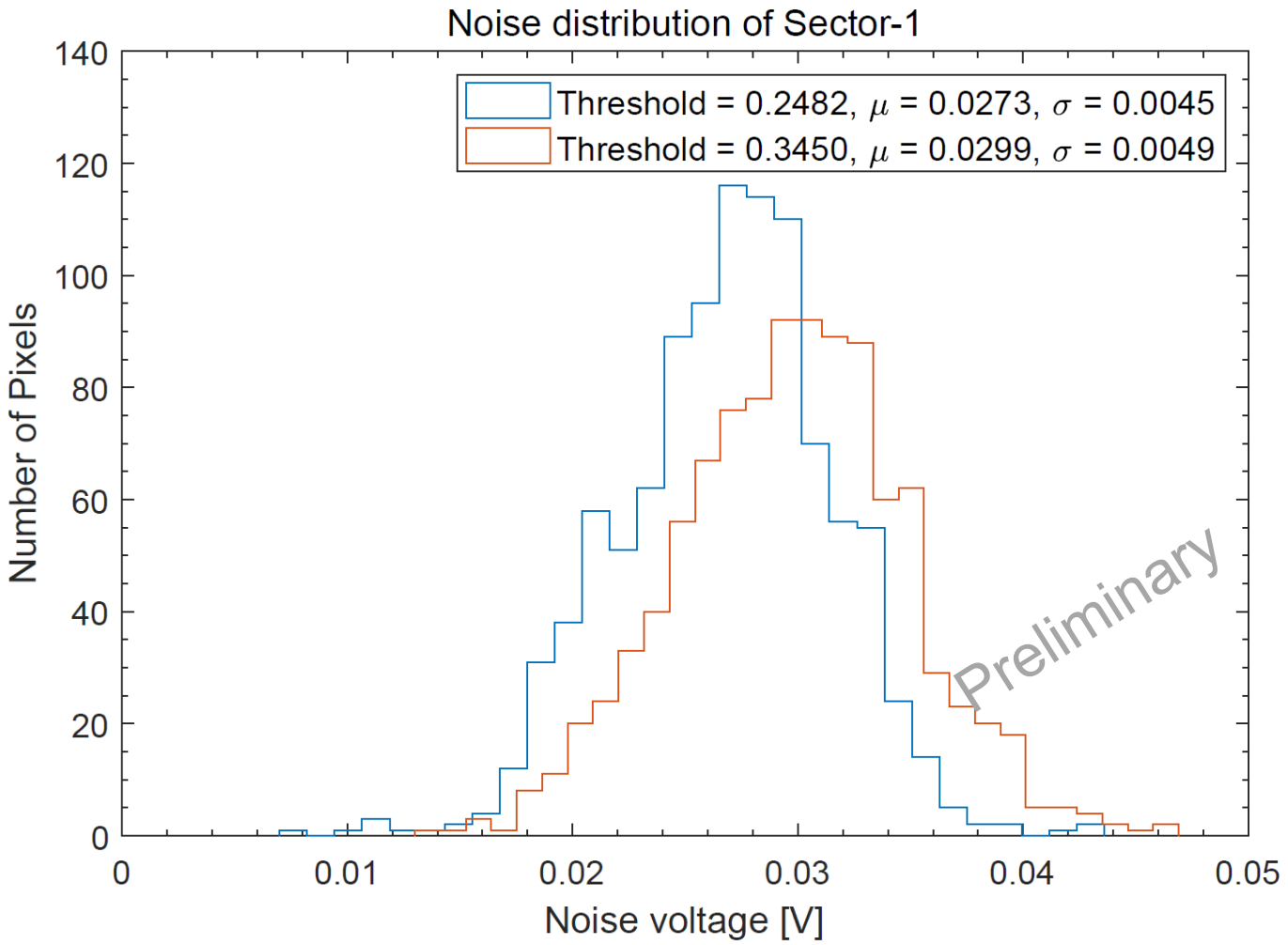
- **Factor of charge to voltage (0.88 mV/e- in simulation) need to be calibrated**

Threshold distribution measured on S1

- **S-curves measured on different bias conditions of front-end for S1**
- **The effect of bias condition on threshold coincides with design**

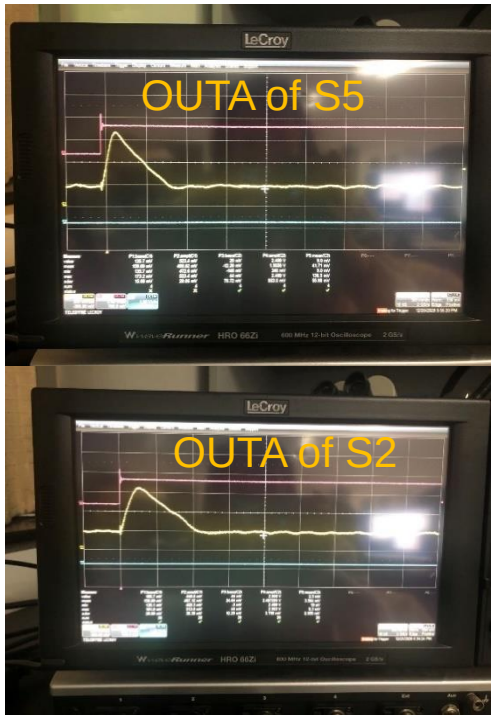


Noise distribution measured on S1



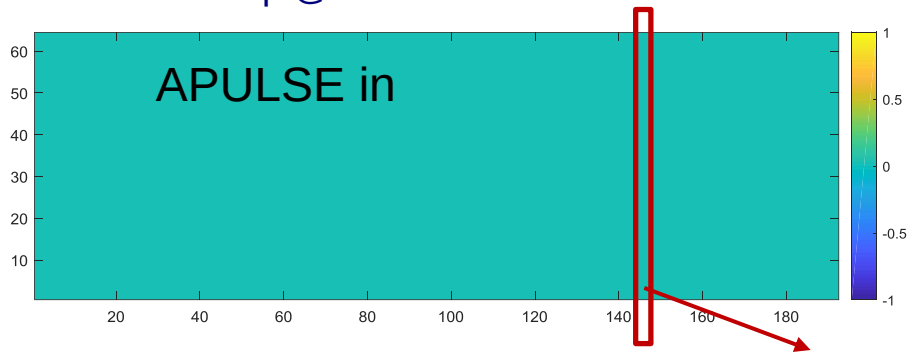
Response of sector 5

- **Sector 5 has same FE but smaller sensor as in S2, with ALPIDE-like pixel digital**



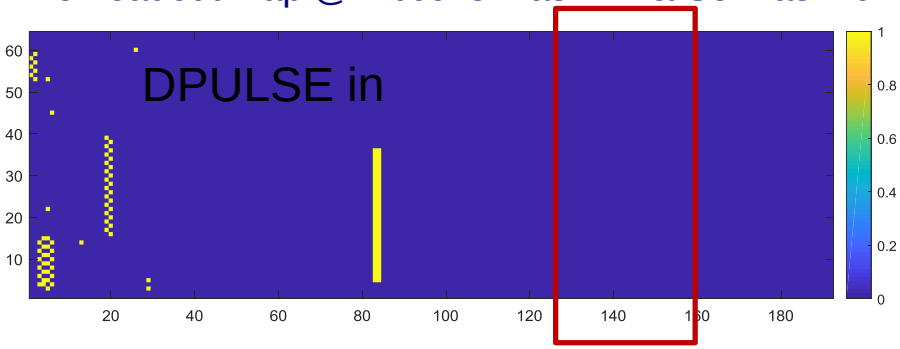
Analog output of S5 shows same amplitude and lightly faster rising edge, which coincide with design

Pixel readout map @S5 unmasked and Dbcol.73 enable



Analog outputs have response to APULSE, but NO pixel readout through digital output

Pixel readout map @ Dbcol.8 mask =1 & S5 mask=0



NO pixel in S5 responses to DPULSE

Digital logic of S5/S6 has no response to APULSE and DPULSE

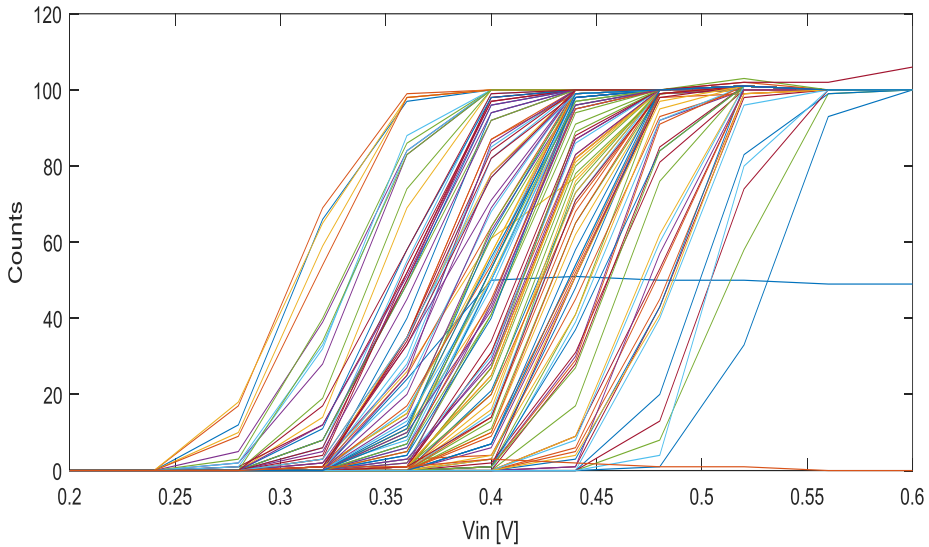
Analog performance with negative VSUB

- **Measured response of the front-end on the monitoring pixel in S1**
- **APULSE @ VHIGH= 1.2 V, VLOW = 0.47 V (~ 830 e^-) with the same bias**

Analog output of pixel <8,124> vs. VSUB

VSUB (V)	Analog output baseline (mV)	Analog output amplitude (mV)
0	184	432
-1	152	472
-2	123	488
-3	92	412
-4	76	274
-5	550	--

s-curves of 128 pixels in Dbcol <8>



Threshold and noise of 128 pixels in Dbcol <8>

VSUB (V)	Threshold Mean (mV)	Threshold RMS (mV)	ENC (e-)	ENC Std. dev (e-)
0	248.3	46.3	27.3	4.5
-1	396.0	45.1	27.9	3.5

Issues of negative VSUB

- **Chip is NOT very vulnerable to negative VSUB than the TaichuPix1**
- **Negative VSUB changed the current of VDD to GND and VRESET to VSUB (the sensor branch)**
  - The first time test with negative VSUB, no current increasing occurred for 1.8V power and VRESET. The baseline of analog output decreases quickly with VSUB, so that the bias condition has to change due to the threshold of NMOS increased.
  - In the later test, the current increased ~60% for 1.8V power and 300% for VRESET. The current will decrease to the normal level when turn the VRESET down to below 0.9 V, and it will not increase when turn up the VRESET again.
    - The functionality of chip is normal
    - The measurements in page10 were done in this case
  - More chip need to be tested to understood the issue

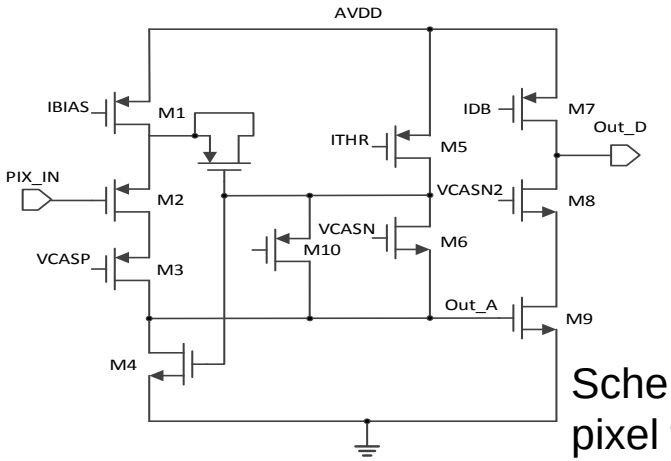
- **When VSUB < -2.5 V, analog output has response to APULSE, but no digital output and sometimes no response to DPULSE**
  - to adjust bias condition
  - to test new chips

Summary

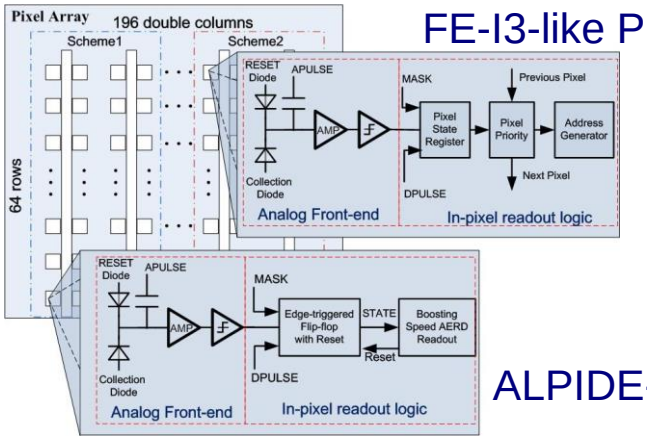
- **6 sectors of analog FE works stable at VSUB = 0 V, good SNR proved**
- **S1 shows smallest threshold, and S3 shows best noise performance**
- **Some resonance effect observed during the multiple pixels calibration, not understood yet**
- **FE performance with negative VSUB (-6 V) need more investigation**
- **Proposed improvement in the next version**
  - To enhance power mesh
  - To increase the charge injection capacitance (C_{inj})
  - To decrease FE layout to fit pixel size to 24 ×24 μm^2

Backup

Sector	Pixel front-end	Pixel digital	Pixel size
Sector 1	Same as S1 of TC1, reference design	FEI3-like	25 μm × 25 μm
Sector 2	M6 with guard-ring, PMOS in independent nwell	FEI3-like	25 μm × 25 μm
Sector 3	M6 in enclosed layout, PMOS in independent nwell	FEI3-like	25 μm × 24 μm
Sector 4	Increasing M3, M4, M9. M6 in enclosed layout, PMOS in independent nwell	FEI3-like	25 μm × 25 μm
Sector 5	Same FE as S2, with smaller sensor	ALPIDE-like	25 μm × 25 μm
Sector 6	Same FE as S1	ALPIDE-like	25 μm × 25 μm



Schematic of in-pixel front-end



FE-I3-like Pixel

ALPIDE-like Pixel