Report (only problems)

Zhan Li

- VBF Sample used:
  - mc16_13TeV.500372.MGPy8EG_A14_NNPDF23LO_VBFH125_sbi_4l_m4l130.root
  - mc16_13TeV.500374.MGPy8EG_A14_NNPDF23LO_VBFH125_sbi5_4l_m4l130.root
  - mc16_13TeV.500375.MGPy8EG_A14_NNPDF23LO_VBFH125_sbi10_4l_m4l130.root
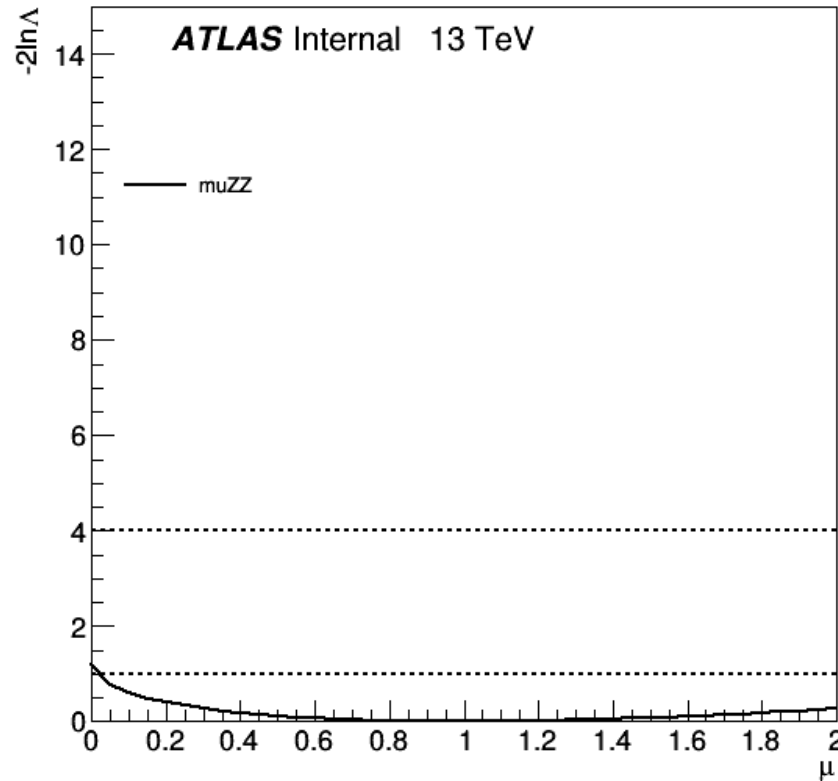 - mc16_13TeV.500373.MGPy8EG_A14_NNPDF23LO_VBFH125_bkg_4l_m4l100.root
- categories:

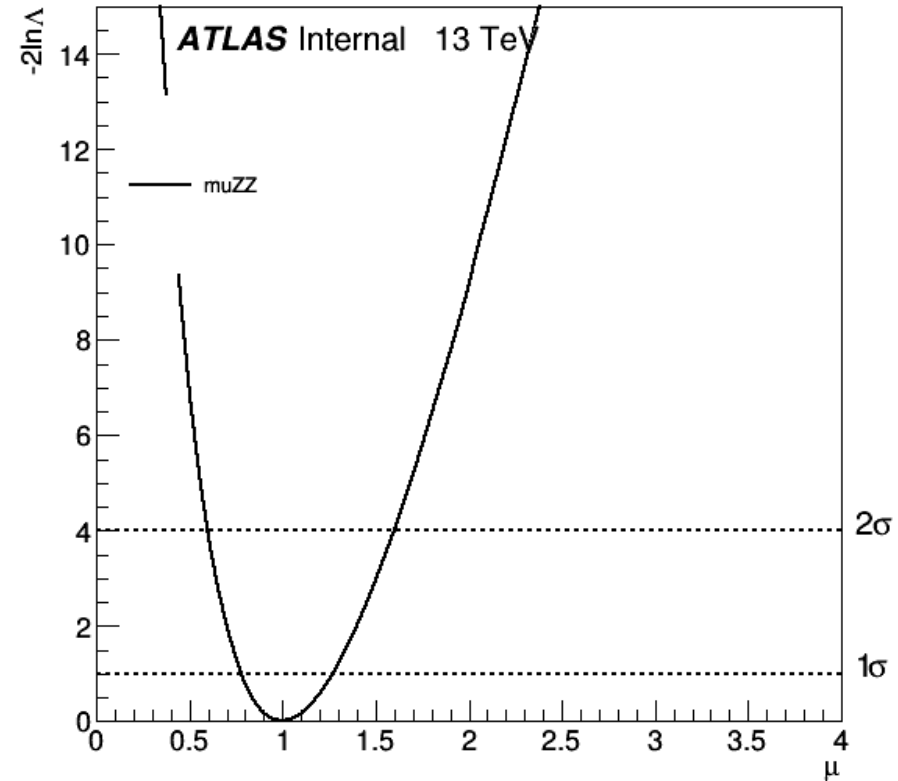VBF_4mu_13TeV, VBF_4e_13TeV, VBF_2e2mu_TeV, VBF_4l_13TeV

- mcsets:

qqZZ, VBFSBI, VBFSBI5, VBFBKG, ggHSIG, ggHSBI

m4l bin by bin


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[cuts]
VBF_4mu_13TeV_bin01 = (130<m4l_fsr && m4l_fsr<140 && (event_type==0))
VBF_4mu_13TeV_bin02 = (140<m4l_fsr && m4l_fsr<150 && (event_type==0))
VBF_4mu_13TeV_bin03 = (150<m4l_fsr && m4l_fsr<160 && (event_type==0))
VBF_4mu_13TeV_bin04 = (160<m4l_fsr && m4l_fsr<170 && (event_type==0))
VBF_4mu_13TeV_bin05 = (170<m4l_fsr && m4l_fsr<180 && (event_type==0))
VBF_4mu_13TeV_bin06 = (180<m4l_fsr && m4l_fsr<190 && (event_type==0))
VBF_4mu_13TeV_bin07 = (190<m4l_fsr && m4l_fsr<200 && (event_type==0))
VBF_4mu_13TeV_bin08 = (200<m4l_fsr && m4l_fsr<210 && (event_type==0))
VBF_4mu_13TeV_bin09 = (210<m4l_fsr && m4l_fsr<220 && (event_type==0))
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[cuts]
VBF_4mu_13TeV = (130<m4l_fsr && m4l_fsr<220 && event_type==0)
VBF_4e_13TeV = (130<m4l_fsr && m4l_fsr<220 && event_type==1)
VBF_2mu2e_13TeV = (130<m4l_fsr && m4l_fsr<220 && event_type==2 || event_type==3)
VBF_4l_13TeV = (130<m4l_fsr && m4l_fsr<220)
```

Next

- I am trying to learn how to generate uncertainties.
- Continue to work on CRs.