



TaichuPix-2 test results

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Analog performance with negative VSUB

- When VSUB < 0 V, bias setting needs to be tuned to make the FE in work region</p>
 - > i.e. VRESET & VCASN2 & VCLIP increased, VCASN increased/decreased
 - > To keep similar baseline of OUTA, and similar pulse duration



s-curves of 128 pixels in Dbcol <8>

CEPC

Threshold distribution measured on S1-S2

S-curves measured for S1&S2, at VSUB = 0 V & -6 V



Noise distribution measured on S1-S2





500

400

Performance of S3

- CEP
- Based on the same bias setting as S1 and S2, many pixels in a column of S3 do NOT work normally
- Preliminary tuning on the bias setting did not work, need more investigation

s-curves of 128 pixels in Dbcol <40>



Discussion on test results



- S1 & S2 can work normally with negative VSUB
- S1 & S2 show higher threshold (~200 mV higher) and higher threshold dispersion (~ 15 mV higher) at VSUB =-6 V than at VSUB = 0V
 - > Inconsistent with theoretical analysis
 - > Differences induced by the different bias setting were not evaluated
 - > Effect of different chip performance was not evaluated
 - This chip shows increased current after the first time test with negative VSUB → performance maybe changed (s-curves @VSUB =GND can not recur at VSUB = 0V)

Need to test more chips