Progress on CALO crystal array

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IHEP

The 9th HERD International Workshop

Feb. 22-23, 2021

outline

1. Progress on WLSF readout part

1.1 New WLSF chips for CALO system on-orbit calibration in short time scale, and low range WLSF signal enhancement

1.2 Vibration test

1.3 CALO crystal array AIT prototype

2. Progress on dual-readout

2.1 WLSF arrangement and PD and flat cable layout

2.2 The variation of WLSF output to PD coupling area

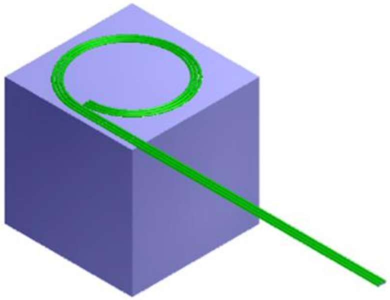
2.3 Thermal analysis of CALO with PDs system

3. Plan of CALO crystal array prototype

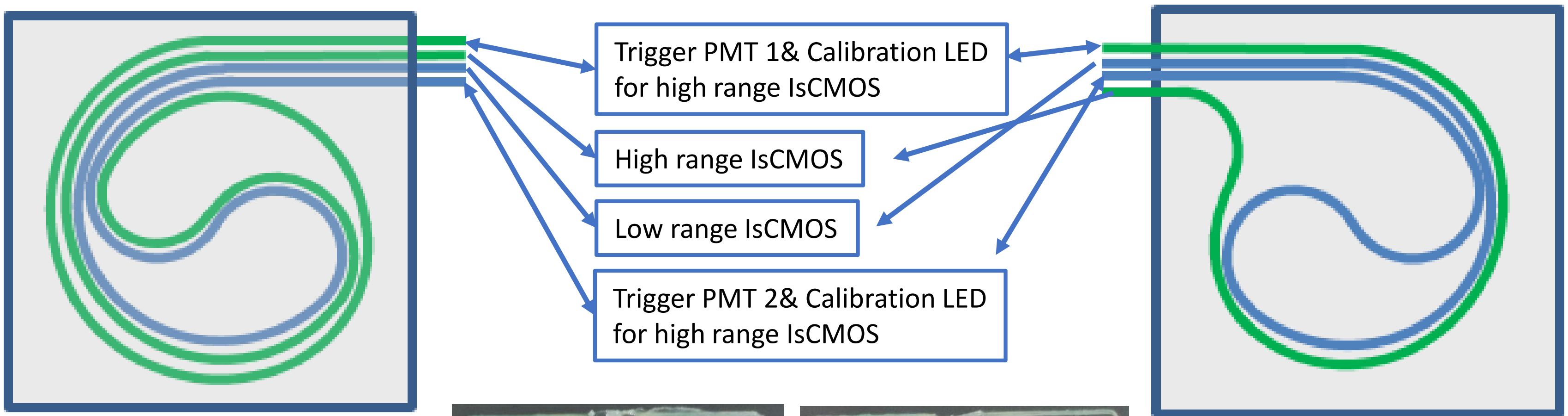
Structure and dual-readout cubes arrangement

1.1 Candidates of WLSF chip

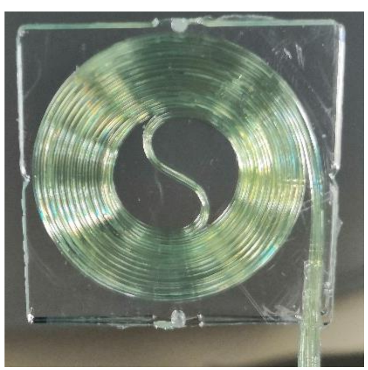
- ➢ Monitor WLSFs amplitude in IsCMOS system in real time
- Two trigger WLSFs injected light for IsCMOS calibration in short timescale
- ➢ Enhance amplitude of low range WLSF

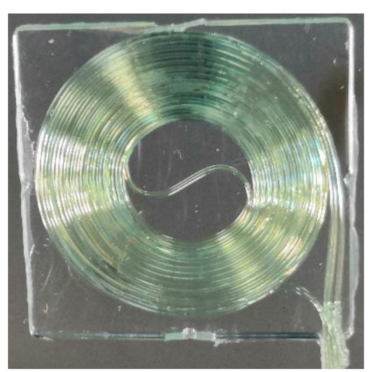


Old version



C-1:**Four output** with **two identical** WLSFs

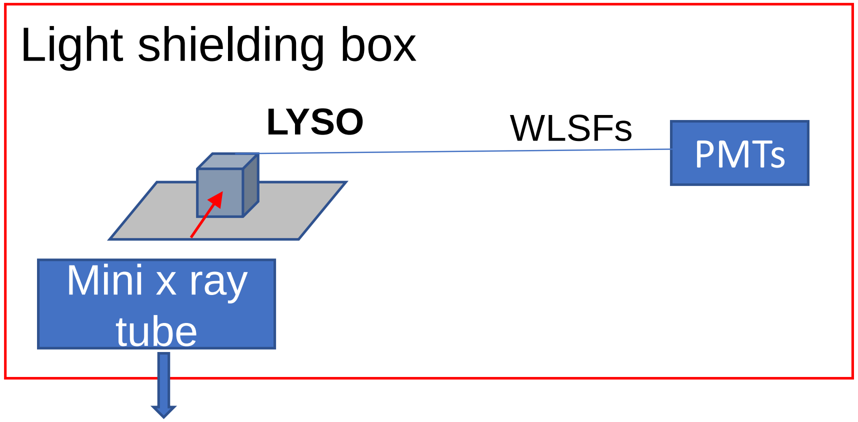




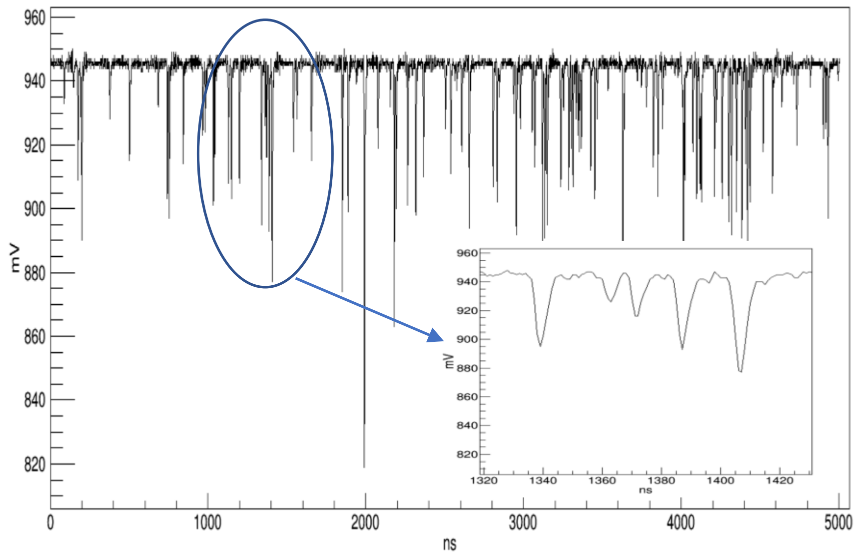
C-2:**Four output** with **two different length** of WLSFs

1.1 WLSF chip test

- **Amptek Mini x ray tube(Max HV 50kV)** irradiated LYSO
- Four PMTs XP2020 collected WLSFs light and analyzed by CAEN DT5751
- Mini x ray tube work on **continuous mode** , an external 150Hz signal triggered DT5751 acquire in pulse mode
- The pulse is discrete single P.E. waveshape in PMT linear range
- **Counting number of P.E. of every pulse instead of charge integration**



Spot diameter is 2mm after installed collimator



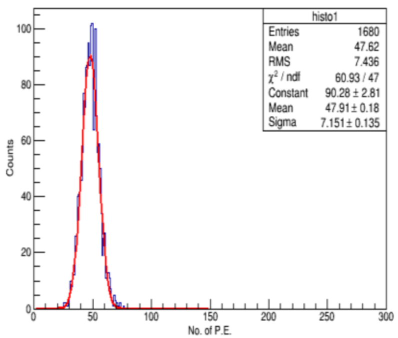
Single pulse

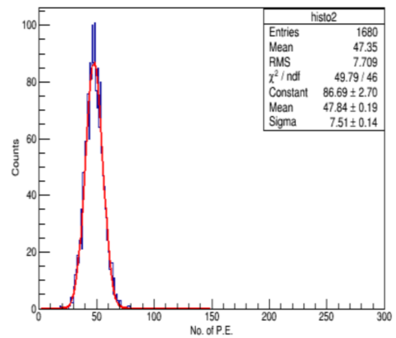
1.1 P.E. spectrum

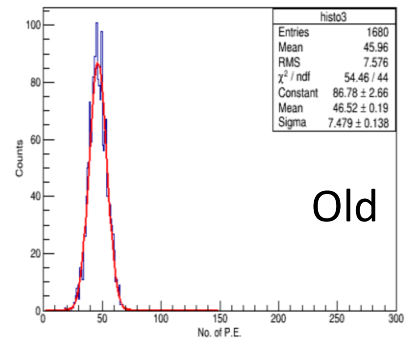
- x ray tube irradiate center of bottom

WLSFs	Ave. P.E.	Ratio(N/N_{old}
old	47.42	**1.00**
C-1	64.68	**1.36**
C-2-H	94.07	**1.98**
C-2-L	13.40	**0.28**

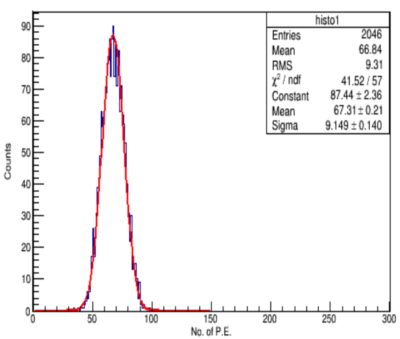
High gain/Low gain:7.1

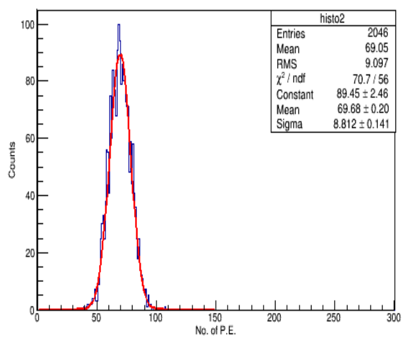


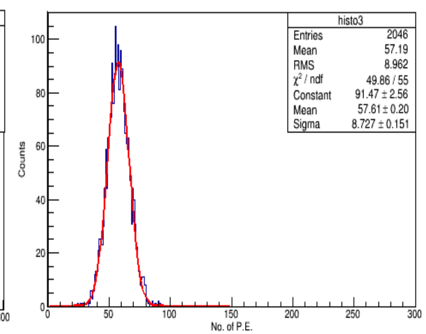


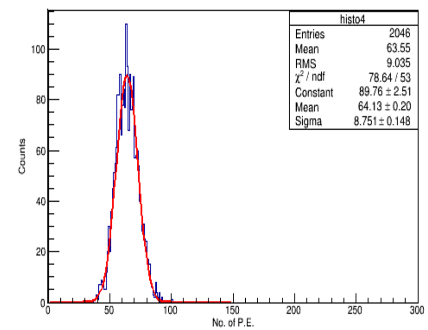


Old

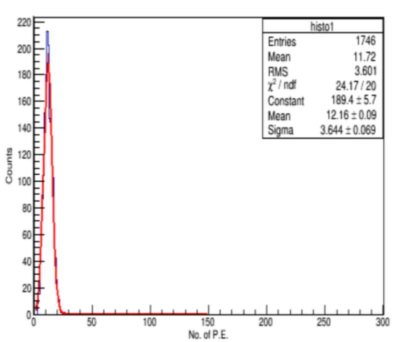


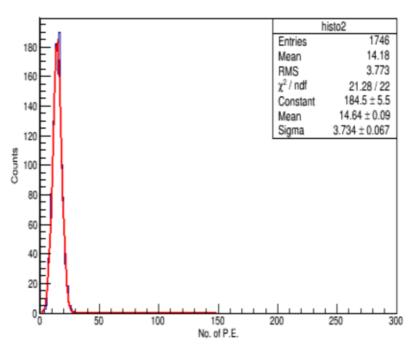


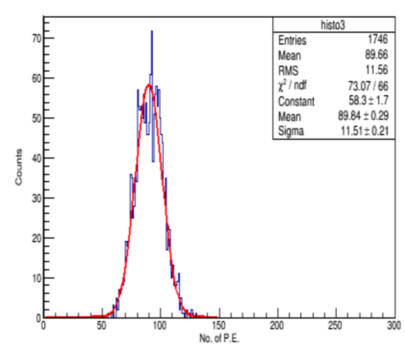


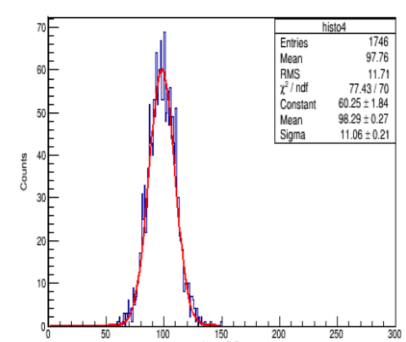


C-1





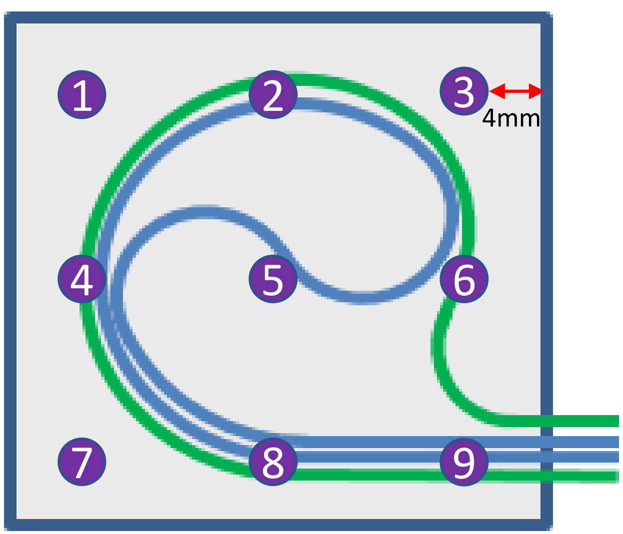




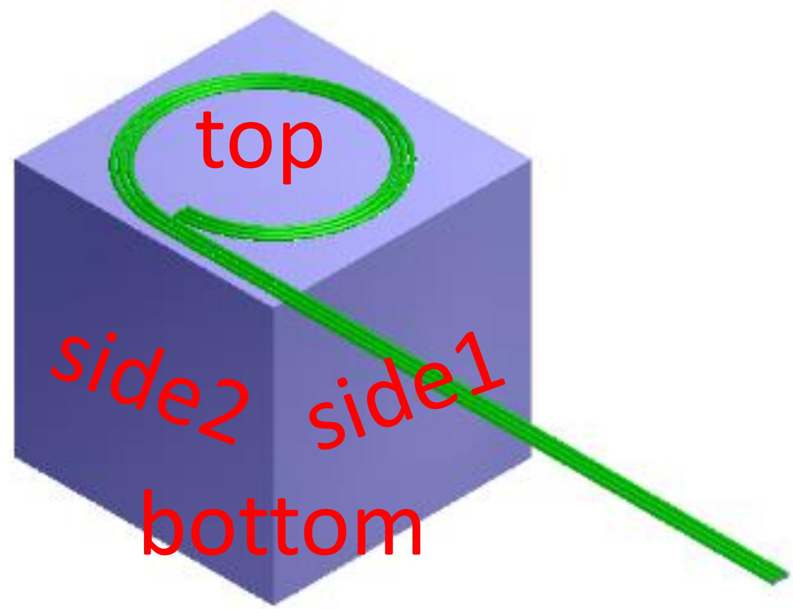
C- 2

1.1 Nonuniformity

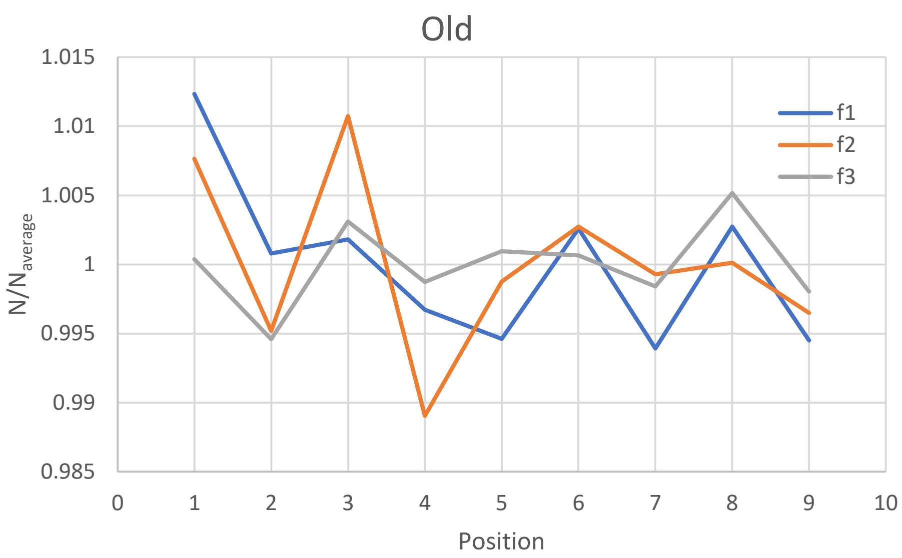
- Nonuniformity on bottom surface
  - 9 irradiated point on bottom surface
- Nonuniformity on different surfaces
  - All six surfaces were measured and only center of each surface is irradiated



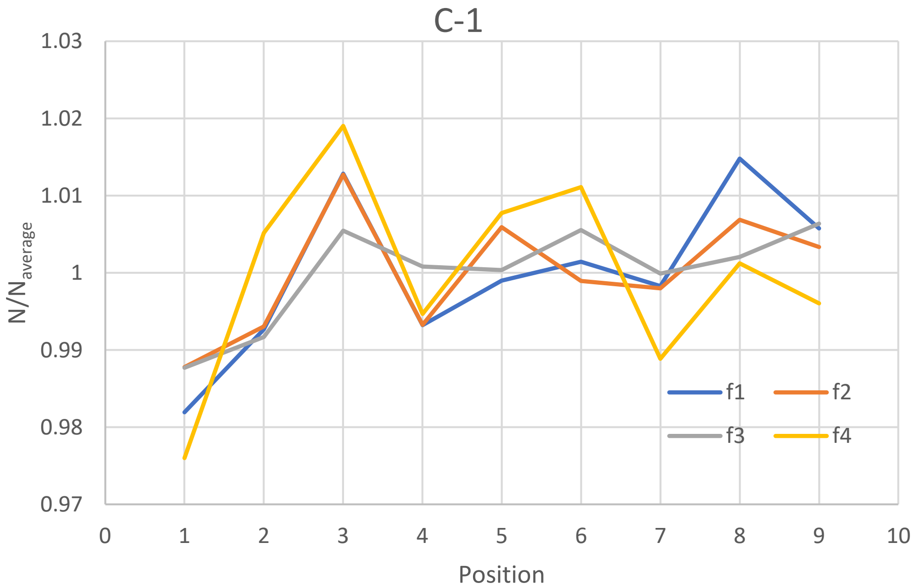
irradiate position on each surface

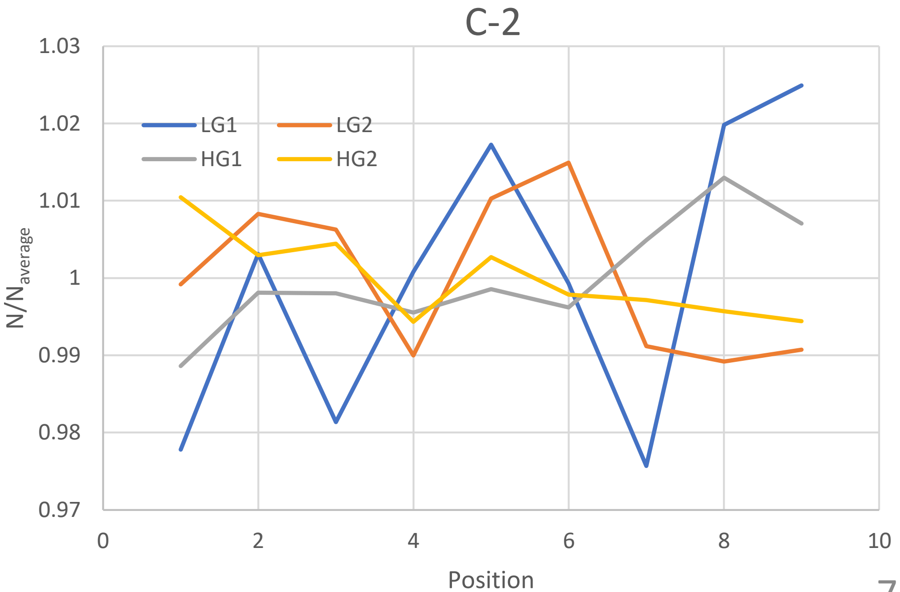


1.1 Nonuniformity on bottom surface

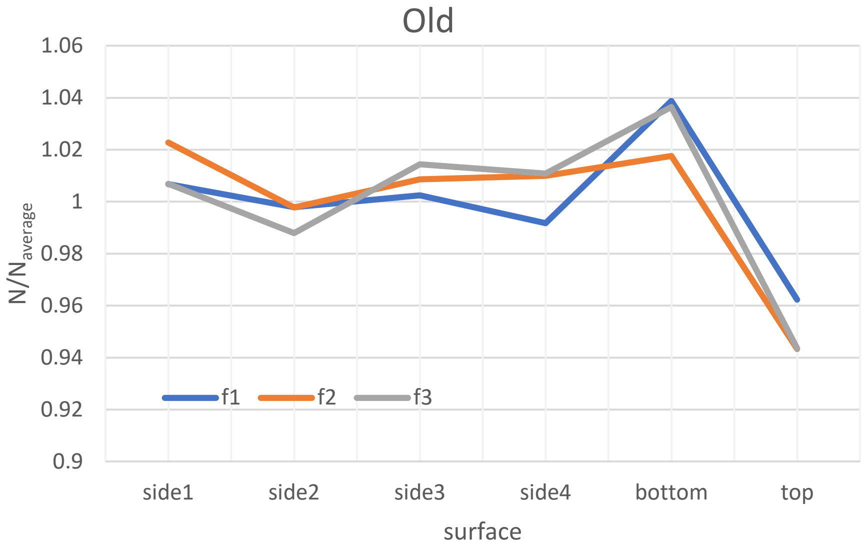


- The nonuniformity on bottom surface is from 0.97-1.03
- **No significance difference among 3 types**

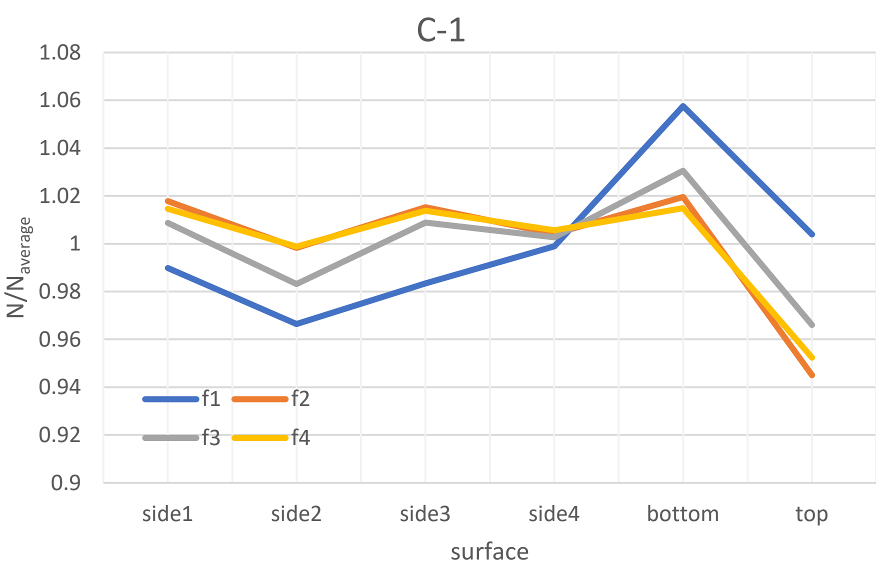


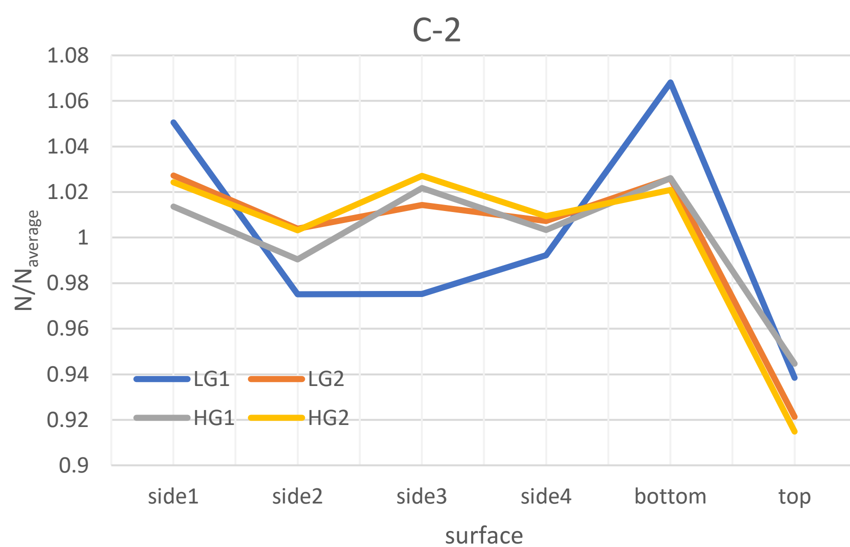


1.1 Nonuniformity of different surfaces



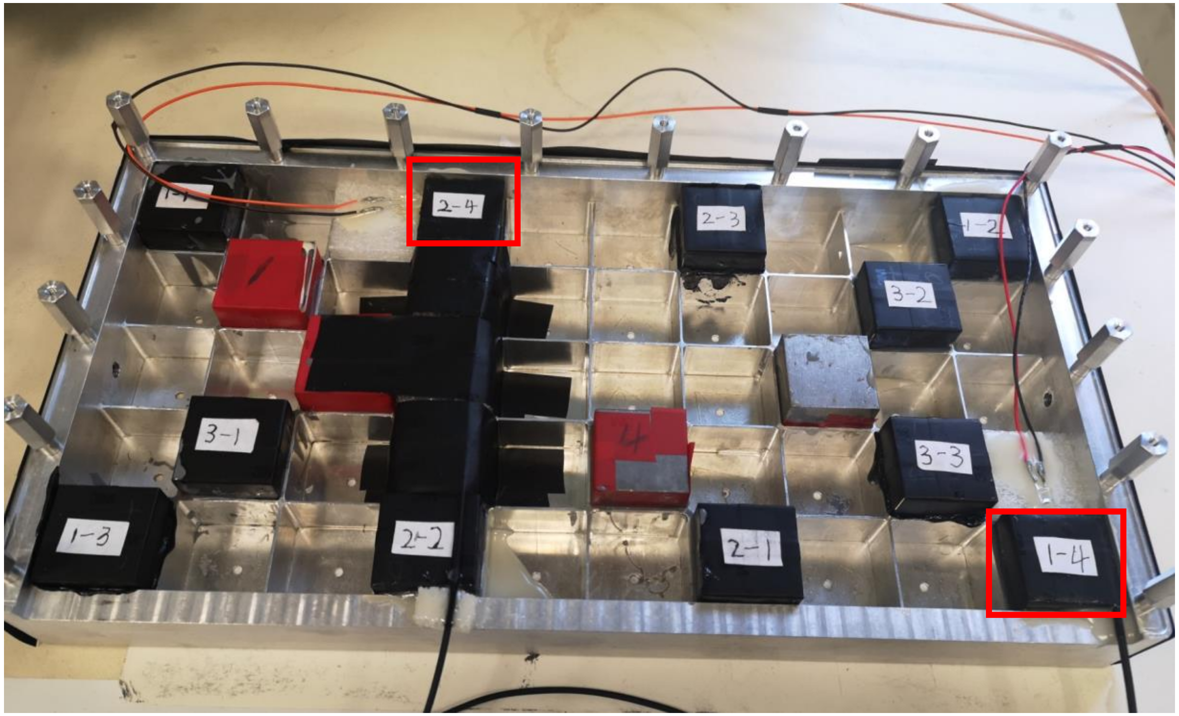
- ➢ The intensity on top irradiated is lower than other side irradiated
- X ray attenuated through WLSF chip on top surface measurement
- **No significance difference among 3 types**
- **C-2 will be the priority option**





1.2 Vibration test

- One small plate prototype was made for vibration test.



Vibration test module

- 2 LYSO+WLSF cells
- 10 stainless steel cubes
- Three types of potting adhesive
- The intensity output of 2 LYSO+WLSF cells are recorded by PMT.

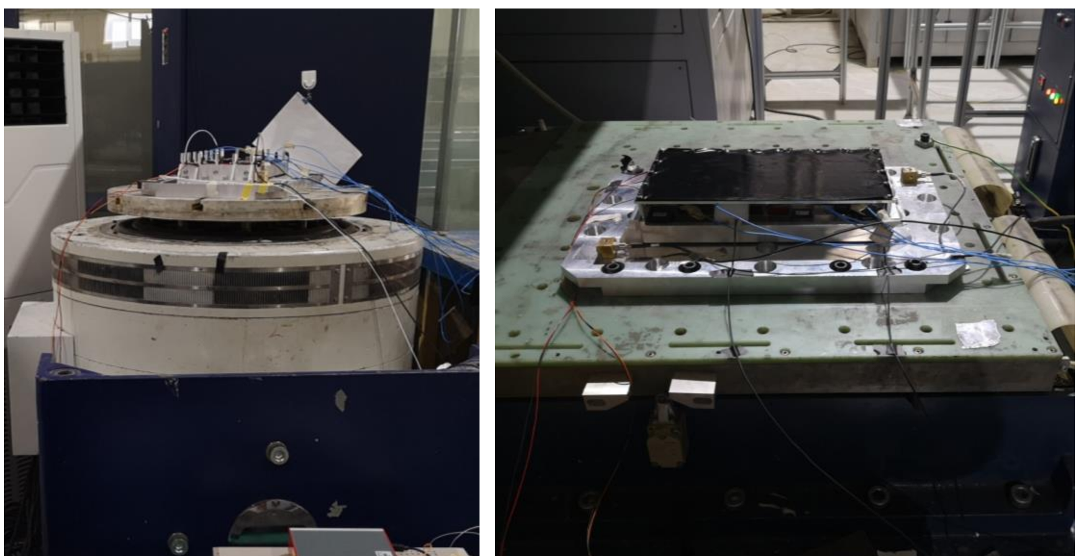
➢ To test the properties of potting adhesive used in the gap between cell and grid.

➢ To test LYSO+WLSF resistance to vibration

1.2 Vibration test

Specification on vibration plate

POS.	1-1	1-2	1-3	1-4	2-1	2-2	2-3	2-4	3-1	3-2	3-3
Cube material	stainless steel			LYSO	stainless steel			LYSO	stainless steel		
Type of adhesive	Sylard 160	J133	AileteGL 3365	J133	Sylard 160	J133	AileteG L 3365	J133	Sylard 160	J133	AileteG L 3365

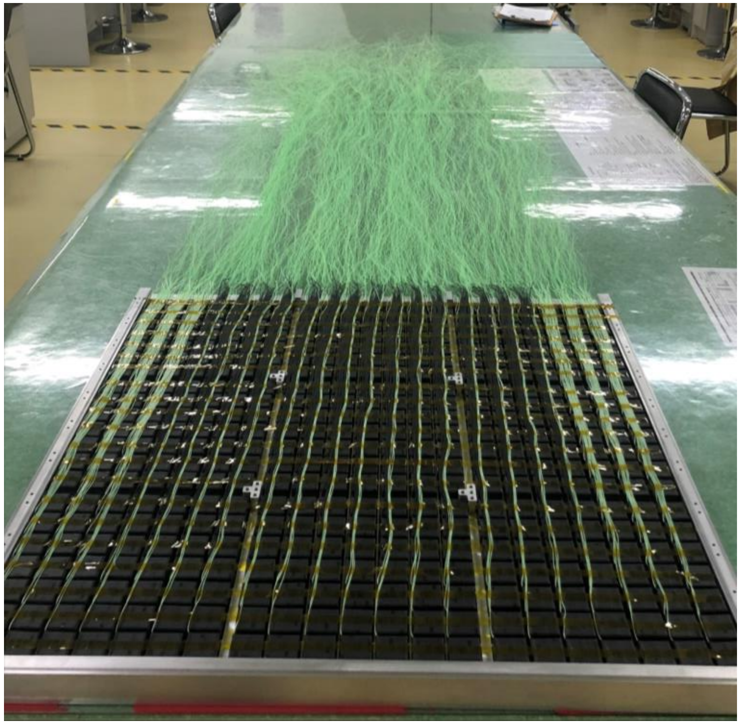


Vibration test

- ➢LYSO, WLSF and coupling disk look in good condition through whole vibration test .
- ➢The output from 2 LYSO+WSLF are stable.

1.3 CALO crystal array AIT prototype

- A CALO prototype was built for AIT verification .
- Total cells:7497 plastic
- Fiber: plastic fiber



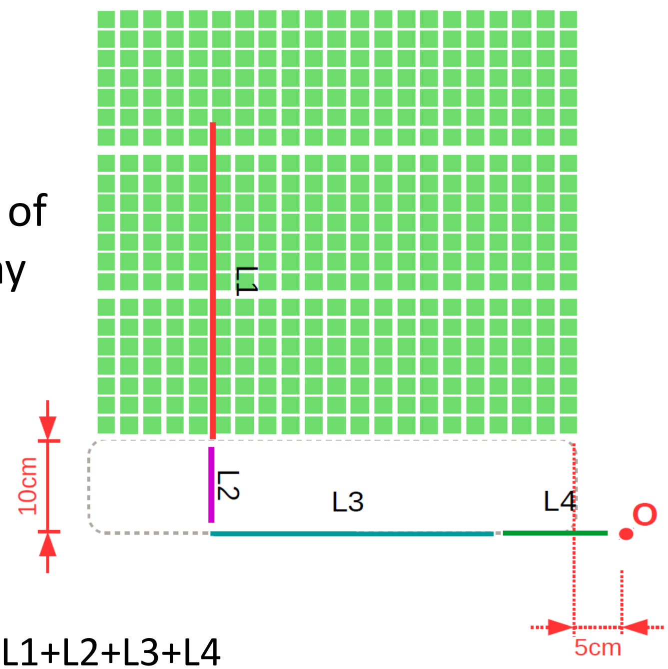
One layer from AIT prototype

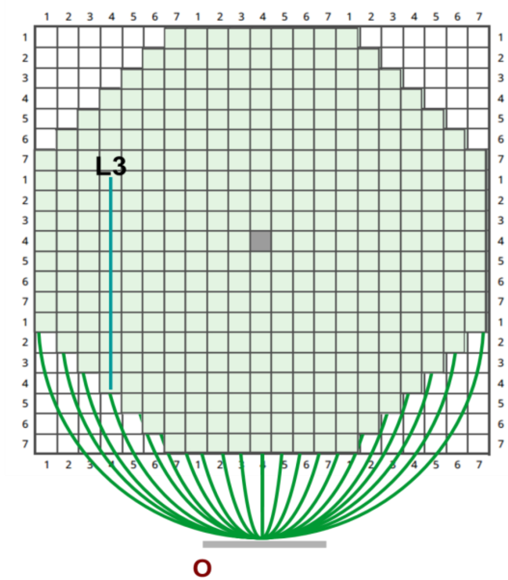
1:1 AIT prototype

1.3 Calculation of fiber length redundancy

- The max redundancy length of WLSF is 1647 mm.

Side view of CALO array





Top view of CALO array

L=L1+L2+L3+L4

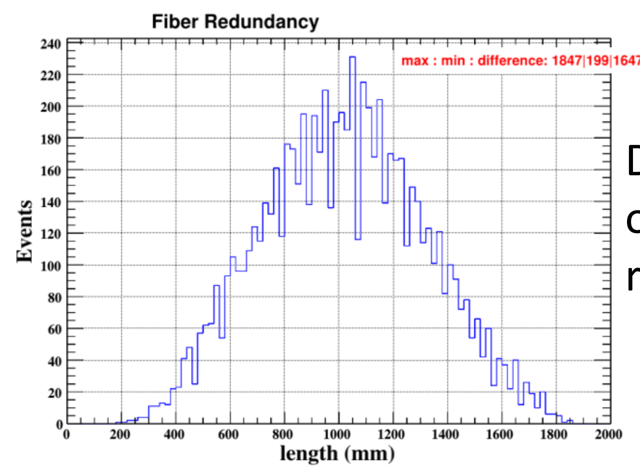
L1:length of fiber inside array

L2:length of fiber between array edge and baseboard

L3:length of straight fiber in baseboard

L4:length of curve fiber in baseboard, approximated with quadratic function curve

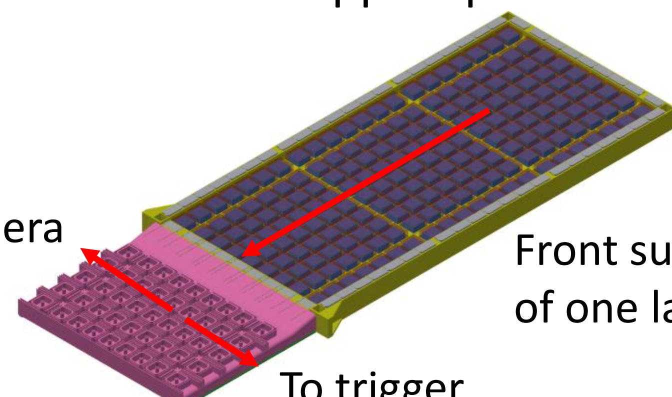
O :position of coupling IsCMOS

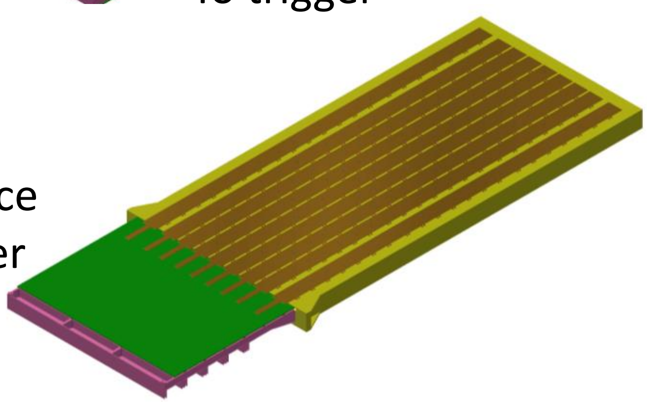


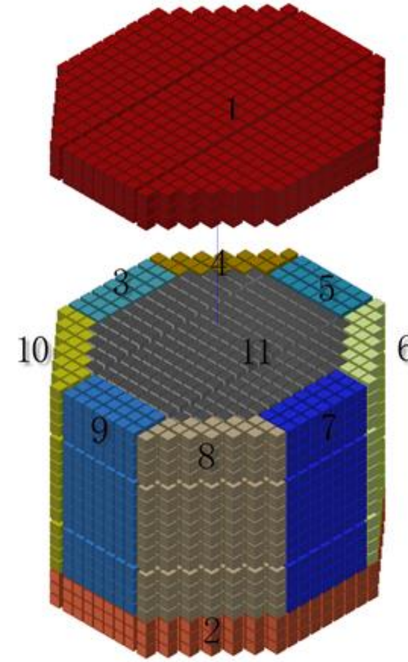
Distribution of all fiber redundancy

2.1 WLSF arrangement and PDs layout

- ➢ **A support plate installed to the CF structure**
- ➢ WSLF arranged on the front of support plate
- • Adapt to different length of WLSFs
- ➢ PDs and electronics layout on the back of CF structure and support plate



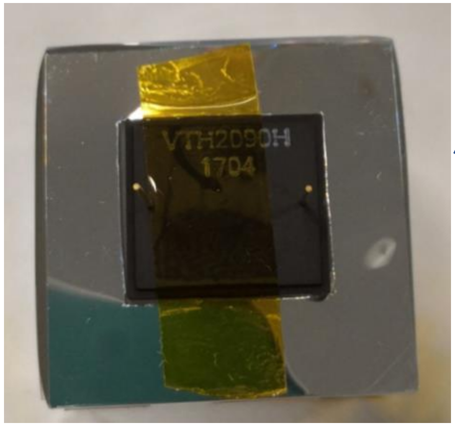




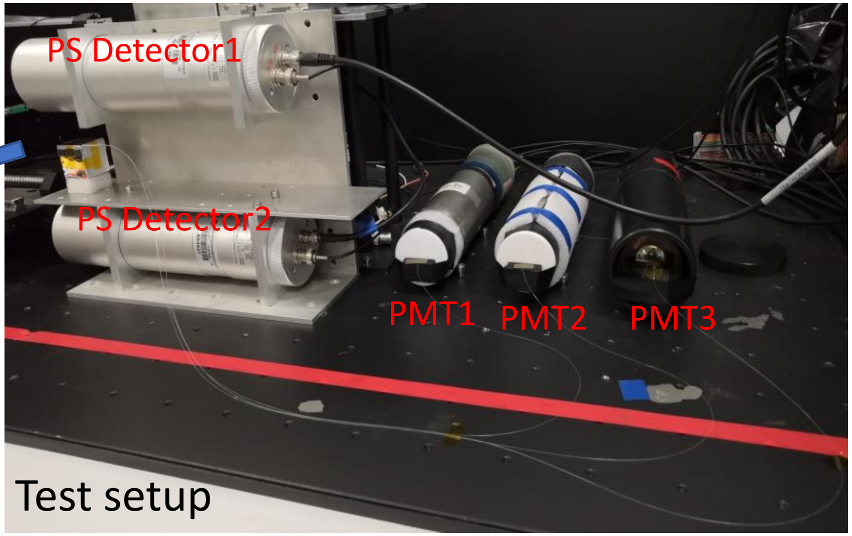
- ➢ Both trigger WLSFs from outer 3 layer cubes will be divided into 10 trigger channels individually.
- ➢ Trigger WLSFs from interior cubes will be divided in to 2 or 4 channels according to trigger system design.
- ➢ **For each trigger fiber bundle, a calibration light source is implemented.**

2.2 WLSF output VS PD coupling area

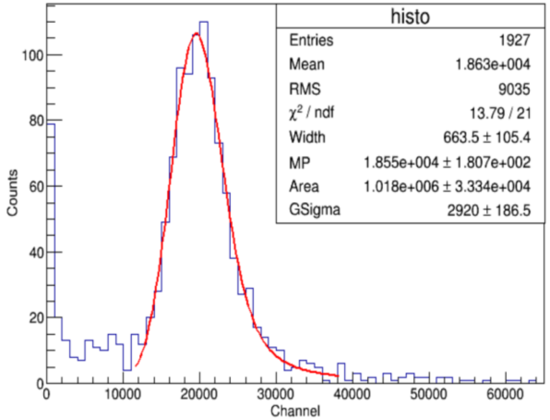
➢ Reduction of WLSF amplitude is roughly linear to PD coupling area.



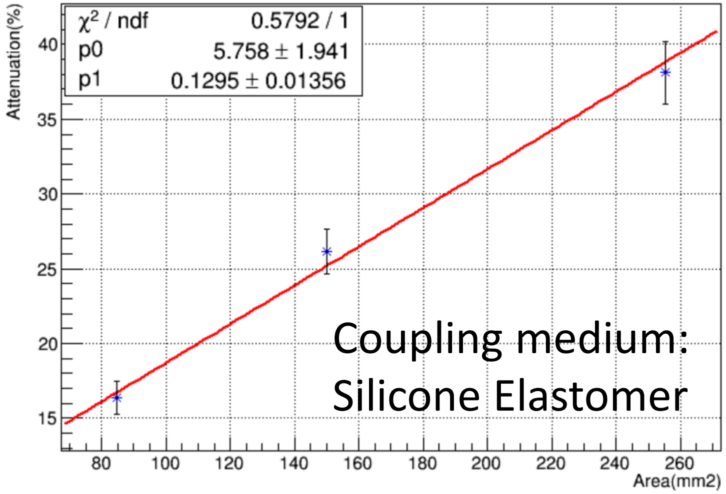
Bottom view of LYSO cube



Test setup

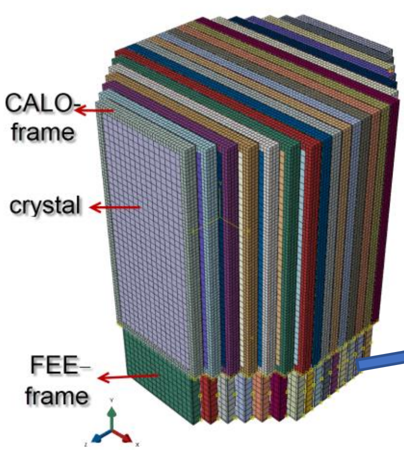


A typical MIP spectrum

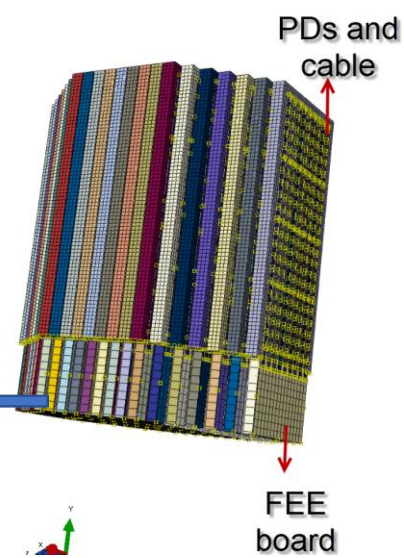


2.3 Thermal analysis of CALO with PDs

- Power consumption for each PD (taking into account cable and components inside CALO)<**4uW**
- TOTAL = $(4{,}33_{\text{HIDRA mW/Ch}} + 2{,}15_{\text{T+ROC2 mW/Ch}} + 0{,}63_{\text{T+ROC1 mW/Ch}}) * 16000\ \text{Ch} \Rightarrow 6{,}61\ _{\text{mW/Ch}} * 16000\ _{\text{Ch}}$ => **114W** (without IO)
- crystals in one layer are simplified to one plate
- Crystal and CF frame are well conducted
- PDs Electronics –PCB+CF frame& PCB+Al frame



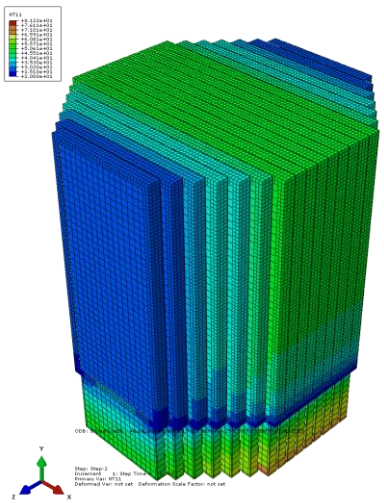
Contain HIDRA2, T+ROC2 and T+ROC1 power consumption



2.3 Thermal analysis

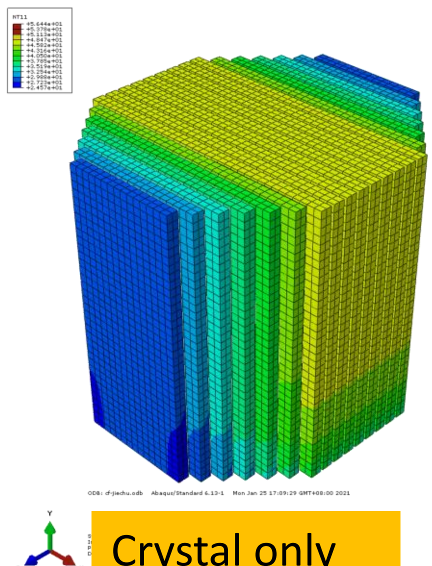
- **No PDs and flat cables**
- CALO frame and PDs electronics frame conductance : 0.2(mW/mm2K)
- Boundary conditions on the bottom edge of crystal array :20℃

CF-frame



Whole model

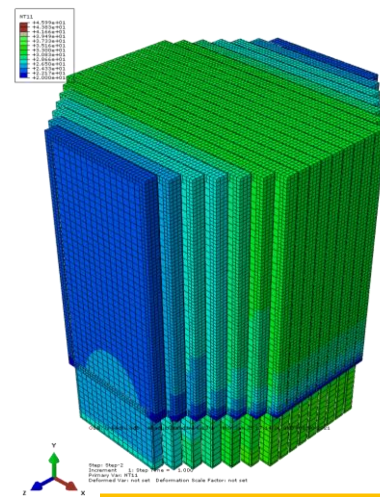
Maximum temperature:81 ℃



Crystal only

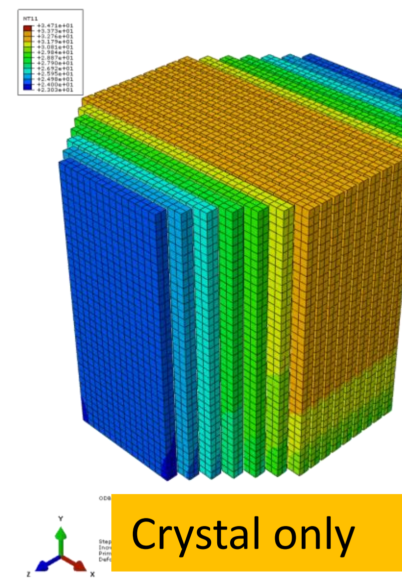
25~56 ℃

Al-frame



Whole model

Maximum temperature:46℃



Crystal only

23~35 ℃

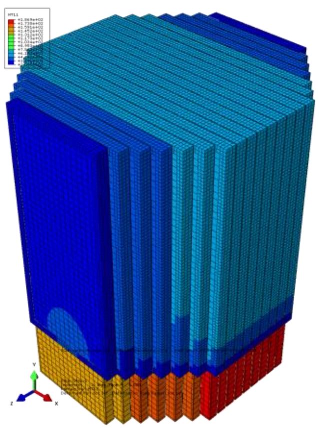
Al-frame have a better dissipation than CF-frame

2.3 Thermal analysis

- **With PDs; Al PDs Electronics frame**
- CALO frame and electronic frame- thermal insulation
- Boundary conditions on the bottom edge of crystal array :20℃
- PD cable and electronic board conductance : 0.2(mW/mm2K)

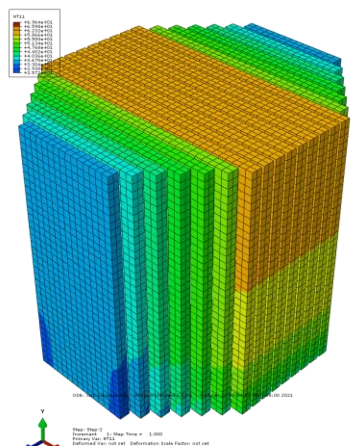
It may be necessary to implement heat dissipation for PDs electronics

No heat dissipating plate(20 ℃)



Whole model

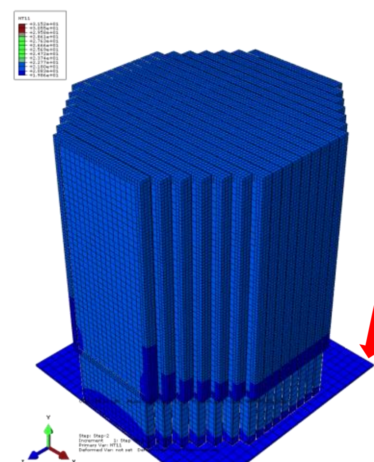
Maximum temperature:187 ℃



Crystal only

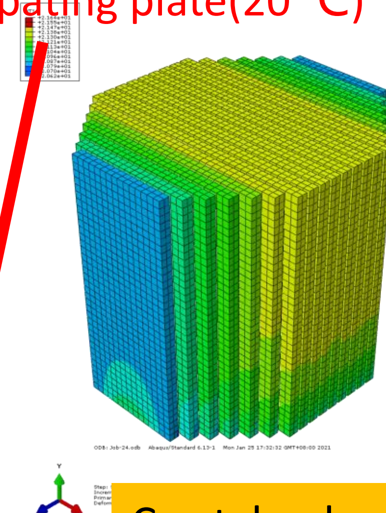
26~69 ℃

Add heat dissipating plate(20 ℃)



Whole model

Maximum temperature:32 ℃

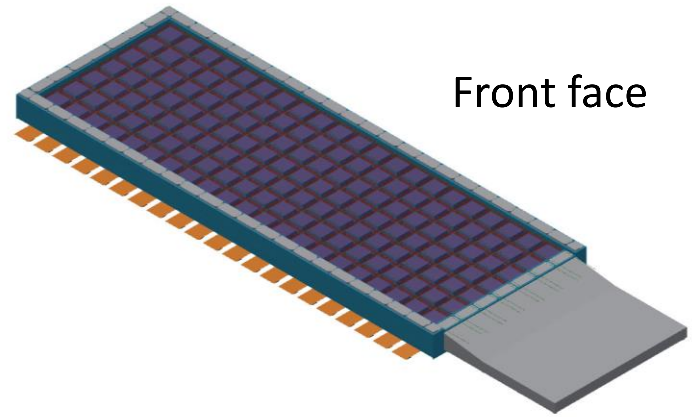


Crystal only

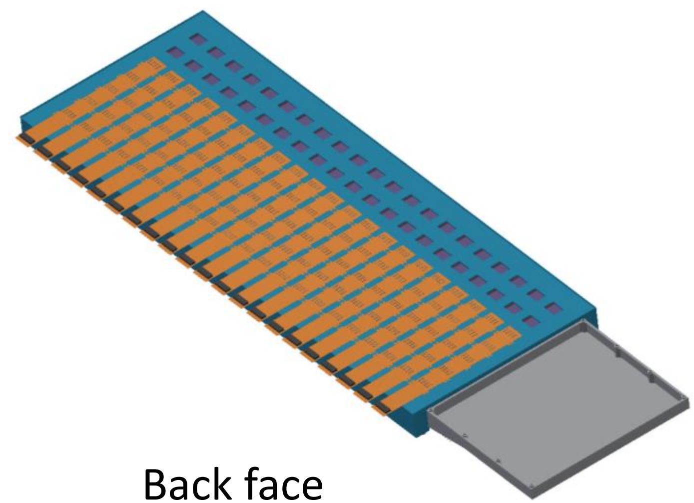
20~22 ℃

3. CALO crystal array prototype

- ➢ structure
- Structure for crystal array: 7*7*21
- **Crystal array: 5*5*21 (extendable to 7*7*21)**
- Gap between crystals:4mm\4mm\8mm
- ➢ Dual-readout cubes plan
- **PD coupled to bottom face of crystals**(3 columns of middle layer,3*21=63)
- **PD cable layout is perpendicular to WLSF**
- Dual-readout cubes will be wrapped in IHEP without WLS fibers
- Attaching the PDs and small cables in Florence.
- Connections between PDs and cables in IHEP.



Front face



Back face

Summary

- Two new candidates of WLSF chip were measured, the intensity output were higher than old version
- An AIT prototype and a small vibration plate were made for AIT verification and vibration test individually
- WLSF arrangement and PDs flat cable layout were taken into account
- Thermal analysis of CALO with PDs system was carried out
- Development plan of CALO crystal array prototype was considered preliminarily

➢ to do next,

- More detail measurement & study of WLSF read-out
- Construction of new CALO prototype by using new WLSF chip design
- Realization of stable calibration light source
- FIBER routing implementation on the AIT prototype

Thanks！