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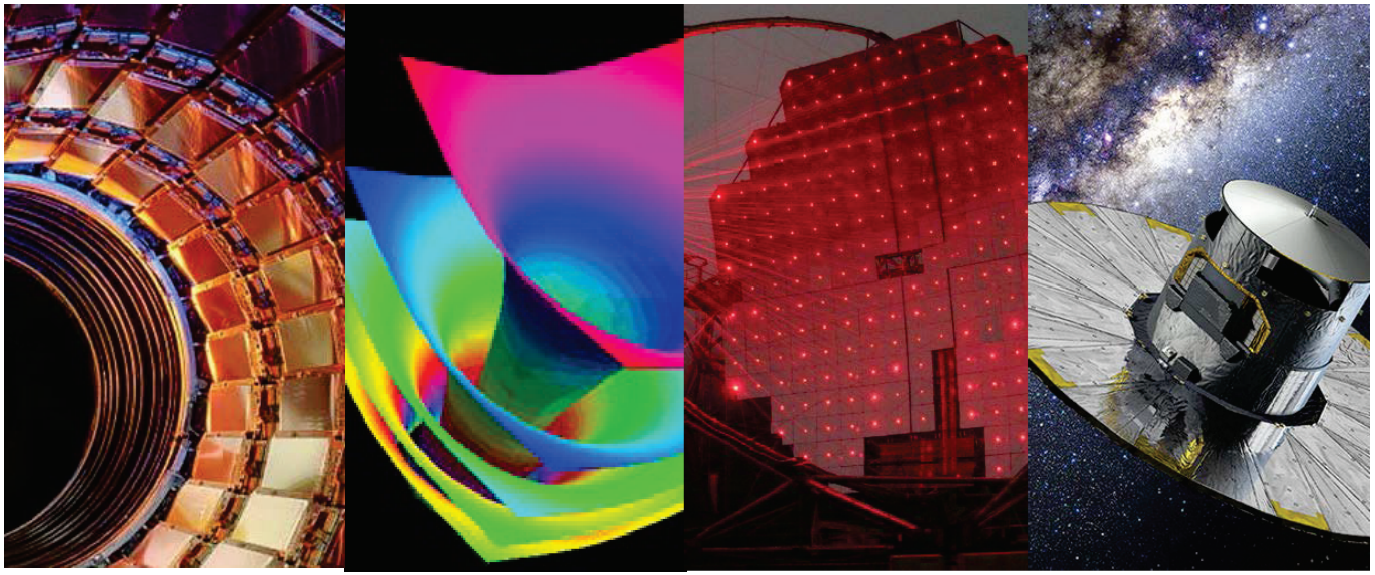

HERD – BETA ASIC status

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HERD 9th international workshop

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UNIVERSITAT DE BARCELONA

HERD - β Architecture Block Diagram

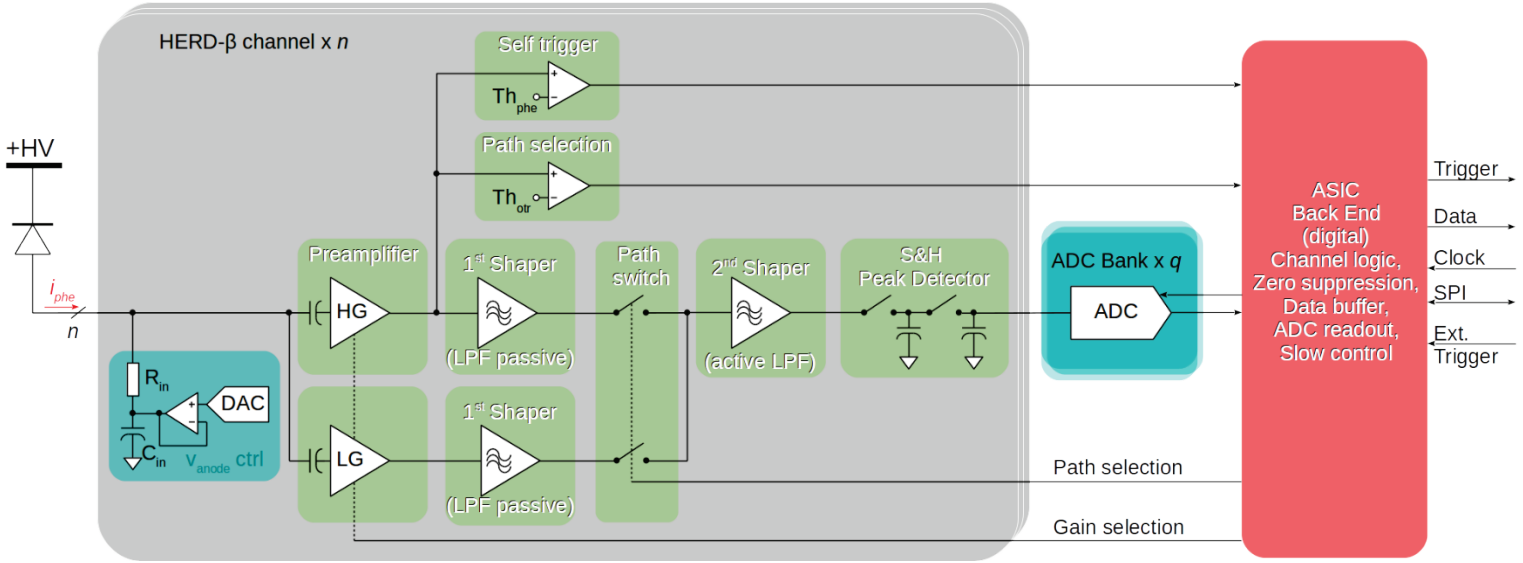


Fig 1: HERD-β Architecture initial block diagram

HERD-β Architecture Specifications:

- ✓ Channels: 64 or 128
- ✓ Input rate : 1 KHz max
- ✓ Power Budget : < 0.4 mW/ch
- ✓ SNR* for calibration : > 10
- ✓ Slow Digital Control : I2C
- ✓ Dynamic Range : 676 MIP
- ✓ SiPM Firing cells :3800
- ✓ Radiation Hardness : 80 Gray

***SNR : is defined as the signal of 1 firing cell divided by the total integrated noise**

HERD - β Architecture Block Diagram

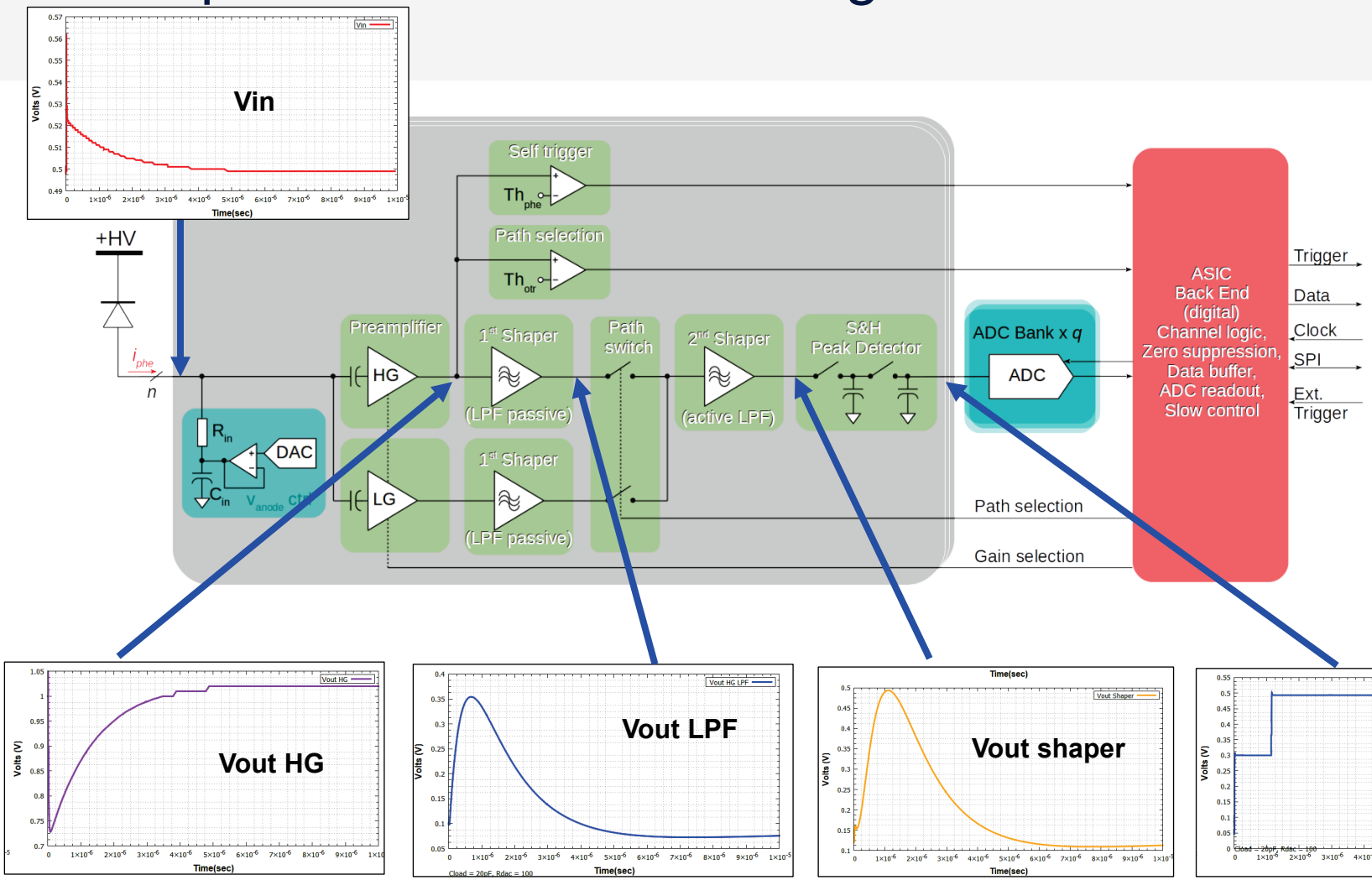


Fig 2: HERD-β Architecture time response simulation

HERD - β Architecture Block Diagram

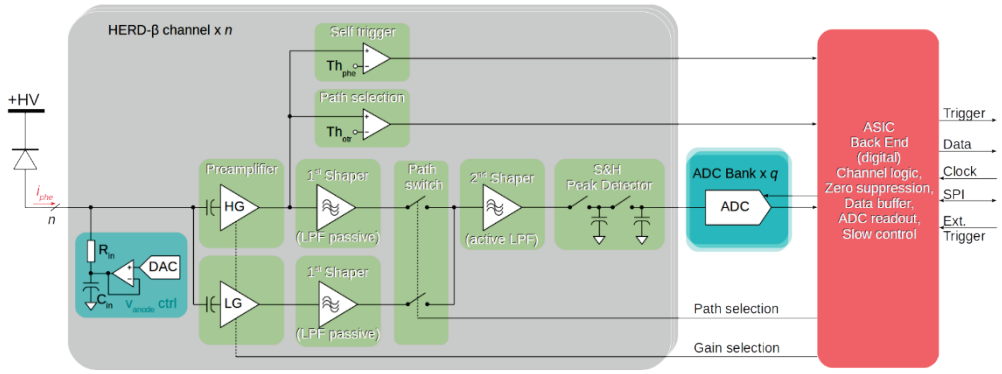


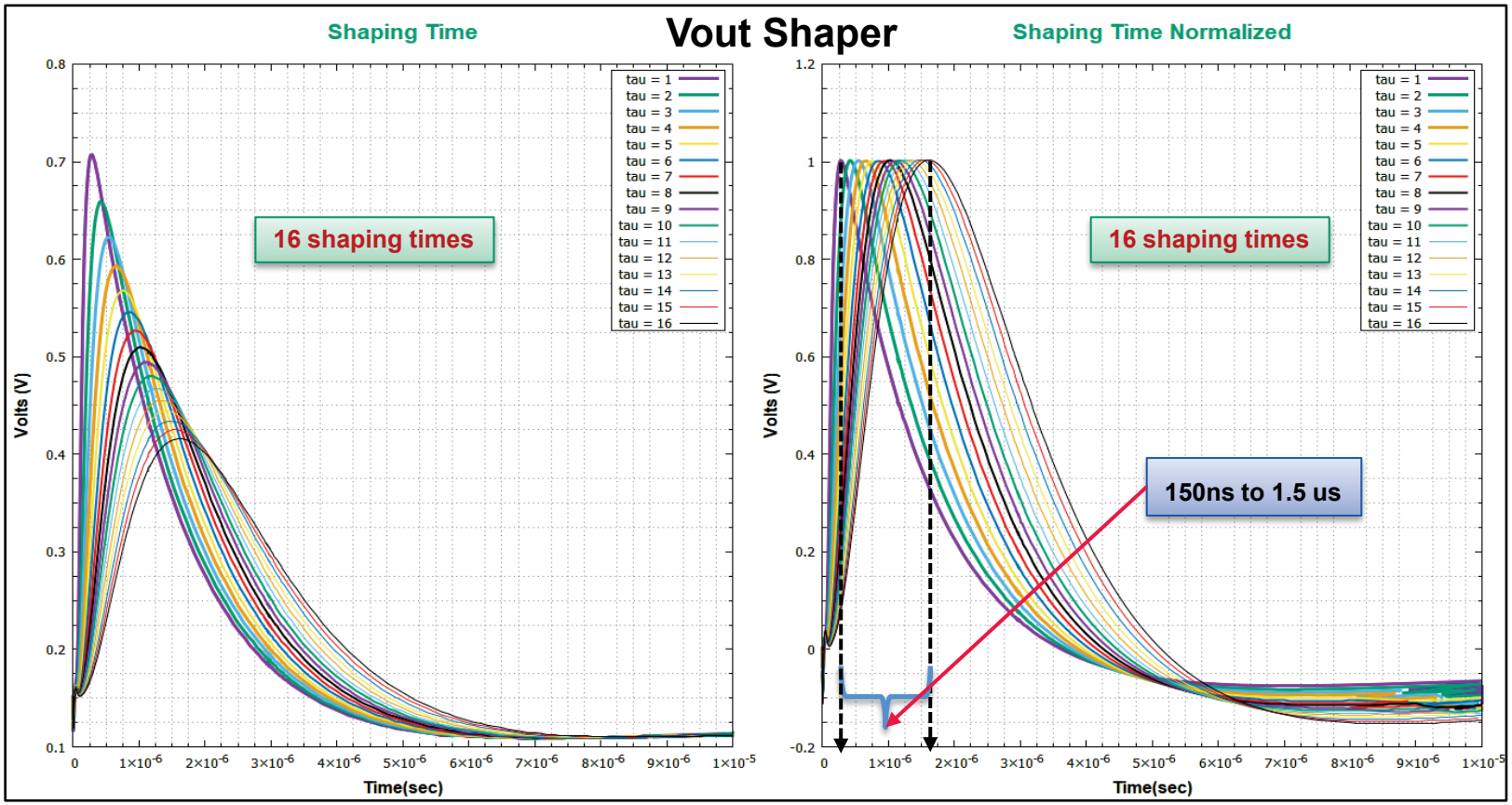
Fig : HERD-β Architecture initial block diagram

Classical voltage mode readout approach:

- **Best noise performance**
- Best with short signals
  - Long tails: pile-up!
  - **Need to discharge Cf**
- Best with small capacitance
  - BW=Cf/Cdet*GBW, with Cf<<Cdet typically…

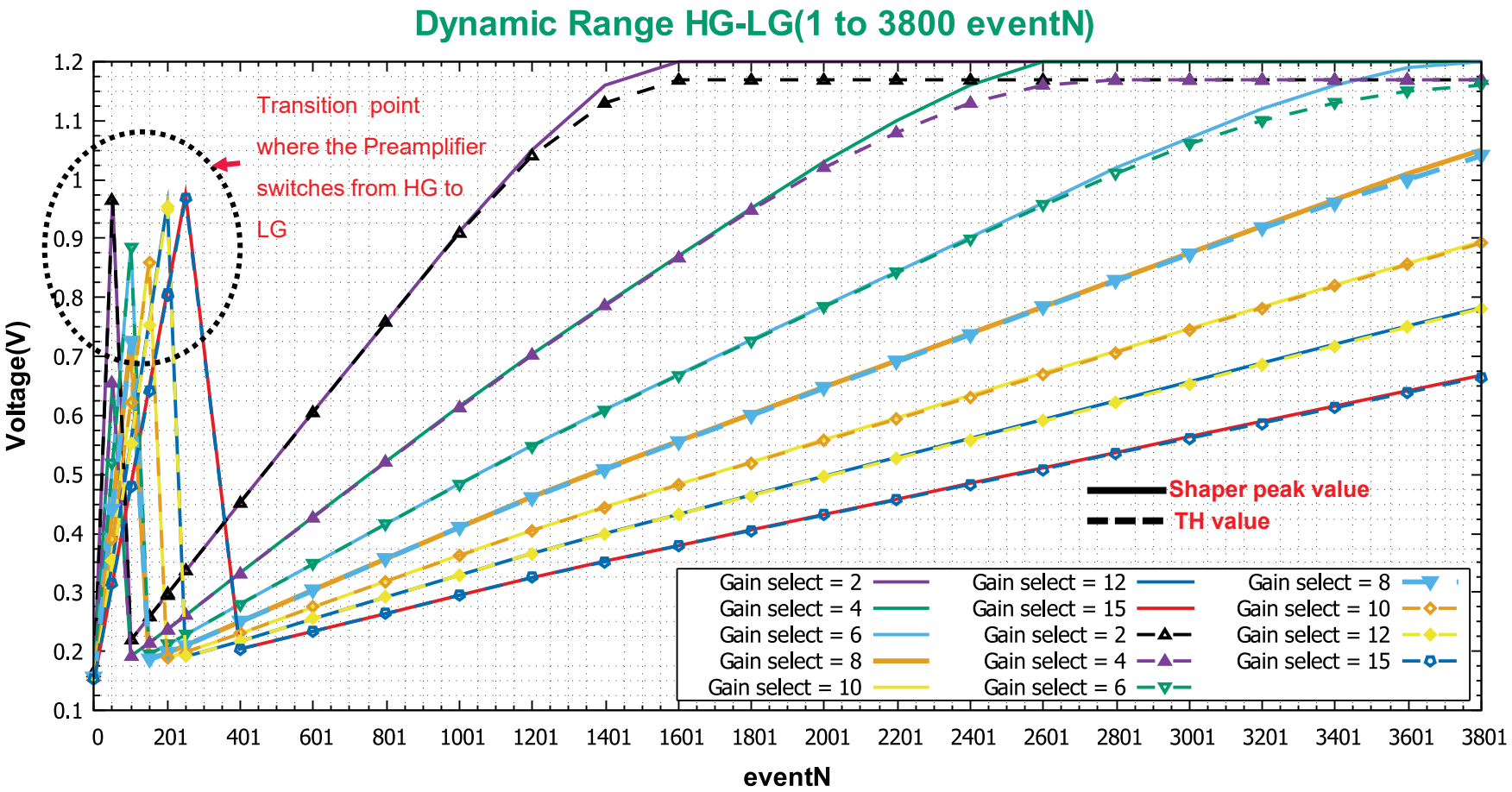
- Preamplifier Block
  - AC coupled with a pair of adjustable High gain(HG) & Low gain(LG) capacitive feedback amplifiers
- Slow Shaper Block
  - A noise shaping section for noise filtering composed of 1st order passive low pass filter and 2nd order active low pass filter .
- Peak Detector/ Sample Hold
  - To sample the shaper output peak signal for digital data acquisition.
- Two threshold discriminator for TRIGGER & path selection
- A DAC is added at the input of the preamplifier to allow fine adjustments of the bias voltage of the detector.

Shaping time - Transient Response



- Butterworth filters provides a roll off of -20 dB/decade/order
- Total 16 shaping times (from ~150 ns to ~ 1.5 µs) are available for these slow shapers

Dynamic Range – Front End



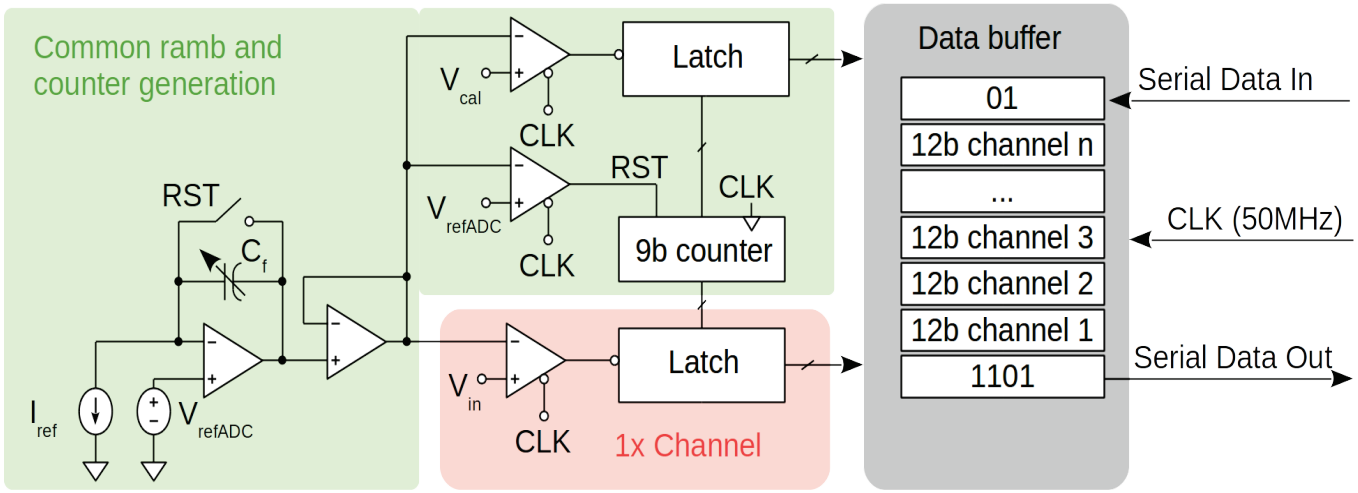
- SiPM EventN from 1-300 in HG configuration depending on the gain selection of High gain preamplifier
- SiPM EventN from 50-3750 in LG configuration depending on the gain selection of High gain preamplifier

Analog Specification Summary

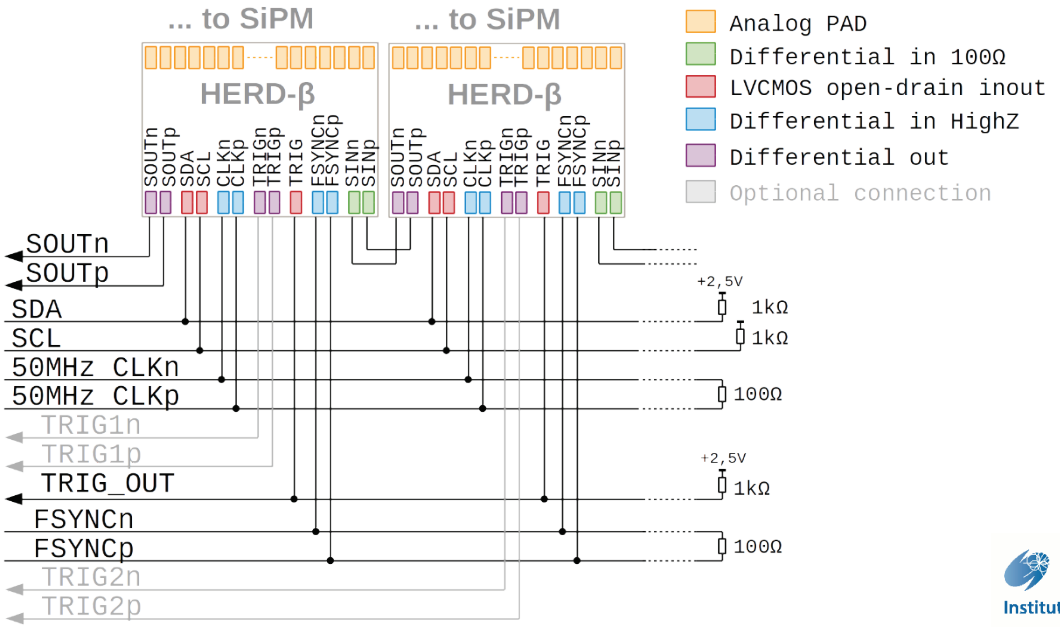
No.	Parameters		Specification	
1	Power / Channel		**686 µW** + Common Bias Block + Digital Block	
2	SNR(1 pe)		13.3(RMS intg. Noise) & 15.5 (Transient Noise)	
3	Preamplifier Variable Gain	High Gain	2 to 18	16 configuration (4 bit control)
		Low Gain	0.1 to 1.1	
4	Shaping time(τ)		150 ns to 1.5 µs	
6	Dynamic Range **(35.15 fC to 132 pC)** (A total Dynamic range from 4000 pe to 0.1 pe)		1 to 300 (High Gain) (LSB = 0.097 pe) 200 to 3800 (Low Gain) (LSB = 1.85 pe)	
7	Rate of Operation (Recovery rate from peak value within 1mV DC base line)		10 kHz	Nominal (Rf = 10 MΩ)
			100 kHz	Bipolar Shaper (Rf = 1 MΩ)+ Gated Restorer
8	Linearity Error	High Gain	< 0.8%	
		Low Gain	< 1.1%	200- 2000 cells (pe)
			~ 1.2% to 3%	2000 – 3800 cells (pe)

ADC and interfaces

- Wilkinson ADC
  - < 50 uW/ch

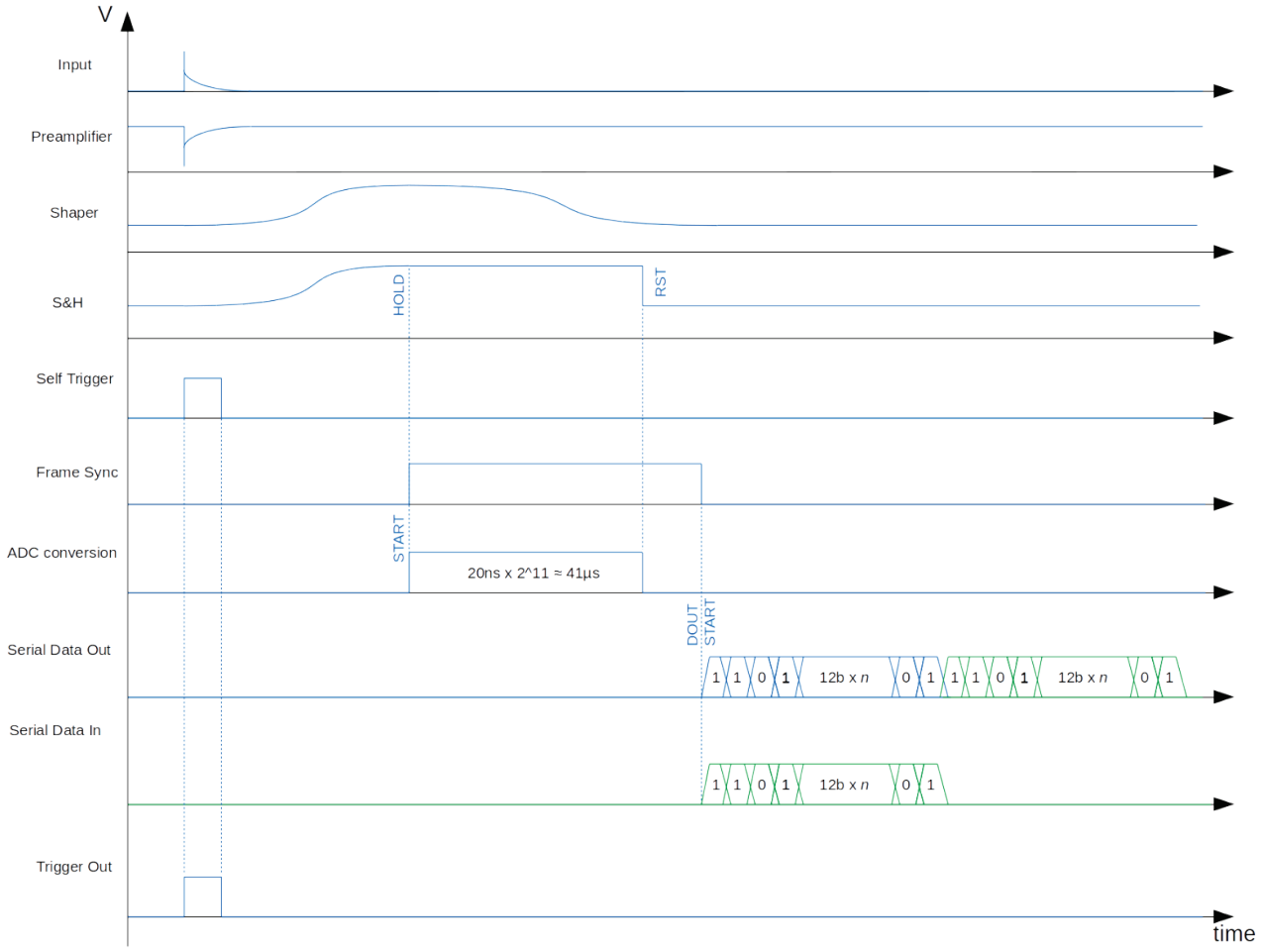


- Interfaces



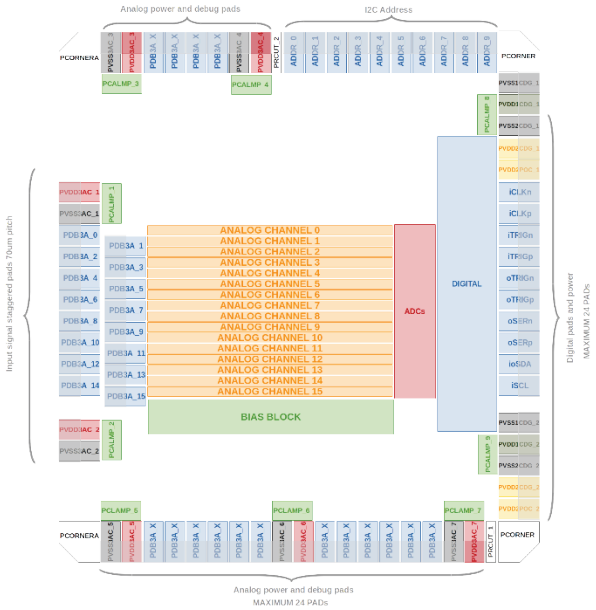
Readout sequence

- Default mode:
  - “Frame Sync” rise from detector trigger

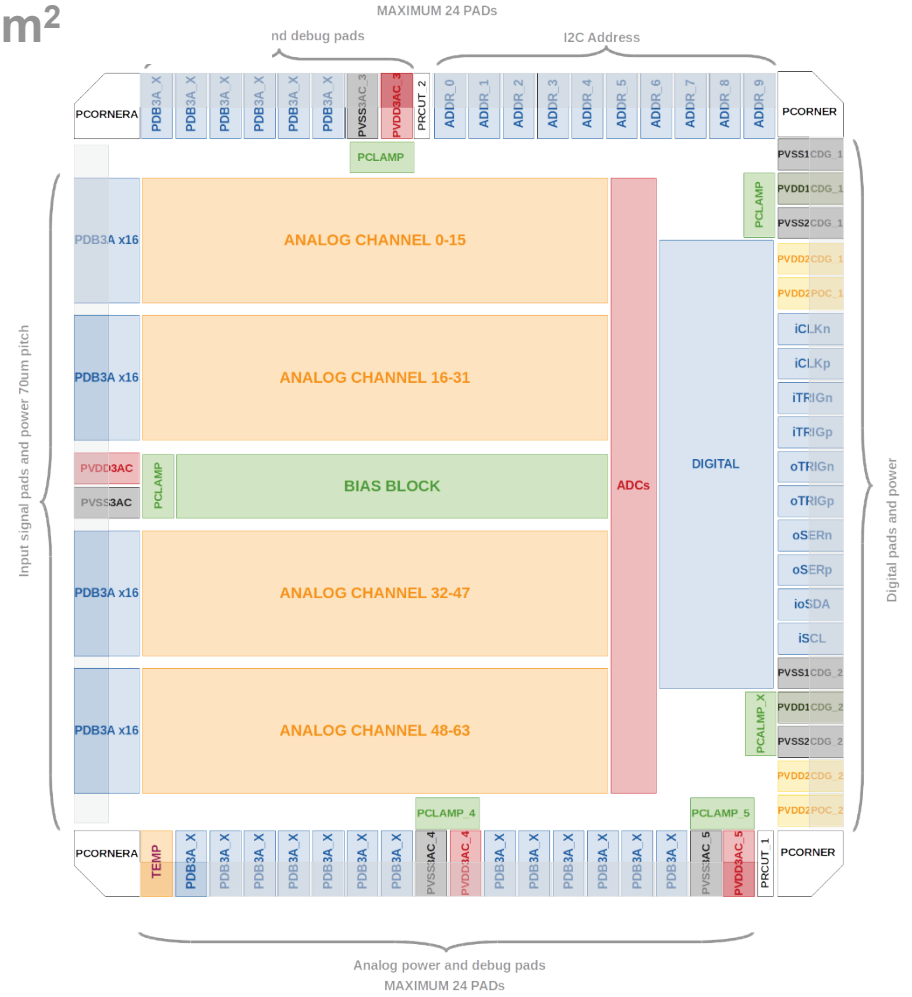


Floorplan

HERD 16 ch proto
2x3 mm²



HERD 64 ch final
5x3 mm²



- Full functionality and final readout
- To be submitted in April

Backup Slides

Block Diagram – DAC controlled SiPM bias Voltage

Due to the gain sensitivity of silicon photomultipliers to temperature and bias voltage variations

- A DAC has been added at the preamplifier input to tune the input DC voltage in order to adjust individually the SiPM high voltage (V_{anode})

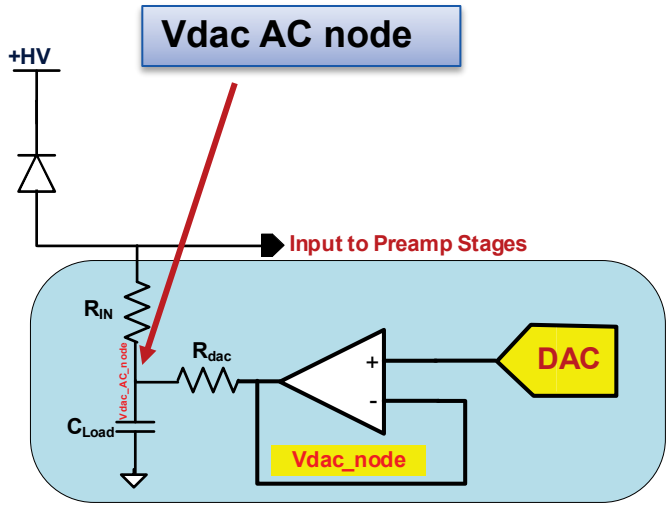


Fig 3: Block diagram of DAC controlled SiPM bias Voltage

- RIN : The input impedance of the front-end amplifier
- C_{Load} : Decoupling capacitance
- Rdac : The DAC resistor value and this value needs to be sufficiently higher to avoid any current entering the DAC part.