

Progress of the CEPC SDHCAL

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饮水思源•爱国荣校



Outline

Why highly granularity calorimeter needed?

- Introduction of SDHCAL technological prototype
- Glass RPC production and cosmic ray test
- Progress of SDHCAL based on RWELL
- Timing electronics design of 5D T-SDHCAL
- Summary and future plan



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Why high granularity calorimeter?

- ~70% of Higgs directly decay to a pair of Jets
- ~20% of Higgs indirectly decay to jets
- ~70% of heavy boson (W, Z) decay to hadronic final states
- Second CEPC as a "Higgs Factory" => Jet Energy Resolution is important.









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Calorimeter based on PFA

In the second second



Introduction of SDHCAL prototype

- Semi-Digital Hadronic CALorimeter technological prototype (SDHCAL)
- Igh granularity calorimeter based on Glass RPC (cell size 1cm × 1cm)
- Hits associated to three thresholds:
 - 1st threshold = 110fC
 - 2nd threshold = 5pC
 - 3rd threshold = 15pC
- 48 layers with GRPC as sensitive medium
- \rightarrow Dimensions: $1m \times 1m \times 1.3m$
- \otimes 6 Interaction length ($6\lambda_I$)
- Test beam at CERN since 2012







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Glass RPC production

See Francois Lagarde's talk

SJTU group built 50cm x 35cm, 100cm x 100cm RPCs







Cosmic rays test





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SDHCAL based on RWELL



MPGD : Micro-Pattern Gas Detector.
 Typical detectors: GEM, THGEM...

Daojin Hong, Jianbei Liu

- RWELL : compact & simple structure
 - Only a drift gap
 - Only one stage amplification, high gain
 - Resistive layer-DLC





RWELL detector fabrication

Daojin Hong, Jianbei Liu



RWELL detector performance

Daojin Hong, Jianbei Liu

Gain of different zones vs Voltage on film





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Motivation using timing information

Timing could be an important factor to identify delayed neutron and better reconstruct their energy.





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Timing information

Time information can be very helpful to separate close by showers and reduce the confusion for a better PFA application.

1 ns resolution

100ps resolution



Introduction of PETIROC chip

Time measurement

- Coarse time is from a counter
- Fine time by interpolating 40MHz

Charge measurement

- 32chs input connected
 - with PAD (readout unit)

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• Variable time shaper



Fast timing measurement

- Purpose: => Identify neutral and charged hadrons
 Position, Energy and Timing => 5D HCAL
- Adding MRPC layers in the SDHCAL
- Front-end board for MRPC readout
 - Charge and timing measurement
 - High resolution timing measurement





✓ First step:
 Design a front-end prototype board
 with four PETIROC2B chips

Second step:
Build the 1m×1m PETIROC2B FEE



Prototype of timing electronics

- The FEE prototype includes four PETIROC chips, 128 readout pads at the PCB bottom side.
- **Detector Interface(DIF)** card was designed to connect FEB and FPGA board ۲
 - Data transmission, power rail and clock source.
- The ethernet (TCP/IP) is used to transfer data between FPGA and PC. ۲





Hardware of prototype







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Test system and setup

The test platform has been setup.

- The system includes
 - FEB, DIF card, DAQ system
- Status of the platform:
 - Configuration of PETIROC chips
 - Data transmission between PETIROC, ZCU102 and PC with ethernet port
 - Performance test of PETIROC chips, such as timing measurement





PETIROC chips configuration

- 648 bits data with SPI method is sent to Shift **Register inside PETIROC.**
 - All bias voltage values are correct.
- PETIROC chips can be successfully configured through the Xilinx ZCU102 platform.





zcu102.xdc

Bias Voltage	Value(V)
vref_inpdac	0.989
vref_time	1.664
vref_charge	0.976
vref_tdc	0.133
vref_adc	0.961
vref_time_pad	1.658



Timing Diagram of configuration

Data acquisition system design

- DAQ system is based on Xilinx ZCU102(FPGA) that contains Processing System (PS) and Programmable Logic (PL).
- Embedded design (SDK) in ZCU102 (PS) is applied
 - The UART communication of FPGA and PC
 - Ethernet communication between ZCU102 (PS) and PC used to transfer data
 - Data transmission with AXI Bus between PS and PL, inside of ZCU102



Embedded design based on FPGA -- UART

- The embedded design in ZCU102(PS side) contains:
 - Serial port communication (UART)
 - Ethernet communication (TCP/IP)
- WART test in PS side:
 - Processing System part on ZCU102.
 - UART communication through C/C++ program
- WART can successfully communicate with FPGA and PC.



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UART communication test

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Embedded design based on FPGA -- Ethernet

- Ethernet communication test
 - Processing system sent the data to PC.
 - UART used to print processing system information (IP, Sub netmask, Gateway).
 - Ethernet port connected with PC, used for data transmission.
 - Capture package tool can grab the transmit information.

SCU102(PS) and PC can successfully communicate over ethernet.

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	365 124.045669	192.168.1.2	192.1 Destination	address	54 7 → 52432	[ACK] Seq=1	Ack=12751 W	n=64356 Le	n=0	
	366 125.001710	192.168.1.10	192.108.1.2	ECHO	156 Request					
	367 125.049194	192.168.1.2	192.168.1.10	TCP	54 7 → 52432	[ACK] Seq=1	Ack=12853 W	n=64254 Le	n=0	
	368 126.001727	192.168.1.10	192.168.1.2	ECHO	156 Request					
	369 126.056491	192.168.1.2	192.168.1.10	TCP	54 7 → 52432	[ACK] Seq=1	Ack=12955 W	n=64152 Le	n=0	
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Design of DAQ system

- DAQ system based on the ethernet transmission between FEB, ZCU102 and PC has been completed.
- Data from FEB can be taken in PC side and decoded with python scripts.
- The configuration of PETIROC chips over ethernet will be included.
- Signal injection test will be performed in the future.



Summary and future plan

Summary:

- \checkmark 100cm \times 50cm RWELL was assembled and tested at USTC.
- ✓ Larger GRPCs have been designed and fabricated at SJTU lab.
- The timing electronics have been designed and manufactured.
- Test platform and setup for PETIROC have been constructed.
- ✓ PETIROC chips can be successfully configured.
- DAQ system based on ethernet transmission has been completed.

Future Plan:

- \circledast Test the performance of larger GRPC (1m \times 1m) with cosmic ray.
- Improve the design of DAQ system over the ethernet communication and add the function of configuration for PETIROC.
- Perform the signal injection test for PETIROC FE board (Timing and Charge).



Thanks for your attention!





Backup Slides



Why high granularity calorimeter?

Future collider has been proposed







CEPC Ring length ~ 100km

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Glass Resistive Plate Chamber(GRPC)







GRPC production

Cosmic ray test system for GRPC





Test System and Setup



Sub-component Design and Testing

Front-End readout Board Design with pads and four petiroc2b



Sub-component Design and Testing

- Detector Interface Card Design: mainly jitter cleaner and power system
- IF card will be in charge of the communication and data transfer with the FE electronics(two headers) and ZCU102(two FMCs).
 More Details
- Analog and digital power are separated.

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2th Version