中国科学院高能物理研究所
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Study of the HVCMOS detector

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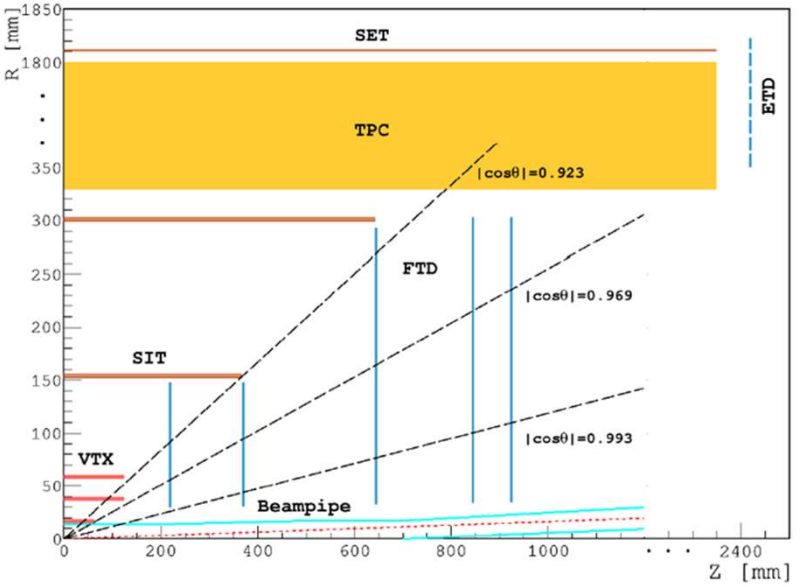
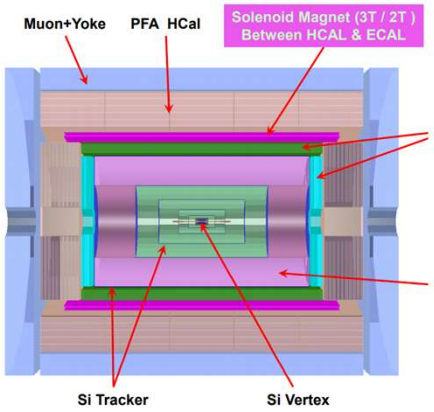
Content

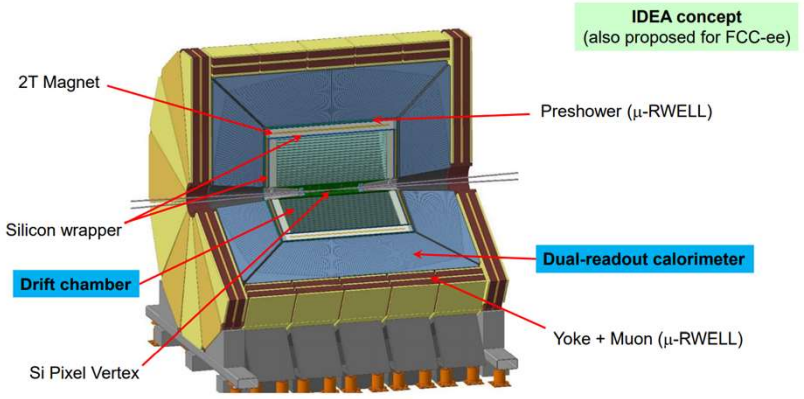
- Background: CEPC silicon tracker
- High Voltage CMOS detector
- A HV CMOS Chip:AtlasPIX3
- Test System: hardware and software
- Test Procedure: Test in the lab
- Radioactive Source Test
- Application: Test with beam
- Future Plan: Multi-Chip Module

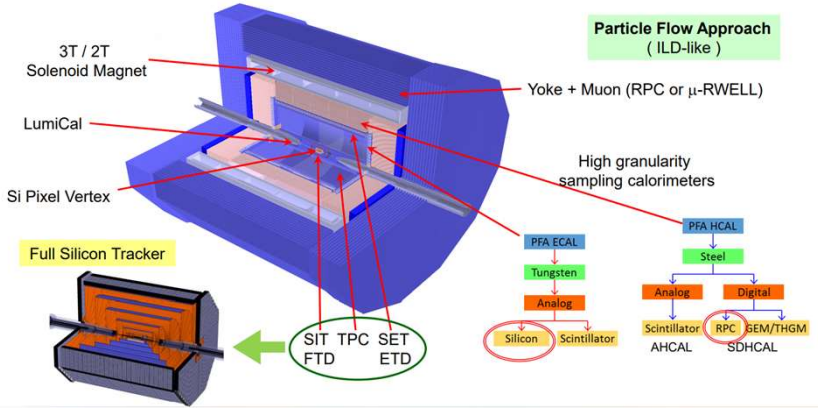
Background

- CEPC Tracker:
  - outside of the VTX
  - TPC/DC + silicon or all-silicon concepts



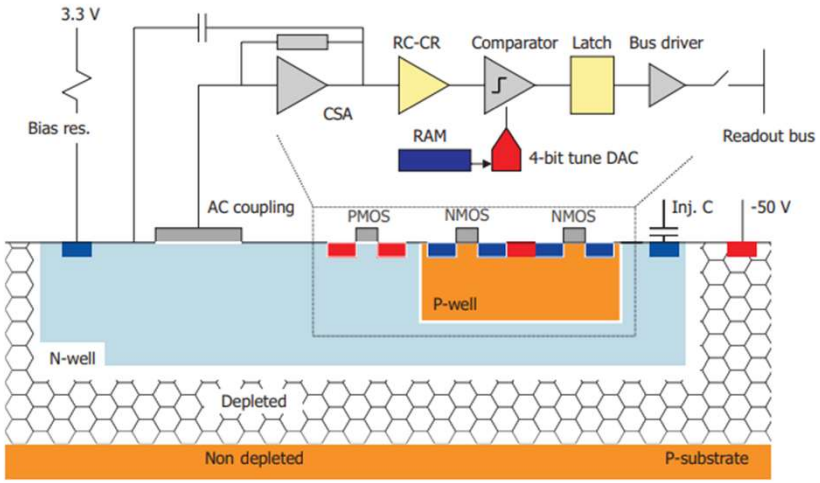


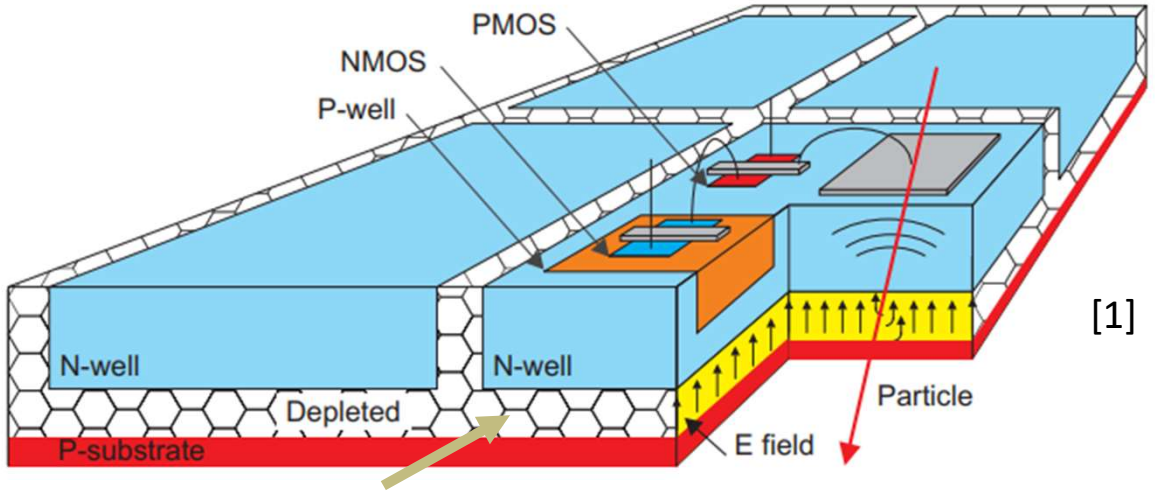




HV CMOS detector

- Detection based on the charge drift in the depleted zone of the reverse biased diode.
- Depleted zone thickness about 10μm(60V)
- Depleted area one magnitude lager than LV CMOS





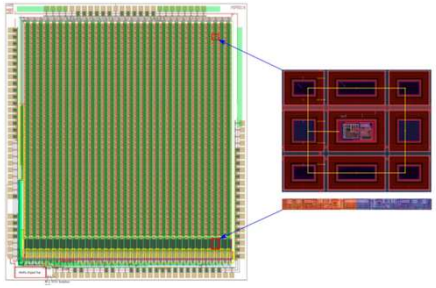
[1]

About 10 μm

Features of HVCMOS

- Good performance on efficiency(99.5%)
- Low noise(lower than 1Hz threshold above 50mV)
- Good time resolution(lower than 10ns)
- Fast charge collection
- Good radiation tolerance(High efficiency >98% at up to $2 \times 10^{15} n_{eq}/cm^2$)

Examples



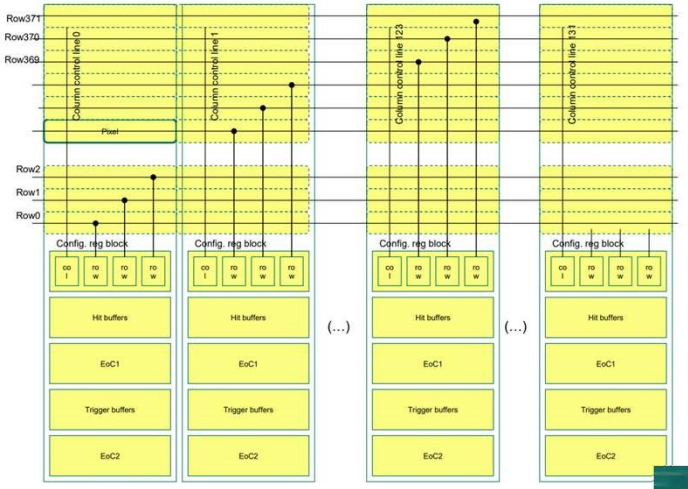
MuPIX7

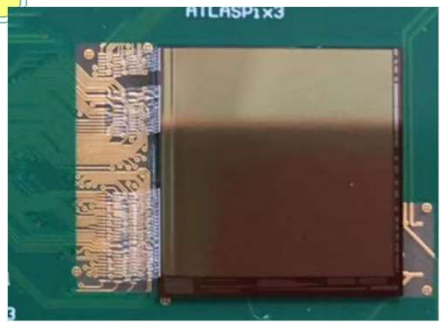
ATLASPIX3

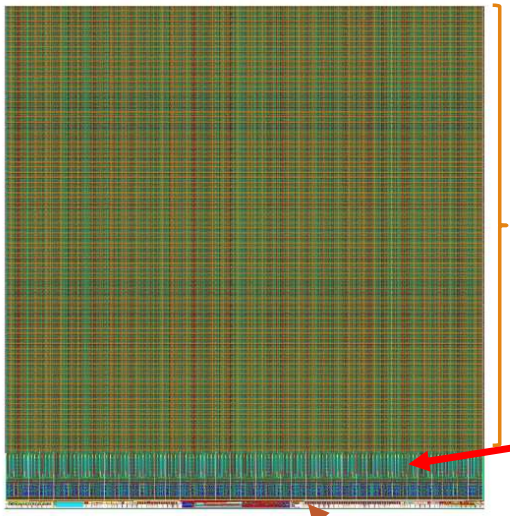
ATLASPIX3

- 372col×132row
- 150×50μm per pixel
- About 2cm×2cm in total
- TSI 180 nm process on 200 Ω cm substrate
- High efficiency 99.5%
- High radiation tolerance

(High efficiency >98% at up to $2 \times 10^{15} n_{eq}/cm^2$)





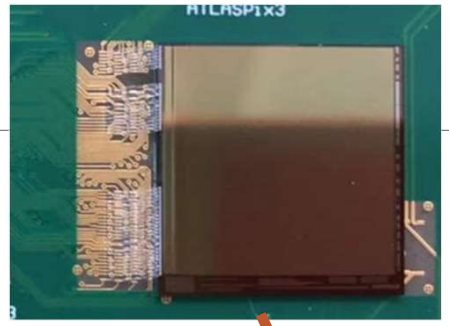


pixels

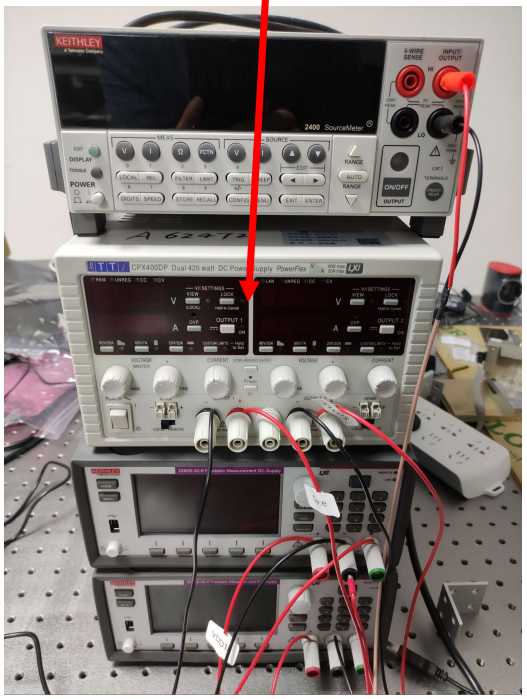
Config register block

Hit buffer, trigger buffer and EoC blocks

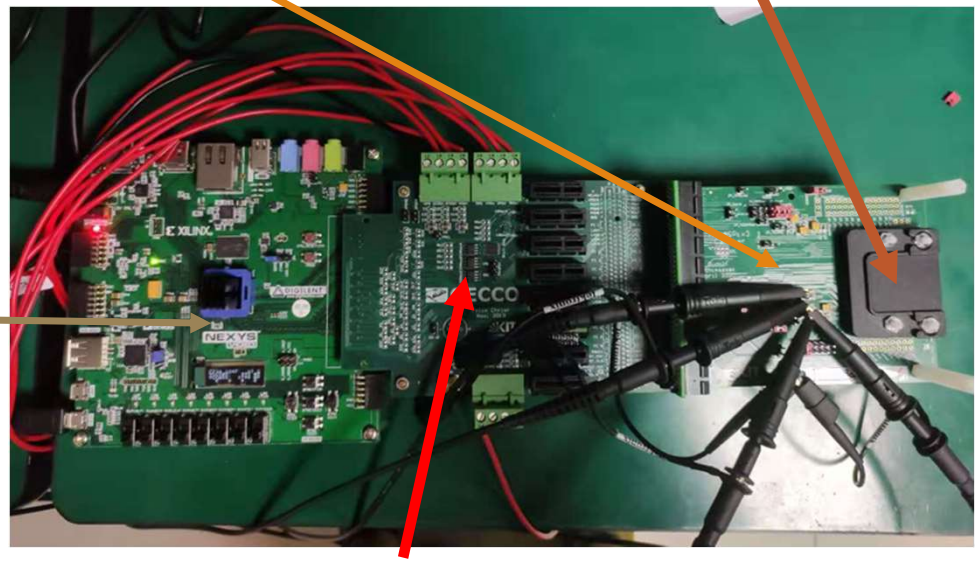
Test System: Hardware



4-Channal Power Supply



Chip Carrier board(KIT)

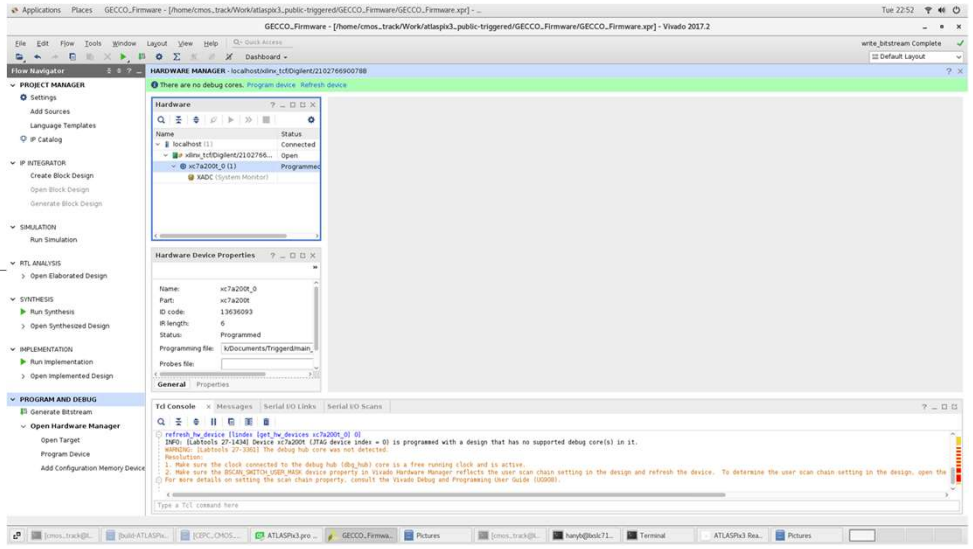


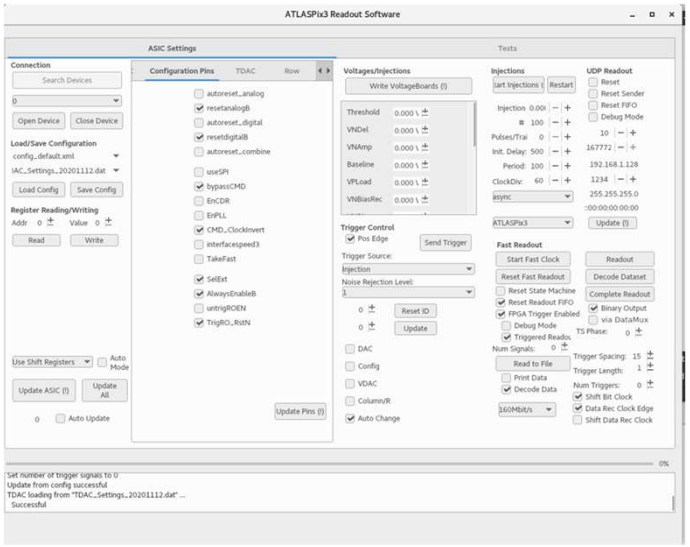
NexysVideo FPGA

GECCO board

Test Software

- Vivado(Configure Firmware)：
  - Compile&Configure Firmware(**Rudolf,KIT)**
- DAQ Software(**Rudolf,KIT**):
  - Connect with the FPGA board
  - Configure Chip registers
  - Fast Readout Test
  - Scan S-curve(Check Threshold)
  - Trimming the chip(Adjust Threshold)

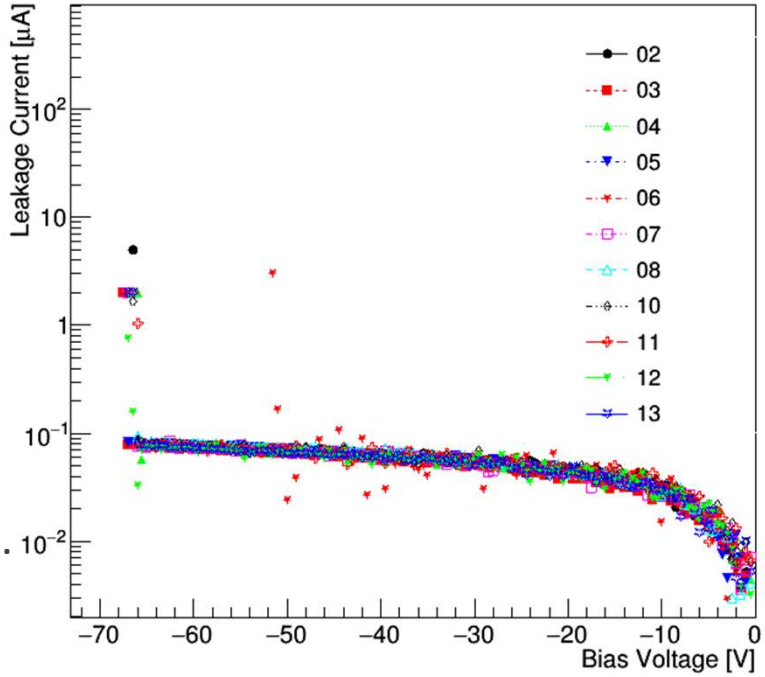




Test in lab: HV Bias Voltage Test

- Change HV Voltage and get an IV curve

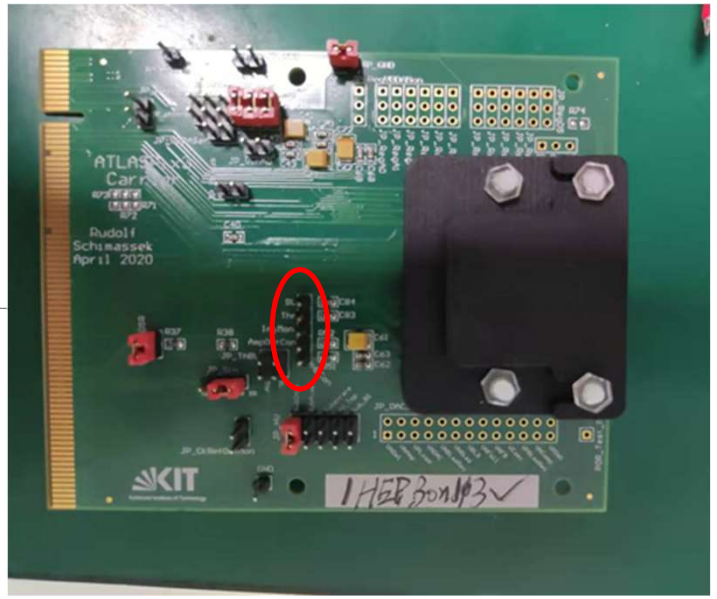
- To check the HV leakage current & Breakdown voltage
  - Break voltage at about -65V
  - Leakage current: about 50nA@-20V at room temperature.

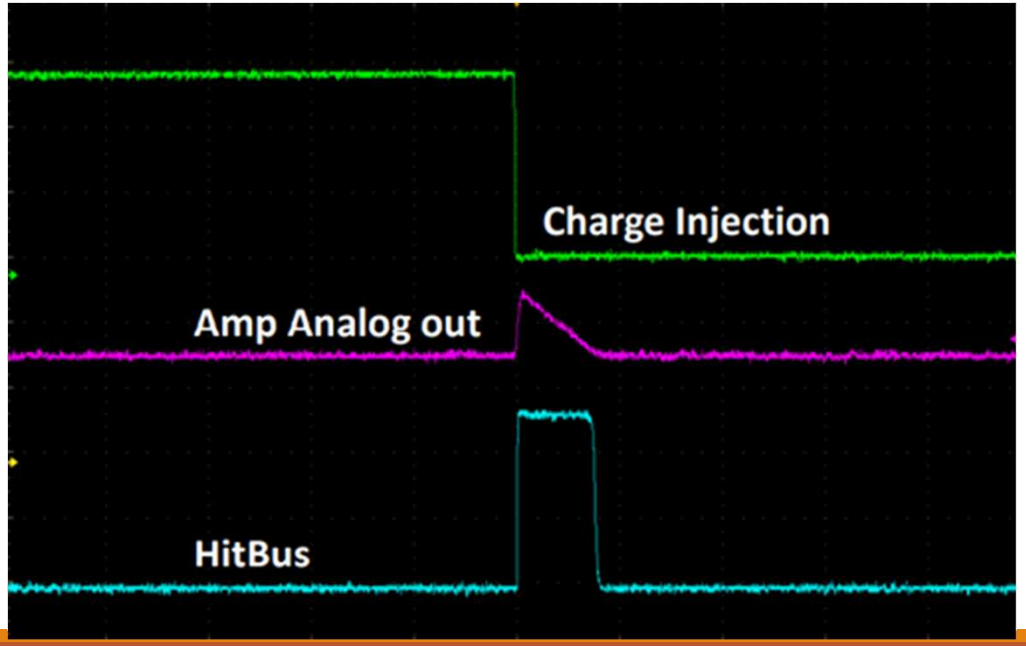


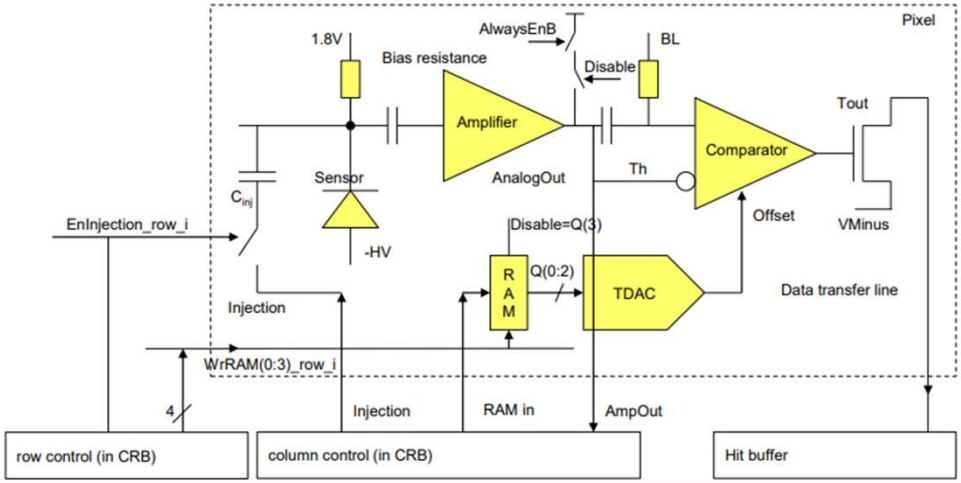
IV curve of several chips

Analog Signal Test

- Use Oscilloscope to measure 5 pins on chip carrier board
- To check and make sure the readout works well







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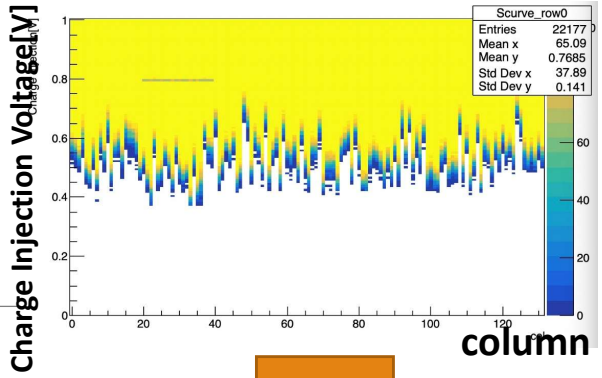
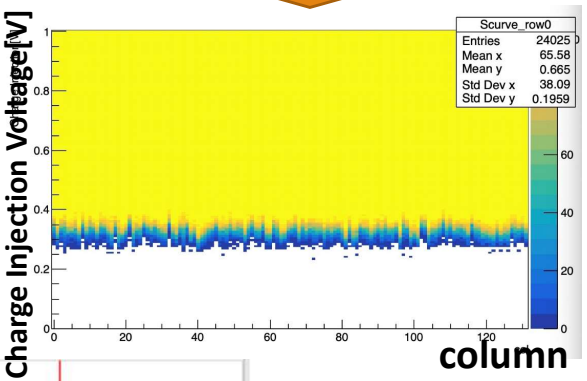
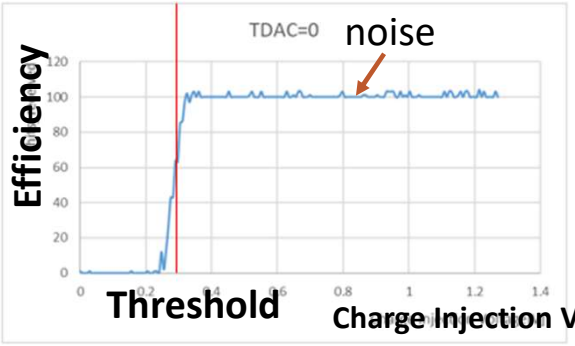
Trimming Test

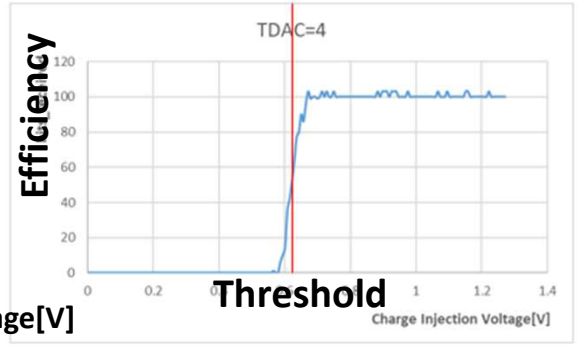
- Threshold : S-curve(Efficiency 0%->100%)
- Trimming Procedure :
  - Measure S-curves of all pixels
  - Threshold distribution
  - TDAC optimization(minimize sigma)
- After trimming, threshold perform similar in different pixels

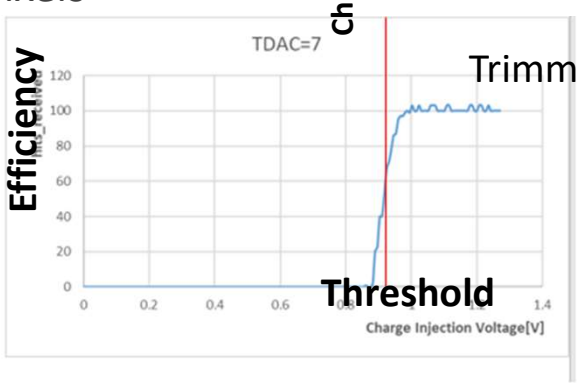




Trimming performance

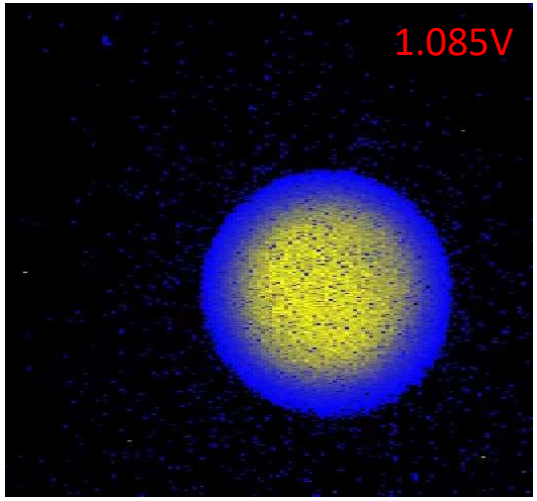




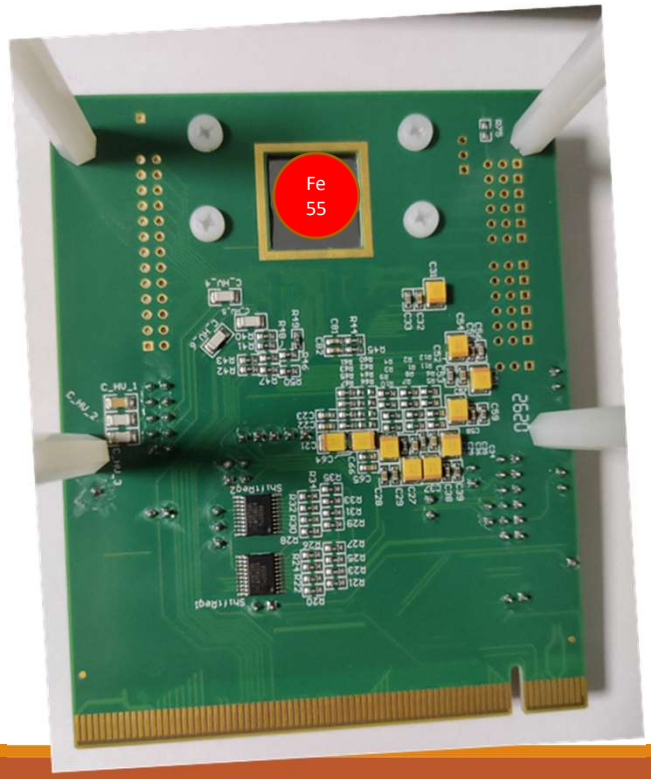


Radioactive Source Test: Fe55 (5.9keV EC)

- To calibrate the Threshold with Energy
- Tape the source at the back side of the chip(with collimation)

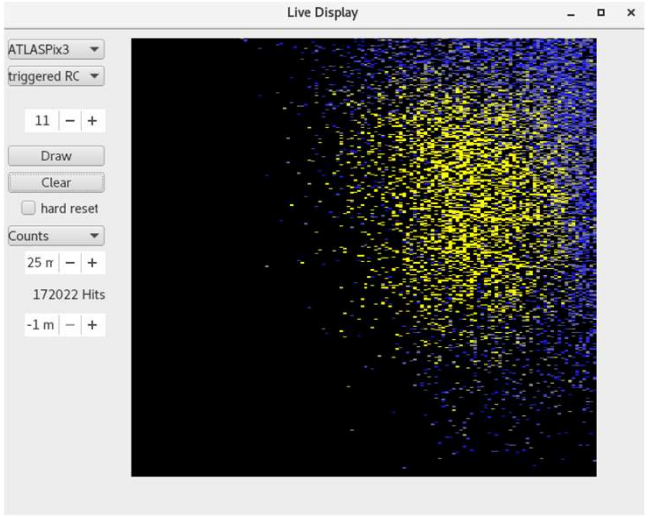


Calibrate the Fe55 5.9keV with threshold 1.085V



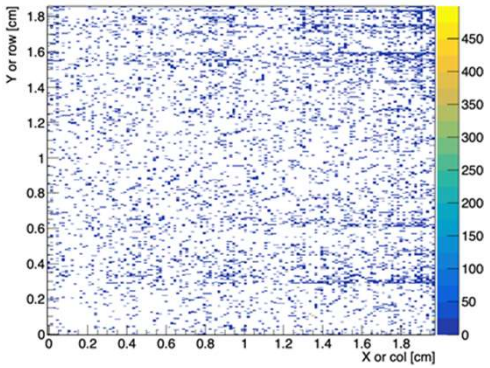
Radioactive Source Test: Sr90 (546keV,β-)

- Can be detected at higher Threshold
- Use a collimation to have a circle shape
- Tape to the back side of the chip
- Read the Hitmap

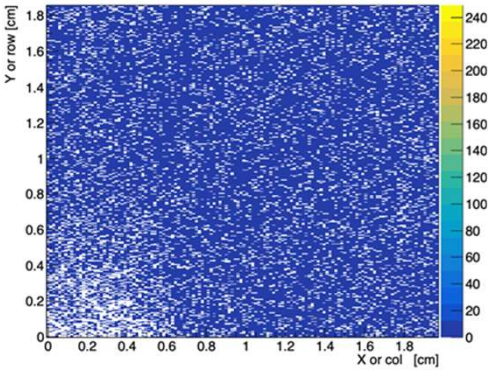


Application :Test with Electron beam

- Detect the Electron and X-ray in the beam
- Electron and X-ray(>6.9keV) can be detected
- When Magnet on, the electron beam will turn

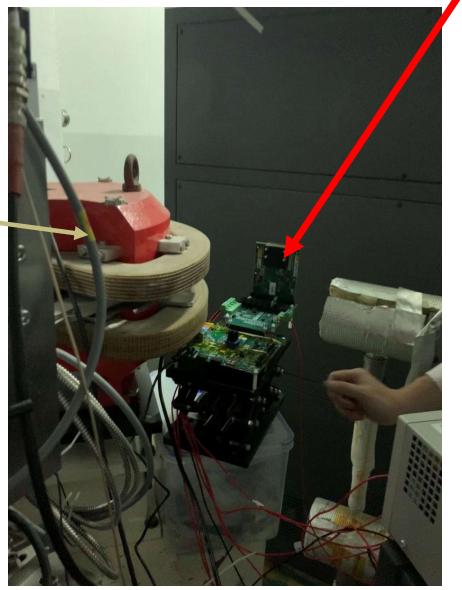


Magnet Off(X-ray)
(Disable electron)



Magnet On(e- and X-ray)
(Enable electron)

Beam direction



- When Magnet off, there are still hits, which are recognized as X-ray.

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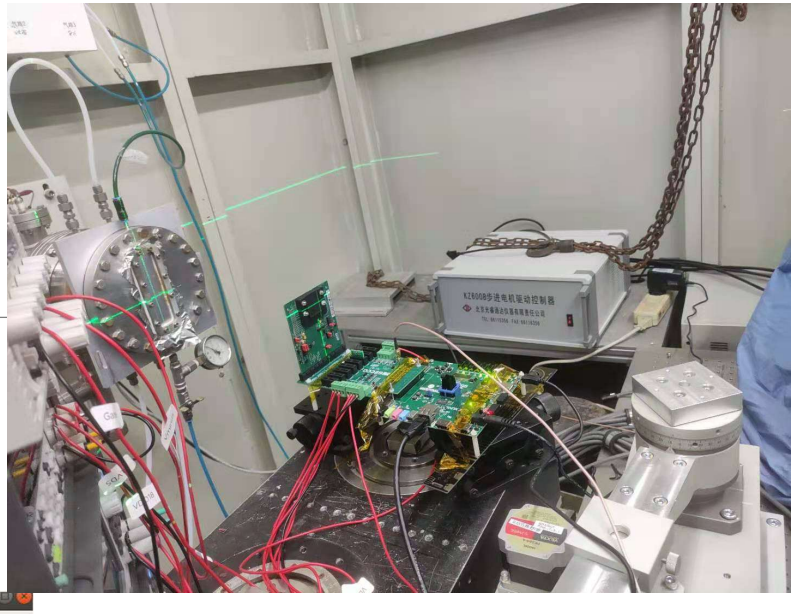
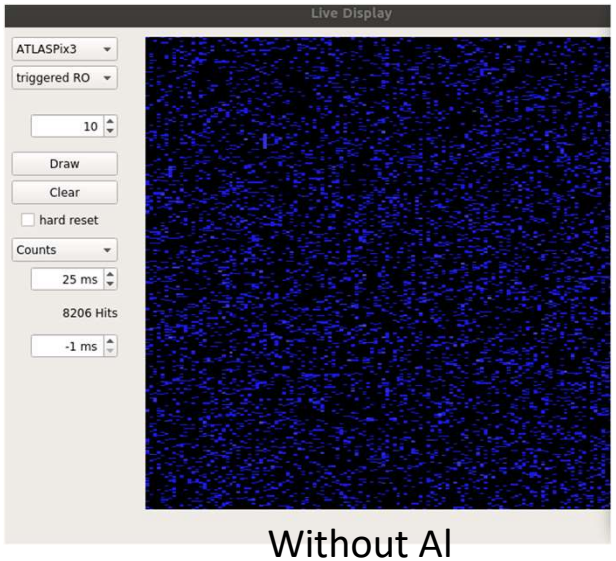
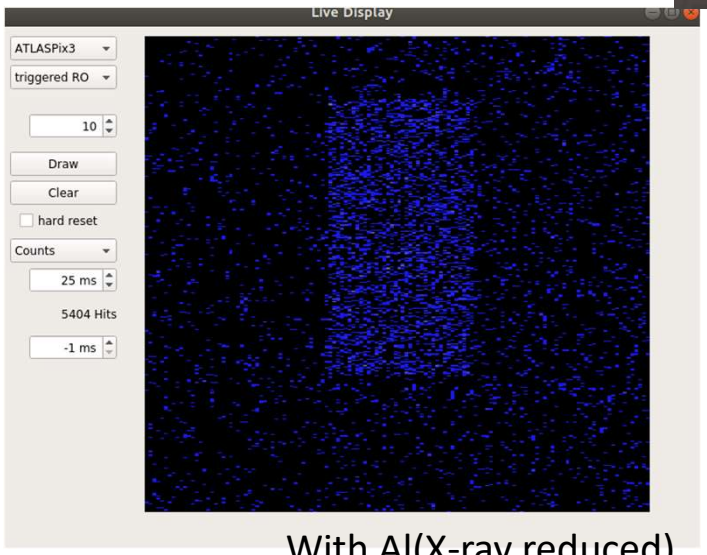
Test with synchrotron X-ray

- Beam open a little rectangle window/shutter
- An Aluminum foil can be placed to shield the X-ray
- Al shield X-ray, electron obvious at the rectangle





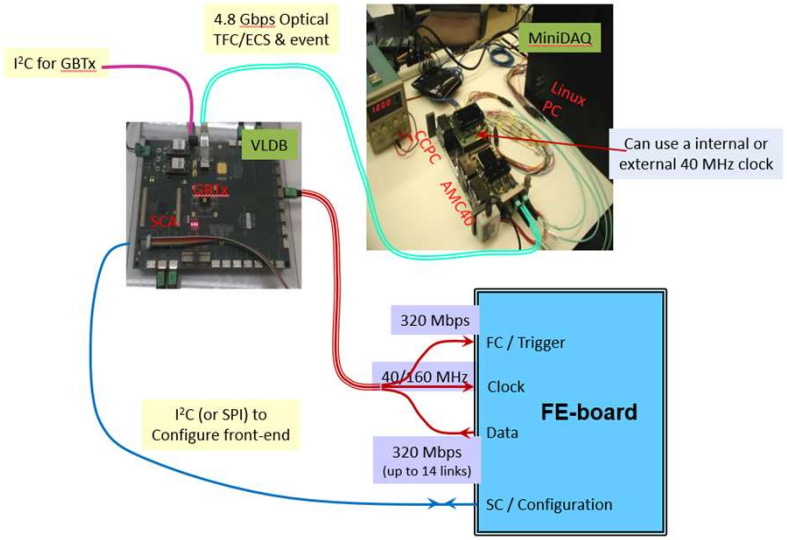
Without Al



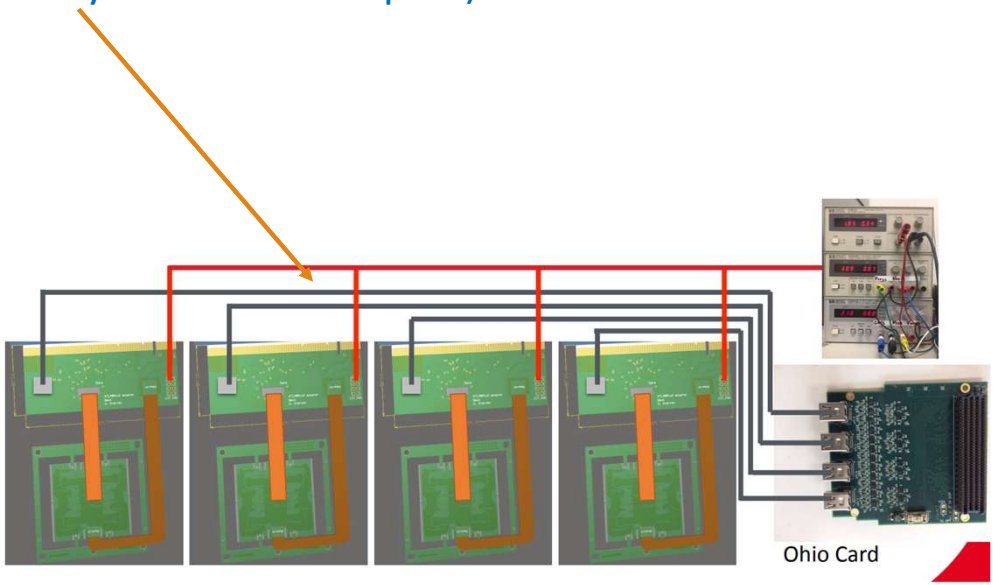
With Al(X-ray reduced)

Future Plan

- Multi-chip Module readout test:
  - YARR(Yet A Rapid Readout)(H .Fox Wednesday afternoon's report)
  - DAQ system based on GBTx(LHCb)



Gbtx DAQ system



YARR

Summary

- HV CMOS silicon tracker simple introduction
- ATLASPix3 tested in lab and works well
- Test with radioactive source Fe55 and Sr90
- Application with electron beam and synchrotron radiation
- Future plan: multi-chip module readout

Thanks for your attention!

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Thanks!

backups

GECCO – The Concept

- **GE**neric **C**onfiguration and **CO**ntrol System
- It is a collection of
  - hardware
  - firmware
  - software

  for testing ASICs
- central element: the GECCO board
- Design Goals:
  - versatile for application with different chips
  - easy change of sample
  - enable hands-free debugging
  - economic

Test Process: Power Supply

- Basically, it needs 7-channal power supply.
- While using on-board regulaters, only 4-channal power supply.
- To save space , use less power supply