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Status of the TaichuPix chip for the high-rate CEPC Vertex Detector

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On behalf of the CEPC MOST2 Vertex detector design team

2021-4-13

Outline

- **Status review**
- **Towards the full size engineering run**
 - Design finalization & test
 - Radioactive source test
 - TID verification
- **Full size chip preparation**
- **Recent plan**

MOST2 project requirements on pixel chip

Silicon Vertex Detector **Prototype** – MOST (2018–2023)

Sensor technology CMOS TowerJazz

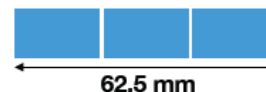
- ✦ Design sensor with large area and high resolution
- ✦ Integration of front-end electronic on sensor chip



Benefit from MOST 1 research program

Double sided ladder

Layer 1 (11 mm x 62.5 mm)
Chip size: 11 mm X 20.8 mm



3 X 2 layer = 6 chips

3-layer sector



Baseline MOST2 goal:
3-layer prototype

Default layout requires different size ladders

Keep it simple for baseline design

L1

L2

L3

3-layers
same size
same chip

Goals:

1 MRad TID
3-5 μ m SP resolution

Integrate electronics
readout

Design and produce
light and rigid
support structures

8

■ Motivation for TaichuPix chip design

- Full size & functionality chip
- Assembled on ladders with backend Elec. & DAQ

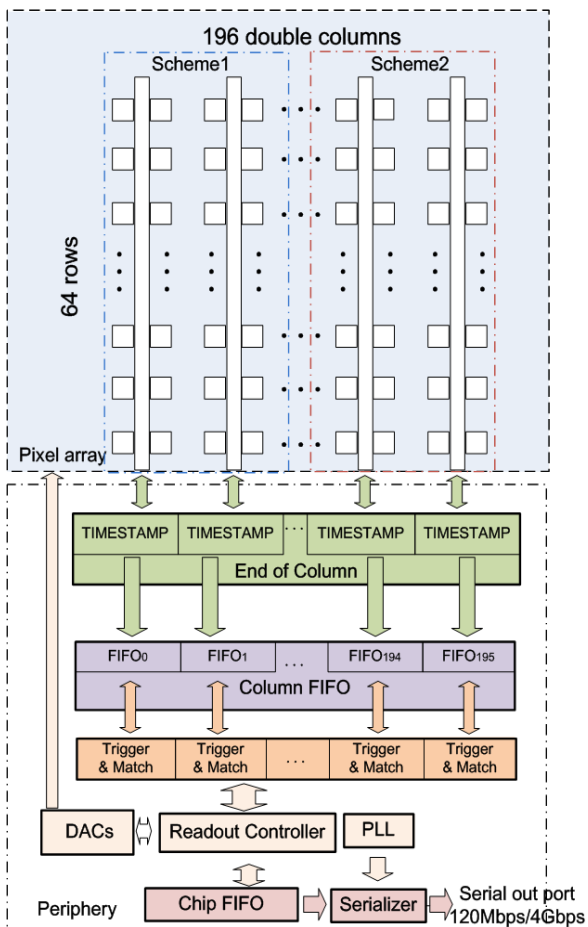
Ref: Introduction to the Pixel MOST2 Project,
Joao Costa, 2018.6

Main specs of the full size chip for high rate vertex detector

- **Bunch spacing**
 - Higgs: 680ns; W: 210ns; **Z: 25ns**
 - Meaning 40M/s bunches (same as the ATLAS Vertex)
- **Hit density**
 - 2.5hits/bunch/cm² for Higgs/W;
0.2hits/bunch/cm² for Z
- **Cluster size: 3pixels/hit**
 - Epi- layer thickness: ~18μm
 - Pixel size: 25μm × 25μm
- **Hit rate: 120MHz/chip @W**
- Two major constraints for the CMOS sensor
 - ↳ Pixel size: < 25μm* 25μm (σ~5μm)
 - aiming for 16μm*16μm (σ~3μm)
 - ↳ Readout speed: bunch crossing @ 40MHz
- None of the existing CMOS sensors can fully satisfy the requirement of high-rate CEPC Vertex Detector
- TID is also a constraint
 - ↳ 1~2.5Mrad/year as required in MOST2 is achievable

For Vertex	Specs	For High rate Vertex	Specs	For Ladder Prototype	Specs
Pixel pitch	<25μm	Hit rate	120MHz/chip	Pixel array	512row×1024col
TID	>1Mrad	Date rate	3.84Gbps --triggerless ~110Mbps --trigger	Power Density	< 200mW/cm ² (air cooling)
		Dead time	<500ns --for 98% efficiency	Chip size	~1.4cm×2.56cm

TaichuPix architecture



- **Similar to the ATLAS ITK readout architecture: “column-drain” readout**

- Priority based data driven readout, zero-suppression intrinsically
- Modification: **time stamp is added at EOC** whenever a new fast-or busy signal is received
- **Dead time:** 2 clk for each pixel (50ns @40MHz clk)

- **Two parallel pixel digital schemes**

- ALPIDE-like: Readout speed was enhanced for 40MHz BX
- FE-I3-like: Fully customized layout of digital cells and address decoder for smaller area

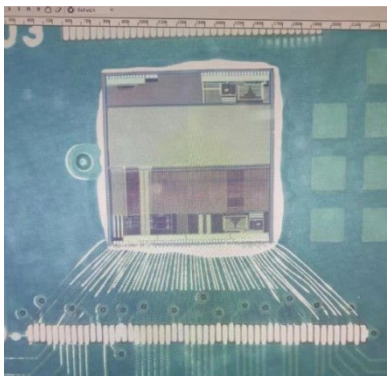
- **2-level FIFO architecture**

- L1 FIFO: In column level, to de-randomize the injecting charge
- L2 FIFO: Chip level, to match the in/out data rate between the core and interface

- **Trigger readout**

- Make the data rate in a reasonable range
- Data coincidence by time stamp, only matched event will be readout

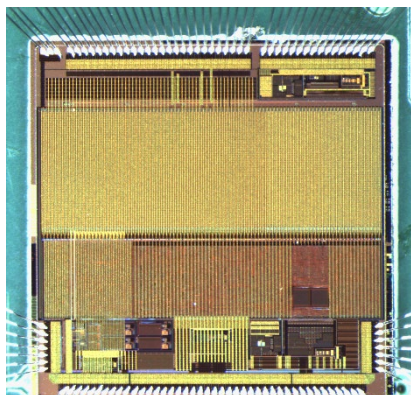
TaichuPix chips overview



TaichuPix-1

Chip size: 5 mm × 5 mm

Pixel size: 25 μm × 25 μm



TaichuPix-2

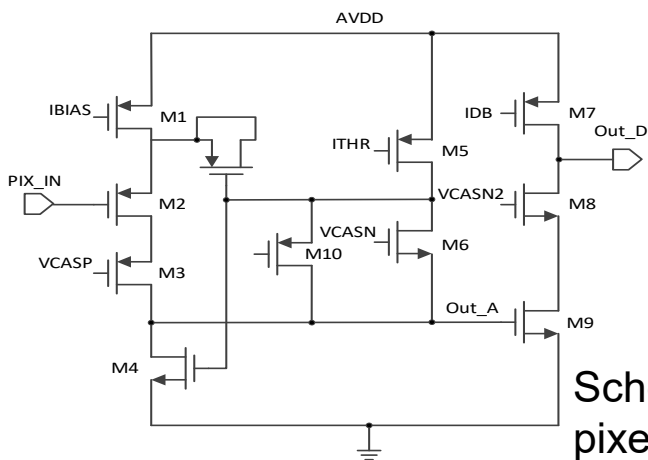
Chip size: 5 mm × 5 mm

Pixel size: 25 μm × 25/24 μm

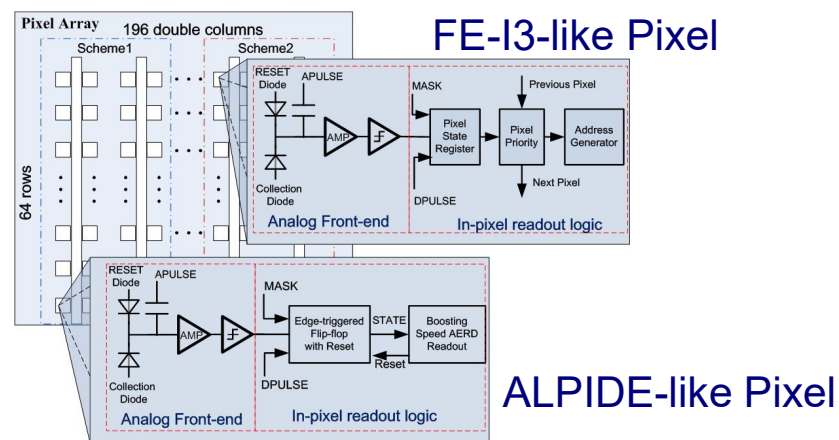
- **Two MPW chips were fabricated and verified**
 - TaichuPix-1: 2019.06~2019.11
 - TaichuPix-2: 2020.02~2020.06
- **Chip size 5 mm×5 mm with standalone features**
 - Pixel size of 25 μm×25 μm (one sector with 25 μm×24 μm pixels in TaichuPix-2)
 - A full functional pixel array (small scale)
 - A 64×192 Pixel array (including 6 pixel variations)
 - Periphery logics
 - Fully integrated logics for the data-driven readout
 - Fully digital control of the chip configuration
 - Auxiliary blocks for standalone operation
 - High speed data interface up to 4Gbps
 - On-chip bias generation
 - Power management with LDOs
 - IO placement in the final ladder manner
 - Multiple chip interconnection features included

Design variations in pixel array

Sector	Pixel front-end	Pixel digital	Pixel size
Sector 1	Same as S1 of TC1, reference design	FEI3-like	25 μm \times 25 μm
Sector 2	M6 with guard-ring, PMOS in independent well	FEI3-like	25 μm \times 25 μm
Sector 3	M6 in enclosed layout, PMOS in independent well	FEI3-like	25 μm \times 24 μm
Sector 4	Increasing M3, M4, M9. M6 in enclosed layout, PMOS in independent well	FEI3-like	25 μm \times 25 μm
Sector 5	Same FE as S2, with smaller sensor	ALPIDE-like	25 μm \times 25 μm
Sector 6	Same FE as S1	ALPIDE-like	25 μm \times 25 μm



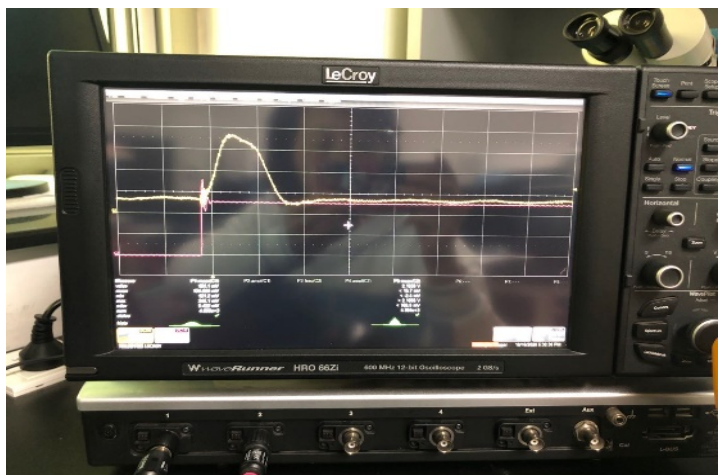
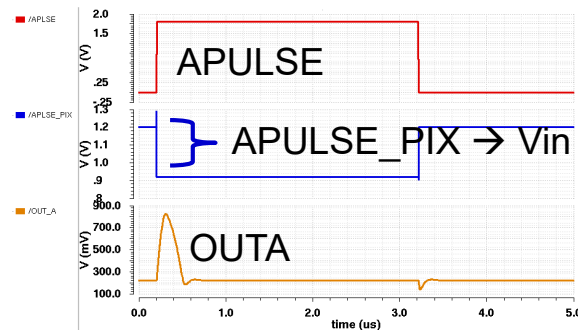
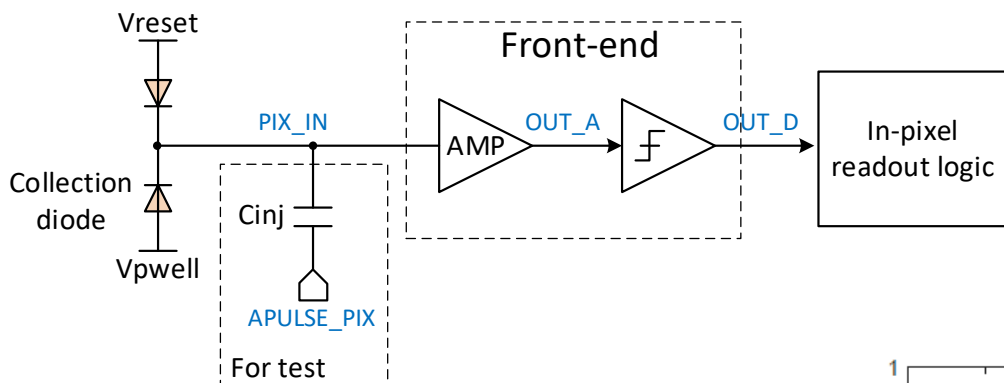
Schematic of in-pixel front-end



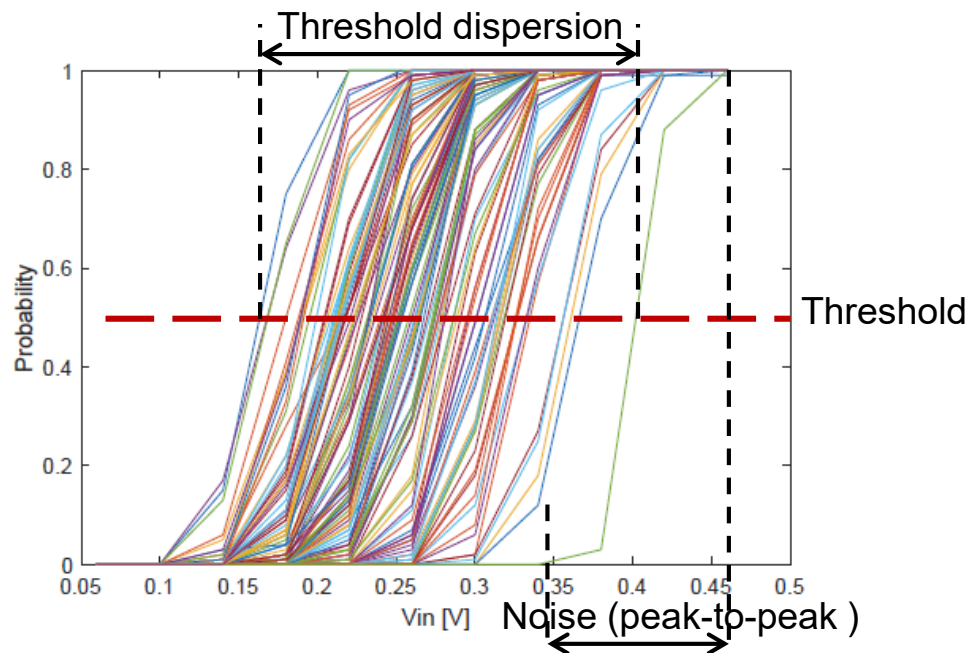
Ref: Tianya Wu in TaichuPix-1 User Manual

Electrical test

- Electrical performance verified by injecting an external voltage step (charge) into pixel front-end



Analog output of a pixel @ V_{in} = 0.9 V



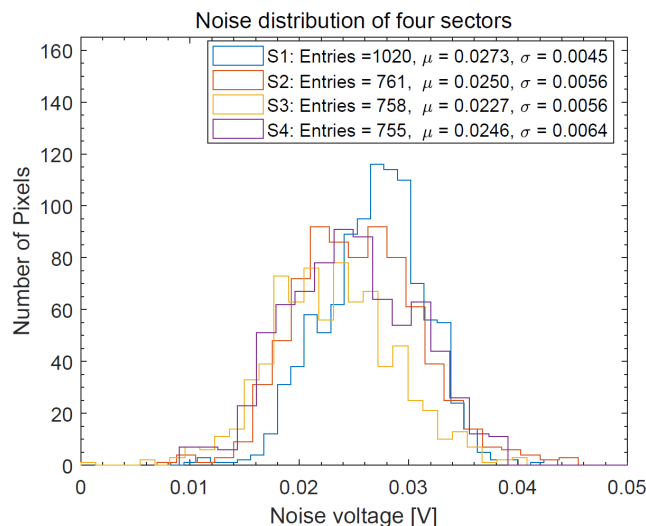
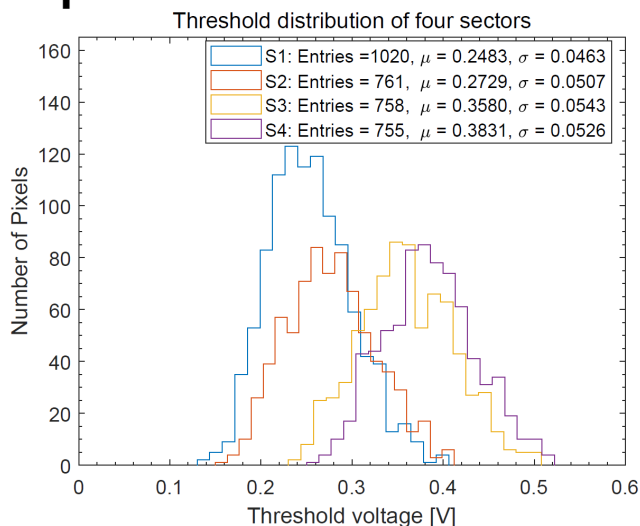
Measured "S-curve" for 128 pixels

Comparison of 4 sectors

■ Threshold and noise performance summary

	Thres. Mean (mV)	Threshold nonuniformity rms (mV)	Temporal noise (mV)	Total noise (mV)
S1	248.3	46.3	27.3	53.8
S2	272.9	50.7	25.0	56.5
S3	358.0	54.3	22.7	58.9
S4	383.1	52.6	24.6	58.1

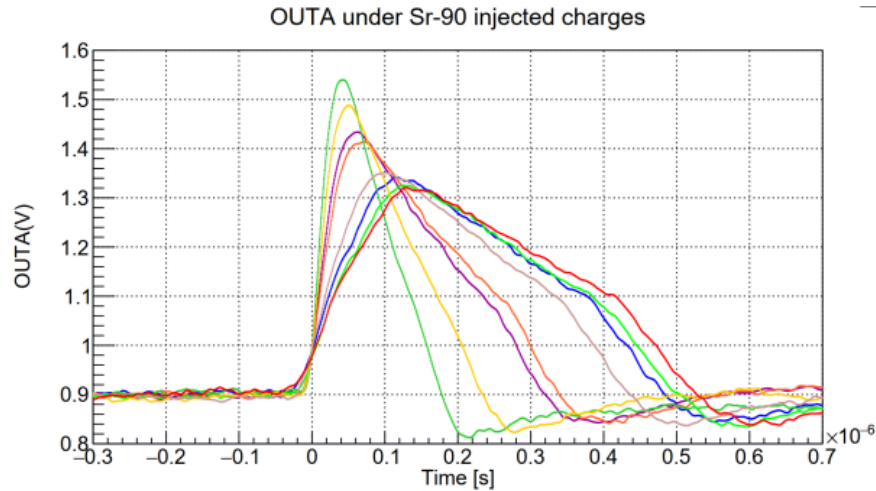
■ Four sectors with FEI3-like digital logic works well, and show similar noise performance. S1 shows the minimum threshold.



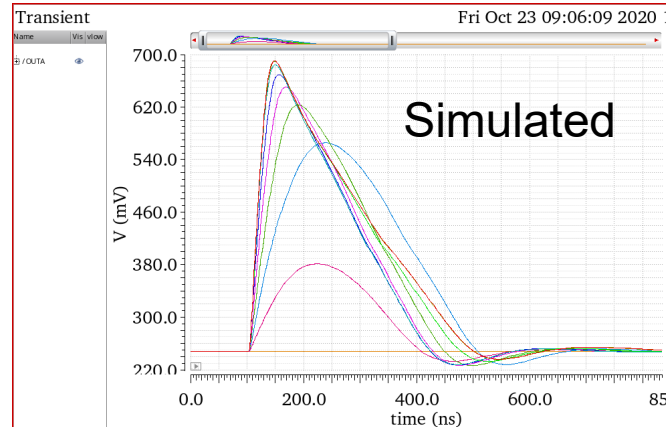
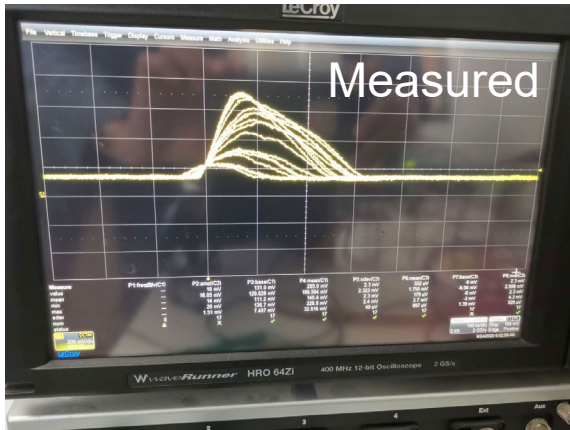
TaichuPix response to Radioactive



TaichuPix1 response to ^{90}Sr beta source

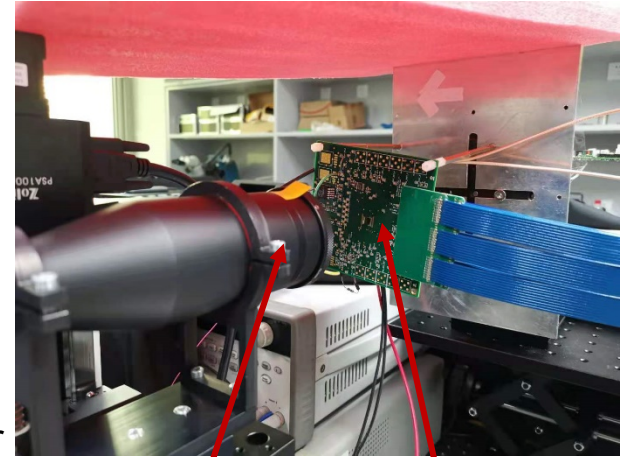
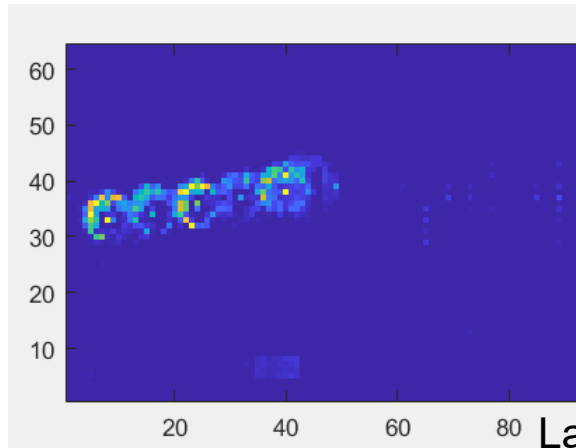
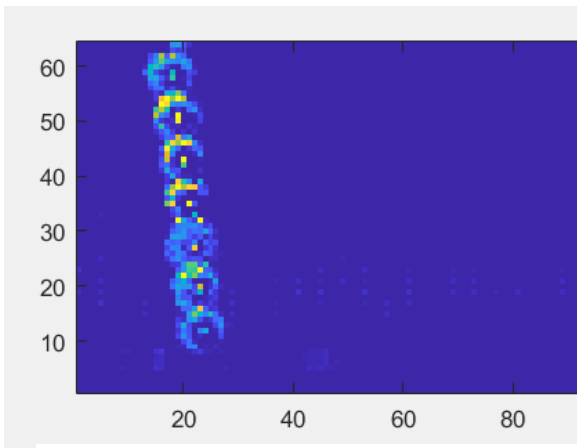


- Analog output waveform agreed with the simulation when tested by X-rays
- Signal amplitude, signal width, edge speed...all are almost agreed
- Note: for the small signal, the S/N ratio was also good, inferred that the noise performance was also normal (good)



TaichuPix2 response to X-ray tube (cutting energy @6keV)

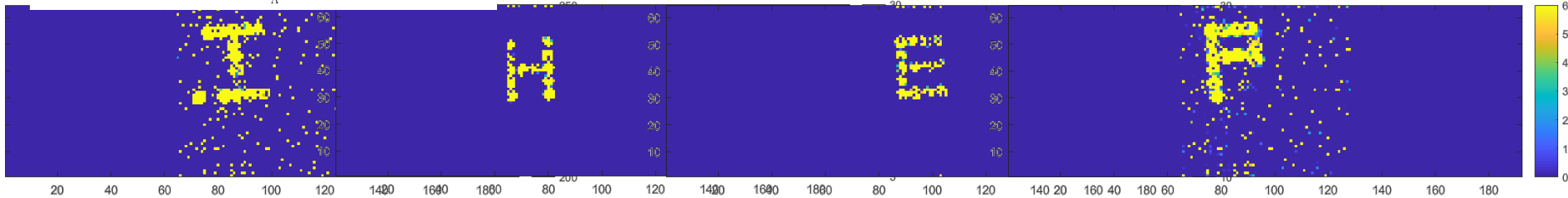
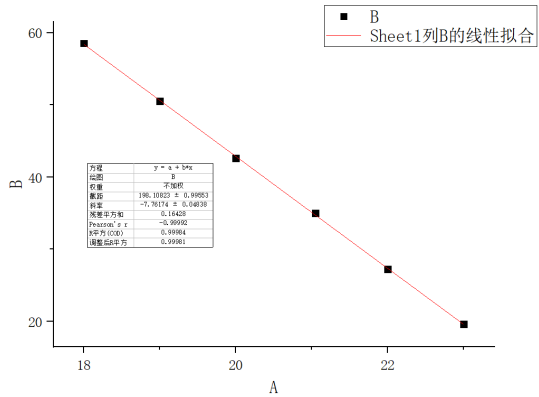
Taichupix radioactive imaging by triggerless readout



Laser
(1064 nm)

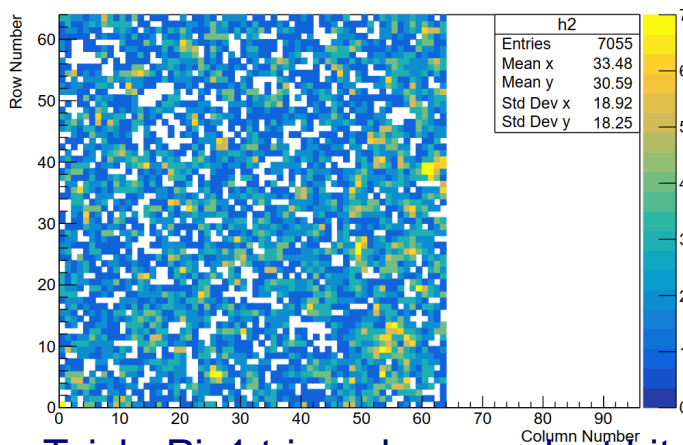
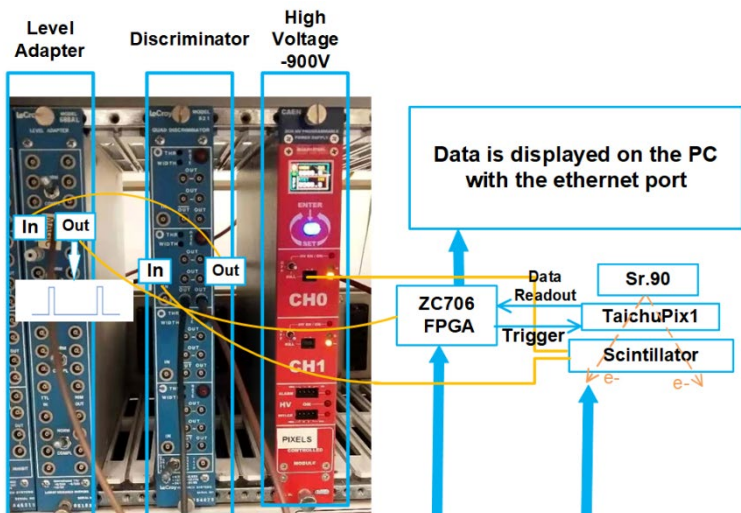
TaichuPix-2

- Triggerless mode was used for the imaging experiment
- Laser was moved every 200 μm in X/Y direction, -7.762 ± 0.05 & $1/(0.162 \pm 0.007)$ were found by linear fit as the fitted pixels per 200 μm , while expects 8 -- the test board surface was not fixed vertically to the platform
- The full signal chain was proved.

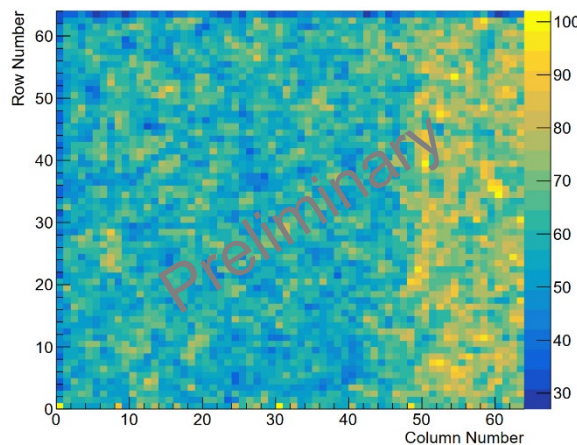
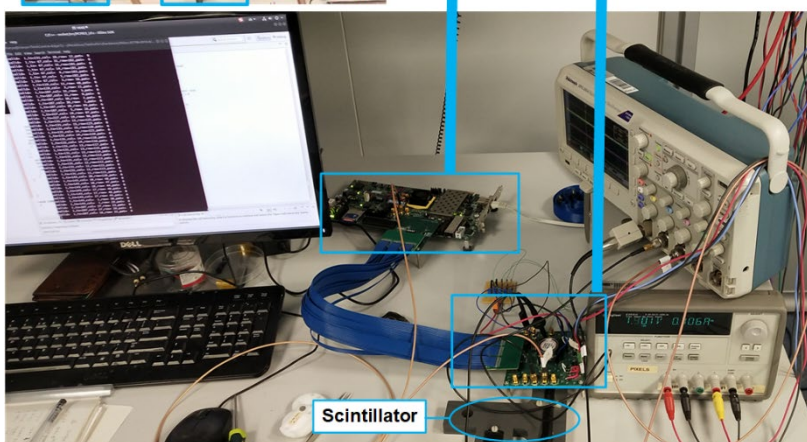


Some letter scanning experiments

Taichupix radioactive imaging by trigger mode



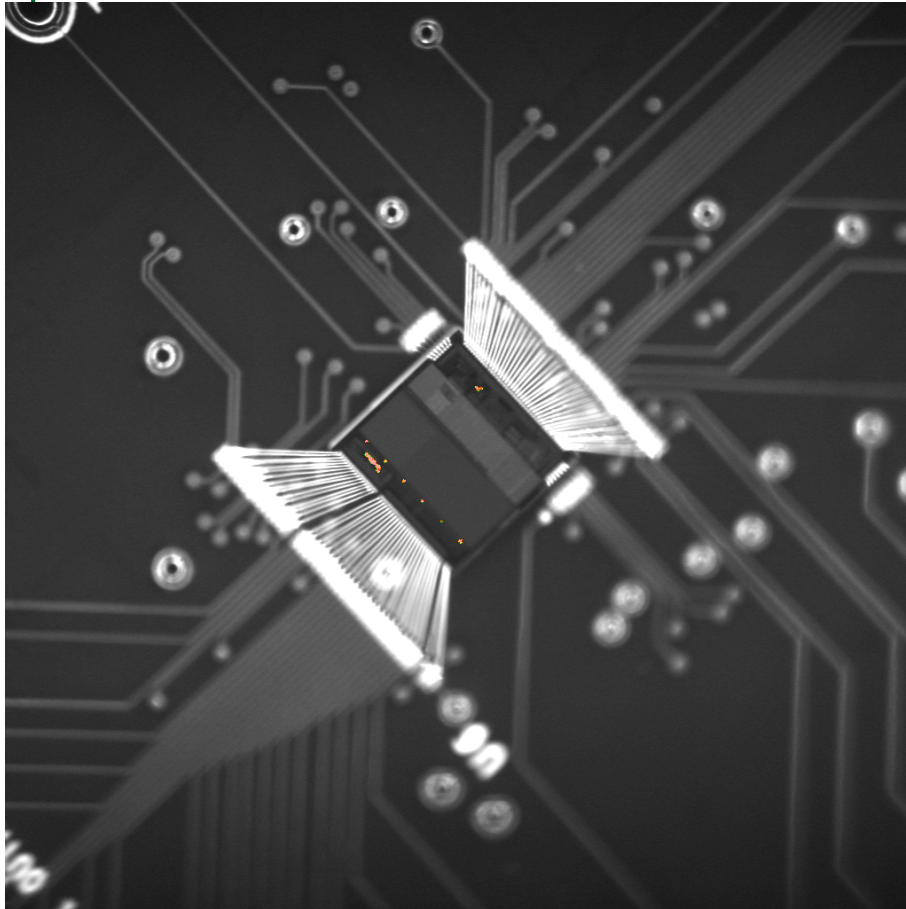
TaichuPix1 triggerless readout hitmap to ^{90}Sr



TaichuPix1 trigger readout hitmap to ^{90}Sr

- Trigger readout hitmap by Tcpix1 chip showed much better uniformity and efficiency, due to Tcpix1's problematic readout chain and limit on-chip FIFO
- Also proved the trigger functionality, that fake event can be eliminated

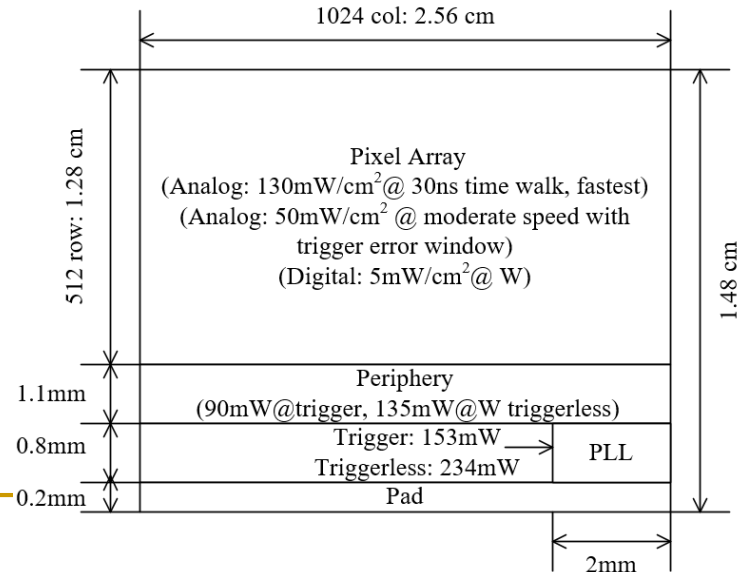
Chip Power consuming test



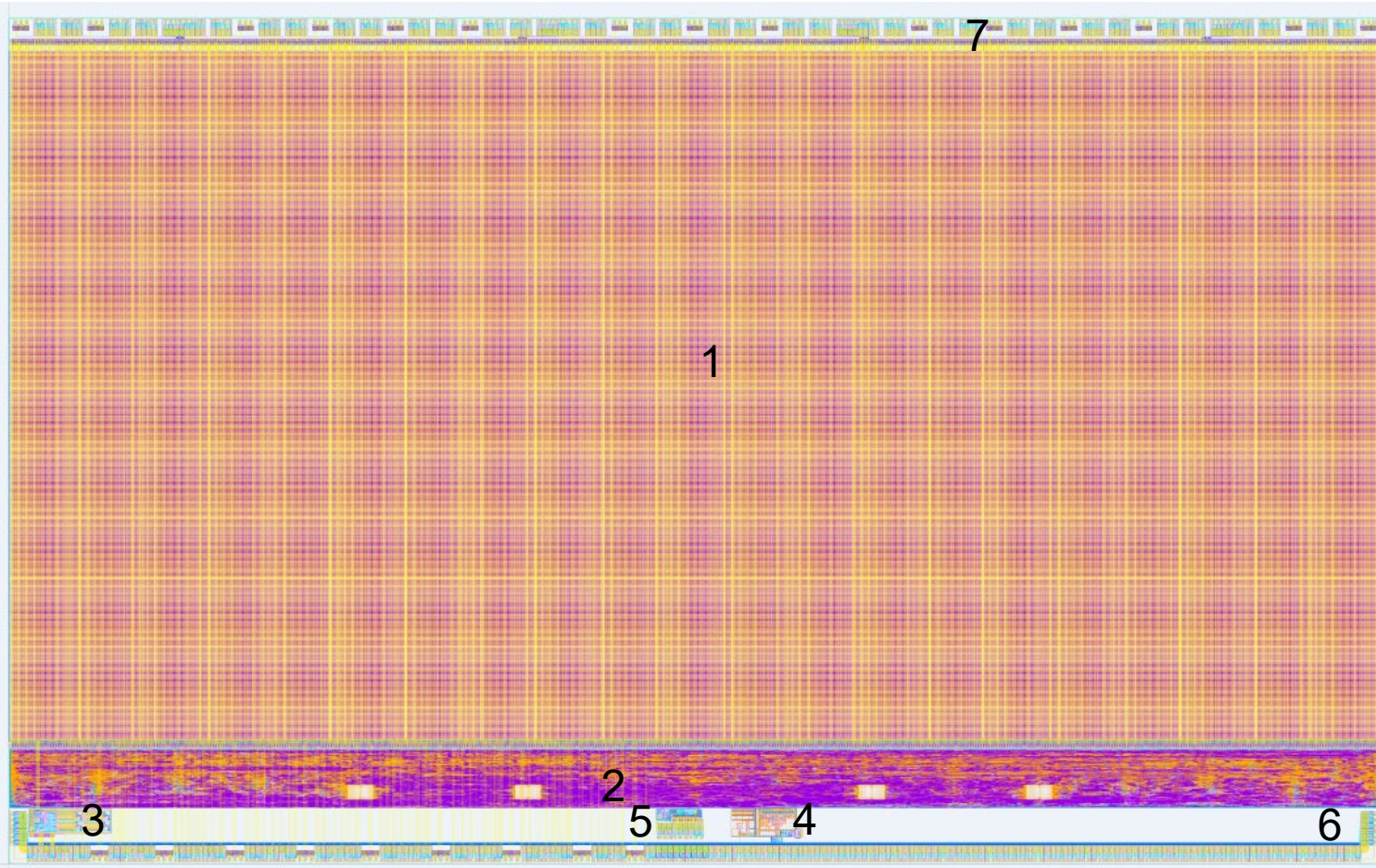
- Tcpx2 chip current consuming tested of 210mA (380mW@1.8V)
- Almost agreed with simulation
 - PLL@trigger speed: 306mW
 - Read by triggerless but at 160Mbps
 - Two PLLs in Tcpx2
 - Analog biased at fastest: 15mW (192*64 pixel array)
 - With 16 probe buffers
 - Periphery@trigger speed: 90mW
 - Read by triggerless but at 160Mbps

- The EMMI (Emission Microscope) test showed the hot points were exactly as expected

- quiet pixel array & periphery = no leakage point



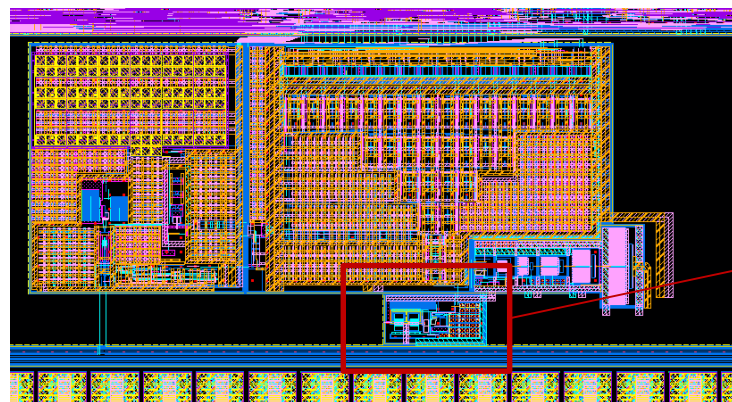
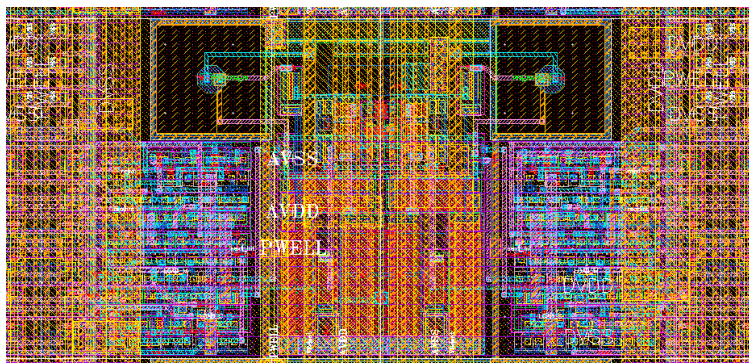
Preparation for the full size engineering run



1. Pixel array
1024*512
2. Periphery
3. DAC & Bias generation
4. Data interface
5. LDO (test blocks)
6. Chip inter-connection features
7. Scribe-able top power connection features

- The full size chip design is almost ready (in less than 2 weeks), will be taped out in May (delayed due to payment issues)

Preparation for the full size engineering run

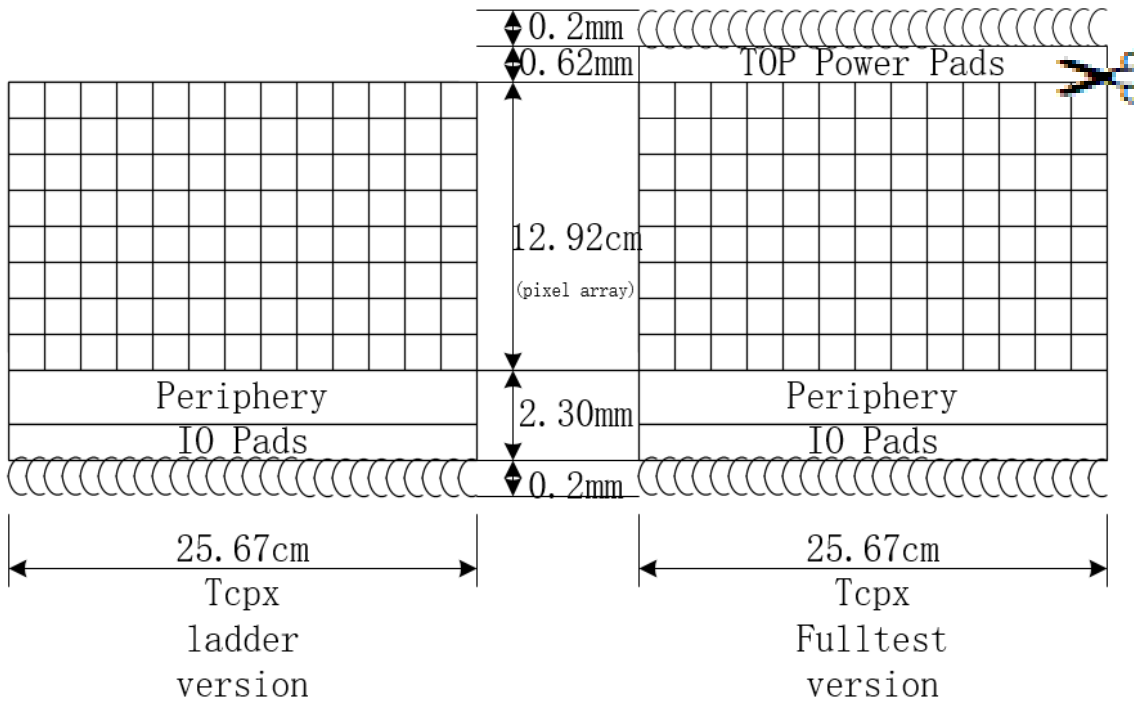


- **Process improved for better power supply: 6 Metals to 7M with 1 Thick Top**
 - Will help for the full size chip power integrity
- **25 μm \times 25 μm pixel, unique design (S1)**
- **A 1024 \times 512 Pixel array**
- **Periphery logics**
 - Unique design for FE-I3 like readout
- **High speed data interface**
 - Optimized for trigger mode and low power: optional low power LVDS port added
- **On-chip bias generation**
 - Bugs detected & solved from the Tcpx2 test
- **IO placement in the final ladder manner**
 - chip interconnection bus features included for ladder
- **LDO will be independently tested as a test block due to the remain issues**

Preparation for the full size engineering run

- **Two versions possibilities were kept within one tapeout**

- Fulltest version keeps all test pads features for the chip study before ladder assembly
- Top power pads & top power bus connections will help for the full chip power integrity, concerning Tcpix is aiming for fast readout with high power
- Tcpix final ladder version
 - If top power bus not necessary, stays in minimum dead zone
 - If top power bus needed for less IR drop, + 200um dead zone on the top but with a good chip
 - If all needed, we learned by test thanks to the full test features



- **Signal pads/routing on ladders were kept minimum with 9/8 wires, other common bus were routed by chip interconnection features**

Summary & recent plan

- **TaichuPix chip were fully verified and preparing to submit the full size tapeout**
 - Full signal chain & functionality verified with both electrical & radioactive test
- **Recent plan**
 - Design will be ready for the engineering run within 2 weeks
 - The final IO planning has to be further cross-checked with the Flex cable design team
 - However due to the payment delayed, the real submission time was expected at about the end of May
 - Full chip simulation and verification till the real submission
 - Two papers in progress (one in MR1, one in preparation)
 - Wafer probe card design
 - June ~ August
 - Chip study board design
 - June ~ August
 - Flex cable design
 - April ~ ?

Backup

MALTA chip power connection pads

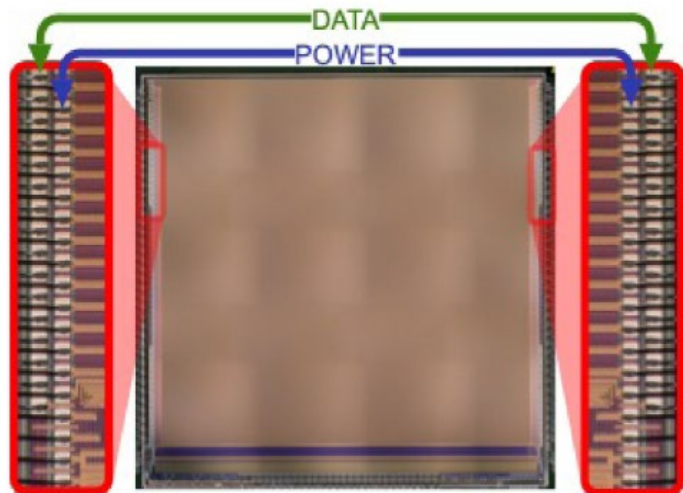


Fig. 2. Data and power connections are located on both sides of the MALTA chip as indicated in this picture. The connections are arranged in two staggered bond rows on each side [7] with a pitch of 120 μm .

- <https://doi.org/10.1016/j.nima.2020.164895>

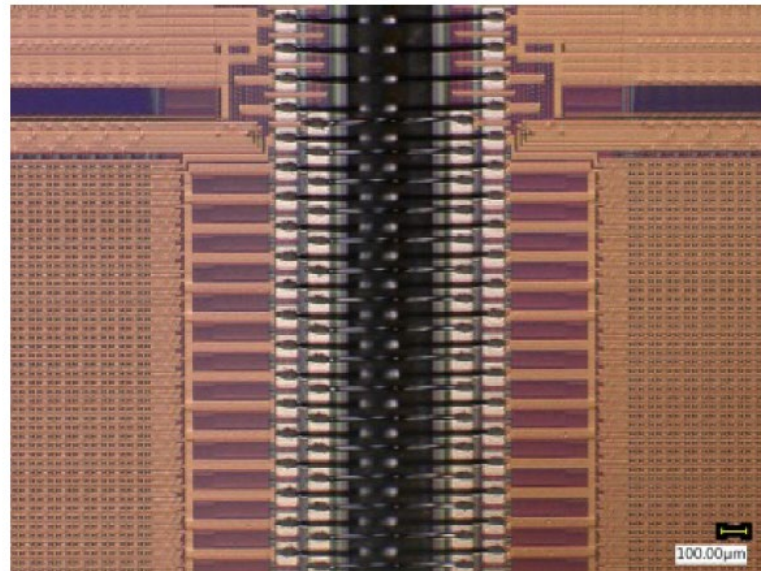


Fig. 4. Picture of two MALTA chips with direct ultrasonic Al wedge wire bonding of the CMOS transceivers and power pads.

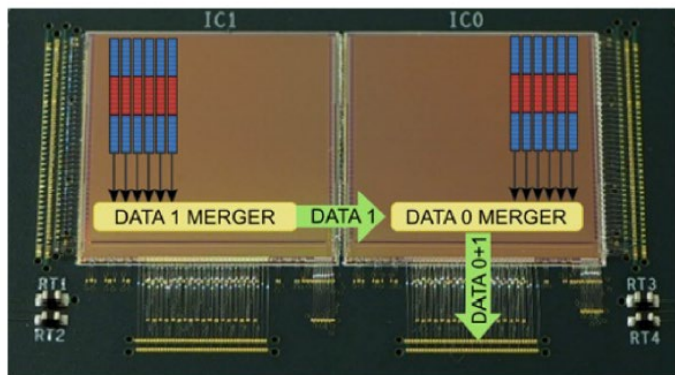


Fig. 5. Picture of two MALTA chips mounted on a PCB with direct wire bond connections as shown in Fig. 4. The data from one chip was transferred to the second chip via the wire bonds and read out.

Scribe-able pads examples

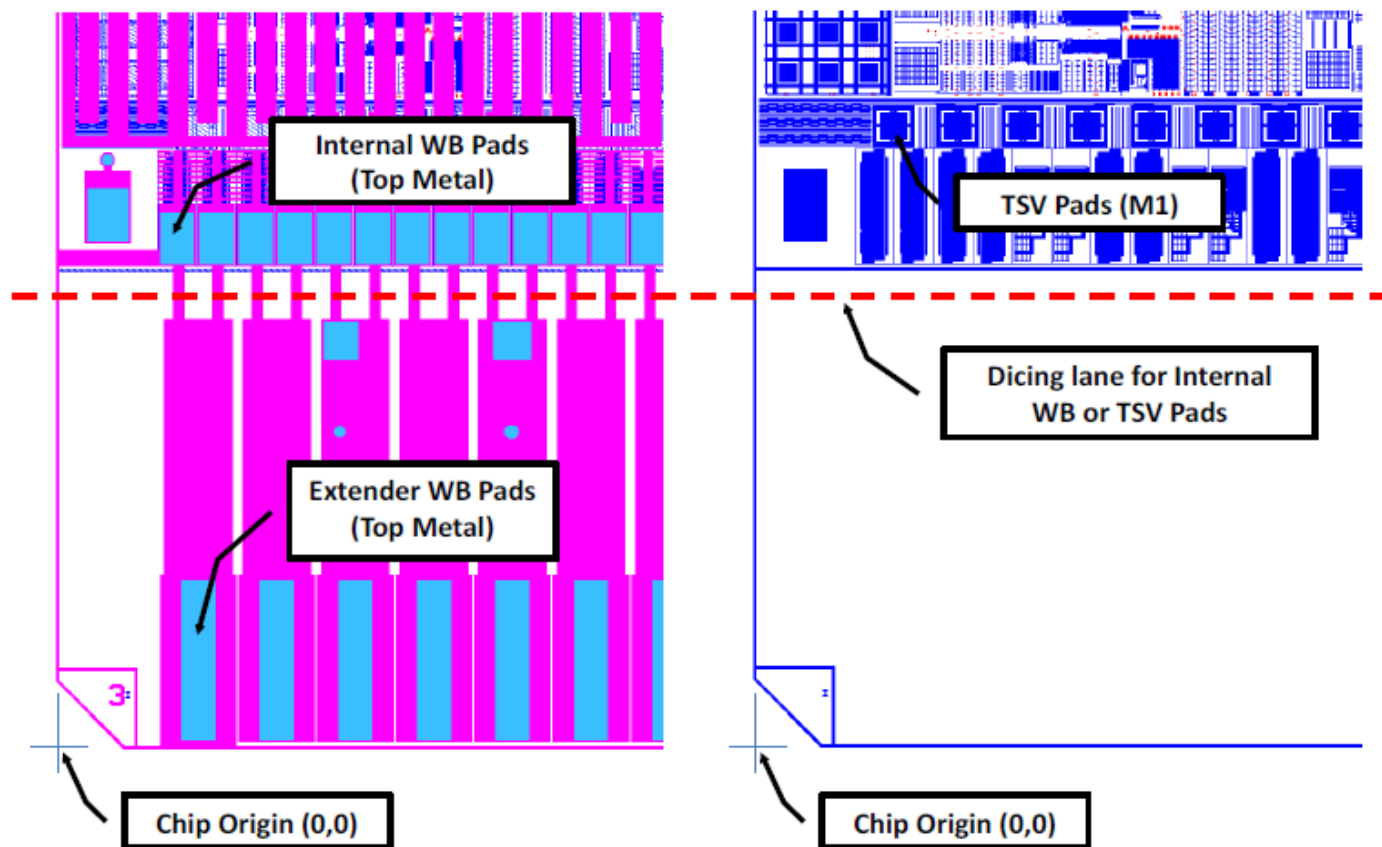
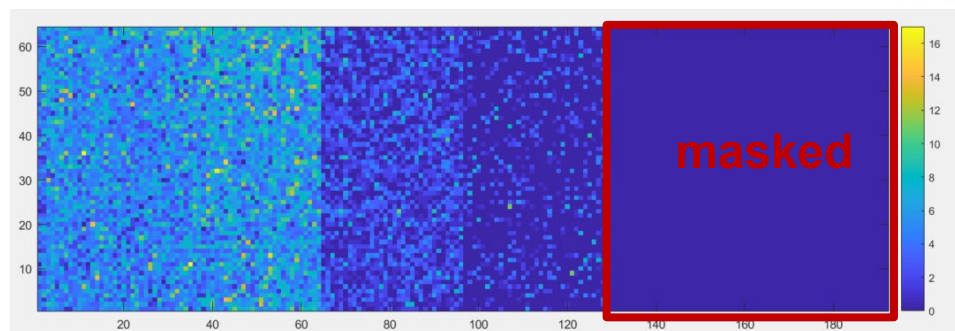
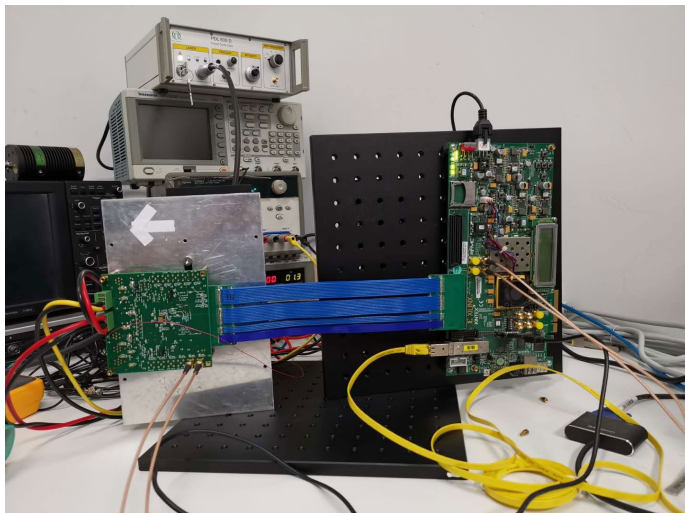


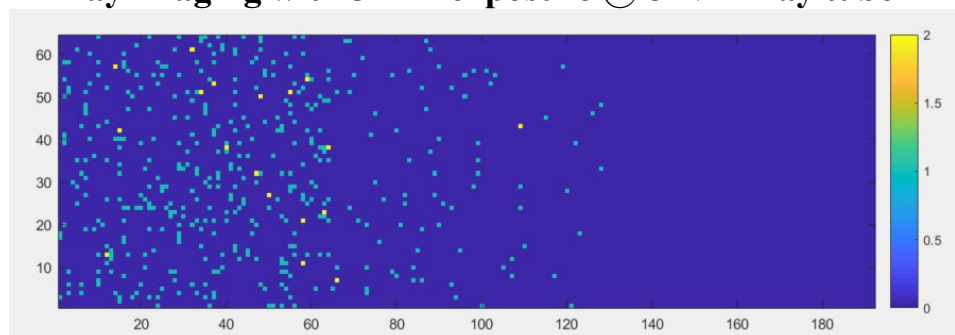
Figure 55. Position of the extender wire-bond pads (top metal), the internal wire-bond pads (top metal), and the TSV pads (bottom metal, M1). Also the dicing lane is shown for the use of the internal WB and TSV pads.

From TIMEPIX3 user manual

X-ray imaging



X-ray imaging with 5 min exposure @ 8kV X-ray tube

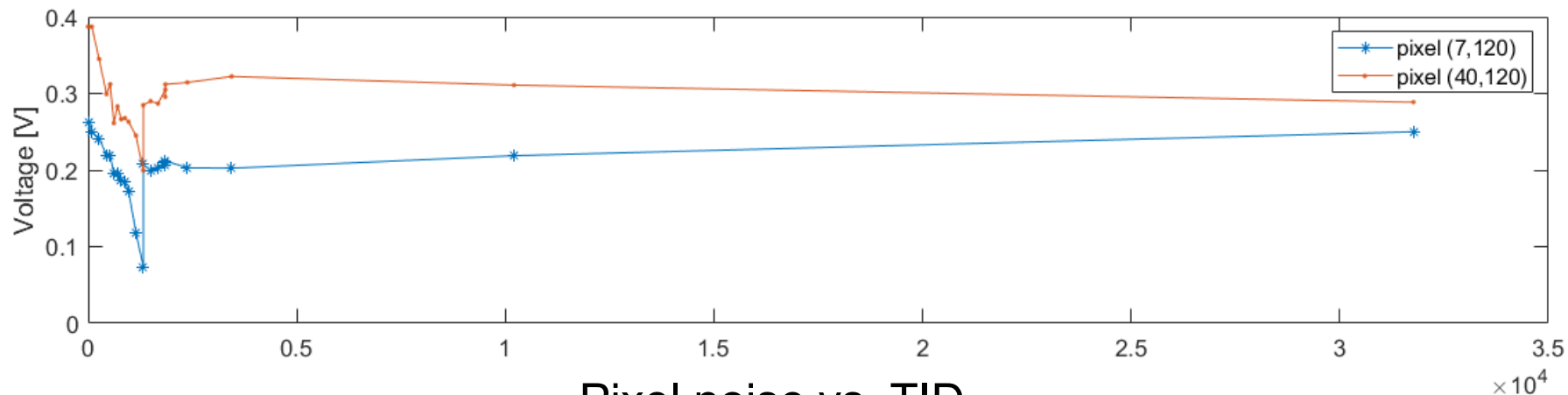


“single frame” X-ray imaging with 10s exposure @ 8kV X-ray tube

- “DAQ” system established for the test system, with continuous data acquisition
- Triggerless readout @160Mbps LVDS were applied at the current stage
- The full signal chain (pixel analog-digital-periphery-data interface) was proved by both X-ray and laser imaging
 - Full array/sector was sensitive
 - “Single frame” imaging showing no crosstalk detected between clusters (good S/N ratio)
- X-ray imaging with 5 min exposure showed clearly the different sectors of the pixel array (2 sectors were masked)

TID results till 30 Mrad

Pixel threshold vs. TID



Pixel noise vs. TID

