Progress of the CMOS pixel sensor JadePix3

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On behalf of the **JadePix3 study group**

Joint Workshop of the CEPC Physics,

Software and New Detector Concept

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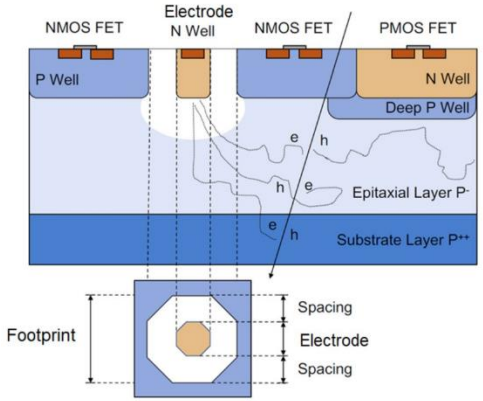
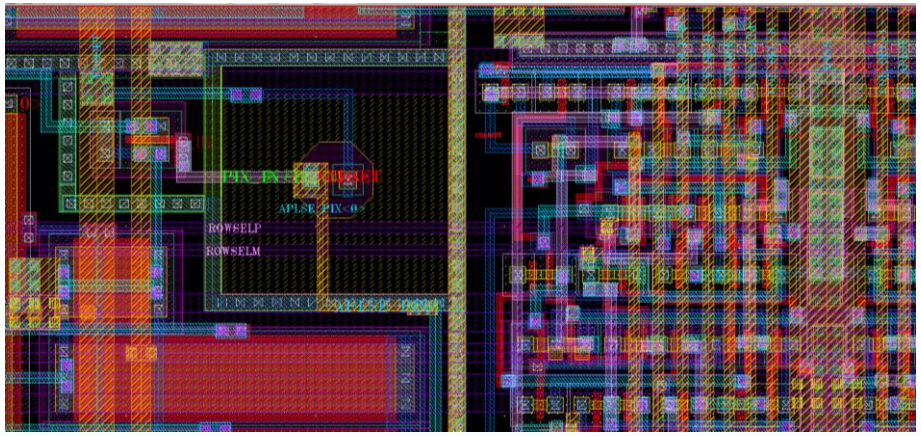
Conceptual introduction

Structure of CMOS pixel sensor

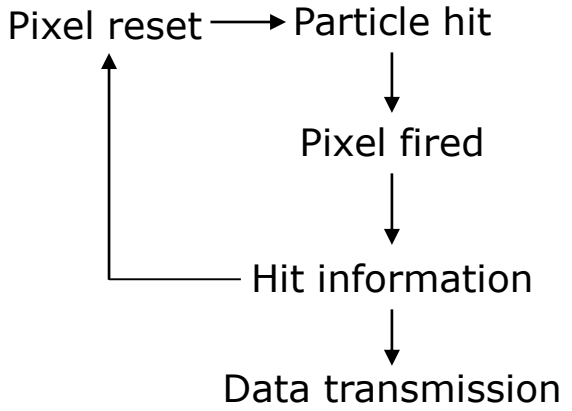
- Vertical stackup
  - Metal layers 1 to 6
  - NMOS/PMOS transistors
  - **HR epitaxial layers**
  - Substrate
- Planar representation
  - "Layout"
  - 51 layers of pattern

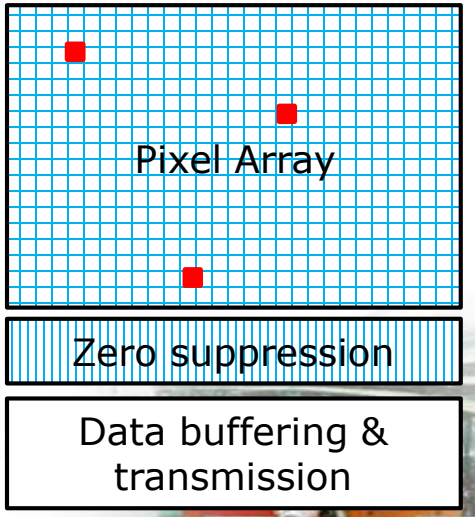




Design of CMOS pixel sensor

- Architecture
  - Sensing diode
  - Amplifier and digitizer
  - Control logic
  - Zero suppression
  - Data buffering and transmission
  - Slow control
  - Bias DAC
- Operation

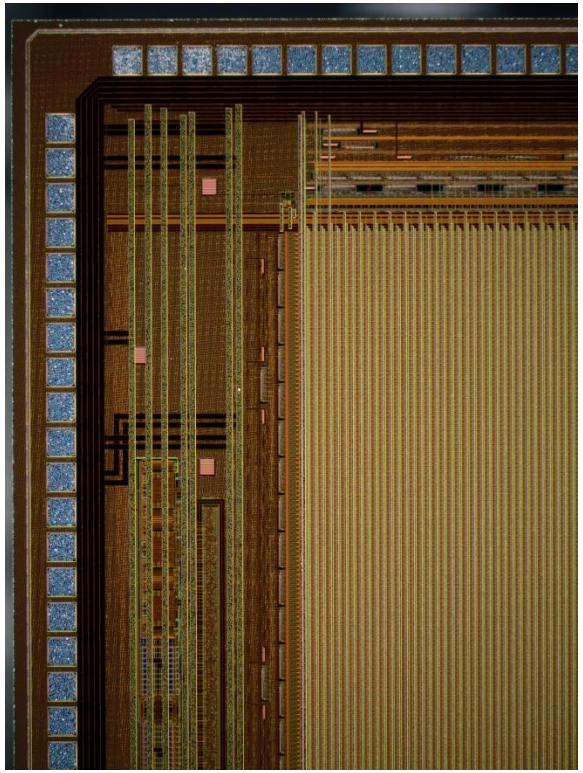




Outline

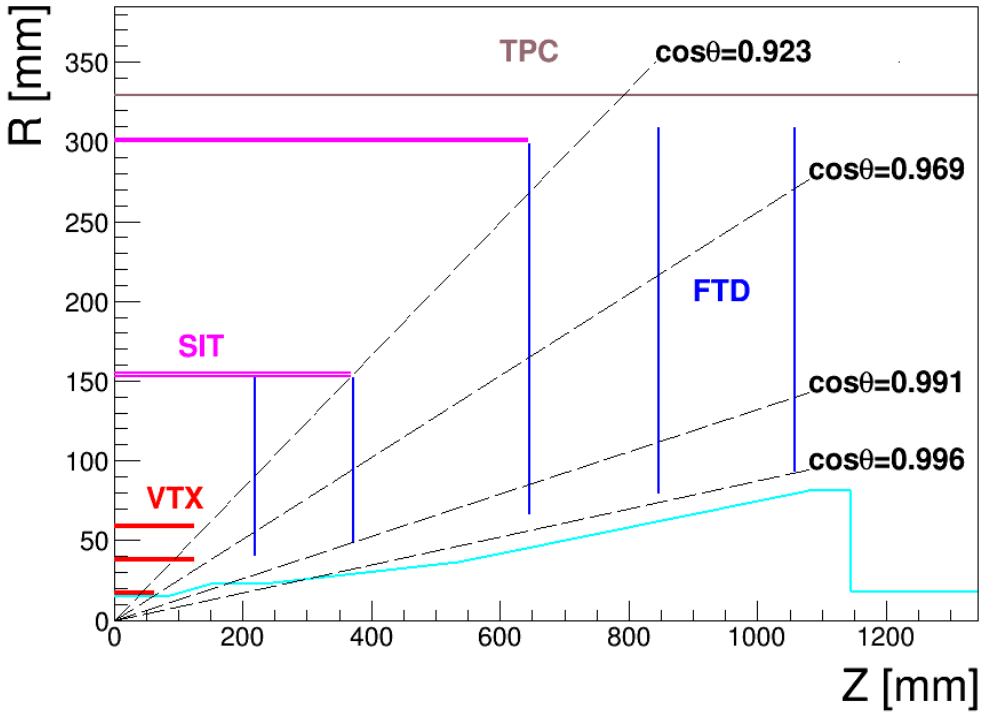
- Motivation
  - Requirements of baseline scheme in the CDR
- Revisit the JadePix3 design
- Progress of test and measurement
  - General situation
  - Highlights of performance study
- Summary and outlook

Microscopic view of JadePix3
(Top-left corner)



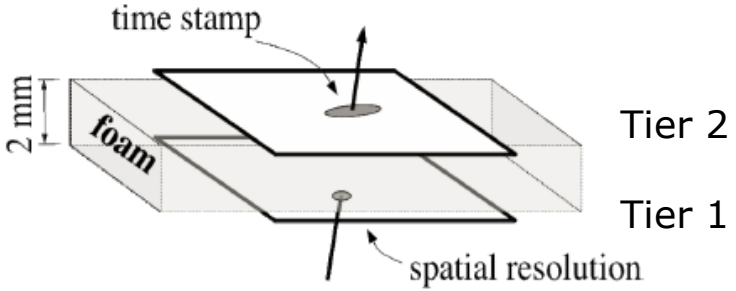
Baseline scheme in the CDR

Silicon tracking system



- SIT: Silicon Internal Tracker
- FTD: Forward Tracking Detector
- SET: Silicon External Tracker
- ETD: End-cap Tracking Detector

- VTX:
  - 3 (mechanical) layers of double-sided pixels
  - σ_{SP} = **2.8 μm** in Tier 1
  - Total number of pixels: 690M



Concept of double-sided structure

Baseline design parameters

	R(mm)	| Z |(mm)	$\sigma(\mu m)$	material budget
Tier 1	16	62.5	2.8	0.15%/X_0
Tier 2	18	62.5	6	0.15%/X_0
Tier 3	37	125.0	4	0.15%/X_0
Tier 4	39	125.0	4	0.15%/X_0
Tier 5	58	125.0	4	0.15%/X_0
Tier 6	60	125.0	4	0.15%/X_0

A complementary design to meet the specs

- Tier 1: high resolution, low power and modest readout speed
  - JadePix3 targeting on: **3~5 μm**, 50~100 mW/cm^2, 100 μs
- Tier 2: Fast readout speed, low power and relaxed constraint of resolution
  - **1 μs**, 50 mW/cm^2, 4~6 μm is foreseen
- Radiation tolerance is a common requirement to Tier 1 and 2

Impact parameter resolution

$$\sigma_{r\phi} = 5\mu m \oplus \frac{10}{p(GeV)\sin^{3/2}\theta}\mu m$$

Vertex detector specs

$\sigma_{s.p.}$ ~ 2.8um

Material budget ~ 0.15% X_0/layer

r of Inner most layer ~ 16mm

Pixel sensor specs

Tier 1

Small pixel ~ 16um

Thinning to ~ 50um

low power ~ 50mW/cm^2

fast readout ~ 1us

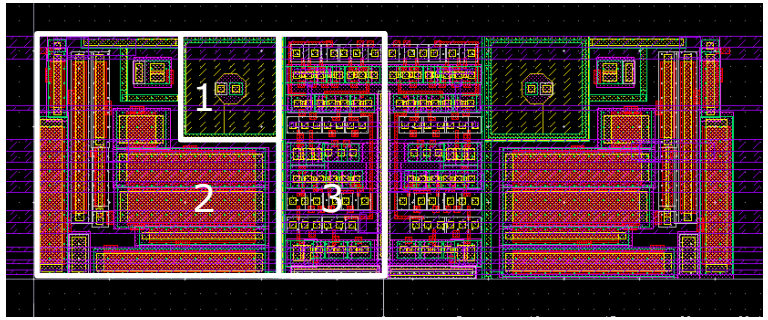
Tier 2

radiation tolerance ~

$\leq 3.4\ Mrad/year$

$\leq 6.2\times10^{12} n_{eq}/(cm^2\ year)$

Small pixel implemented in the JadePix3

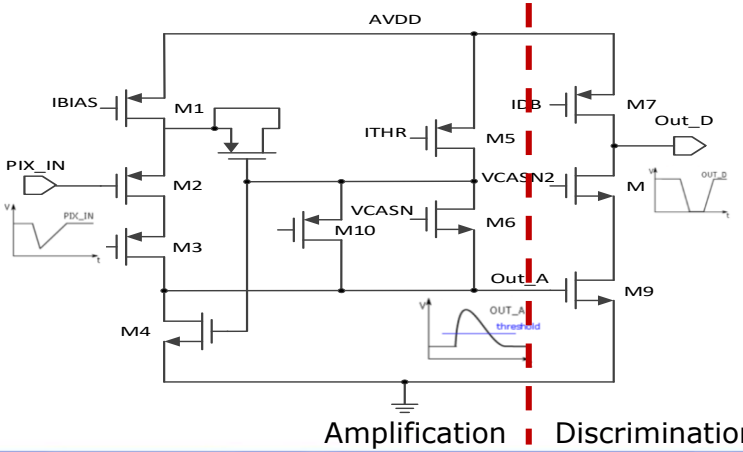


Minimal pixel footprint: **16 μm* 23.11 μm**
1: Sensing diode
2: Analog frontend
3: digital frontend

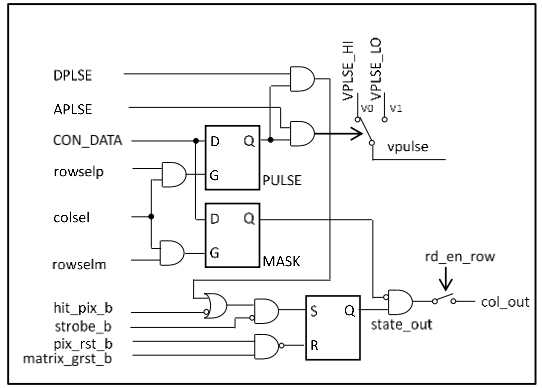
- Small footprint
  - Sensing diode of minimized geometry verified on JadePix1
  - Frontend with **tradeoff** between layout area and FPN
- Fix φ direction* to **16 μm** and allow the z* to vary
  - 3 variants of digital frontend
  - D-FlipFlop vs RS-latch
- Mirrored layout to share bias lines between two columns

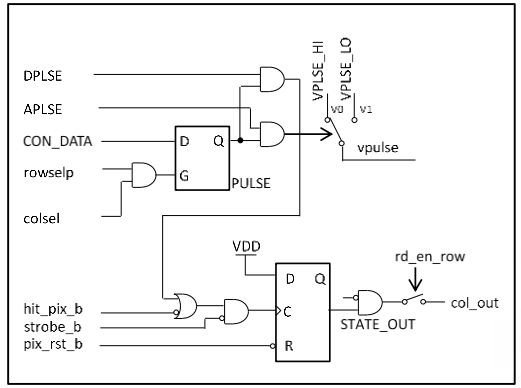
* Detector coordinates in page 4

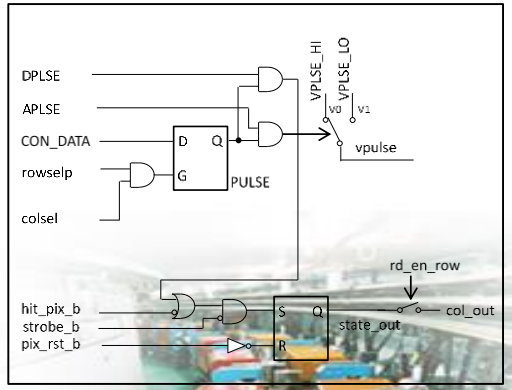
analog frontend



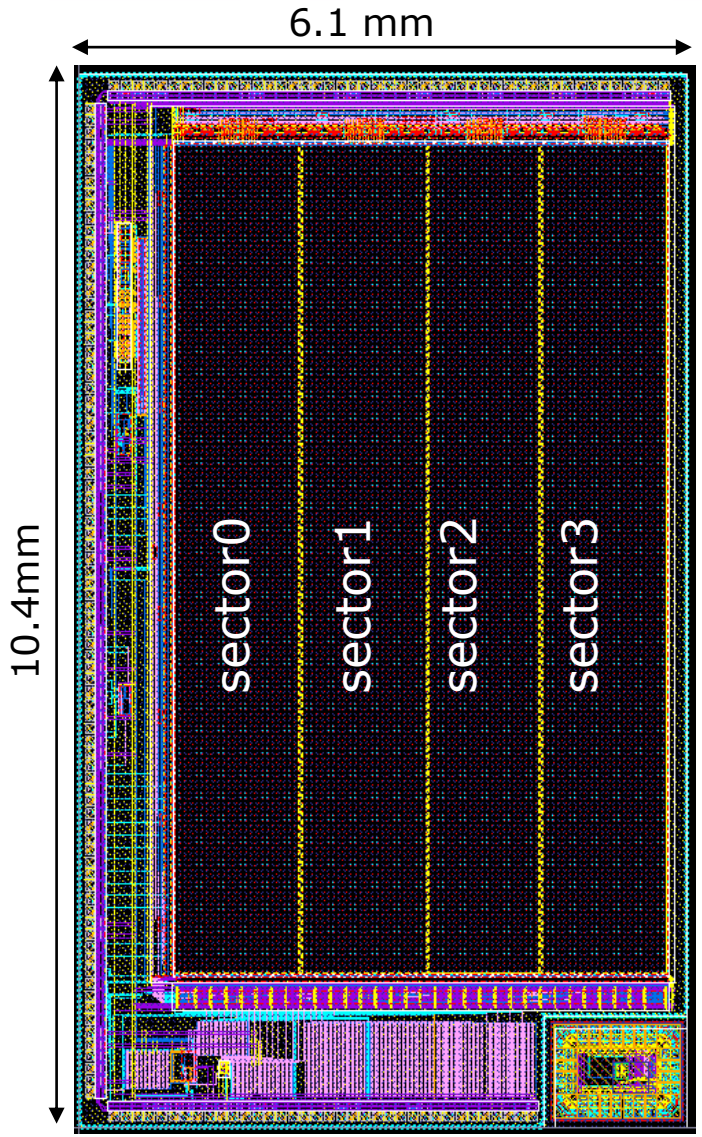
3 variants of digital frontend







Implementation of the pixel array

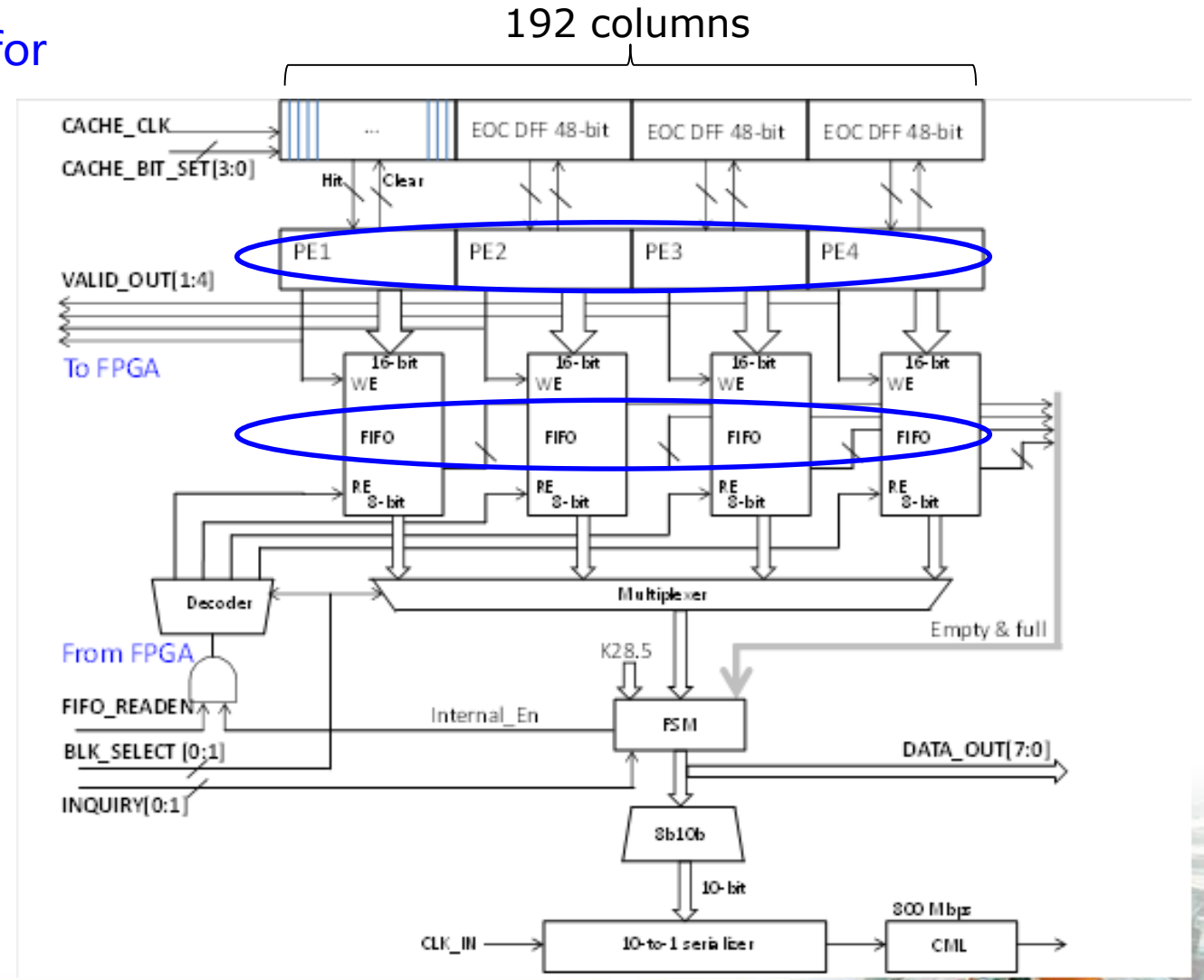


- **Rolling shutter** to avoid heavy logic and routing in the column-wise
  - Shrink the pixel size by ~ 7 μm
- **Full-sized** in the φ direction
  - Matrix coverage: 16 μm * 512 rows = 8.2 mm
  - Matrix readout time: 192ns/row * 512 rows = **98.3 μs/frame**
- **Extensible** in the z direction
  - 48 columns * 4 sectors

Sector	Diode	Analog	Digital	Pixel layout
0	2 + 2 μm	FE_V0	DGT_V0	16×26 μm²
1	2 + 2 μm	FE_V0	DGT_V1	16× 26 μm²
2	**2 + 2 μm**	**FE_V0**	**DGT_V2**	**16× 23.11 μm²**
3	2 + 2 μm	FE_V1	DGT_V0	16×26 μm²

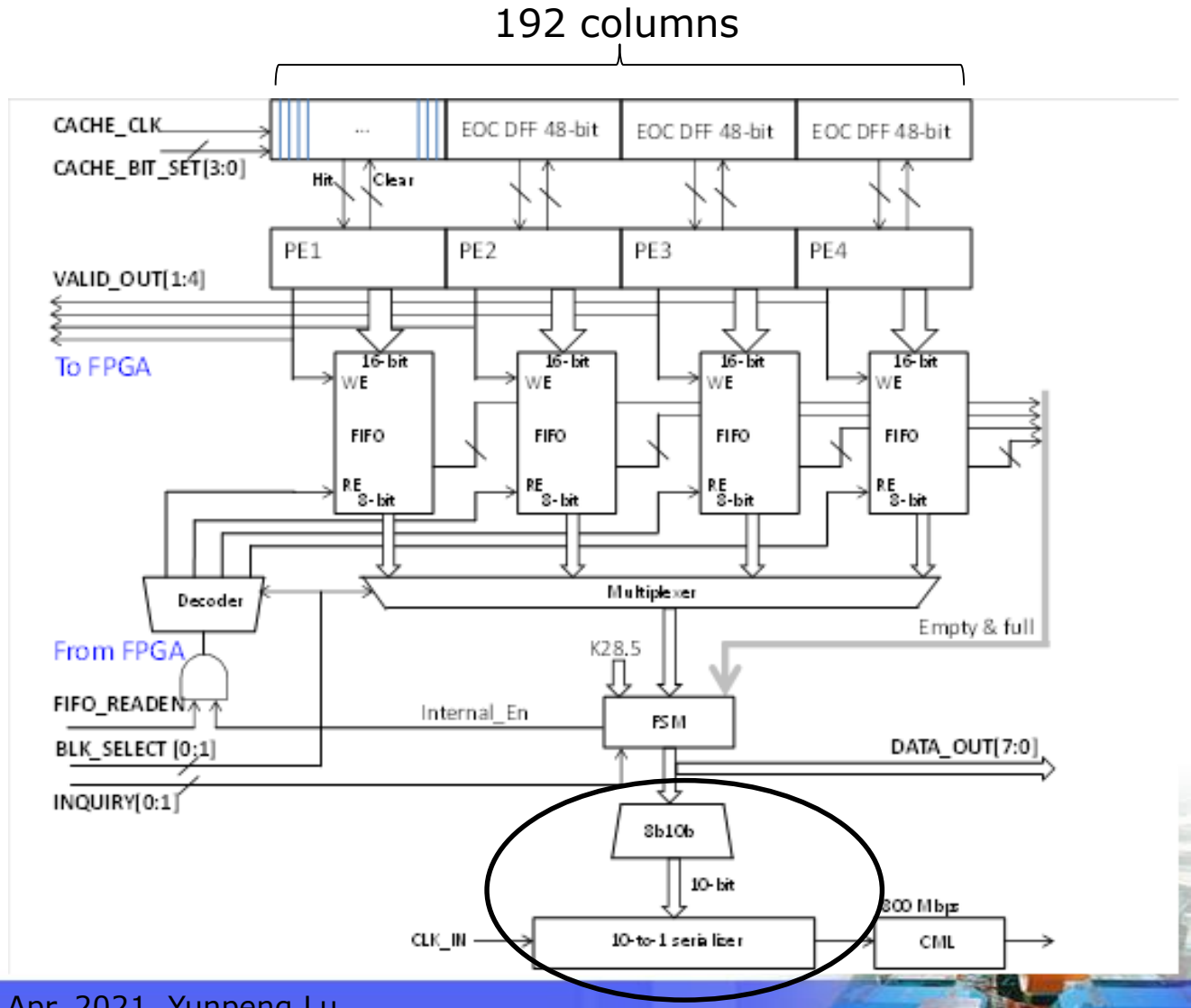
Lower power design in the JadePix3

- A low power frontend of **20 nA static current**, equivalent to 9 mW/cm^2
  - Except for the sector 3, where 60 nA used for the comparison of radiation tolerance
- Zero suppression at the end of column
  - **Priority Encoded (PE)** address of HIT pixel
- Data buffering
  - 4 parallel FIFOs * 48 depth
  - Multiplexer controlled by FPGA
  - Allow the **test of readout strategy**
- Extensible along with the matrix sectors



Engineering consideration in the JadePix3

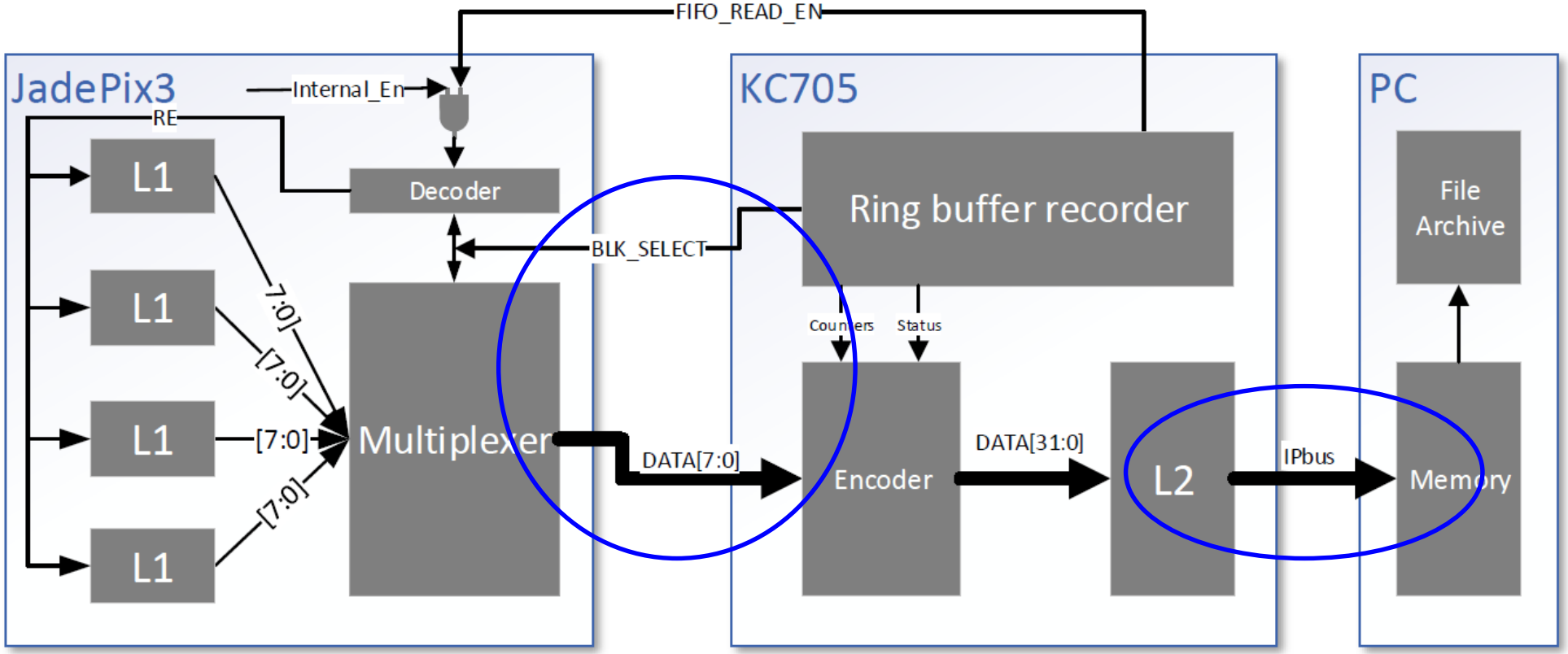
- High speed data transmission modules
  - 8b10b **Encoder**
  - 10-to-1 **Serializer**
  - **PLL**-based clock solution
- **DACs** for the analog biasing
  - 10-bit voltage DAC * 6 channels
  - 8-bit current DAC * 6 channels
- Adjustable **Bandgap** module
- Serial Program Interface (**SPI**)
- Reduced Swing Differential Signal (**RSDS**)
  - Low power differential transceiver



Test system

Sheng DONG, Hulin WANG, Yunpeng LU

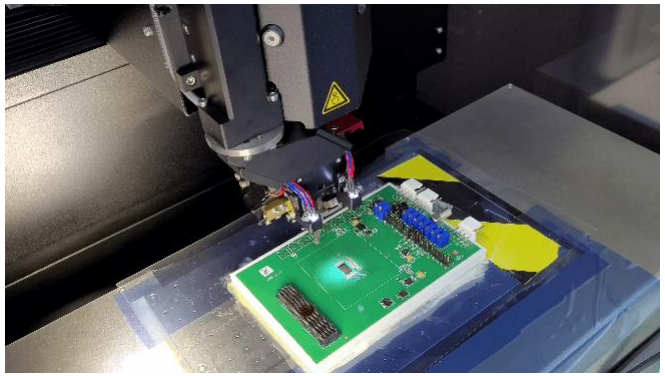
- General-purpose FPGA platform, KC705
  - Well-defined **FPGA firmware**
  - Extensively debugged with the **interactive** JadePix3 chips
- Two test setup deployed in IHEP and CCNU
- IPBUS protocol
  - Reliable high-performance **control link** for particle physics electronics
  - **JUMBO PACKAGE feature** developed and integrated to the new release



Chip-board assembly

Daming SUN, Yunpeng LU

- 7 boards assembled with the Jadepix3 chips
  - **All passed functional tests**
  - Counter measure of ESD proved effective
  - Two chips confirmed broken and replaced
- Good **uniformity** observed
  - Power supply current
  - Bandgap output
  - Analog waveform of frontend
  - Threshold and noise



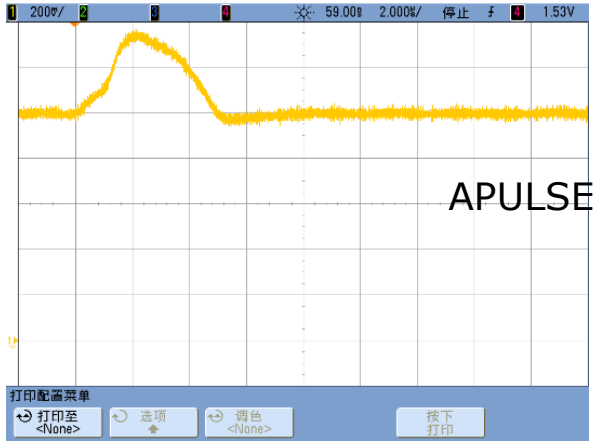
Wire bonding on the JadePix3 chip

Functional verification

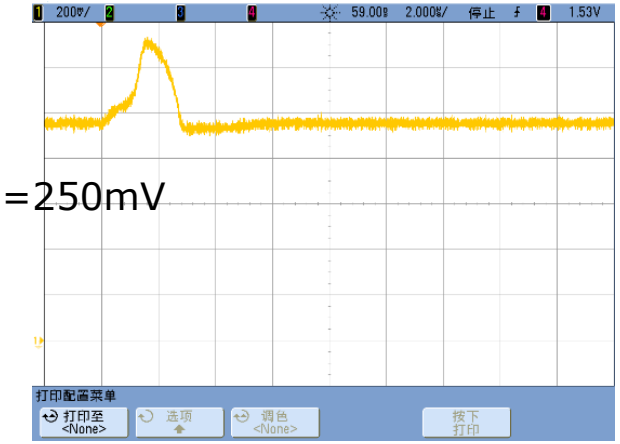
Sheng DONG, Yang ZHOU, Ying ZHANG, Zhan SHI, Yunpeng LU

- **All module** functions verified
  - Configuration of matrix registers
  - Configuration of DAC
  - Pulse test
  - Analog output waveform
  - Data readout
  - PLL clock
  - Serializer output pattern
- Response to the radiation as expected
  - Radiative source ^{55}Fe
  - Cosmic ray
  - **Pulsed laser beam**

Low power frontend



Radiation-enhanced frontend

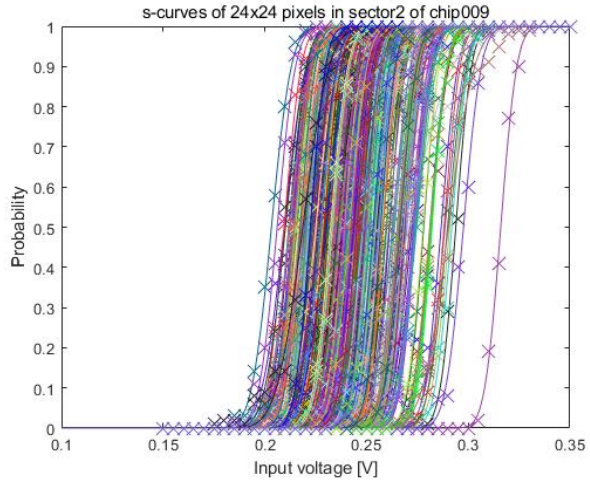


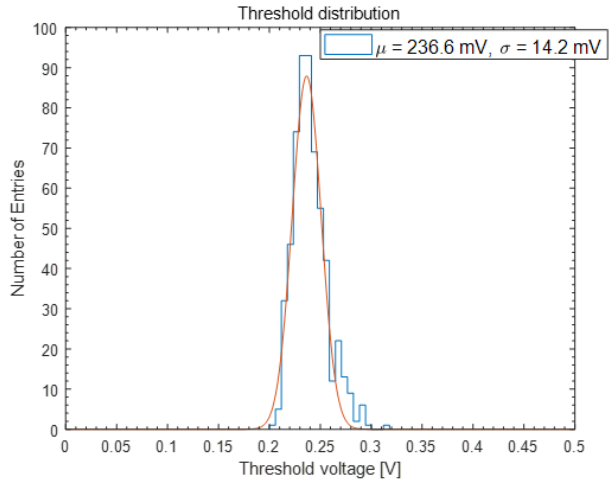
Output pattern of serializer @ 1Gbps

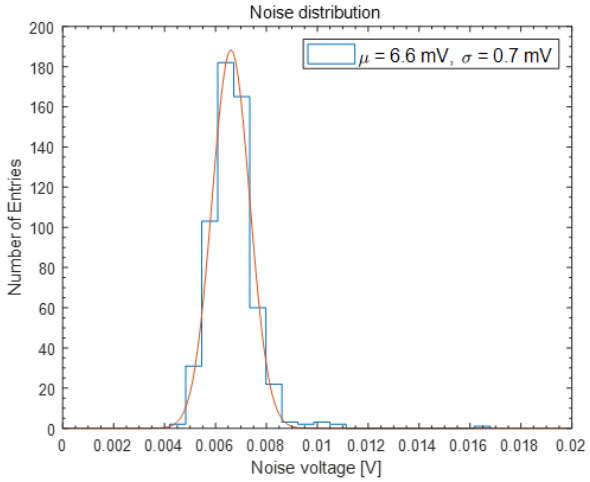
Threshold and Noise

Ying ZHANG, Yang ZHOU, Jing DONG, Yunpeng LU

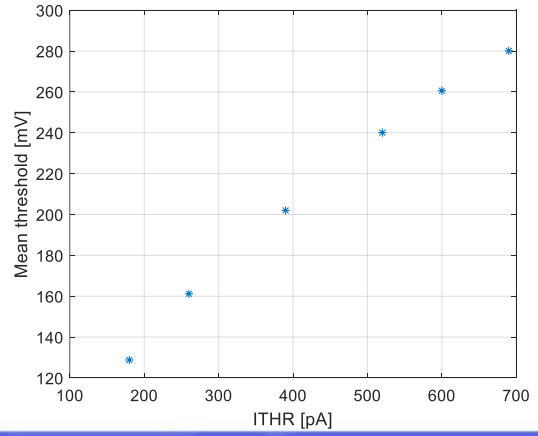
- Pulse amplitude scan and **S-curve** fit (1 mV ~ 0.9 e$^-$)

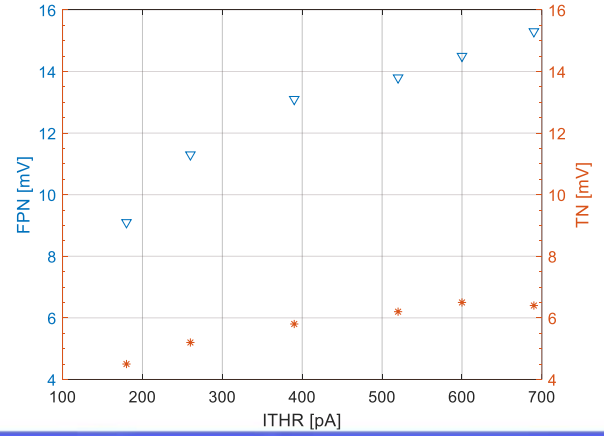


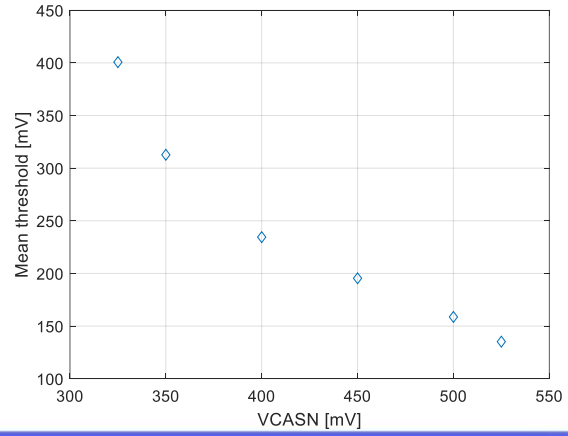


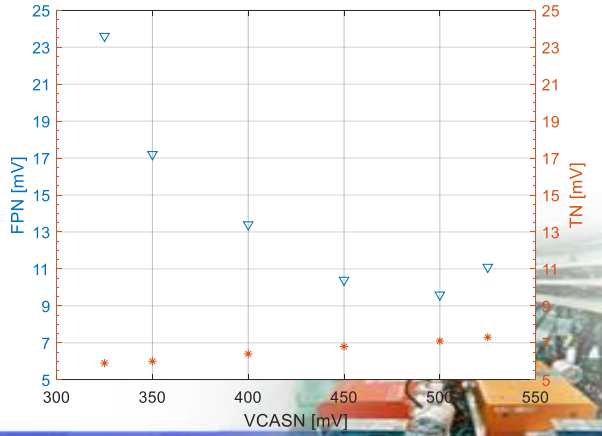


- Parameter scan @ sector 2
  - Threshold = 220e$^-$ @ nominal value of parameter I_{THR} = 0.5 nA, V_{CASN}= 400 mV





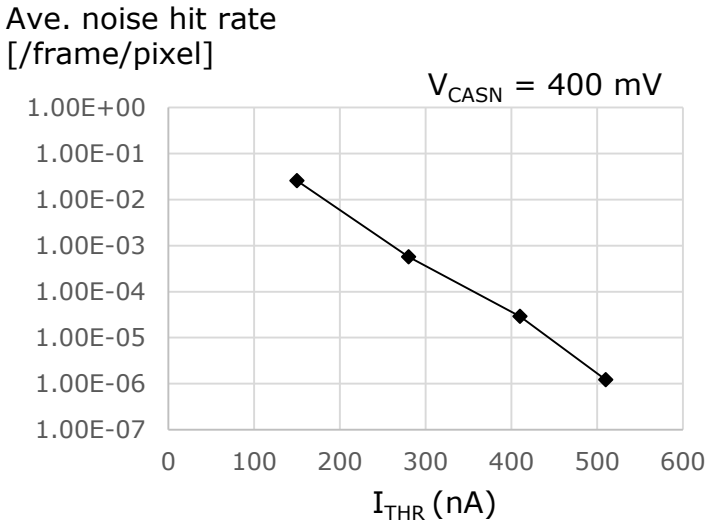


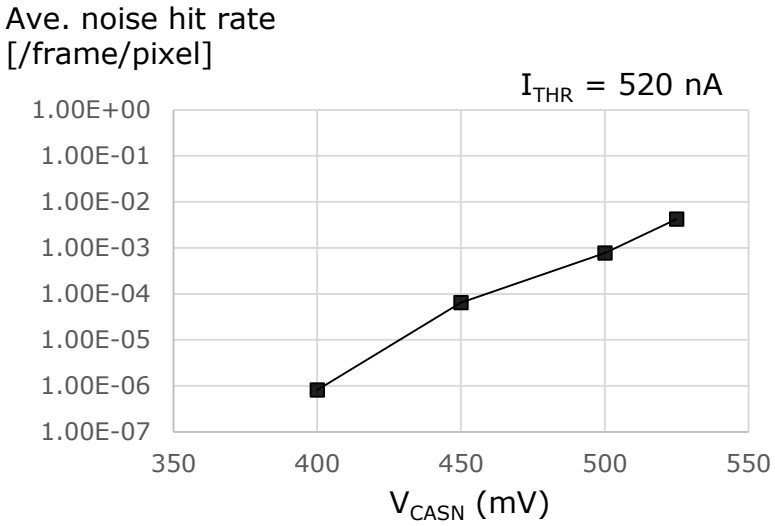


Noise hit rate

Ying ZHANG, Yang ZHOU, Jing DONG, Yunpeng LU

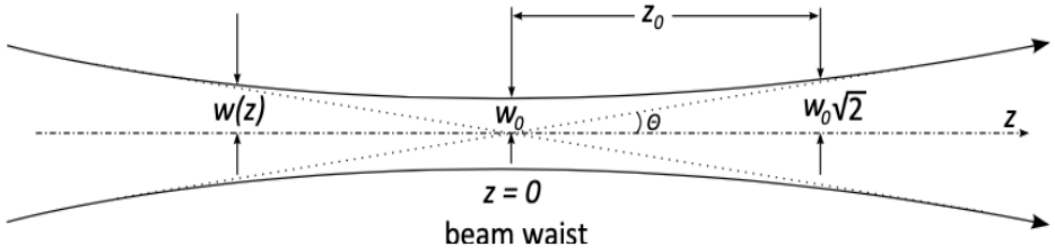
- Average noise hit rate @ Sector 2
  - Noise hit rate ~10^{-6} /frame/pixel

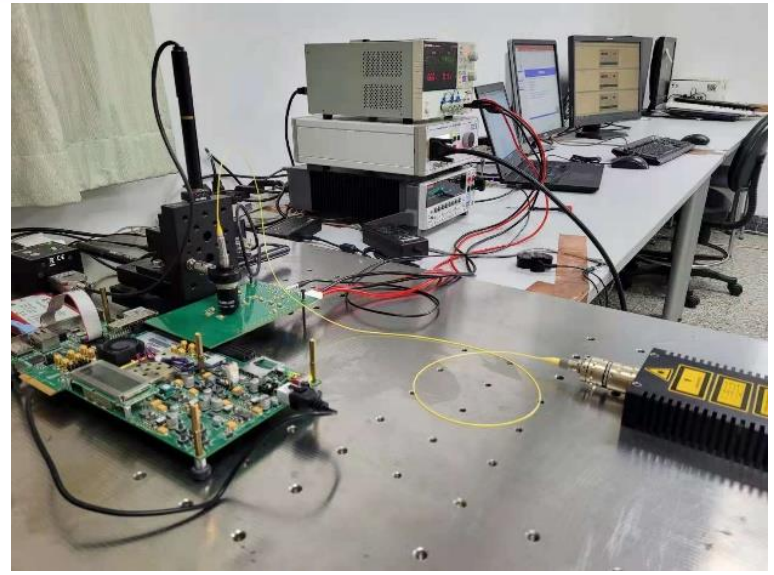




Pulsed laser test

Hulin WANG, Shen DONG, Yunpeng LU



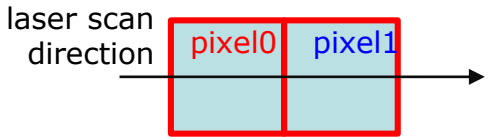


- Laser beam characterization
  - Wavelength: 1064 nm
  - Beam waist ω_0 ~ **1.7 μm**
  - Rayleigh range z_0 ~ 8.5 μm
  - Divergence Angle **θ = ~ 11°**
  - Laser pulse duration ~100 ps
- Laser power tune
  - 0% : maximum power; 100% : minimum power
  - For final results, use 92.7%, 92.9%, 93.3%, 93.5%, 93.7%
  - 92.7% ~ **4 × threshold** (threshold set to ~220 e-)
  - 93.7% ~ **2 × threshold**

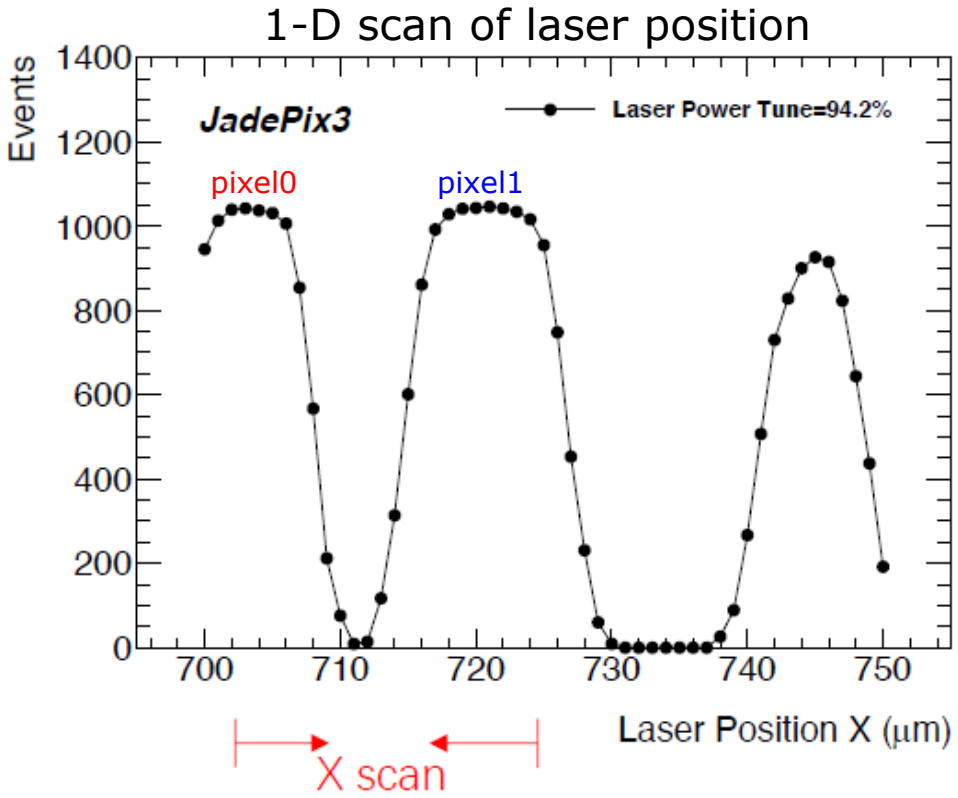
Measurement of position residual

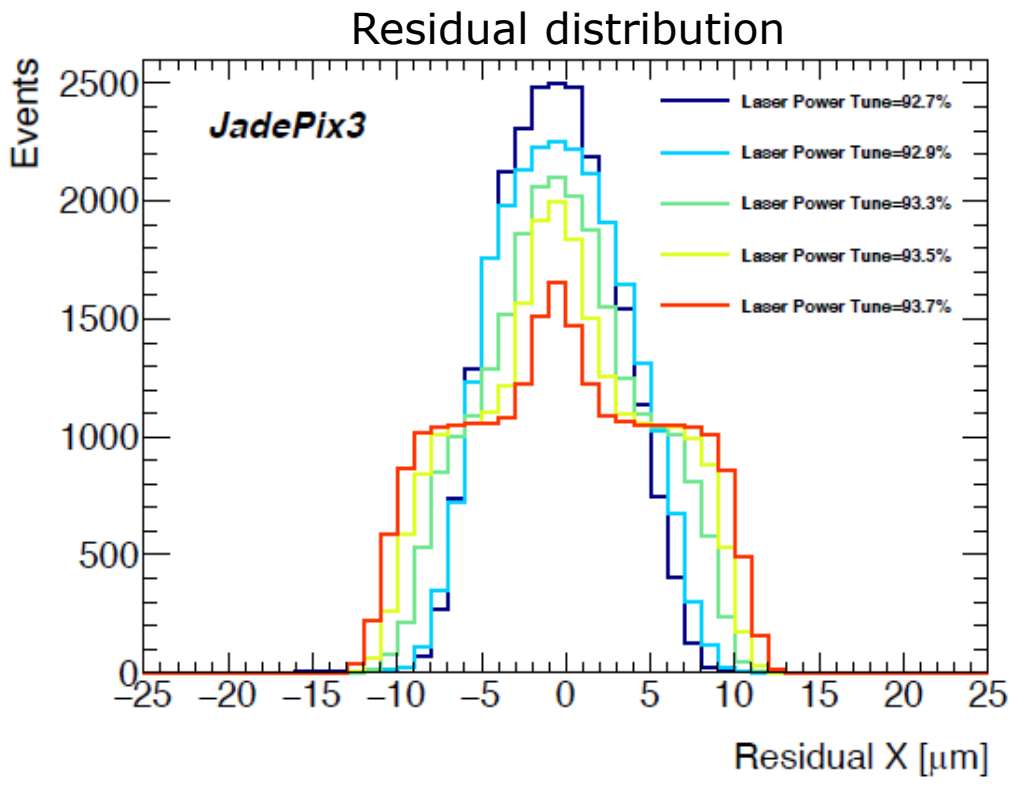
Hulin WANG, Shen DONG, Yunpeng LU

- 1-D scan of laser position
  - Step = 1 *μm*



- Distribution of position residual
  - Reference position: motion stage
  - Measured position: cluster center of weight



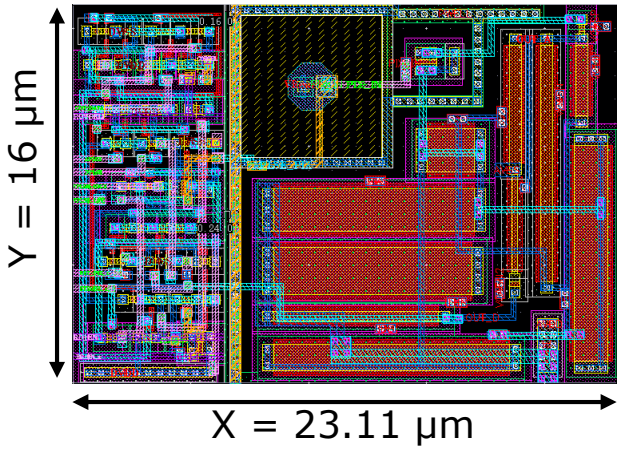


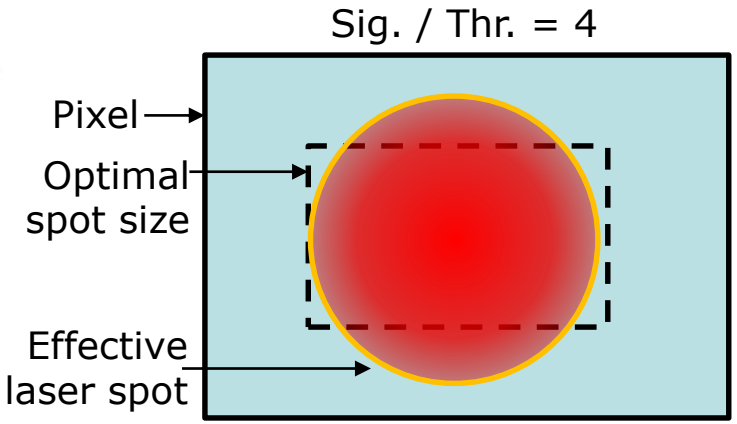
Single point resolution

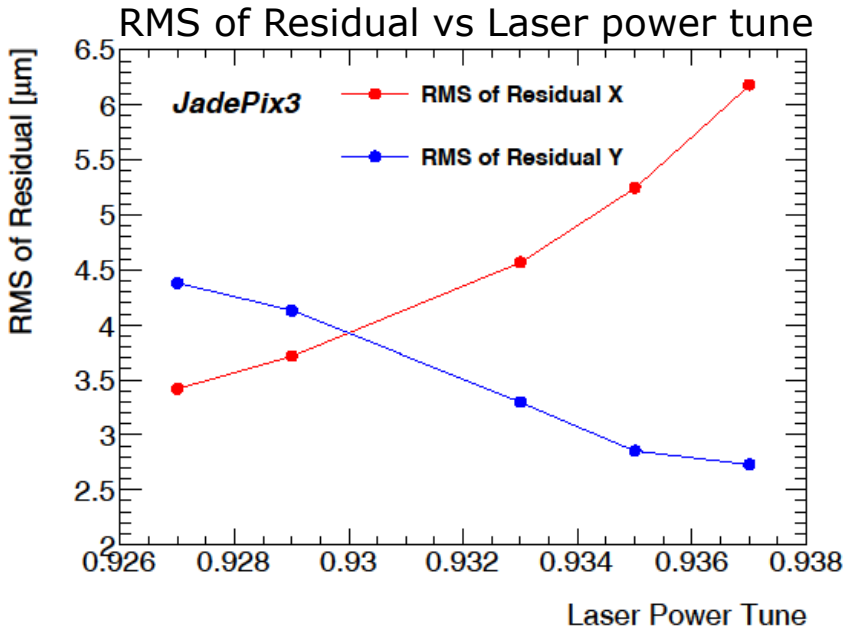
Hulin WANG, Shen DONG, Yunpeng LU

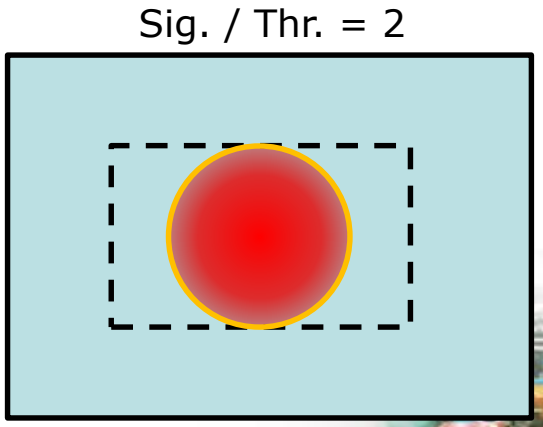
- **Theoretical minimum value** can be approached on both sides
  - 3.34 μm and 2.31 μm respectively
- Charged particle beam is required for a **realistic** measurement
  - σ_y ~ 3 μm is expected thanks to the small pitch on the y side
  - σ_x ~ 5 μm can be achieved by tuning the Sig. / Thr.

Layout of pixel undertest



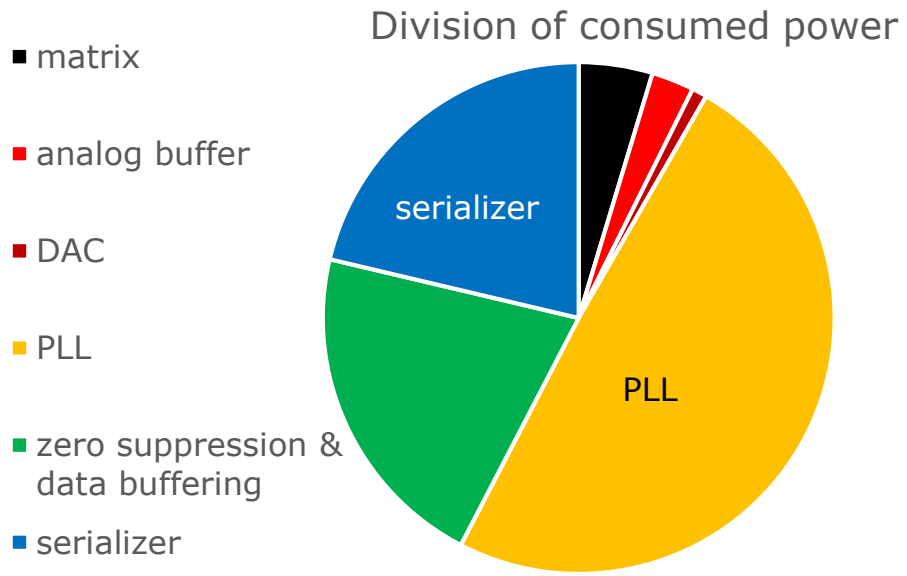






Power consumption

- Average power consumption **46.9 mW/cm²**
  - PLL and Serializer **not included**
- **Extrapolated** to a full size chip of 1 cm*2.56 cm
  - Average power **91.44 mW/cm²**
  - PLL and Serializer included
- **Test-specific** function > 15 mA
  - Analog buffer (1.8mA)
  - LVDS receiver (1.74mA)
  - PLL test output (11.5mA)



Extrapolation of average power consumption

	512*192 (JadePix3)	512*1024 (Full-sized chip)
Matrix	3.15 mA	16.79 mA
Zero suppression and data buffering	12.47 mA	66.47 mA
Other modules	46.82 mA	46.82 mA
Sum	62.44 mA	130.08 mA

Rolling Shutter Readout

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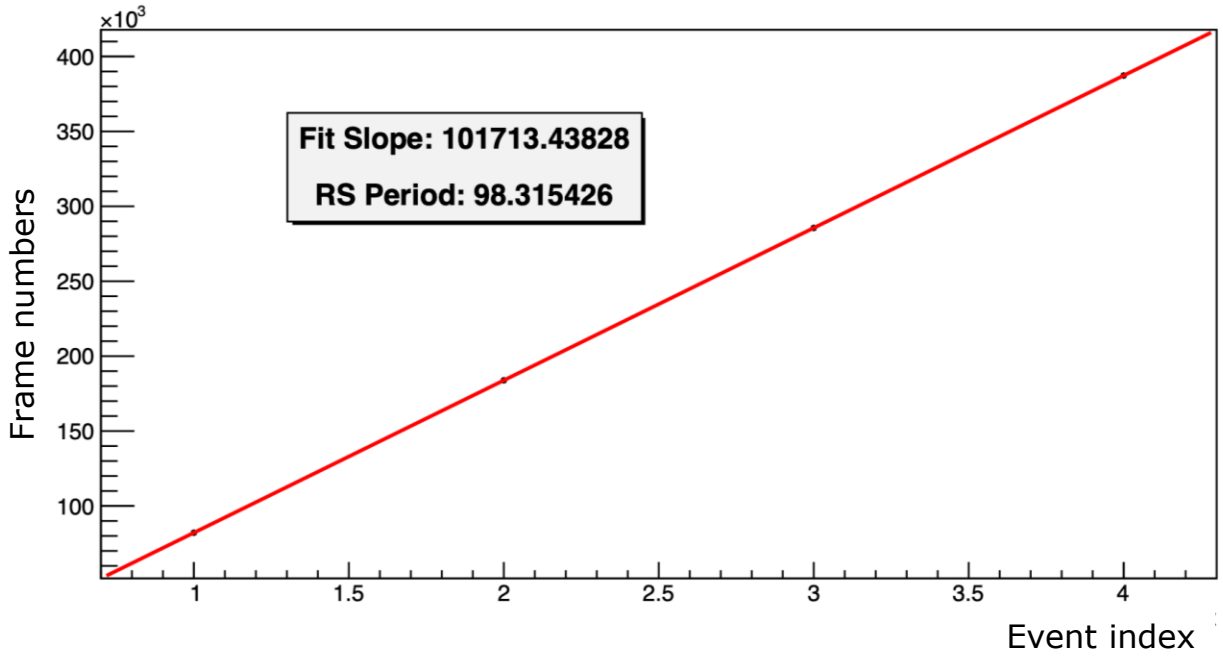
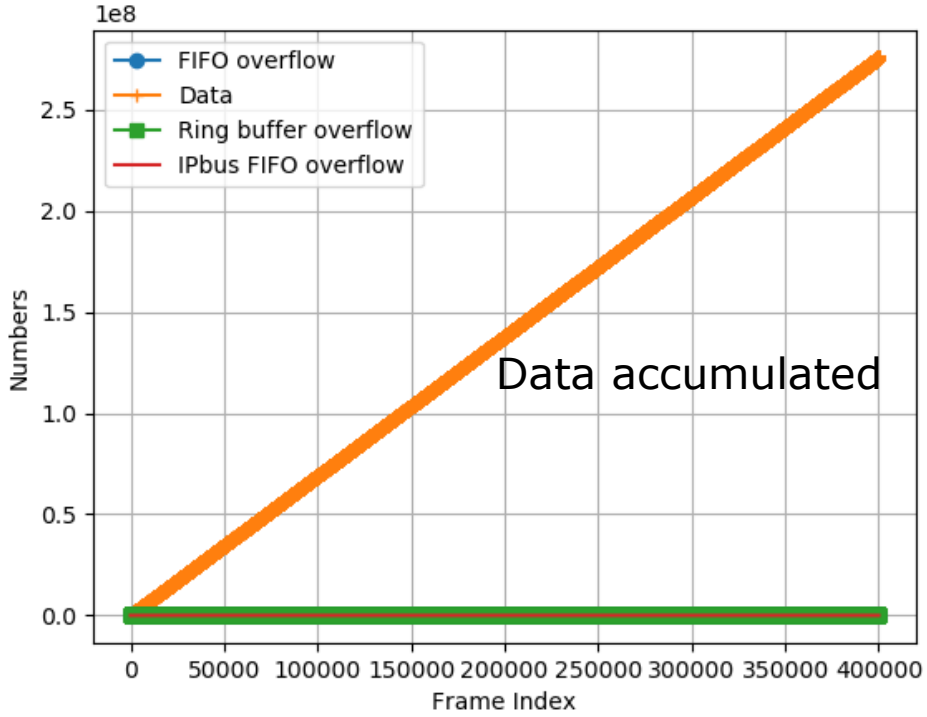
- Frame period (**Integration time**)
  - Count the frame numbers between 2 events
  - Divide the event interval: 10 s
  - Frame period: **98.315 μs**
- Stability test
  - Hit number per event: 2048
  - Event interval: 110 μs
  - Data throughout: **595.8 Mbps * 39.3 s**





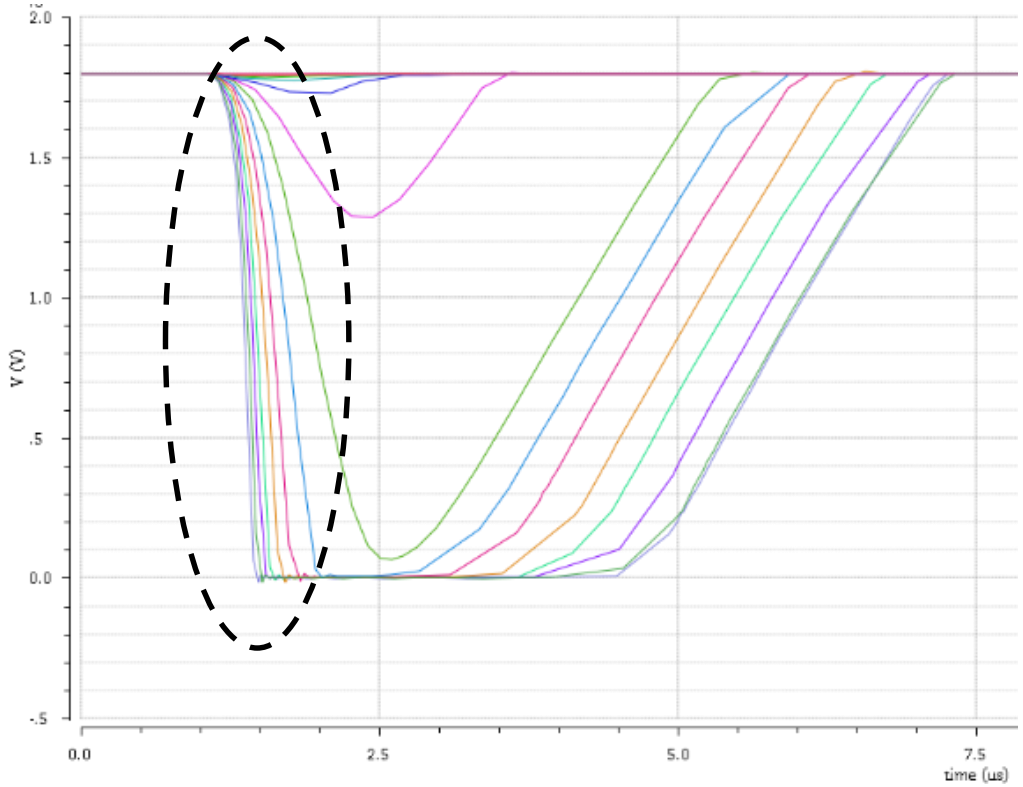
Summary

- JadePix3 is designed for the baseline scheme of **double-sided** structure
  - Optimized for high resolution, low power and modest readout speed
- Portable and reliable **test systems** developed and deployed in IHEP and CCNU
- Performance **consistent with the design** targets
  - Low threshold and noise
  - Single point resolution 3 ~ 5 μm
  - Low power < 100 mW/cm^2
  - Integration time < 100 μs
- More test to do
  - Cosmic Muon and ^{90}Sr
  - Beam test and irradiation

Outlook: Integration time 100 µs → 1 µs

- Hit registered at the **fast leading edge**
  - Customized D-Flipflop verified in JadePix3 / Sector 1
- Priority encoder **embedded into the column pairs**
  - Pixel size ~ 20 µm * 30 µm for tier 2
- Further optimization of power consumption
  - The data transmission modules: PLL, Serializer…
- Design expected in the 2nd half of 2021
  - JadePix3 design team
  - Reuse of verified modules

Pulse shapes of different signal charge



JadePix3 study group

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Thank you for your time!