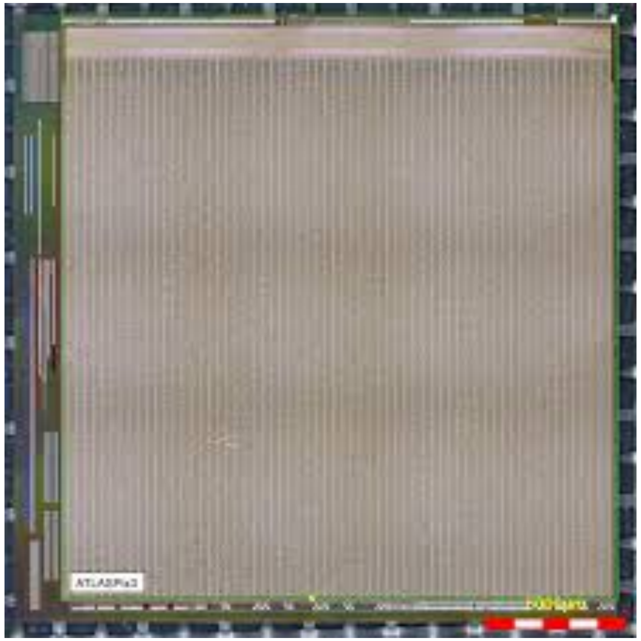
University of BRISTOL

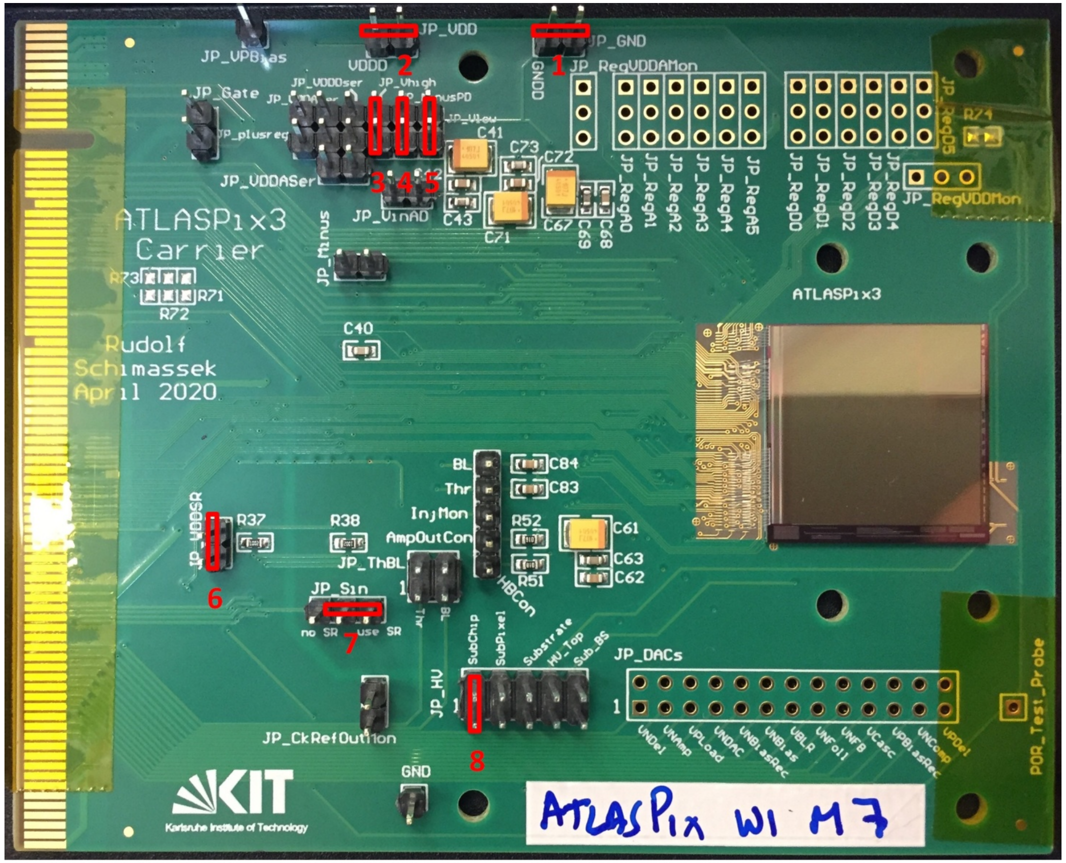
HV-CMOS sensor design and test



Dr. Jaap Velthuis

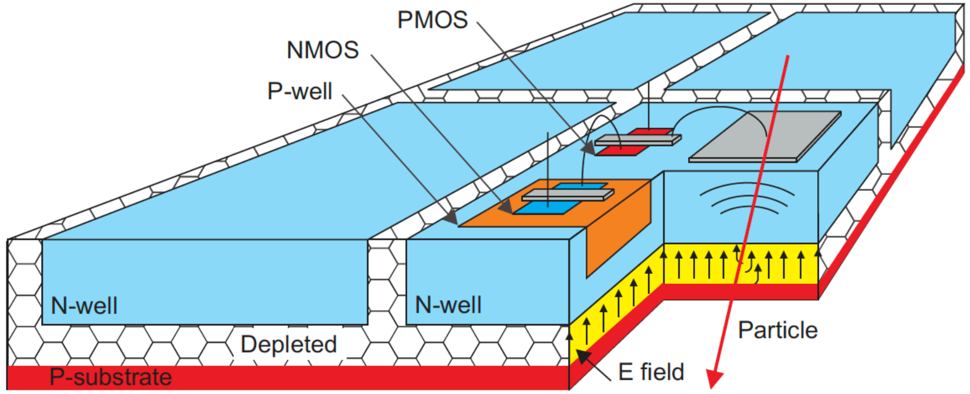
HV-CMOS sensor design and test

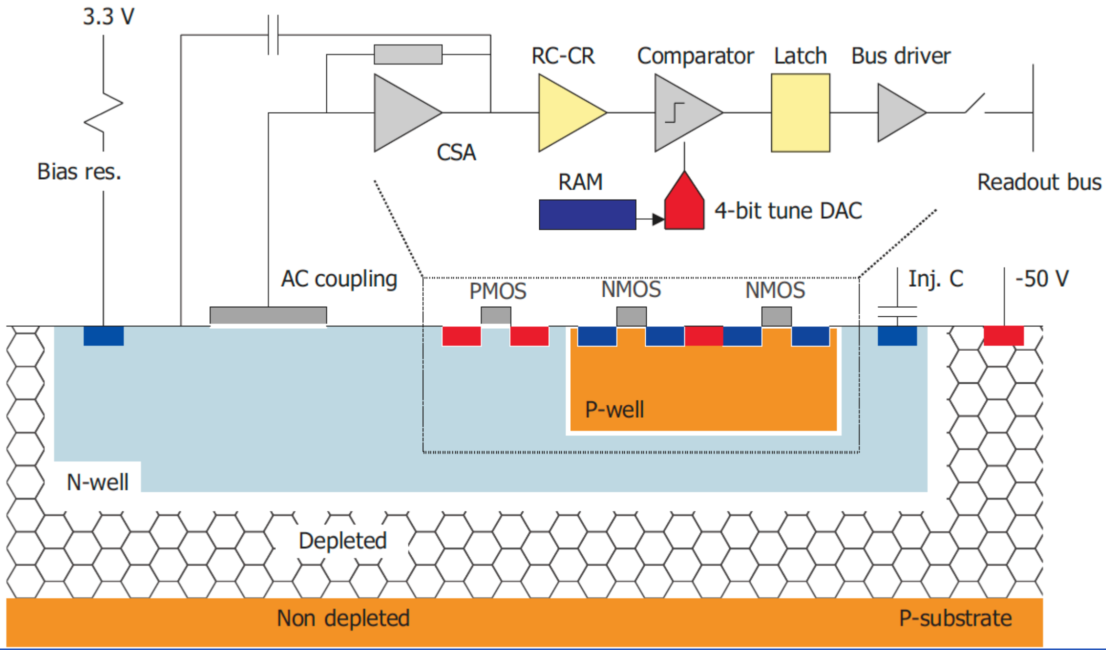
- Workhorse ATLASPix3
- Testing ongoing at 4 sites
  - Tuning
  - Signal tests
    - Cosmics
    - Sources
  - Testbeam
- Read out systems
- Future steps ATLASPix3
- ARCADIA
- Summary



HV-CMOS sensors

- HV-CMOS combines advantages of CMOS sensors
  - Thin, low power
- with the advantages of a depleted sensor
  - Fast and efficient charge collection
- Standard readout chain
  - PMOS transistors AC-coupled in N-well
  - NMOS transistors in P-well inside the N-well
- N-well is biased to generate a depleted region





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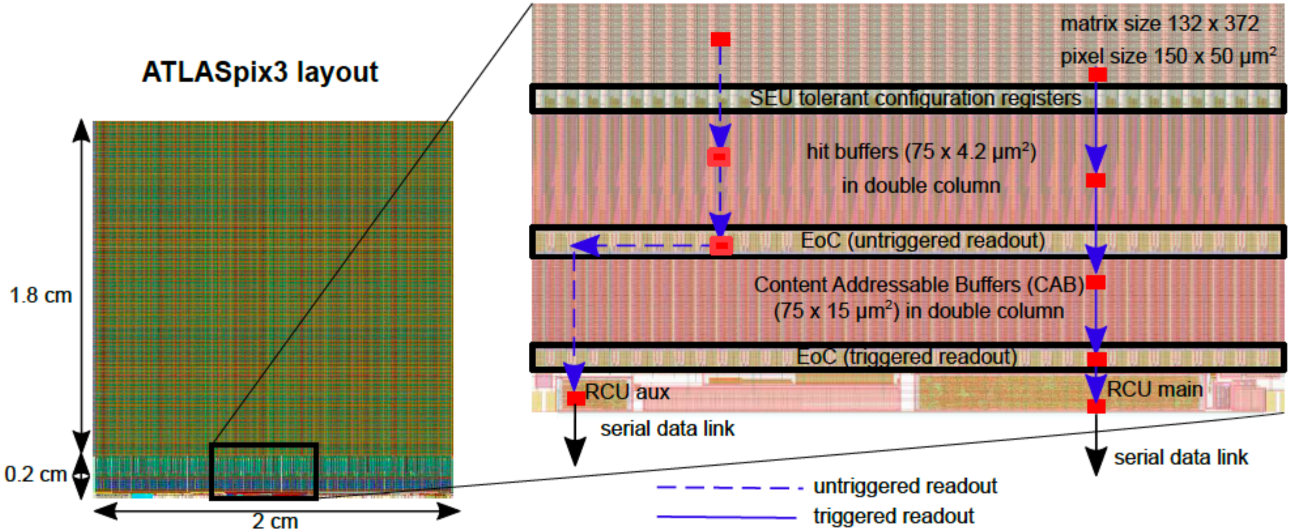
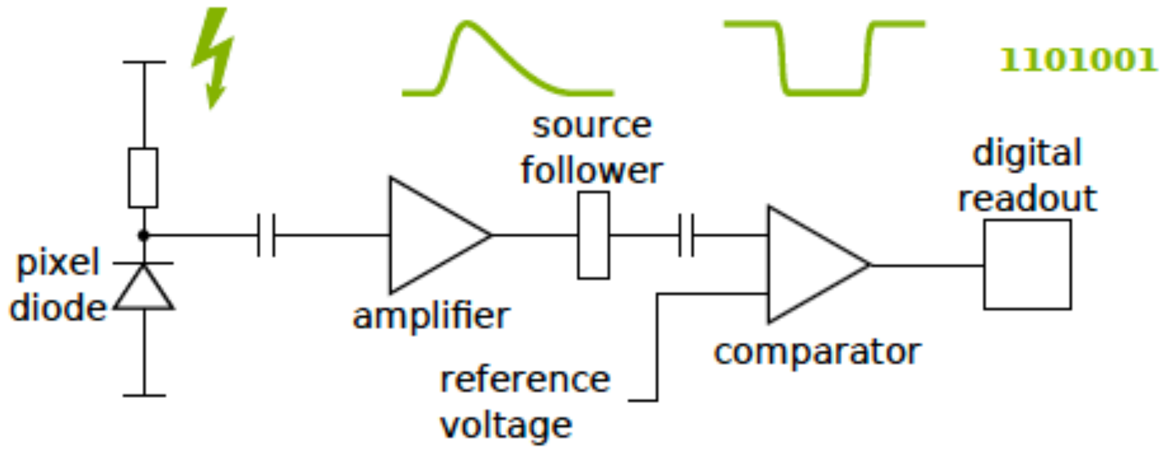
ATLASPix3

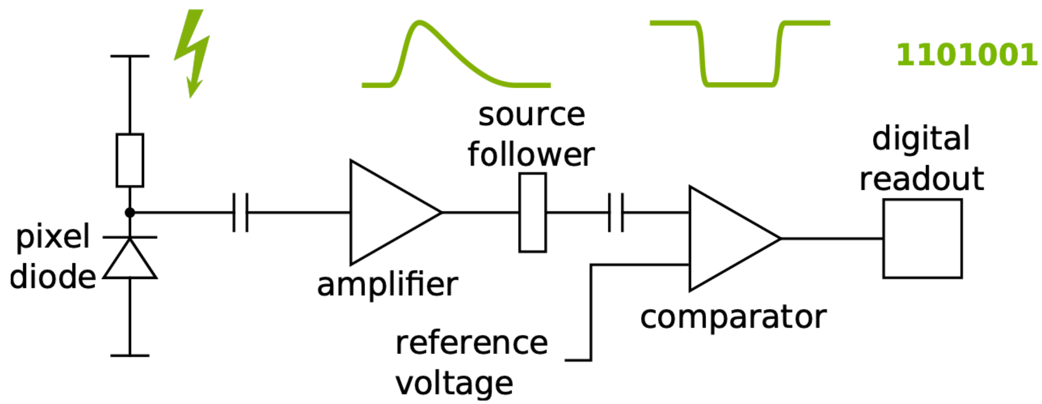
- ATLASPix3 is the first full reticle size HV-CMOS sensor
  - 2×2 cm^2 chip
- Designed in AMS/TSI 180 nm process
- Designed for quad modules
- 132 columns with 372 pixels
- pixel size is $50\mu m \times 150\mu m$
- Binary with ToT as signal proxy

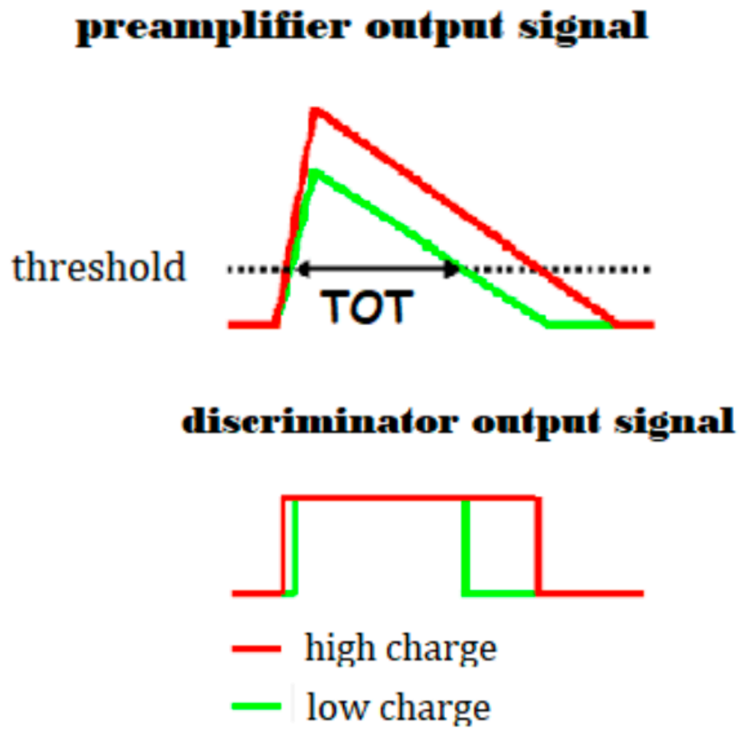




ToT proxy

- A hit is detected and stored when a signal exceeds a threshold.
- The signal is shaped into a triangle. The Time-over-Threshold (ToT) is then stored as the signal value.
- Works great but has issues
  - Trigger time stamp for same event with small signal occurs later.
  - Threshold dispersion leads to local variations in efficiency
  - Relationship between ToT and signal is not linear

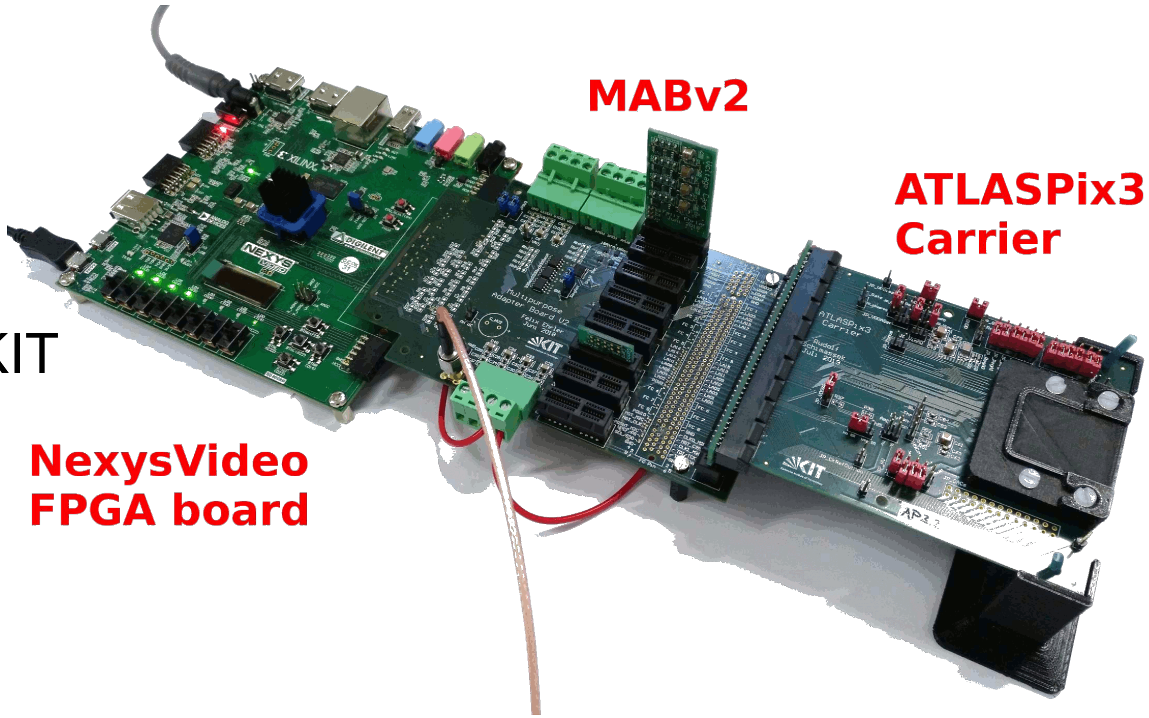




Testing at 4 locations

- IHEP
- Edinburgh/Lancaster
- University of Milan
- Bristol

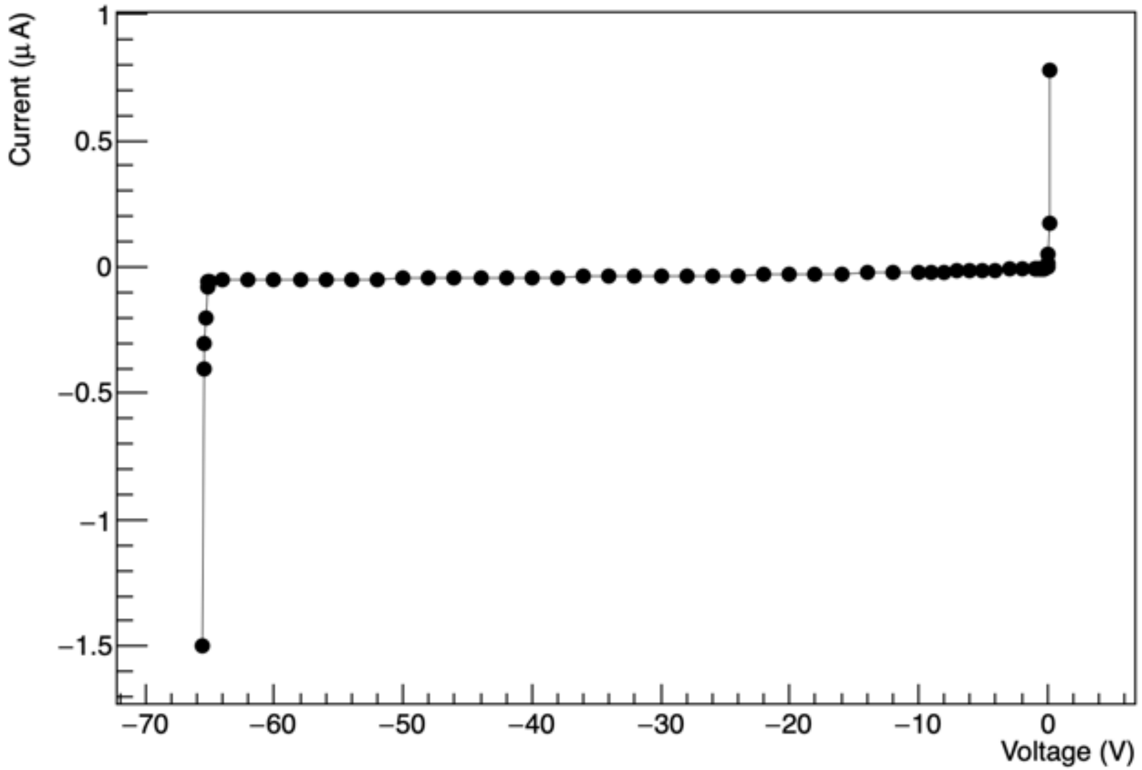
- With great support from KIT (Rudolf Schimassek)



- Results shown are taken from results of all above institutes and not a complete set of 1 sensor.

IV curve

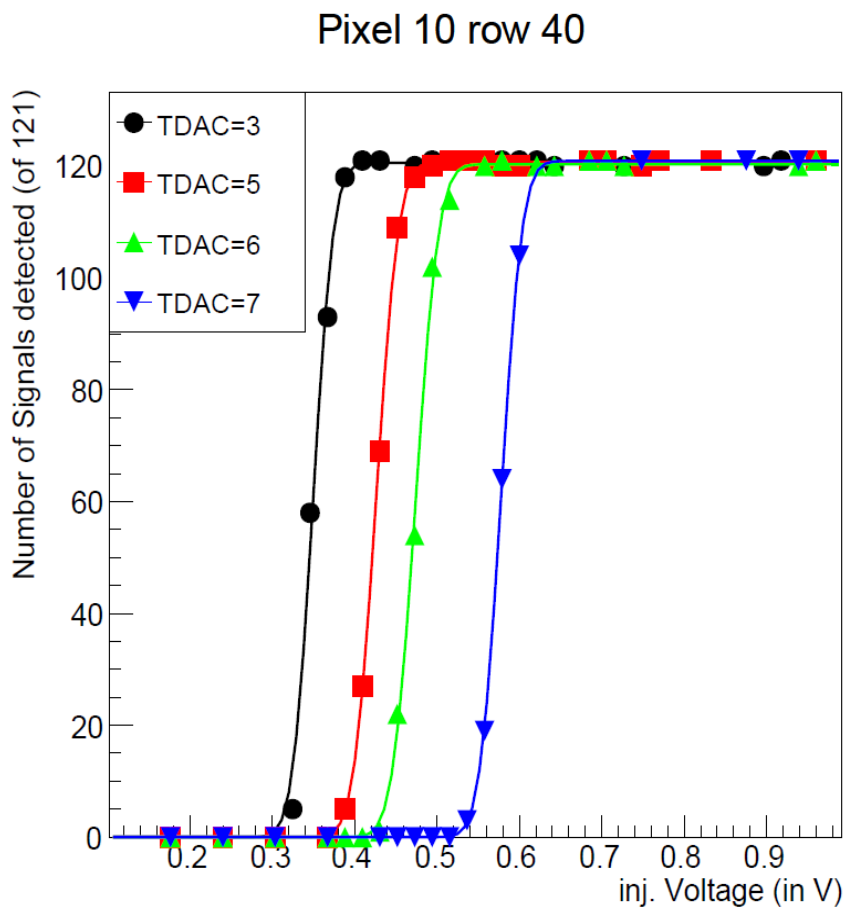
- Sensor behaves like a normal reverse biased diode.



Threshold tuning

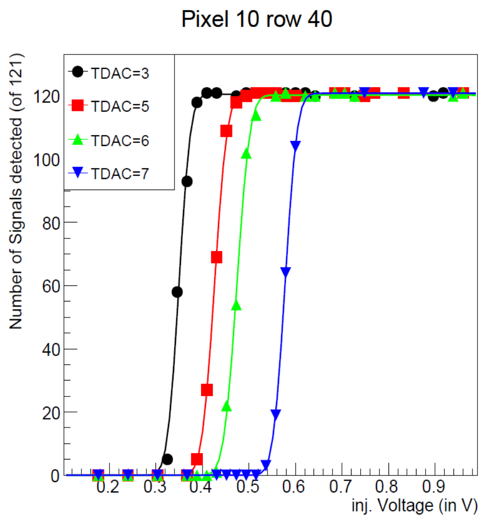
- Threshold voltage for each pixel has to be tuned to get homogenous sensor response.
- S-curves represent the number of impulses that are detected for injected signals of increasing height

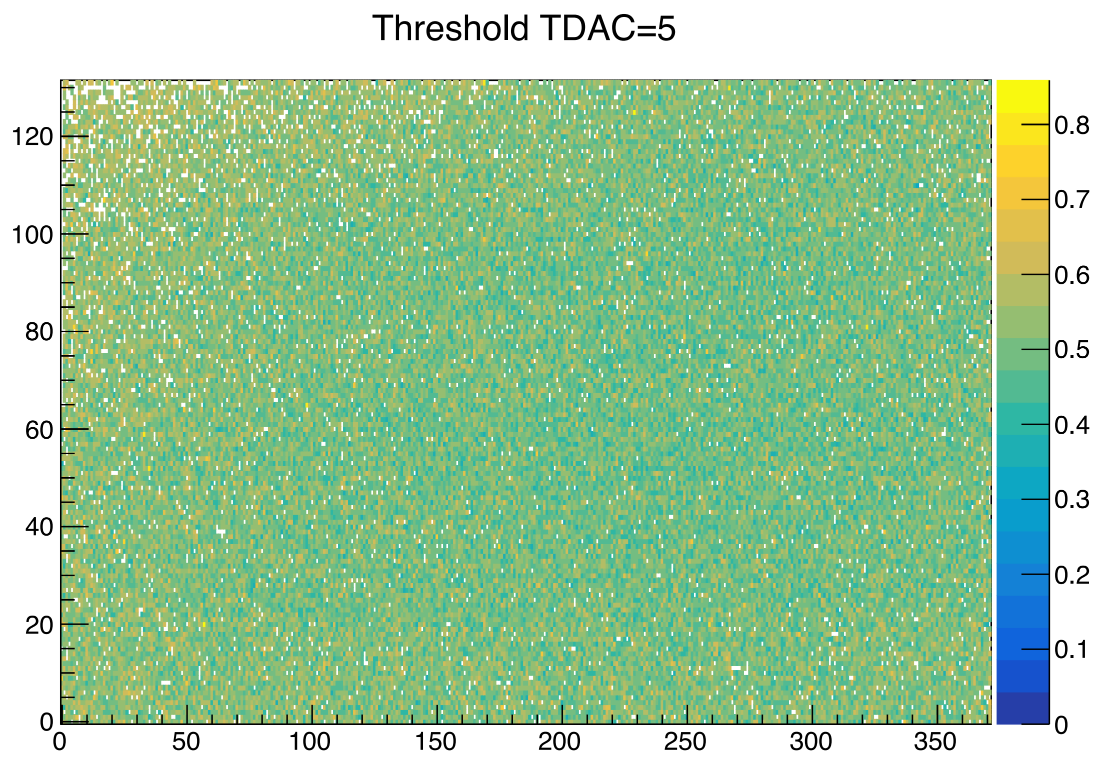
- Studied S-curves for all pixels with various TDAC values.
- S-curves are fitted with an error function. Extracted noise and threshold.
  - Increasing TDAC moves S-curve to higher voltages.



Threshold voltage map

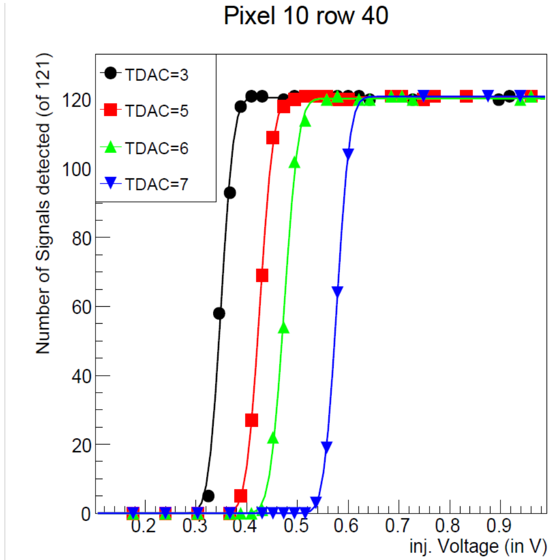
- Threshold is the 50% point of the S-curve
- Threshold map for TDAC=5
  - Some pixels do not switch between on and off for TDAC=5
- The threshold result is quite uniform.

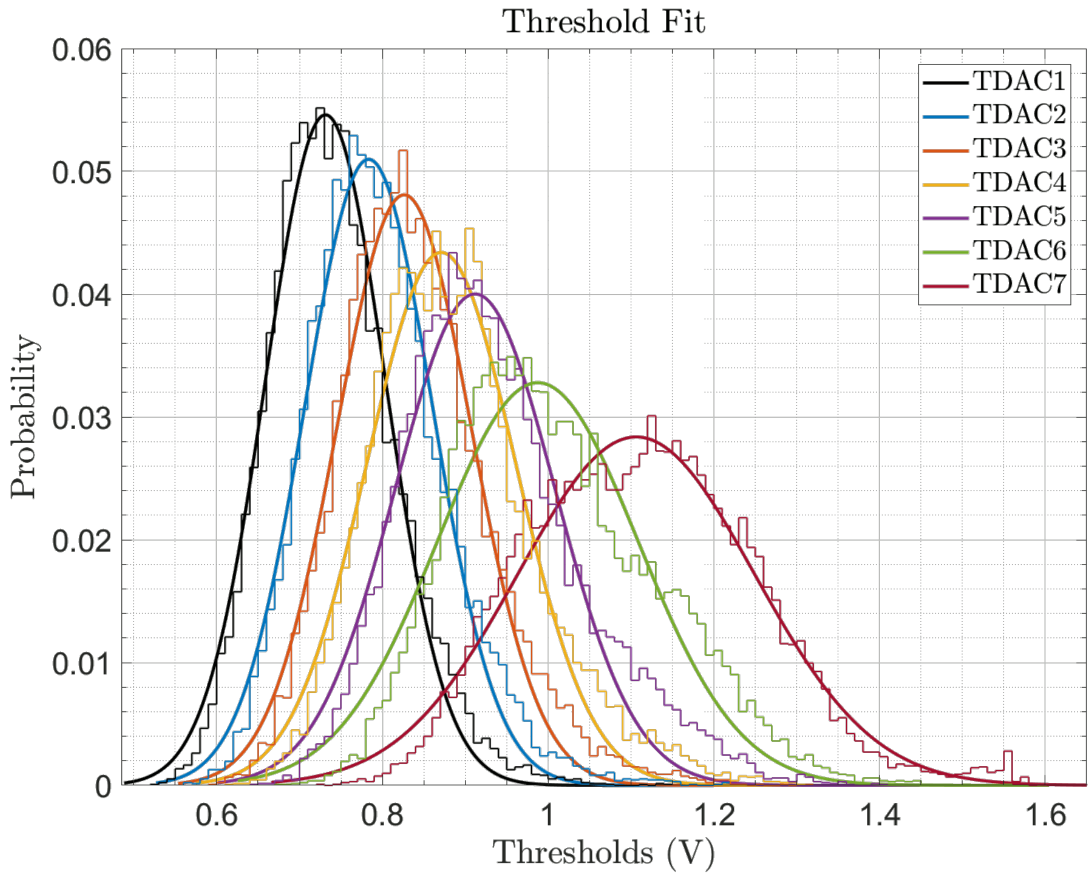




Threshold voltage map

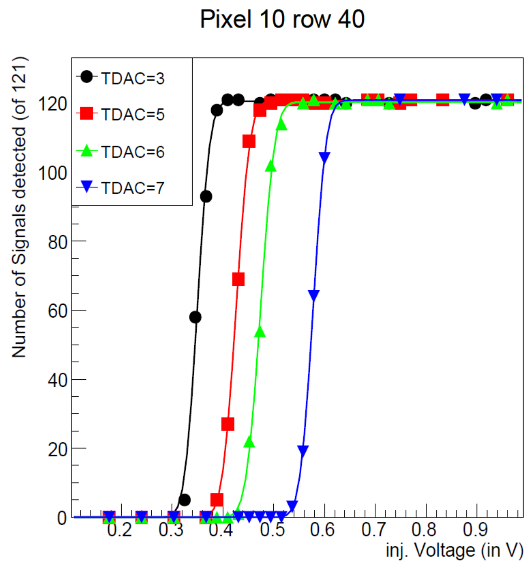
- For larger thresholds, the distributions move towards larger thresholds and the dispersion increases

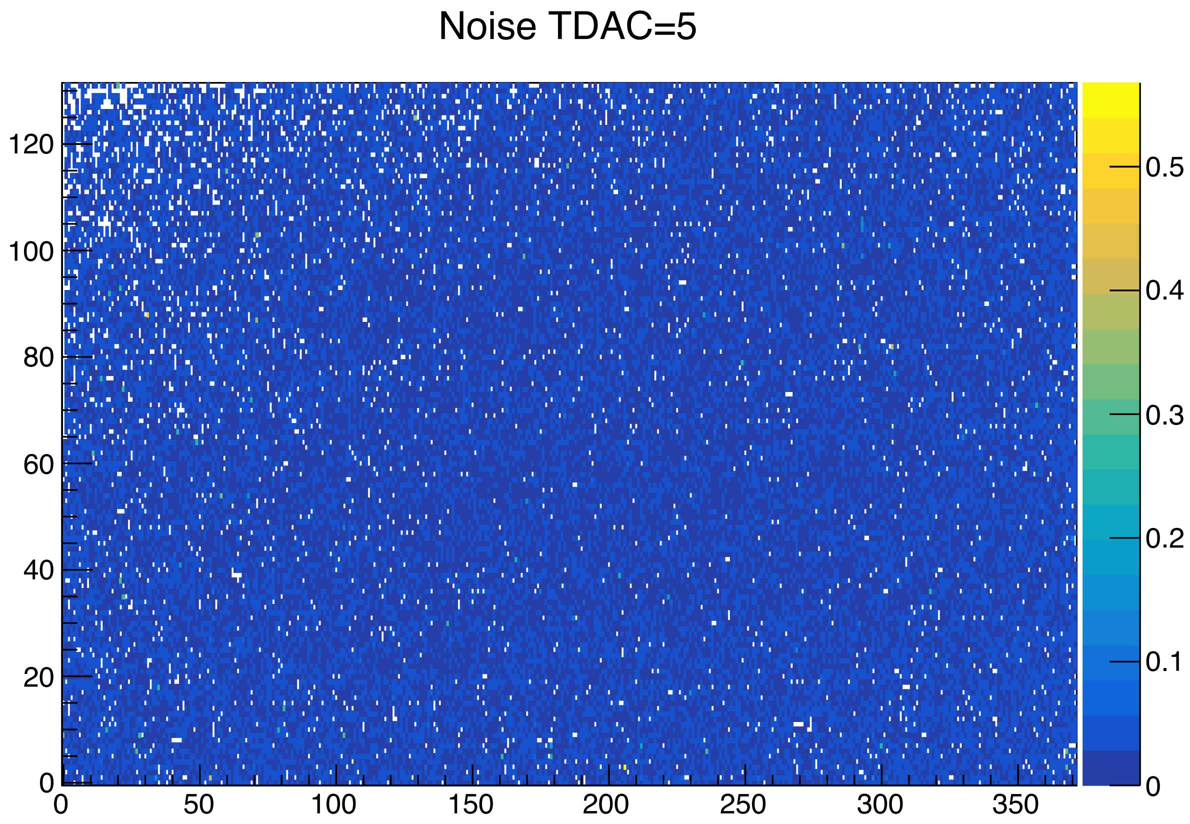




Noise map

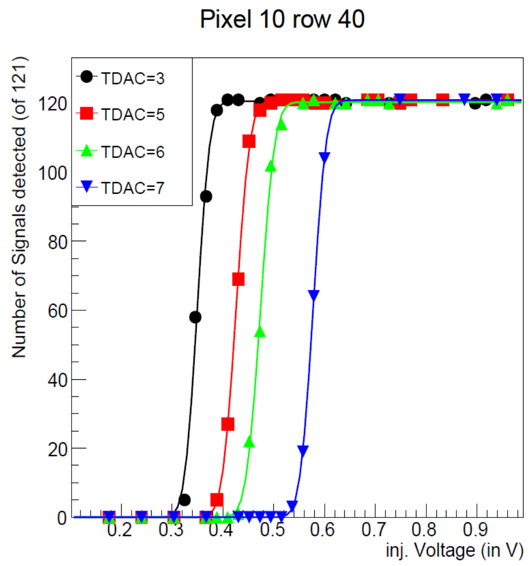
- Noise determines the slope of the S-curve
- Noise map for TDAC=5
  - Some pixels do not switch between on and off for TDAC=5
- Noise result is quite uniform.

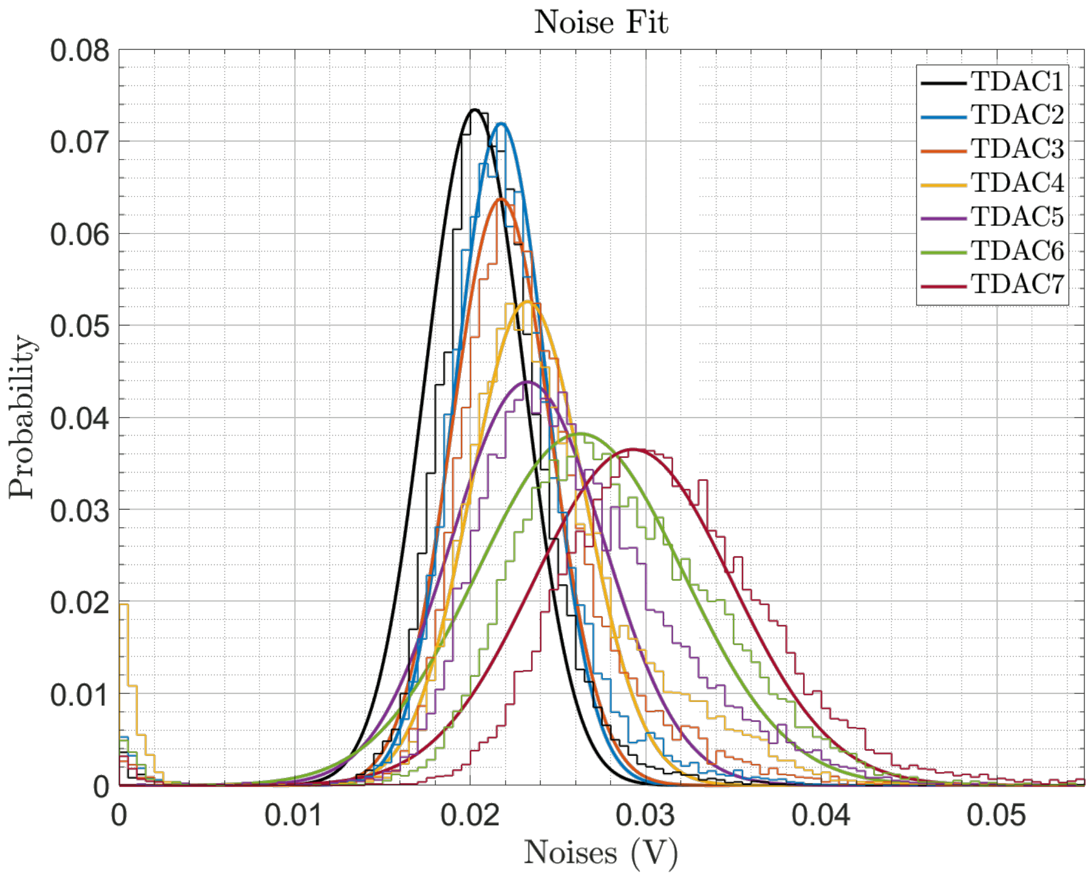




Noise map

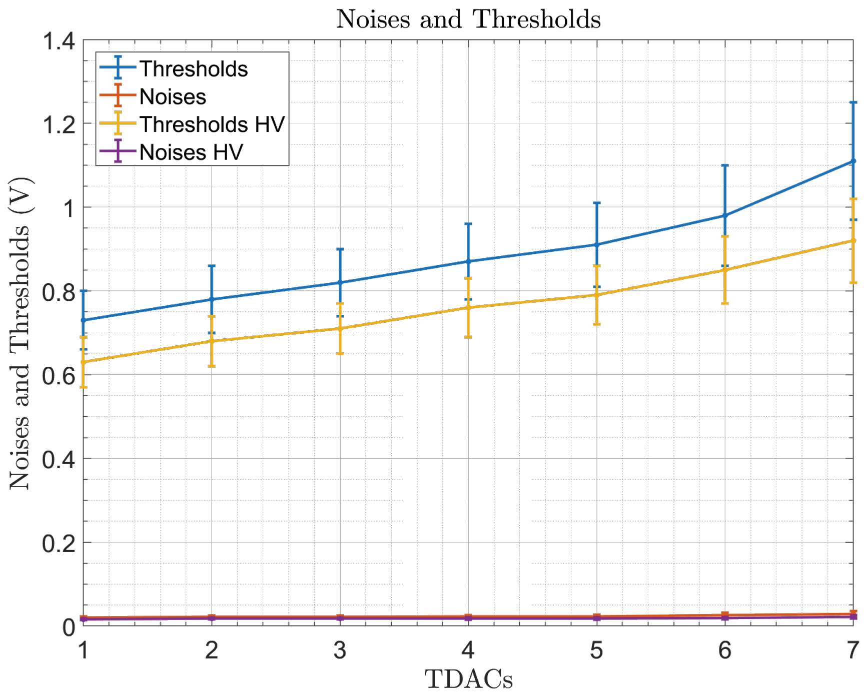
- Higher TDAC yields higher noise and higher dispersion

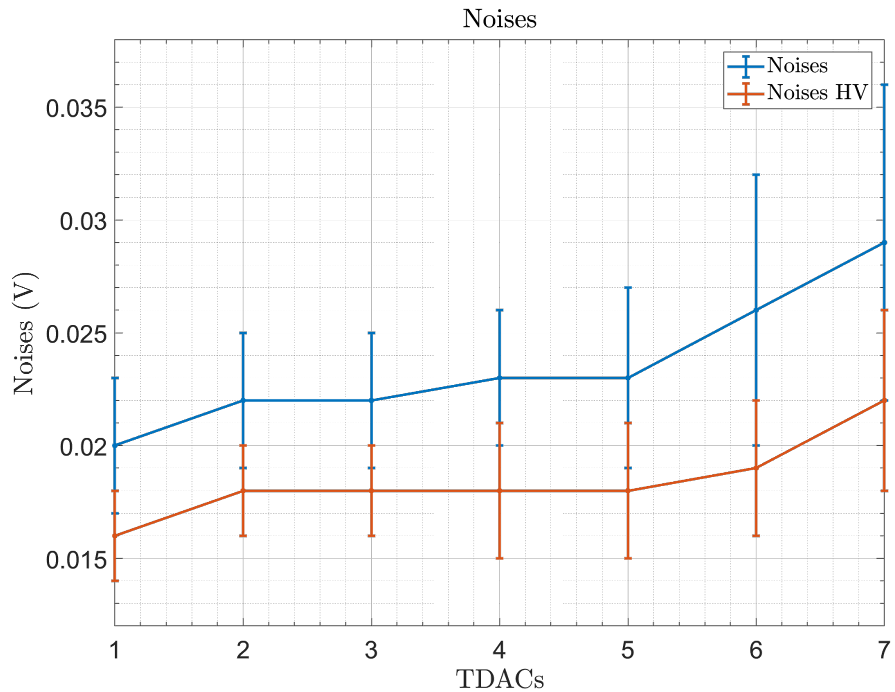




Noise and threshold are HV dependent

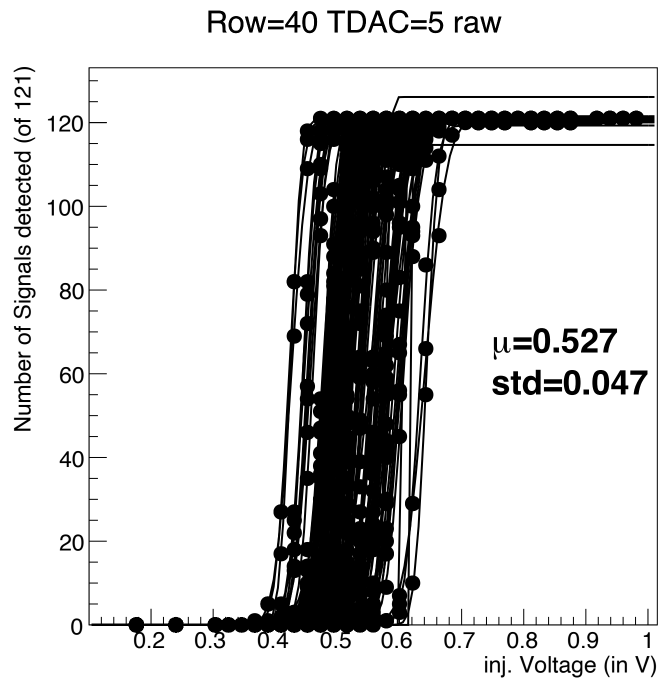
- The threshold and noise are both dependent on the HV and the TDAC.

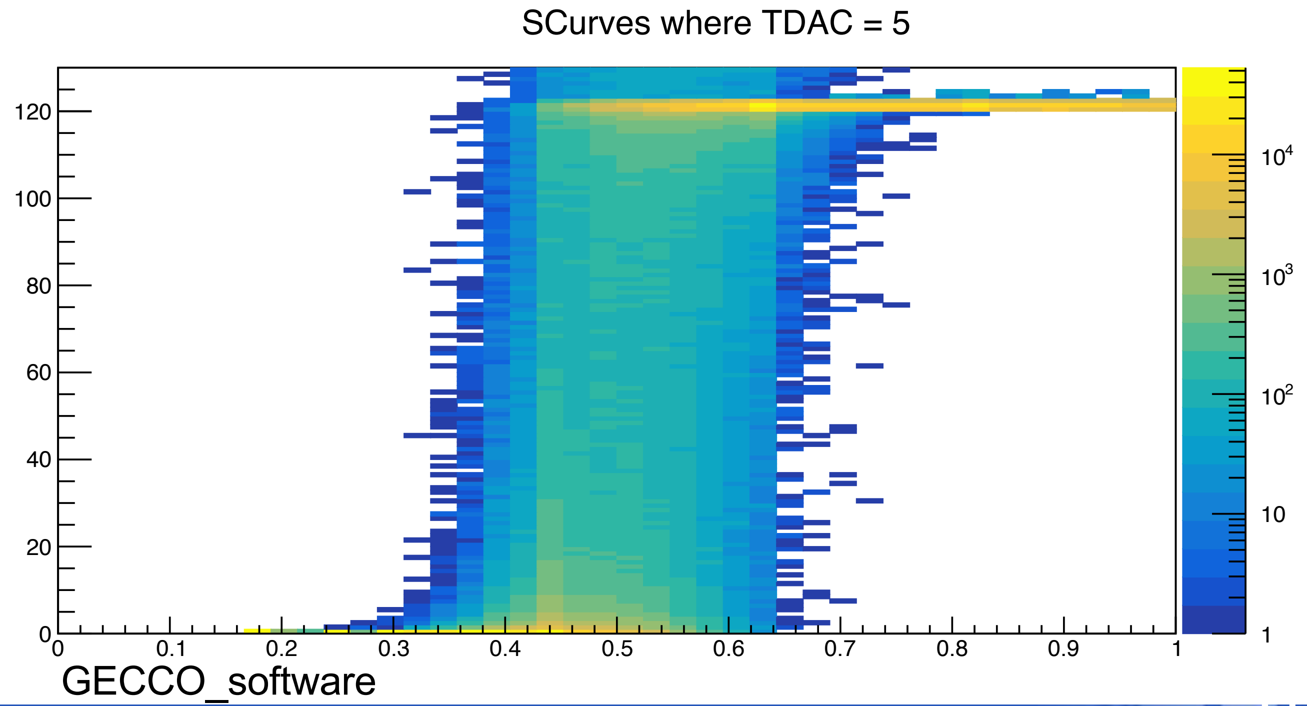




Threshold tuning

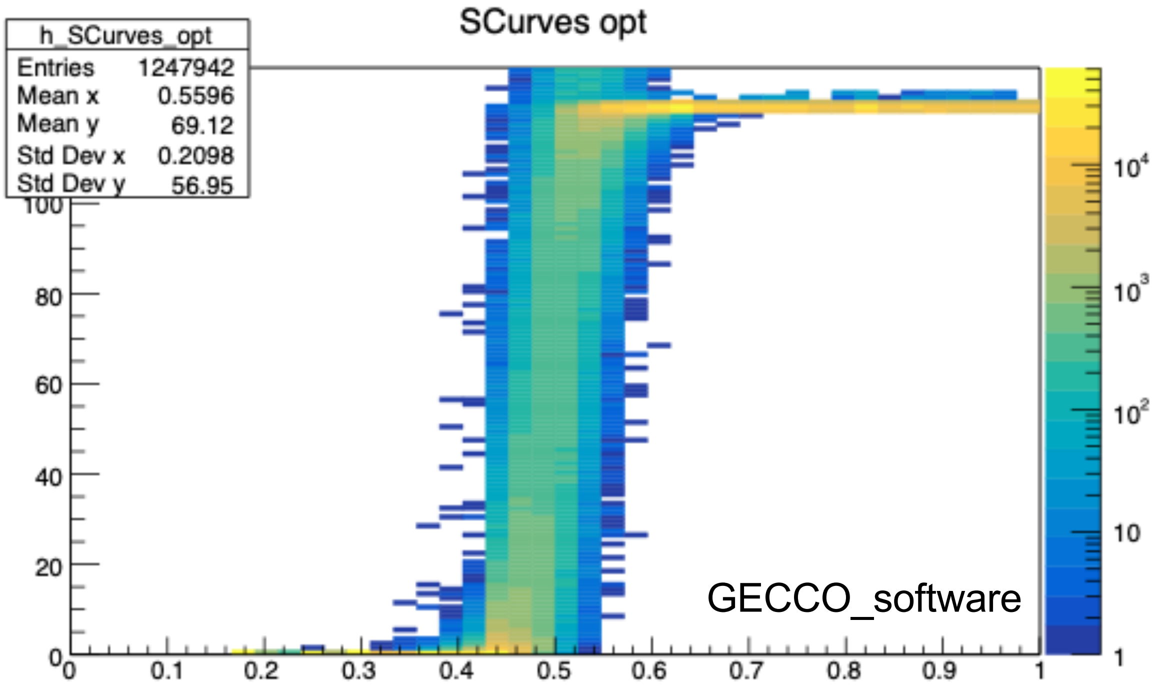
- For fixed TDAC, there is a large spread in thresholds.
- Standard deviation for row 40 at TDAC=5 is 0.047.
- Below are all S-curves for all pixels overlaid for TDAC=5.

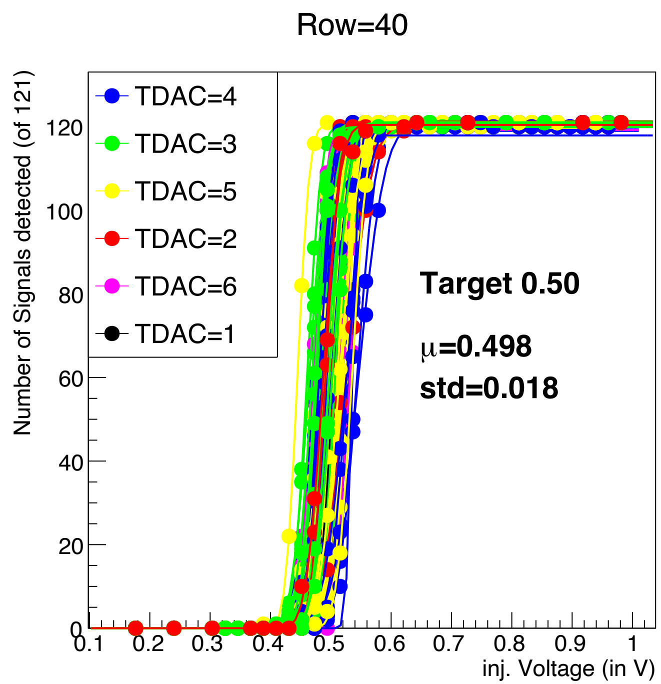




Threshold tuning

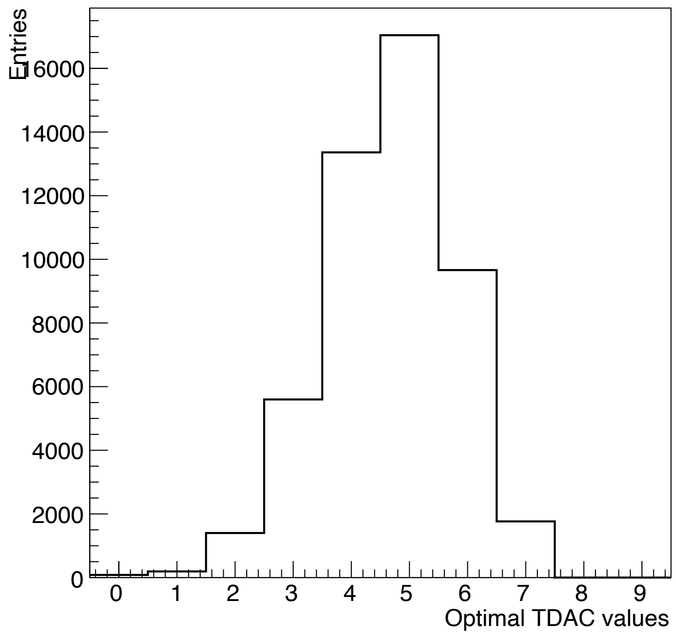
- After picking the TDAC value for each pixel that moves the threshold as close as possible to 0.50V, the standard deviation reduces from 0.047 to 0.018 for row 40.
- The S-curves for optimal TDAC for all pixels is also much narrower.

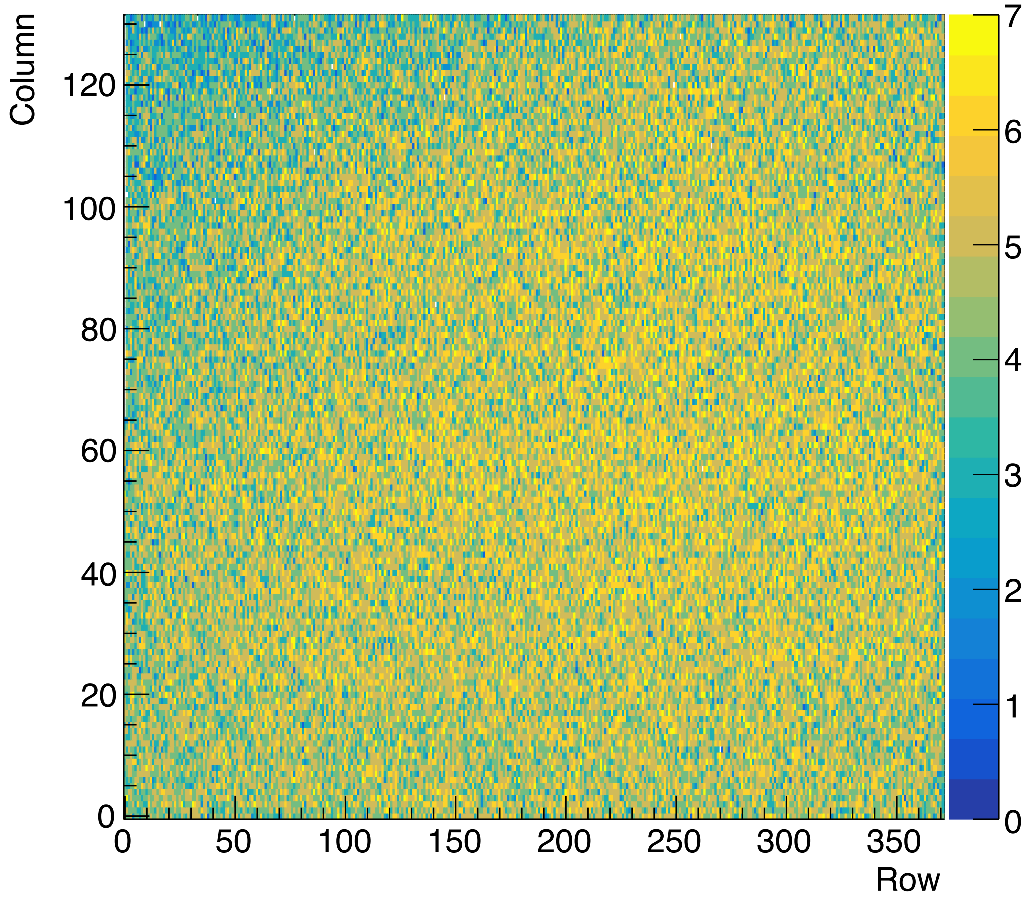




Threshold tuning: optimal TDAC

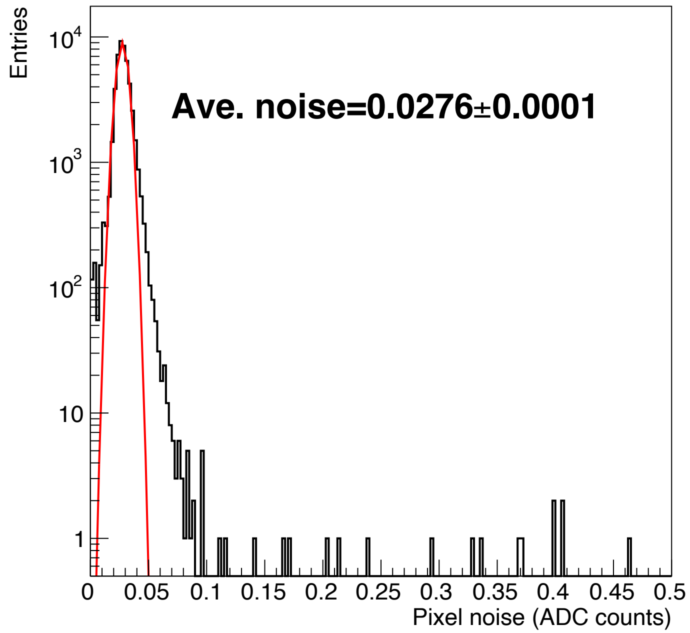
- Here you see the optimal TDAC for each pixel to get as close as possible to 0.5V.
- Most pixels prefer TDAC=5
- Clear area around edges where lower TDACs are preferred.

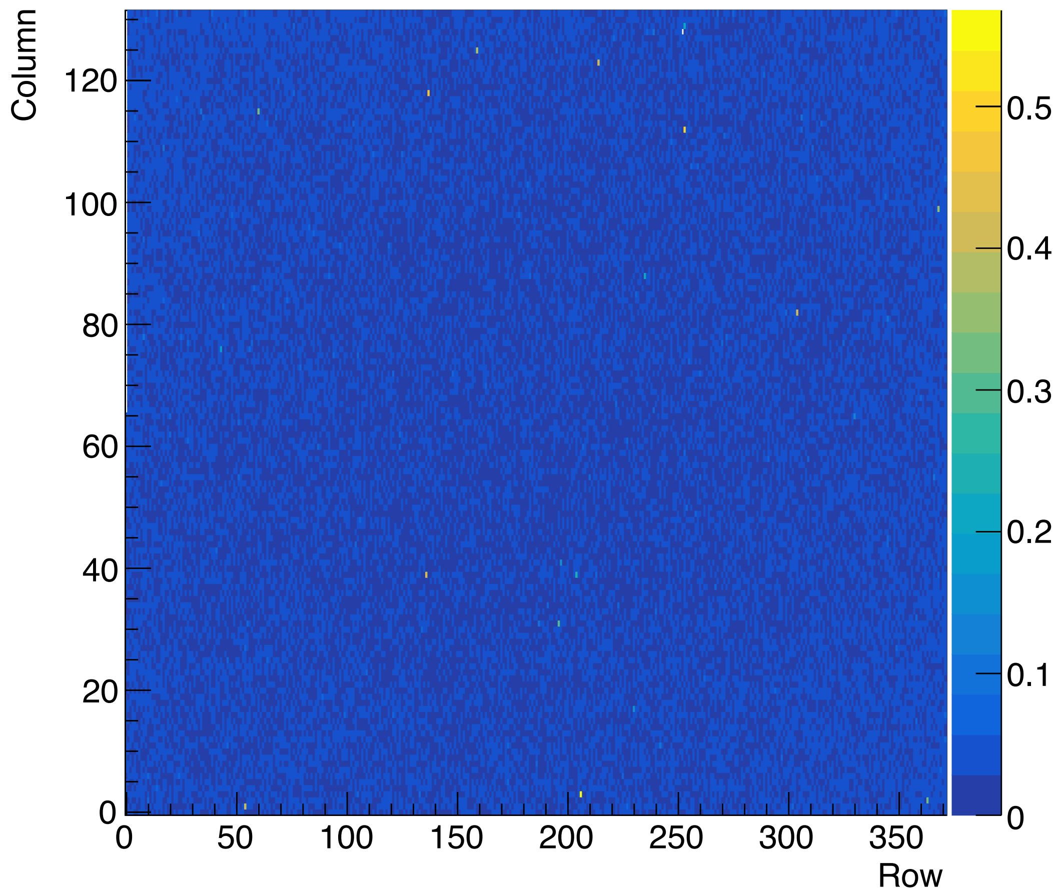




Threshold tuning: noise at optimal TDAQ

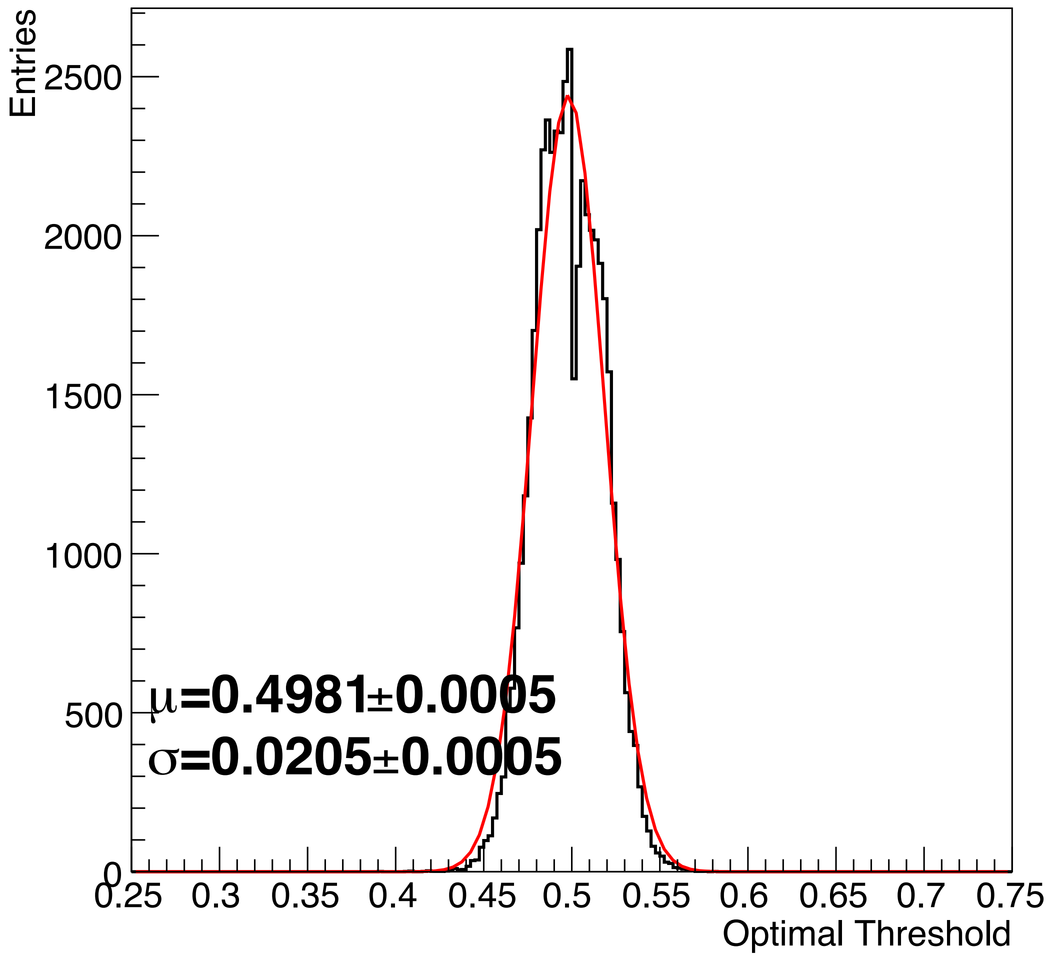
- The pixel noise at the optimal TDAC is around 0.0276 with a non-Gaussian tail to the right.





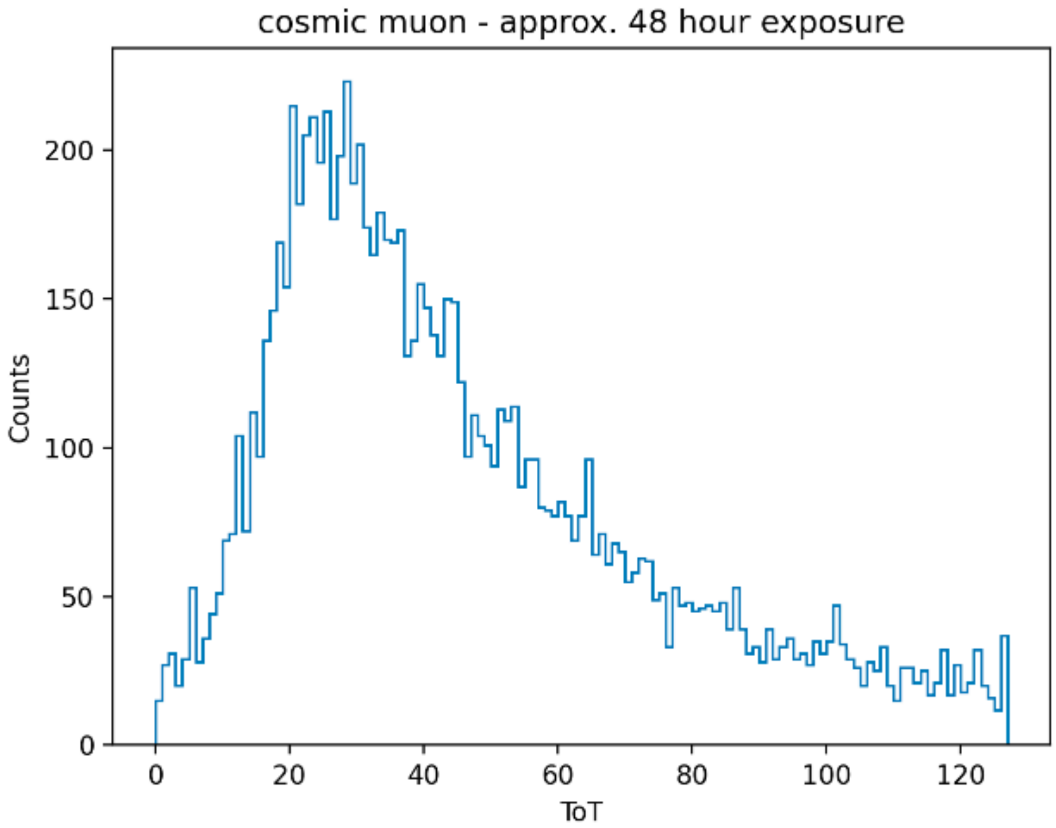
Threshold tuning: threshold at optimal TDAC

- Tuning TDAC values to get threshold as close as possible to 0.5V gives
  - Mean threshold of 0.4981±0.0005V
- Standard deviation of 0.0205±0.0005V.



Radio-active source testing: cosmics

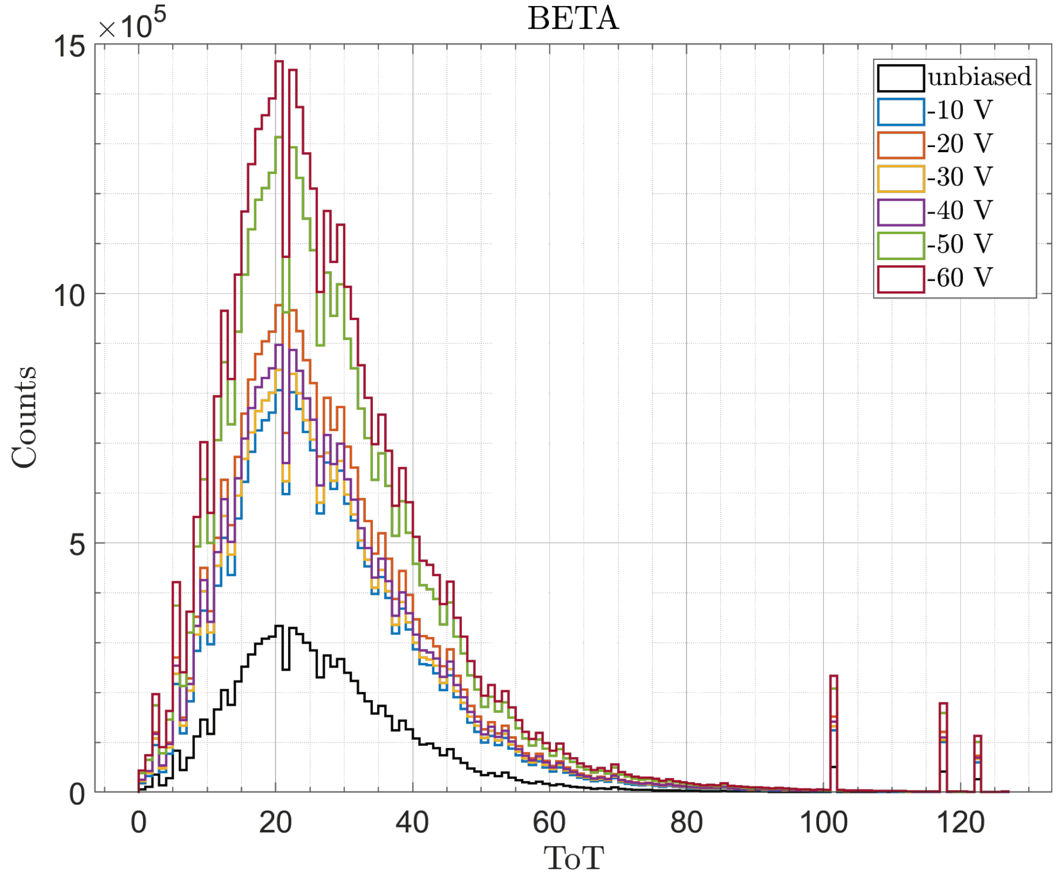
- The sensor has been tested with many radioactive sources and with cosmics.
- Here a spectrum with cosmics is shown. The signal shows the expected Landau like shape.
  - Chip not tuned (TDAC=4 for all pixels)
  - Some spurious peaks in signal values are due to a software bug that is solved meanwhile.



Radio-active source testing: beta

- The sensor has been tested with many radioactive sources and with cosmics.

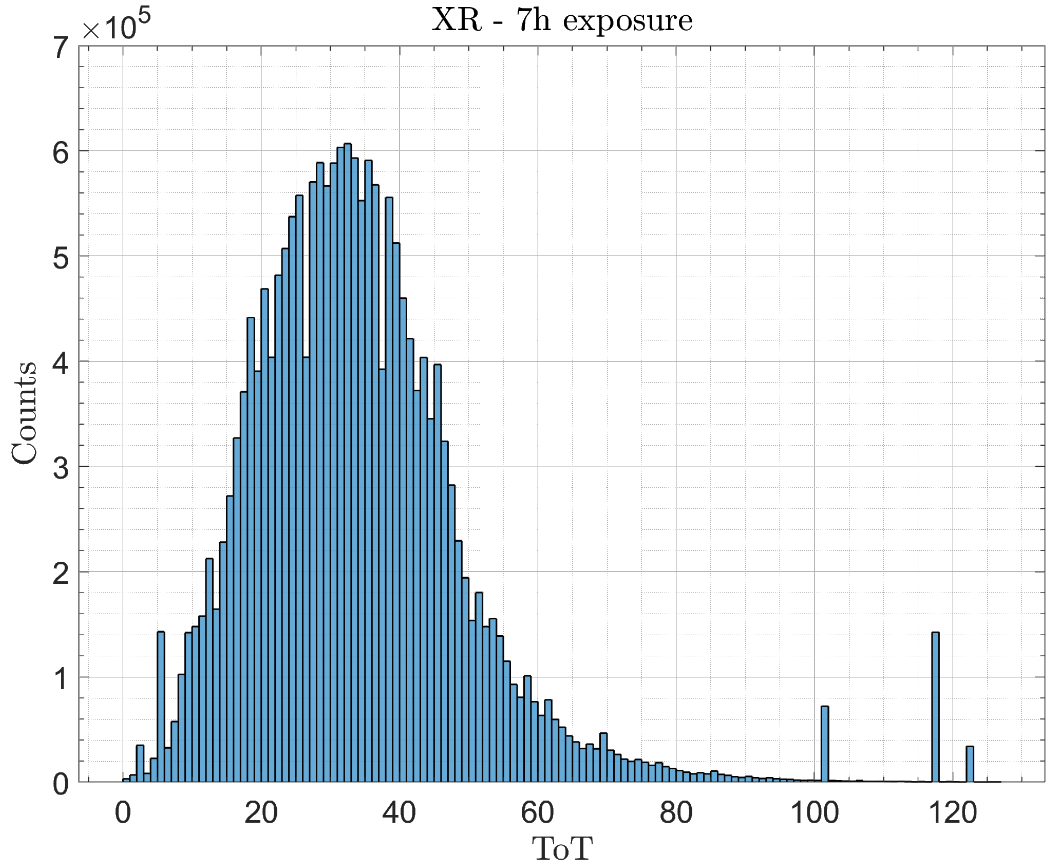
- Here a spectrum with betas is shown for different bias voltages. The signal shows the expected Landau like shape.
  - Some spurious peaks in signal values are due to a software bug that is solved meanwhile.



Radio-active source testing: gammas

- The sensor has been tested with many radioactive sources and with cosmics.

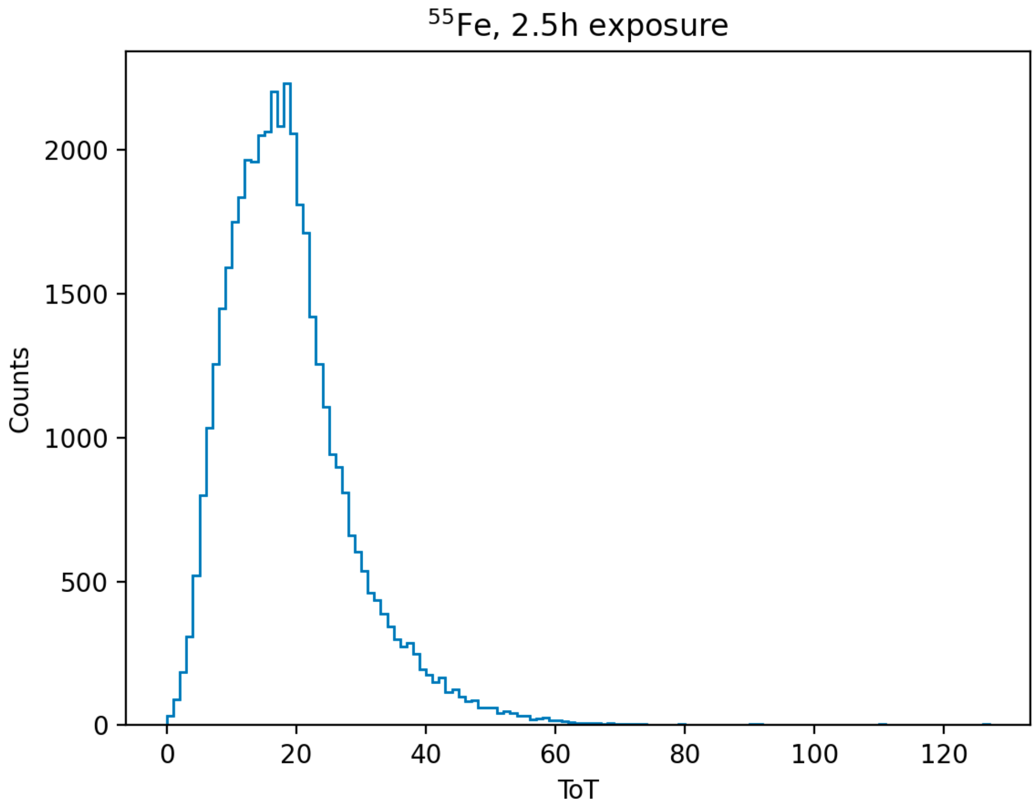
- Here a spectrum with gamma's from ^{241}Am.
  - HV = -20 V and TDAC=4
  - Some spurious peaks in signal values are due to a software bug that is solved meanwhile.



Radio-active source testing: ^{55}Fe

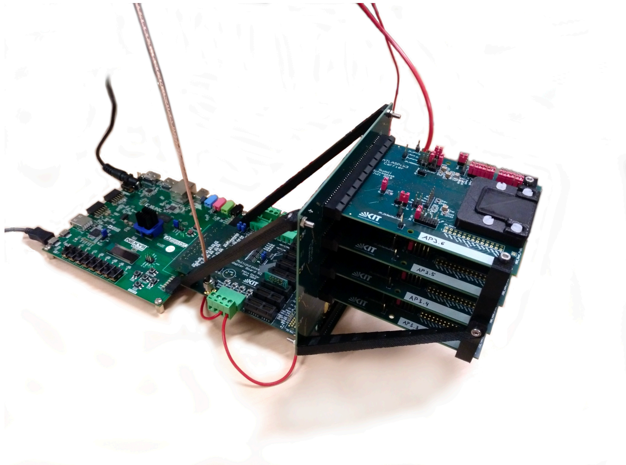
- The sensor has been tested with many radioactive sources and with cosmics.

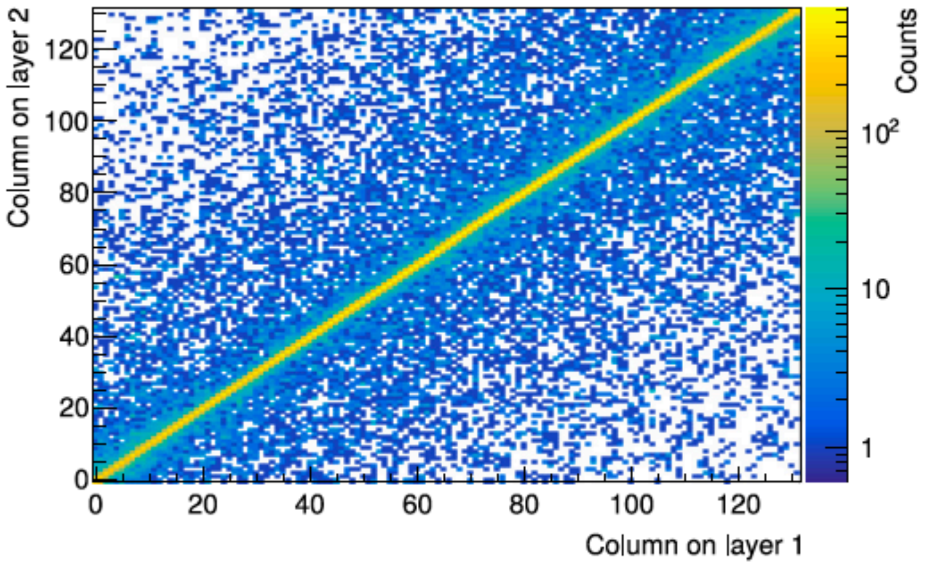
- Here a spectrum with gamma's from ^{55}Fe
  - HV=0 V and TDAC=4
  - Spurious peaks in signal values gone as software bug that is solved.

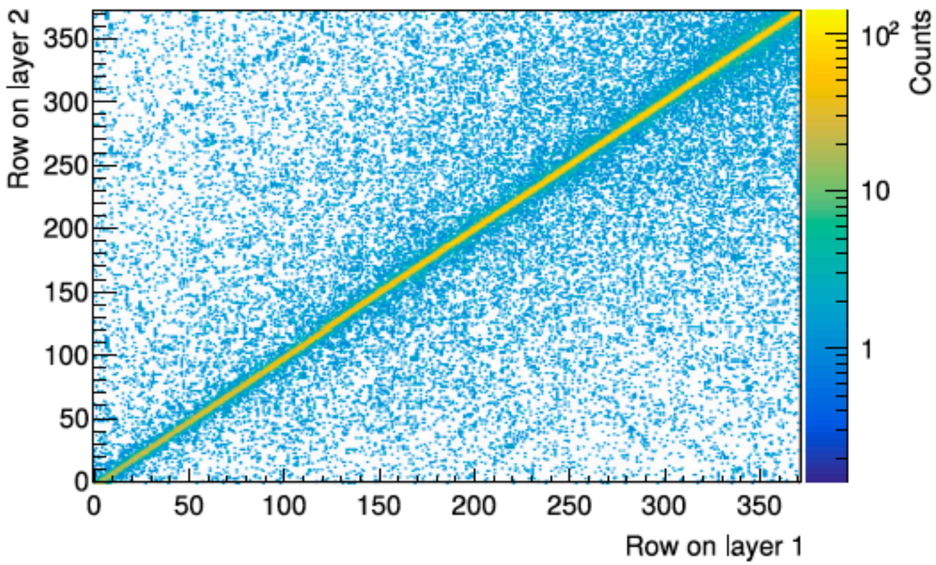


Testbeam

- A stack of 4 sensors was tested in the 3 GeV electron beam at DESY.
- The correlation plots clearly show that the sensor is detecting the particles and tracks are found.
- Full analysis to follow.

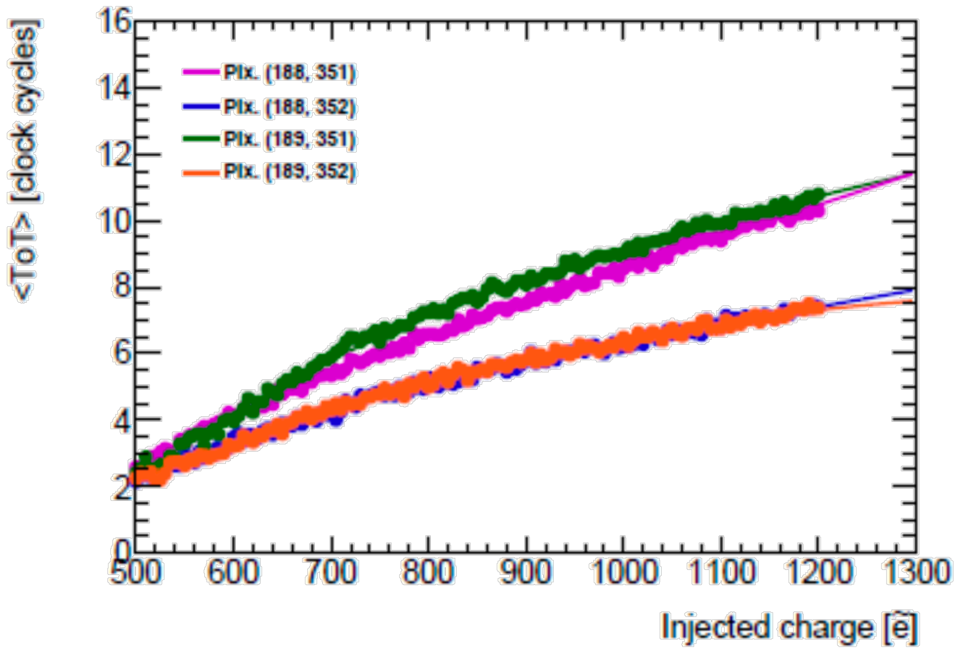


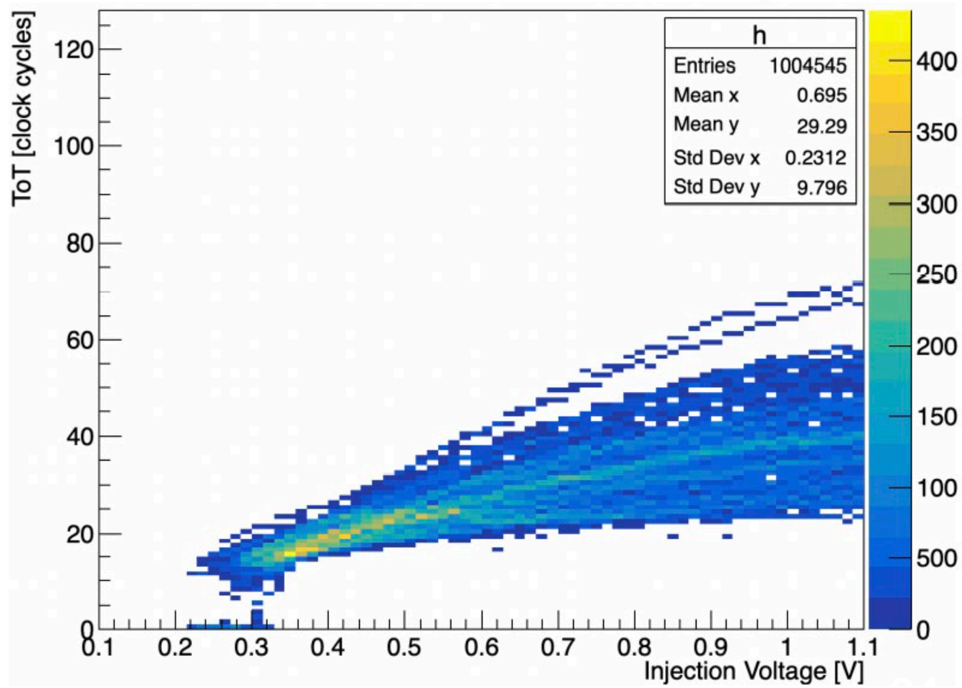




ToT calibration

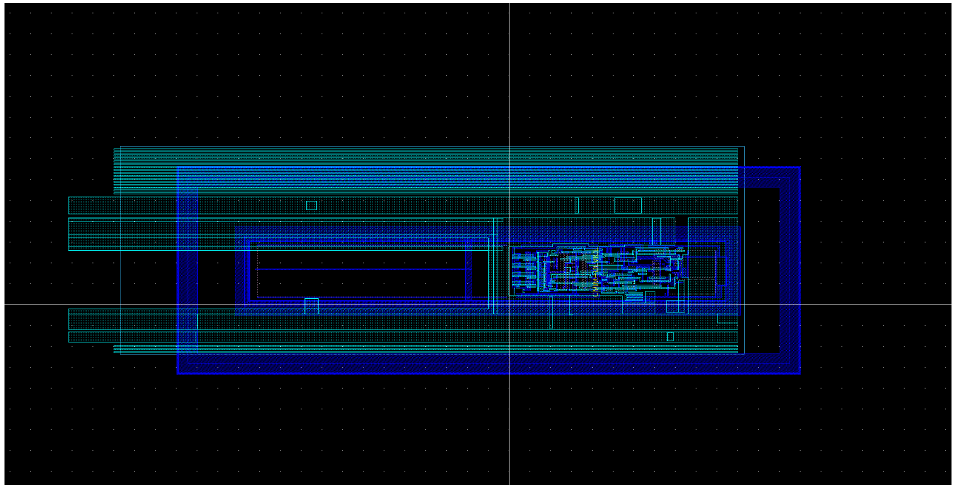
- Relationship between the input signal and the ToT is not linear.
- Here is a calibration study of the output ToT as a function of the injected charge.
- It demonstrates the non-linearity and significant differences in gain.

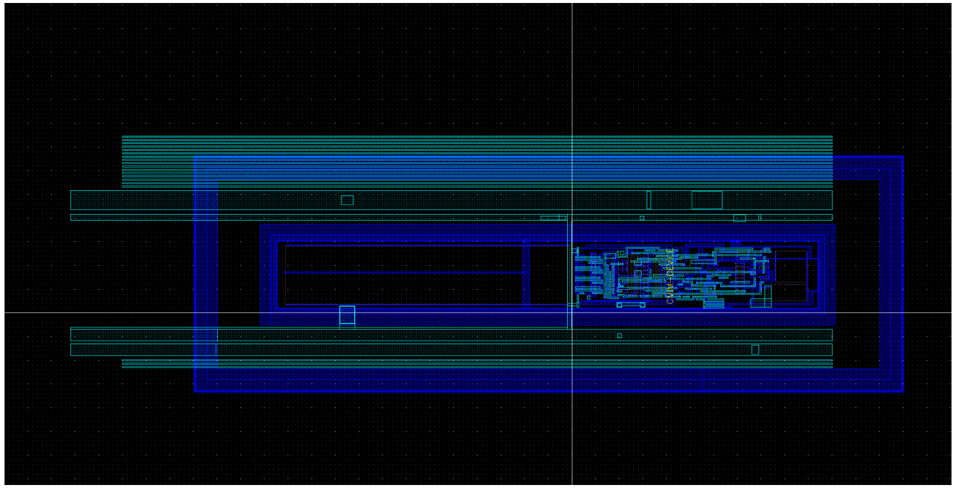




ATLASPix3.1

- ATLASpix3.1 submitted in December and delivered in February
- Redone masks for 8 Layers
- 12 wafers produced
- Reduced detector capacitance by replacing M2 shield with M3 shield (from about 250fF to 130fF)
- Modified design of the guard ring
  - Larger distance between DN and PW ring (see slides)
  - M1 ring disconnected from PW
  - Idea set substrate to -120V and M1 ring to -60V
- Added stability capacitor to the power regulator





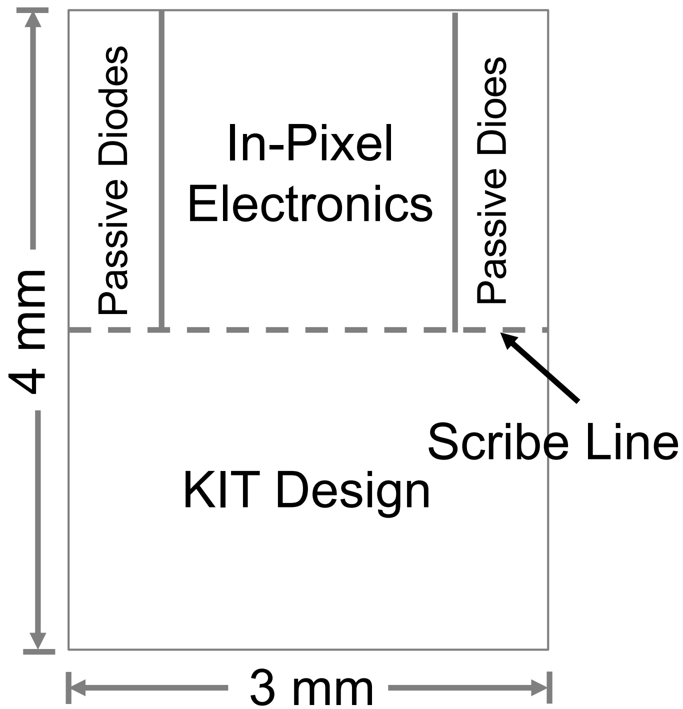
More ATLASPix development

- Test evolvement of ATLASPix3:
  - Smaller pixel size (25µm) in φ direction
  - Lower capacitance
  - Amplifier and comparator design
  - Electronics in pixel or periphery
  - Daisy chain of readout
- Engineering run planned for April this year
- Part of multi-project wafer run with many projects

New Sensor Design

- Starting the new sensor design utilizing a 55 nm HV-CMOS process from a Chinese foundry (HLMC)
  - MPW: 3×4 mm^2, 50 dies; caveats: low bulk resistivity wafers, no deep P-well
  - Engineering run: deep P-well possible (being tried out for their CIS process of the same feature size); high resistivity wafer to be negotiated
- Ready to call for the sensor design meeting, with designers from IHEP, KIT and other participating institutes
  - PDK already shared with KIT, several missing libraries being applied for

Aimed MPW: 16 August, 2021



Personal proposal, *to be discussed*

Readout systems

- Currently, we are using the GECCO system.
  - **GE**neric **C**onfiguration and **CO**ntrol System
- Developed by KIT.
- Provides several auxiliary cards
  - VoltageCard, DACs, PowerCard, ConfigCard and so on
- GUI and DAQ software in C++ based on Qt

- Works well.

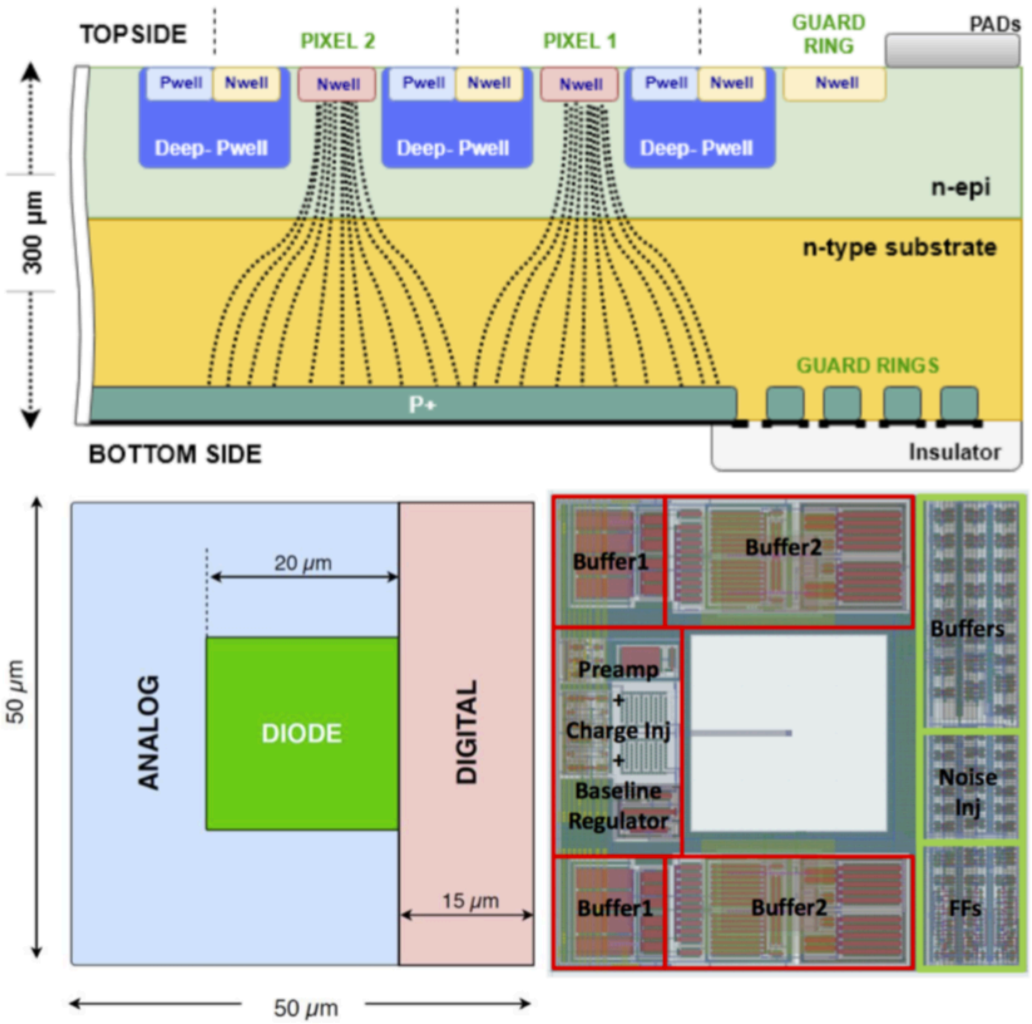
Readout systems

- Another readout system under development: YARR
- YARR is an RD53 development designed for the next generation of Pixel detector readout chips.
- Uses PCIe bus for high bandwidth data transfer
- Needs modification for the ATLASPix3.

- Currently, studying which one to adopt for the future.

ARCADIA

- Besides the ATLASPix3, there is also work being done on the ARCADIA sensor
- 110 nm CMOS CIS technology, high-resistivity bulk with LFoundry
- Pixel size below 25µm x 25µm
  - binary readout
  - sparsified readout
- Full depletion for 50 to 400µm shown
- Reticle size sensor 2.6 cm x 3.2 cm
- DRC compliant with 2D stitching assembly
- Engineering run by mid-2020



Summary

- Lots of work has been done on the testing and development on the Si tracker for CEPC.
  - Workhorse is ATLASPix3
  - Testing program is well underway
  - New iterations are underway
  - There are alternative sensors under consideration as well (e.g. ARCADIA)
- Discussions have started on readout system.