Progress and planning of the Silicon Tracker

H. Fox for the SiTracker project

Joint Workshop of the CEPC Physics, Software and New Detector Concept

YangZhou, 14 April 2021

CMOS SiTracker working group

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- Australia
  - University of Adelaide
- China
  - Institute of High Energy Physics, CAS
  - Shangdong University
  - Tsinghua University
  - University of Science and Technology of China
  - Northwestern Polytechnical University
  - T.D. Lee Institute - Shanghai Jiao Tong University
  - Harbin Institute of Technology
  - University of South China
- Germany
  - Karlsruhe Institut für Technologie
- Italy
  - INFN Sezione di Milano, Università degli Studi di Milano e Università degli Studi dell'Insubria
  - INFN Sezione die Pisa e Università di Pisa
  - INFN Sezione di Torino e Università degli Studi di Torino
- UK
  - University of Bristol
  - STFC - Daresbury Laboratory
  - University of Edinburgh
  - Lancaster University
  - University of Liverpool
  - Queen Mary University of London
  - University of Oxford
  - STFC - Rutherford Appleton Laboratory
  - University of Sheffield
  - University of Warwick

CEPC tracker designs: TPC or DCH + Si

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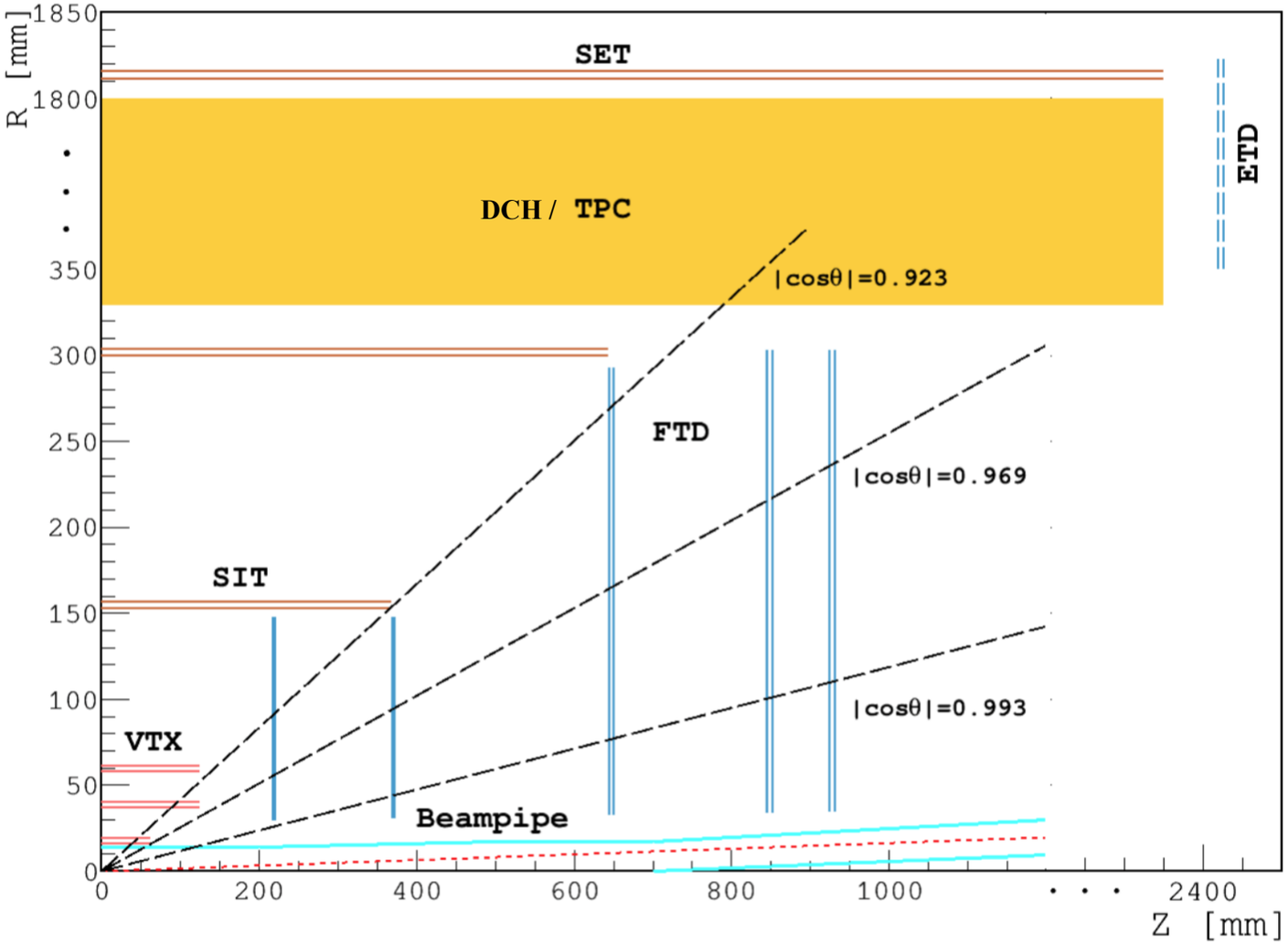
Baseline tracker design: TPC

and 3 layers / 5 disks of silicon sensors,

50 m² (33 w/o ETD) if built in CMOS pixels (strips default)

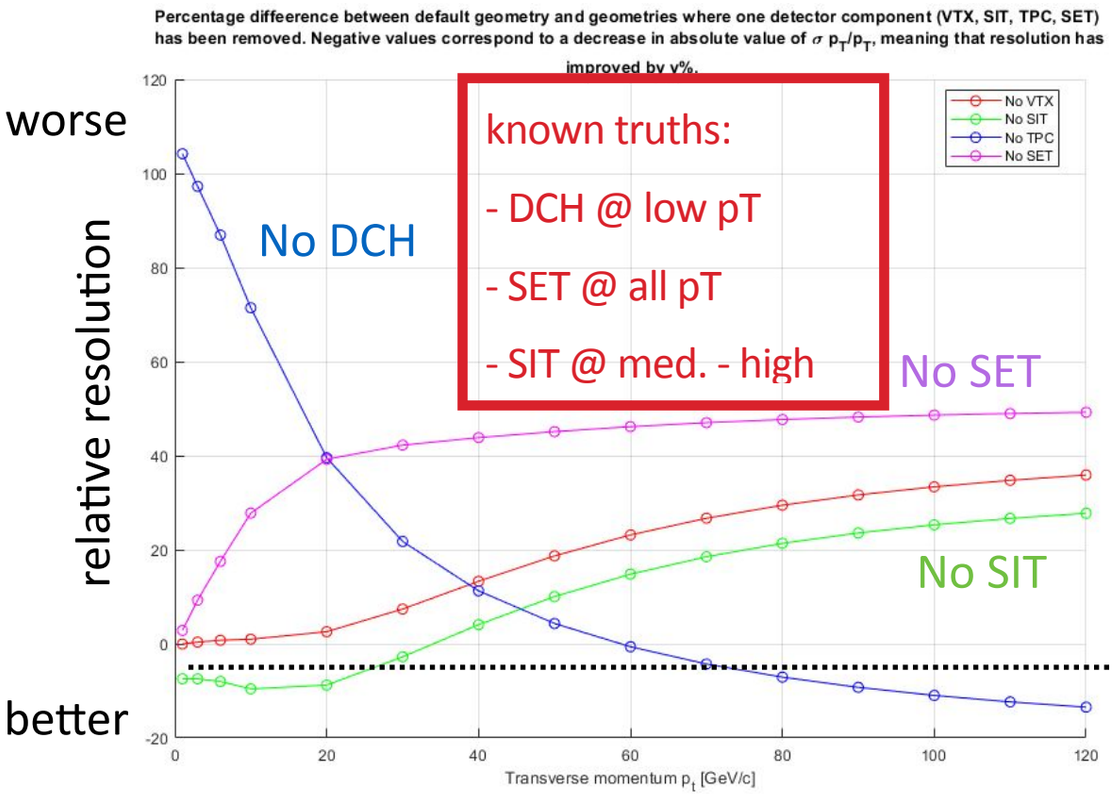


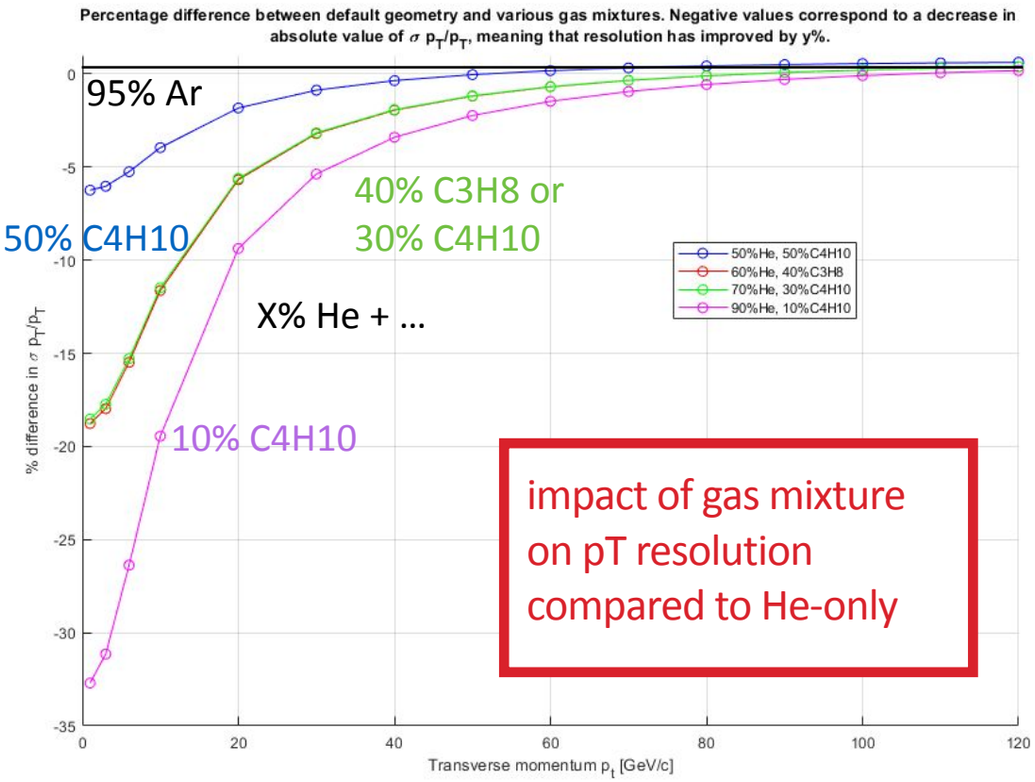
Detector		Radius R [mm]		$\pm z$ [mm]	Material budget [X_0]
SIT	Layer 1	153		371.3	0.65%
	Layer 2	300		664.9	0.65%
SET	Layer 3	1811		2350	0.65%
		R_{in}	R_{out}		
FTD	Disk 1	39	151.9	220	0.50%
	Disk 2	49.6	151.9	371.3	0.50%
	Disk 3	70.1	298.9	644.9	0.65%
	Disk 4	79.3	309	846	0.65%
	Disk 5	92.7	309	1057.5	0.65%
ETD	Disk	419.3	1822.7	2420	0.65%

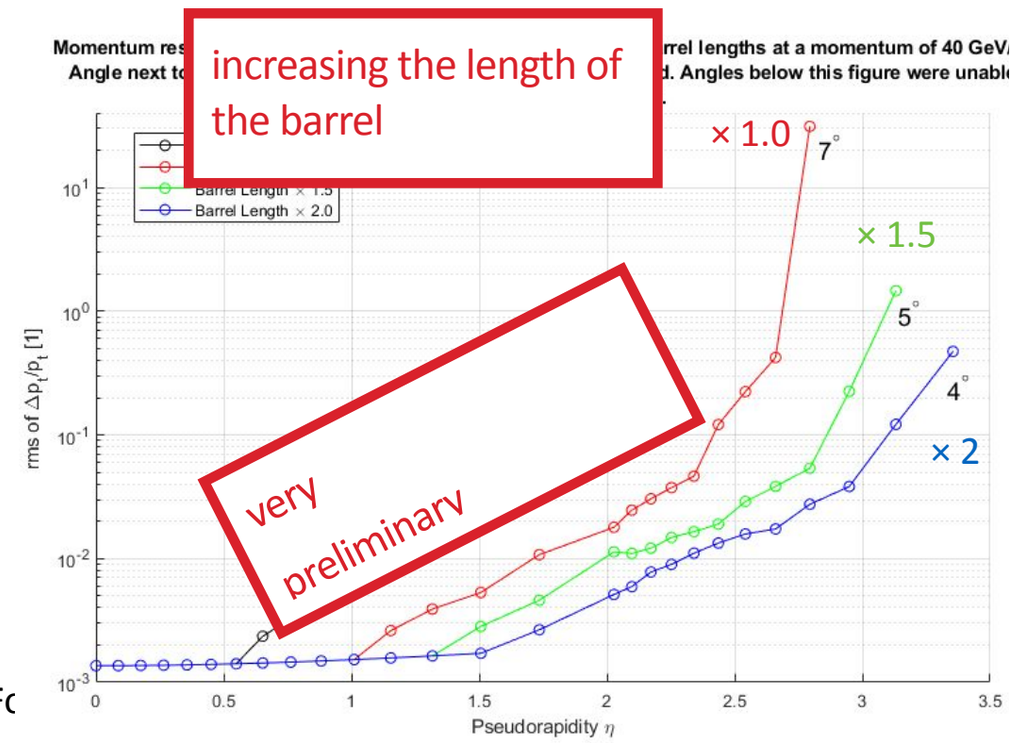
Physics process	Measurands	Detector subsystem	Performance requirement
$ZH, Z \to e^+e^-, \mu^+\mu^-$ $H \to \mu^+\mu^-$	$m_H, \sigma(ZH)$ $\mathrm{BR}(H \to \mu^+\mu^-)$	Tracker	$\Delta(1/p_T) =$ $2 \times 10^{-5} \oplus \frac{0.001}{p(\mathrm{GeV}) \sin^{3/2}\theta}$

$\sigma_{r\phi} \approx 7\mu m$

Tracking Task Force: LiC Toy for fast studies







Sensor(s): **ATLASPix**, 55nm HLMC, Arcadia

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ATLASPix

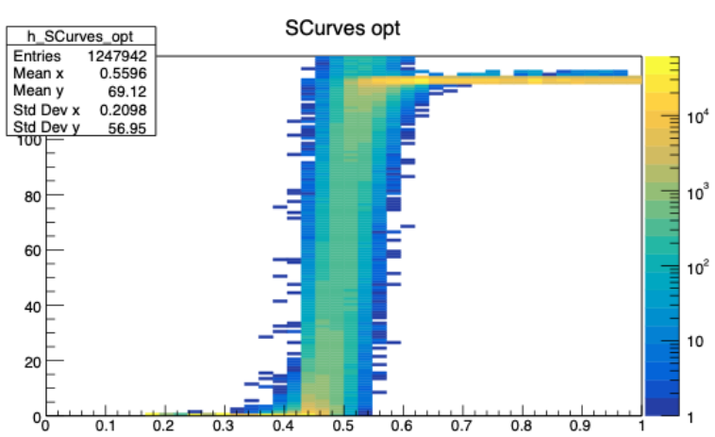
Monolithic CMOS allows to produce **large** areas **fast** and **cheap**

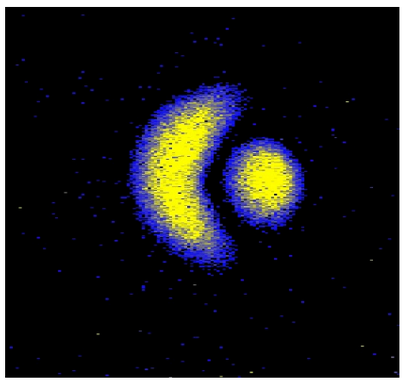
- Reticule: **2.02 cm by 2.1 cm;** Pixel: **150 µm by 50 µm** (or smaller)
- **25ns timing**, 1.28 GBit/s downlink; 2 End of Column buffers

372 hit buffers for triggerless readout

80 trigger buffers for triggered readout

Concentrate on understanding and running the sensor (6 institutes)





Fe-55 with collimation

O(100) sensors ATLASPix 3.0 and 3.1

Submission of **MPW for CEPC**, LHCb & other projects

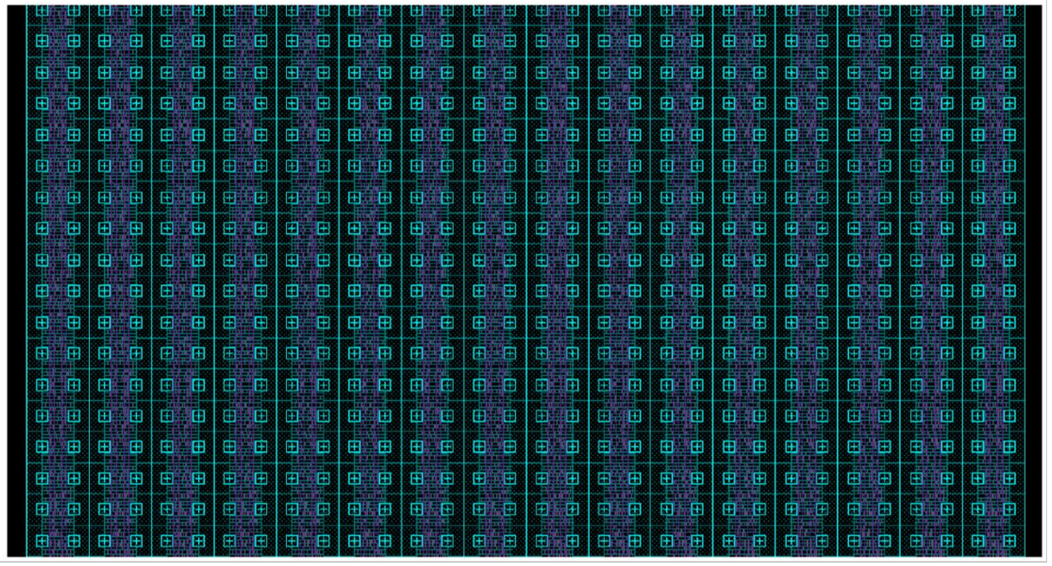
55 nm HLMC design

Chinese foundry

Collaboration between IHEP, KIT & others

Aim for MPW in August

Arcadia



- Pixel size: 25 µm x 25 µm
- Matrix core 512 x 512, side-buttable.
- Matrix, EoC architecture, data links scalable to 2048 x 2048
- Trigger-less binary data readout, up to 10-100 MHz/cm^2

Modules: Quads from 4 sensors

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Readout unit based on 4 chips

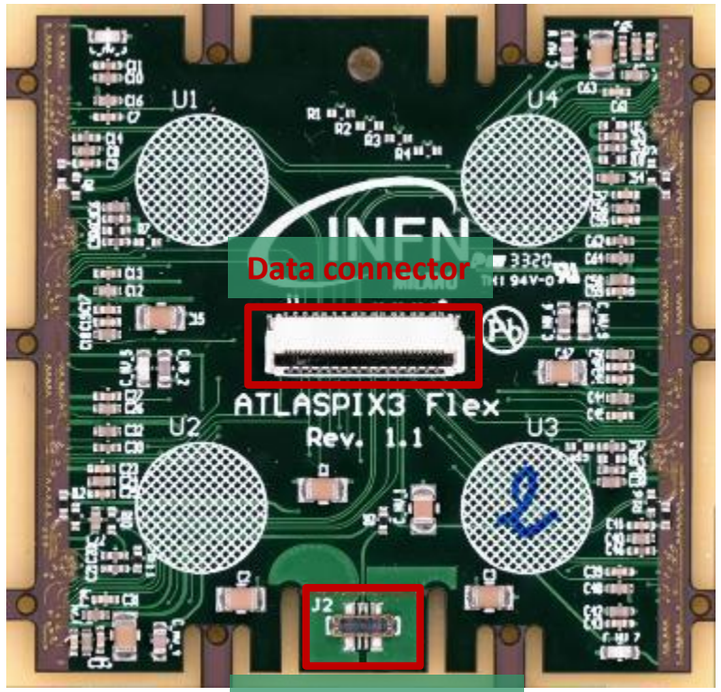
4-layer flex hybrid (2 power, 2 signal)

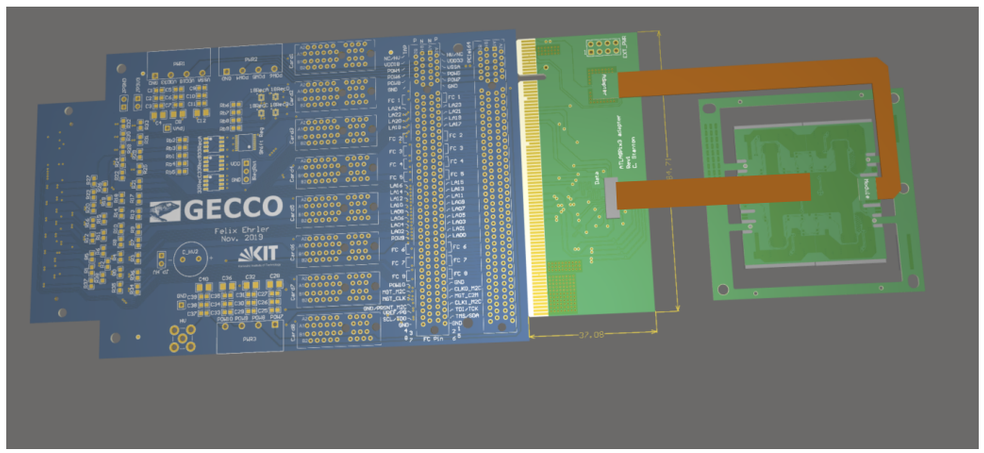
impedance-matched lines

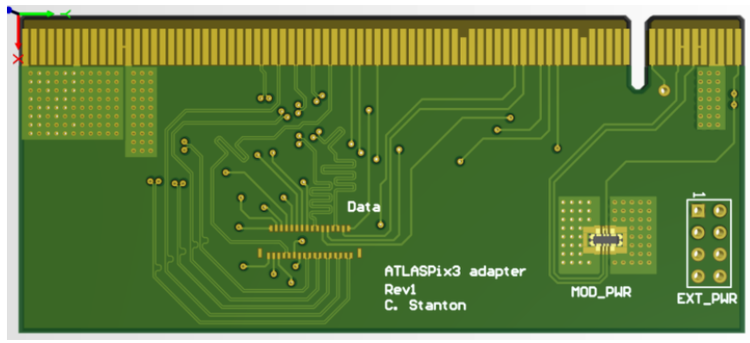
shared services among 4 sensors by common power connections and configuration lines

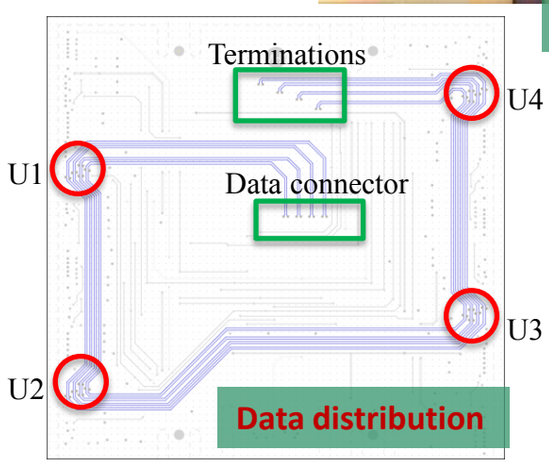
benefits from in-chip regulators to reduce connection

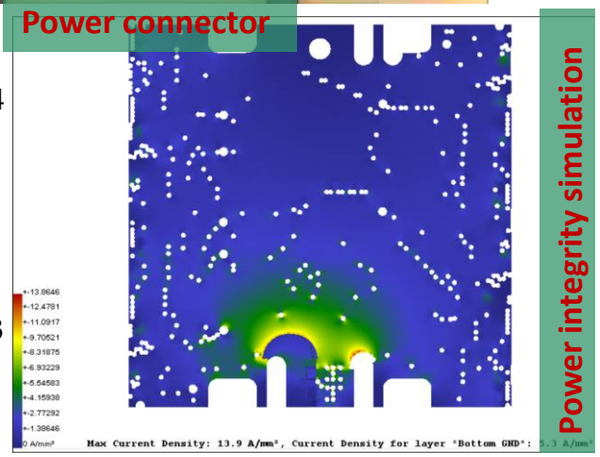
in the minimal configuration 1 power, 1 command in, 4 data out











Electronic testing well advanced, ready for readout-test with sensors.

DAQ: YARR
Yet Another Rapid Readout

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https://iopscience.iop.org/article/10.1088/1742-6596/898/3/032053

YARR is a small **self-contained DAQ system**.

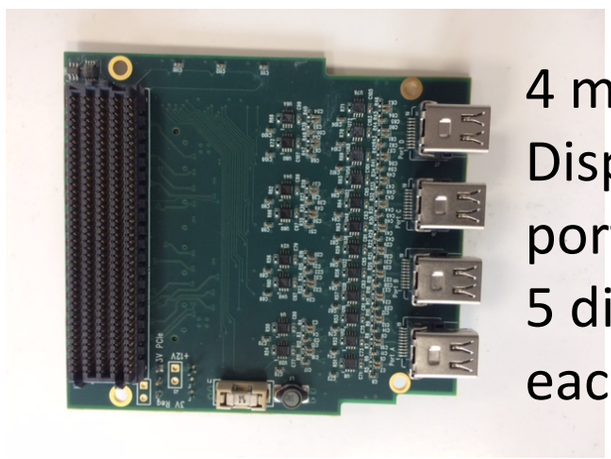
Linux PC with a x4 **PCIe slot** for the FPGA card

FPGA card: e.g. **Trenz TEF1001**, XpressK7,…

FMC cards for FE-I4 and RD53A (“Ohio card”

Trenz TEF1001

Ohio card



4 mini Display ports
5 diff lines each

Up to **1.6GBit/s possible** with this setup.

We have used the YARR readout with a digital RD53A module in **Lancaster & Edinburgh**.

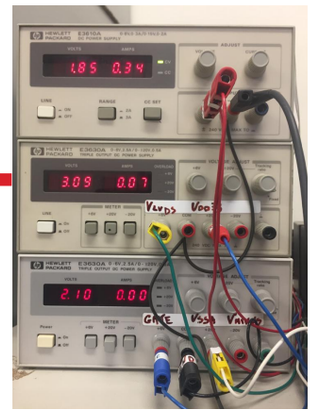
Todo: Adaptation to ATLASPix3 necessary:

- Add a display port to the GECCO system (IHEP) and the module adapter card (Edinburgh)

YARR (multi) module readout

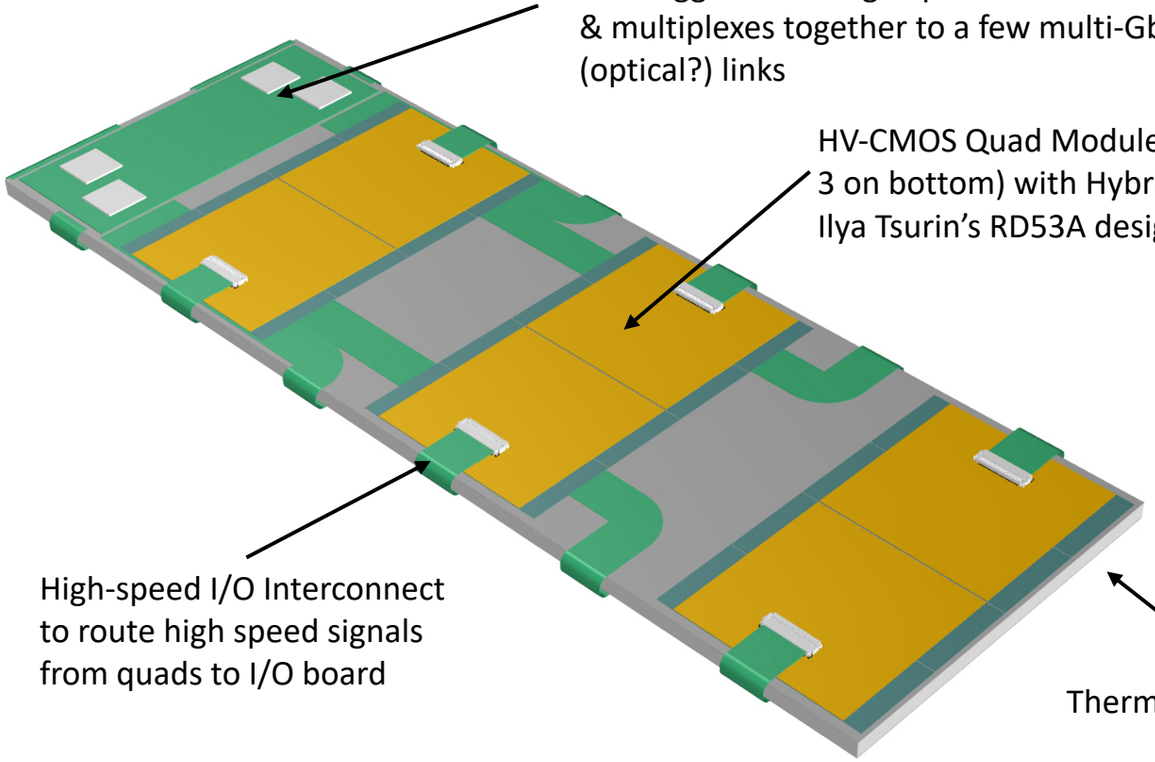
The Edinburgh adapter card needs to be adapted to have a mini display port connector (Edinburgh):

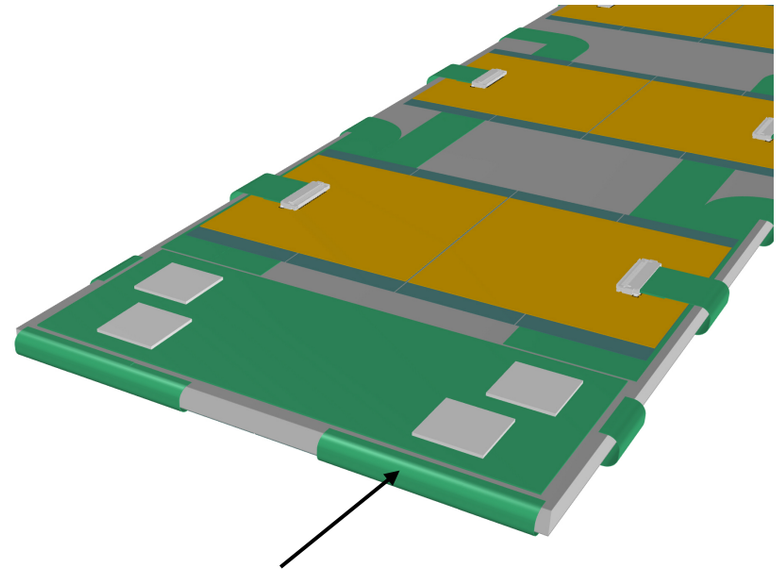
- 1 command line per module (AUX lines of mini display port)
- 4 (differential) data out lines (1 per chip)
- 1 (differential) reference clock line (for debugging)
- additional lines to have a fixed setting (Rudolf, jumpered?)

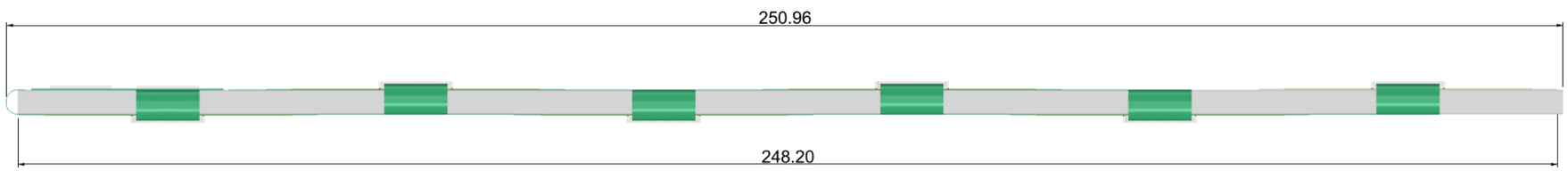


Ohio Card

Tile conceptual design





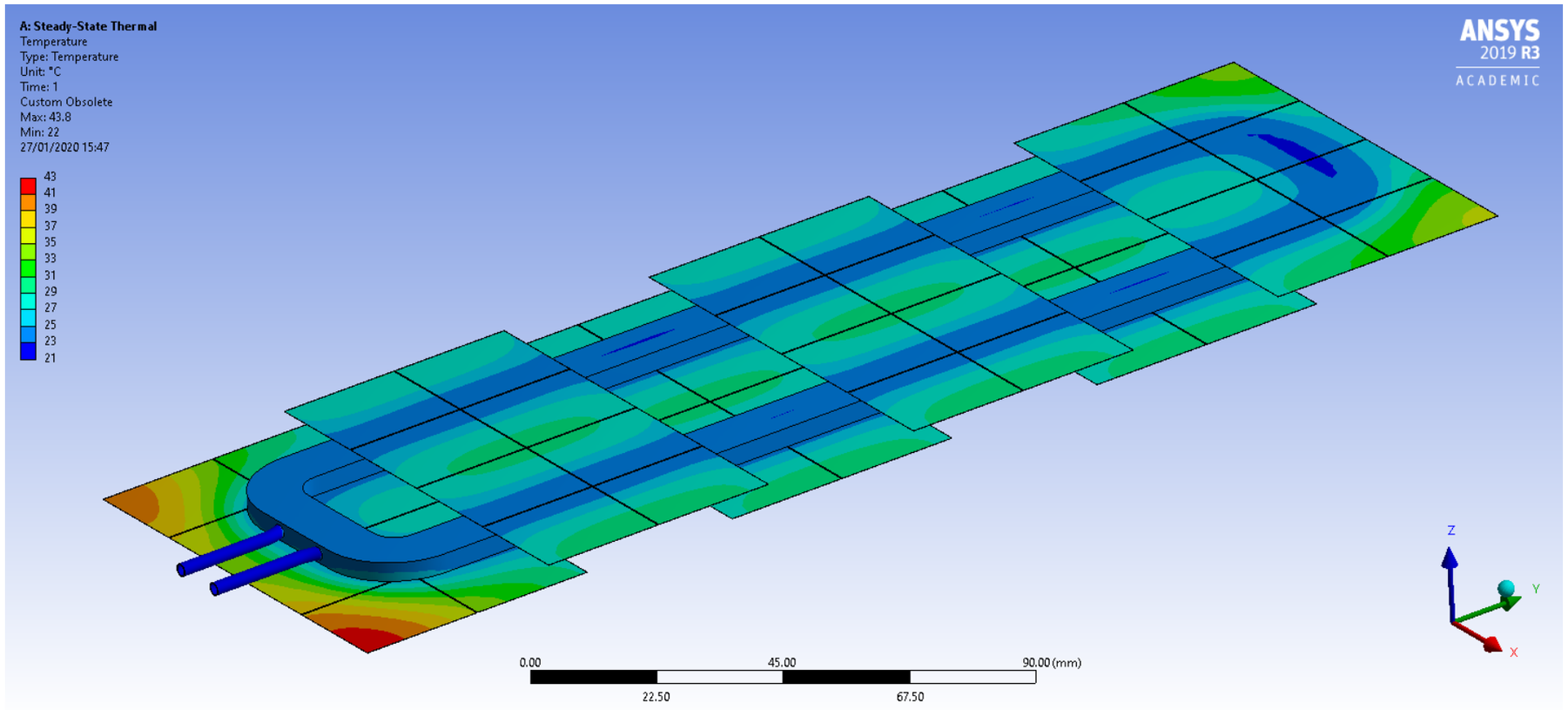


Thermal simulation

Assume a **serial powering scheme** of e.g. 12 modules. Sensors have **on-chip regulators** to make this possible. Reduces the number of power lines significantly.

Power consumption of ~2.4W / quad module. Example of Layer 1 half barrel: 12*2*10*2.4=576W. Layer 2 half barrel: 24*2*16*2.4=1.8kW

Assume CO2 cooling.

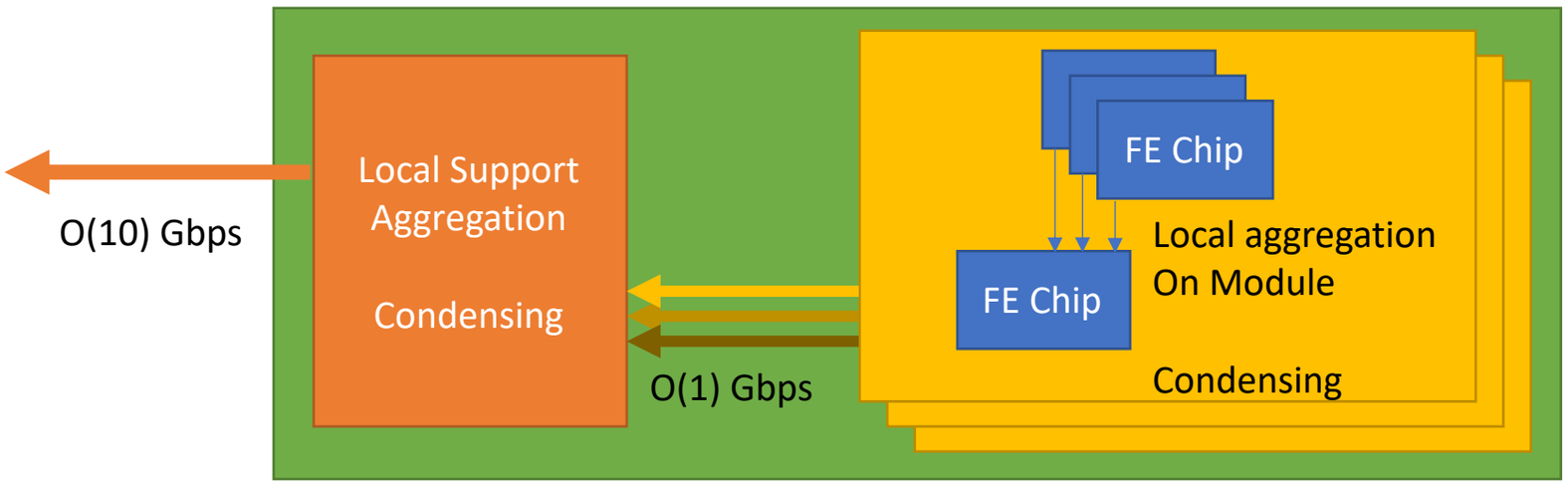


Trigger & DAQ

The chip has very effective zero-suppression

- no noise occupancy
- digital cross talk to be determined
- physics and background occupancy for the tracker is extremely low

Need effective data aggregation



ATLASPix3 can operate

triggerless: no guaranteed event ordering; 10bit timestamp

triggered: event tag for each trigger, easy identification

Carbon fibre support structure

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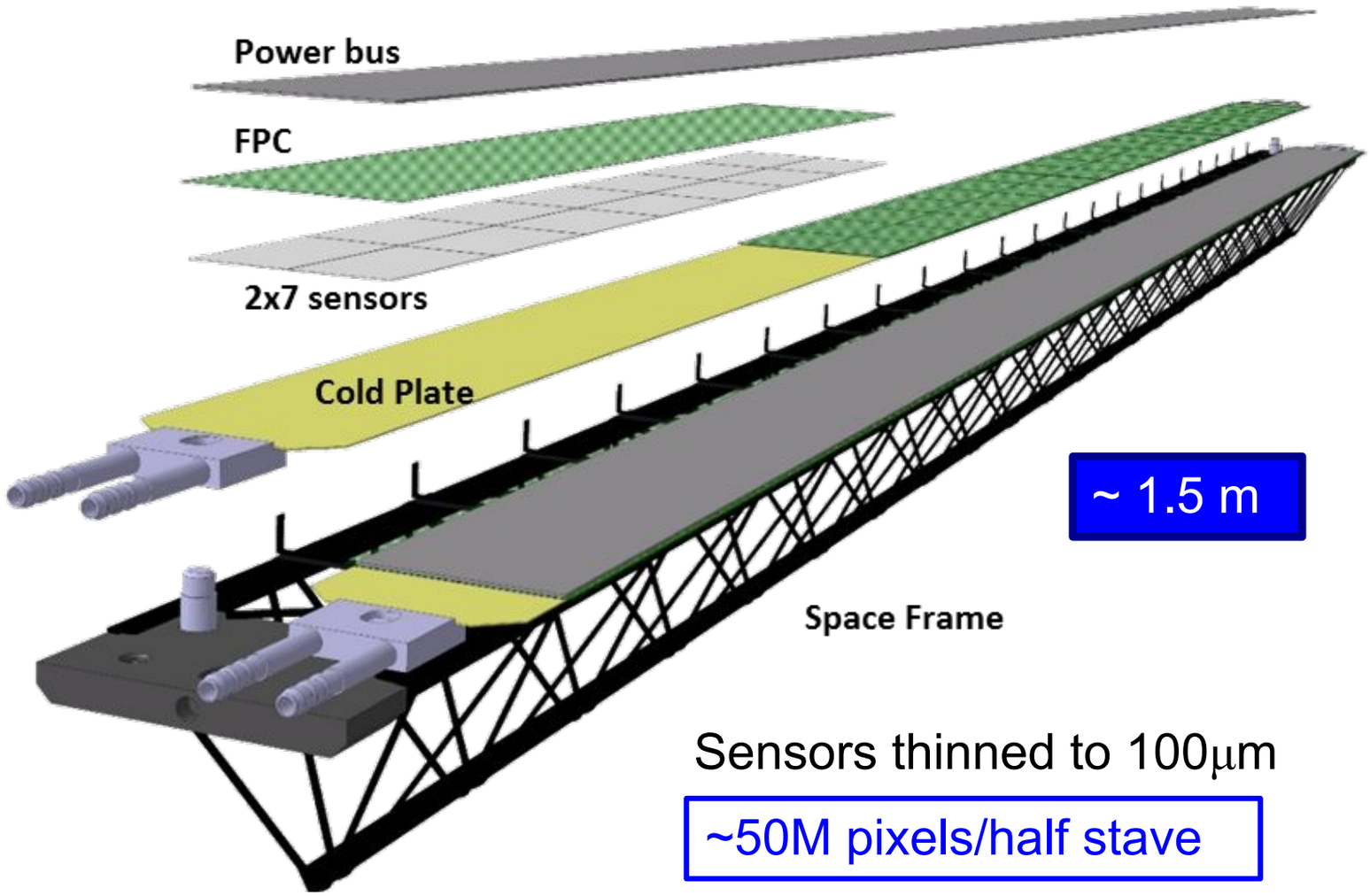
ALICE: Cold plate on a carbon fibre support structure



Sensors thinned to 100μm

~50M pixels/half stave

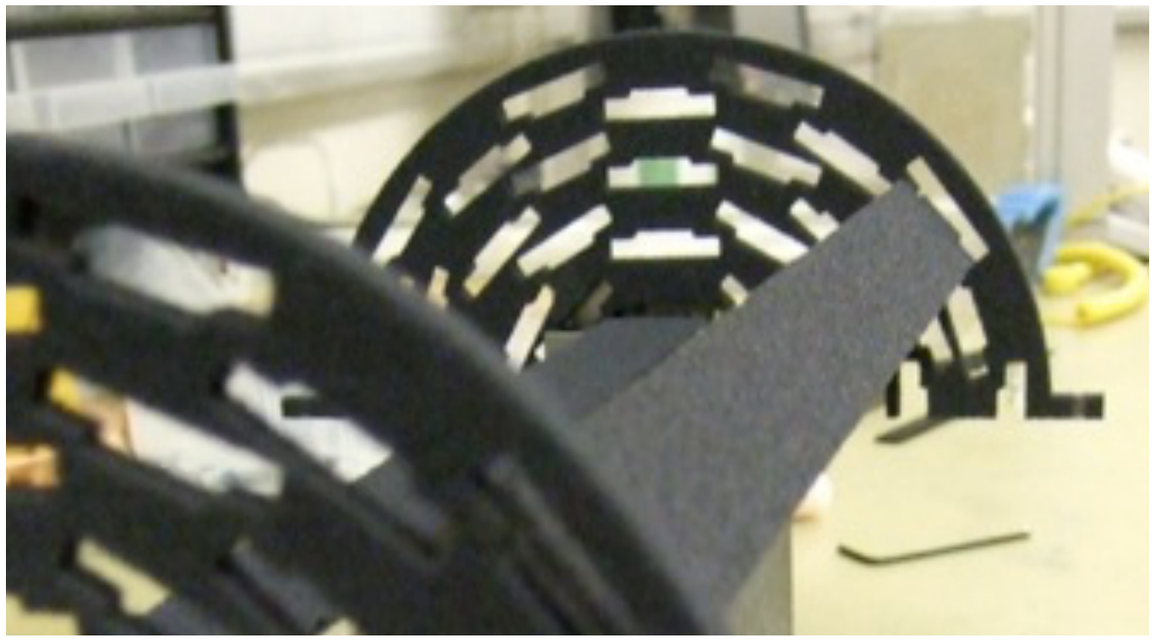
SiC Option

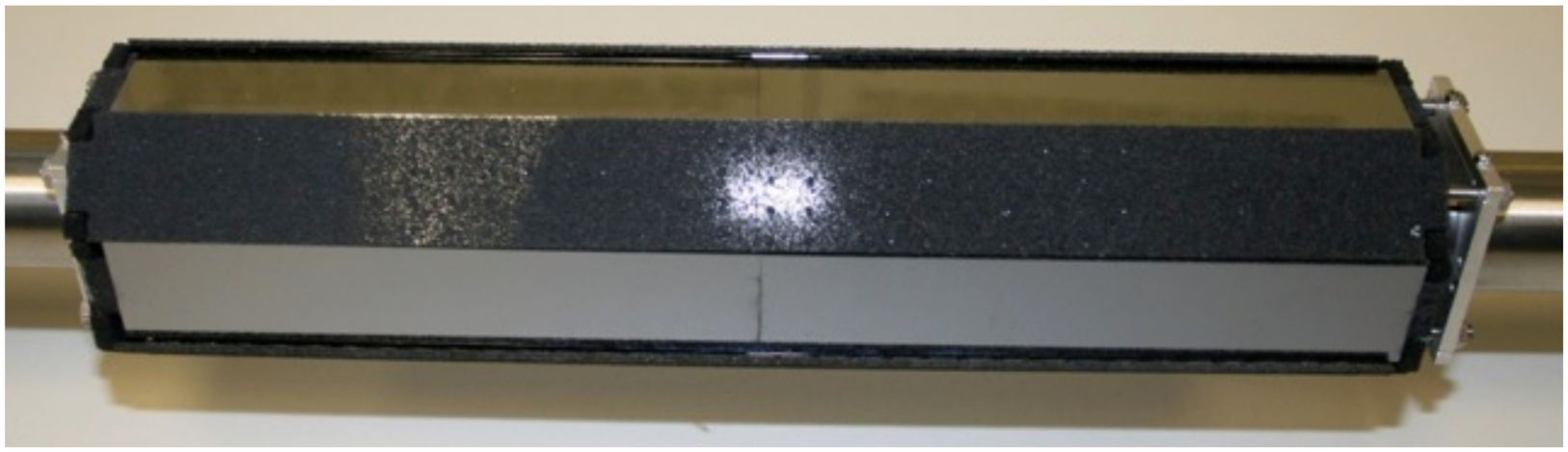
Prototyped all-SiC vertex detector

Machined bulkheads

Layer 2: 30cm long and 2.5 cm radius

Achieved 0.09% X_0 including 20µm silicon sensor

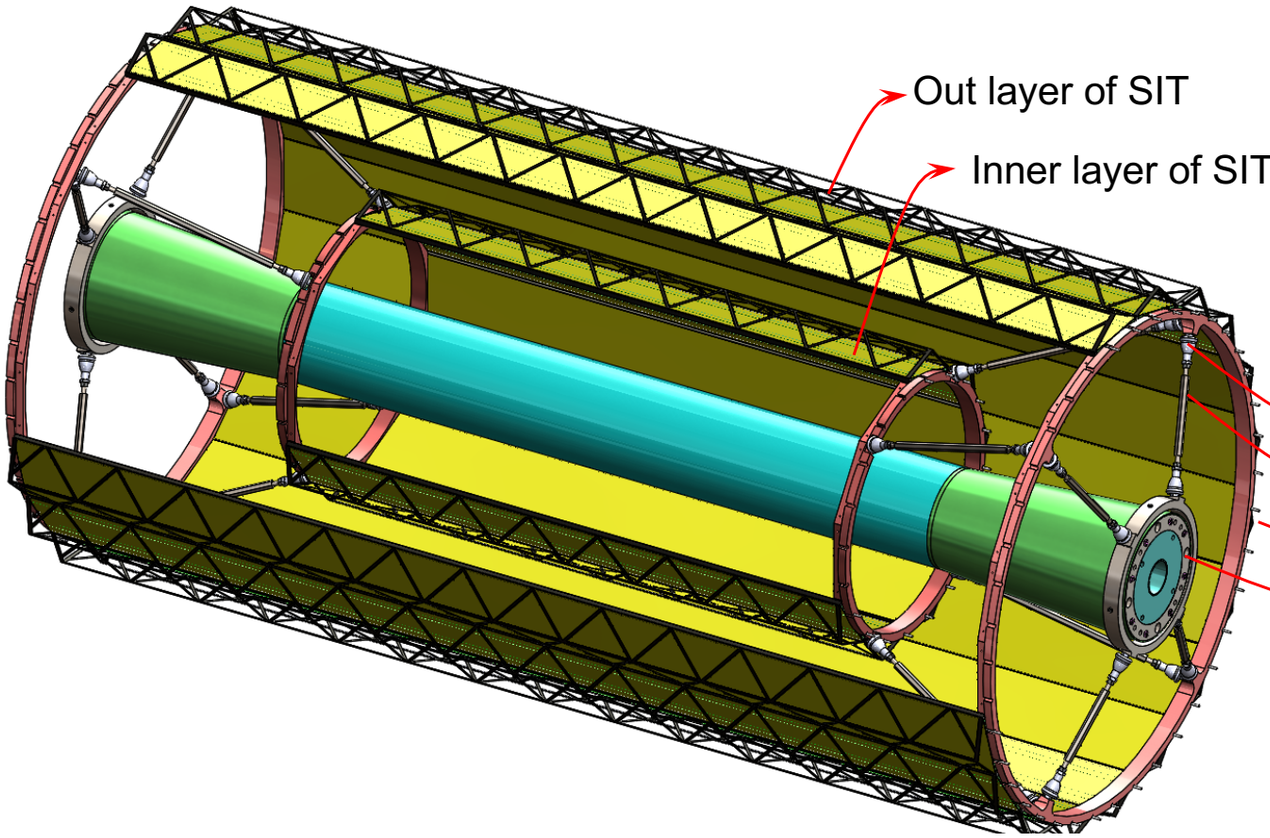


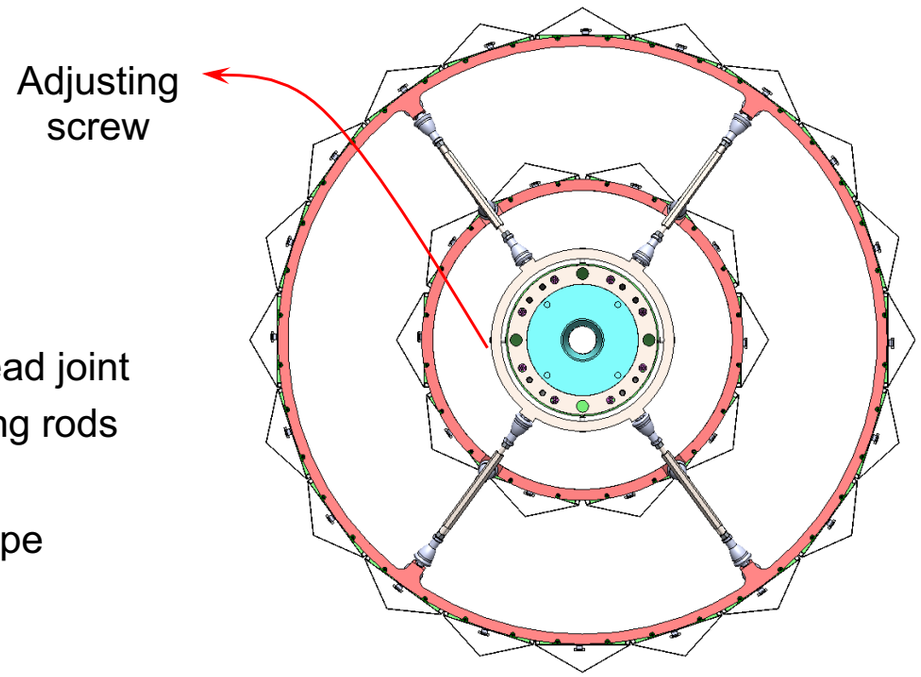


System design: mechanical support

CDR baseline design with 2 SIT layers.

To be optimised: New layout, interfacing between sub-detectors, integration scheme





Conclusions & Outlook

We have a good sensor with ATLASPix3 that fulfils all the requirements.

Full characterisation well advanced and ongoing.

Further evolvements towards CEPC and a new 55nm development are ongoing.

DAQ options for larger (test) systems are under development, in particular YARR.

A first conceptual design for a stave is available.

We plan to have a testbeam with a telescope within a year.

Feedback from the tracking task force feeds into the hardware design.

First mechanical support structure designs are being worked on.

A dedicated group has been kicked off.

Backup