Plan of TDAQ Prototype Design

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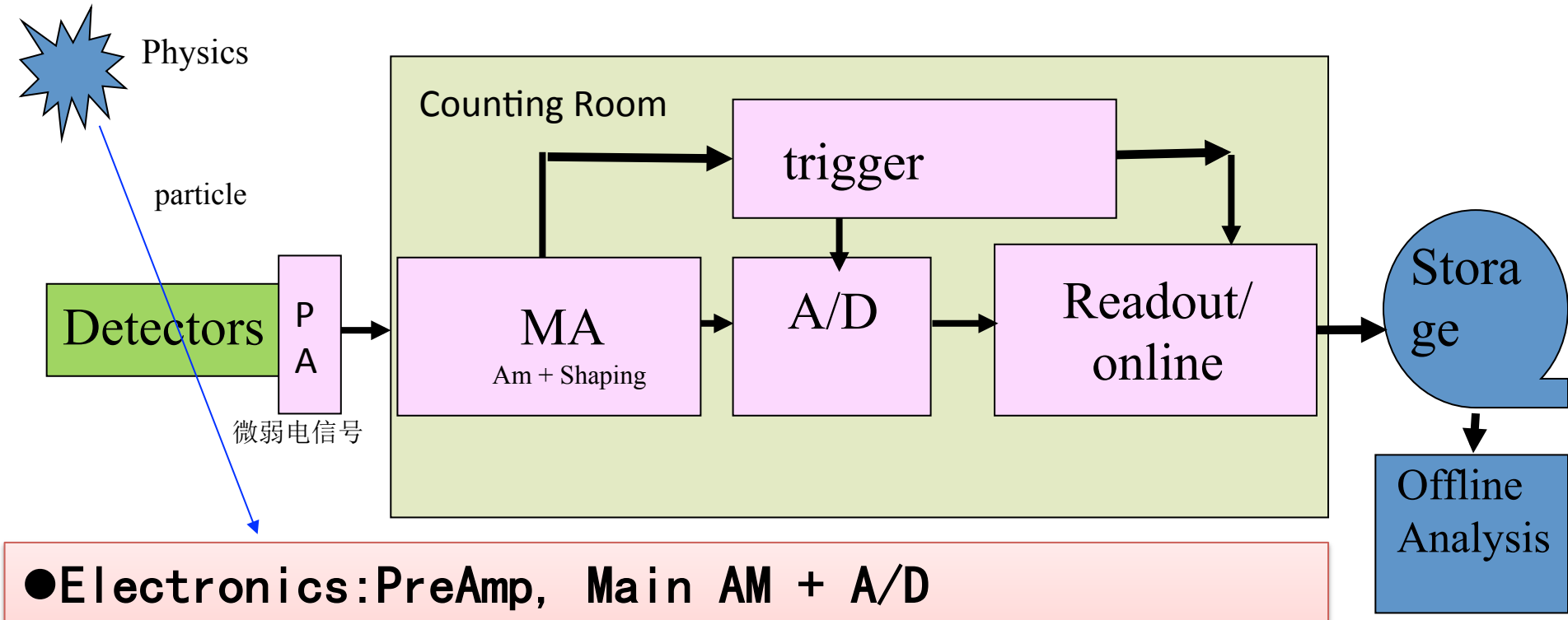
Outline

- New Ides to TDAQ R&D
- Hardware R&D
- Firmare/Software Development
- Demo System with Detector Emulation
- Summary

Preface

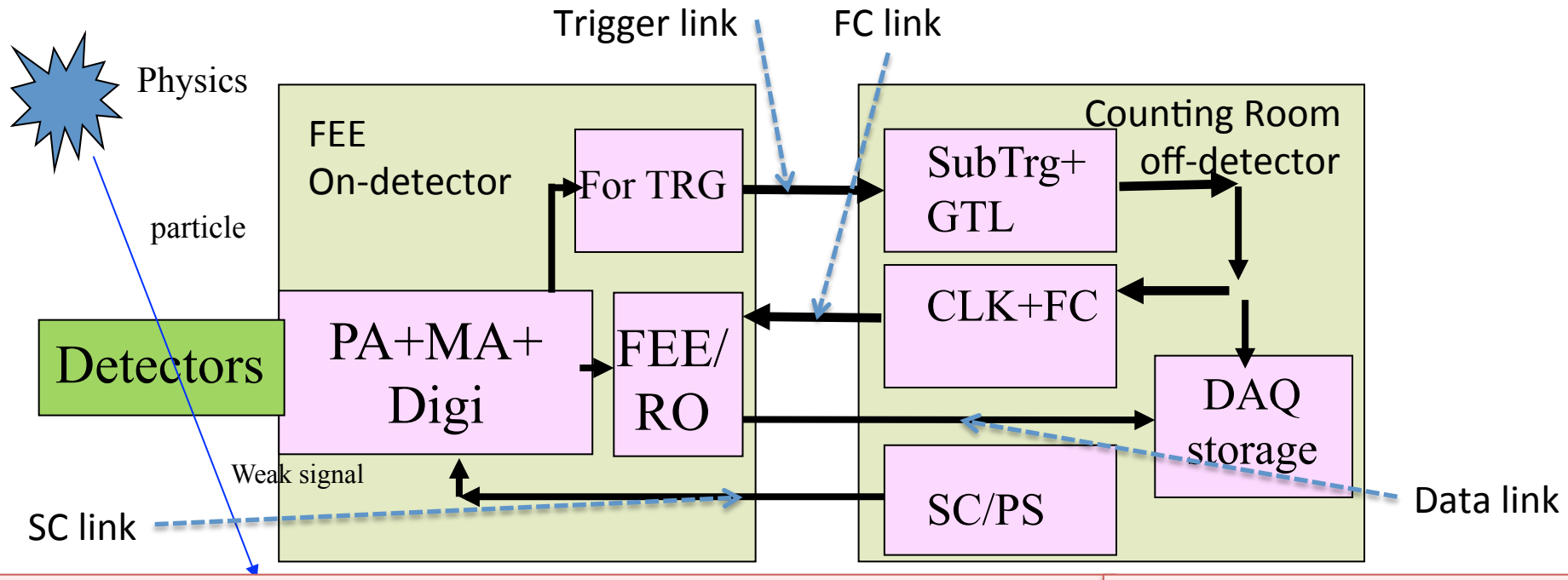
- This proposal is only a state of art mini-TDAQ system R&D to be used for testing purpose of the sub-detector systems development need based on the internal discussion.
- The wide range full TDAQ design will based international efforts.
- Other proposals and efforts/suggestions are welcome!

Traditional experiment and Instrumentation



- Electronics:PreAmp, Main AM + A/D
- Slow ADC(10-100us),decision by trigger
  - Parameter Setting manually
  - Low data bandwidth(3MB/s CAMAC, 320MB/s VME)

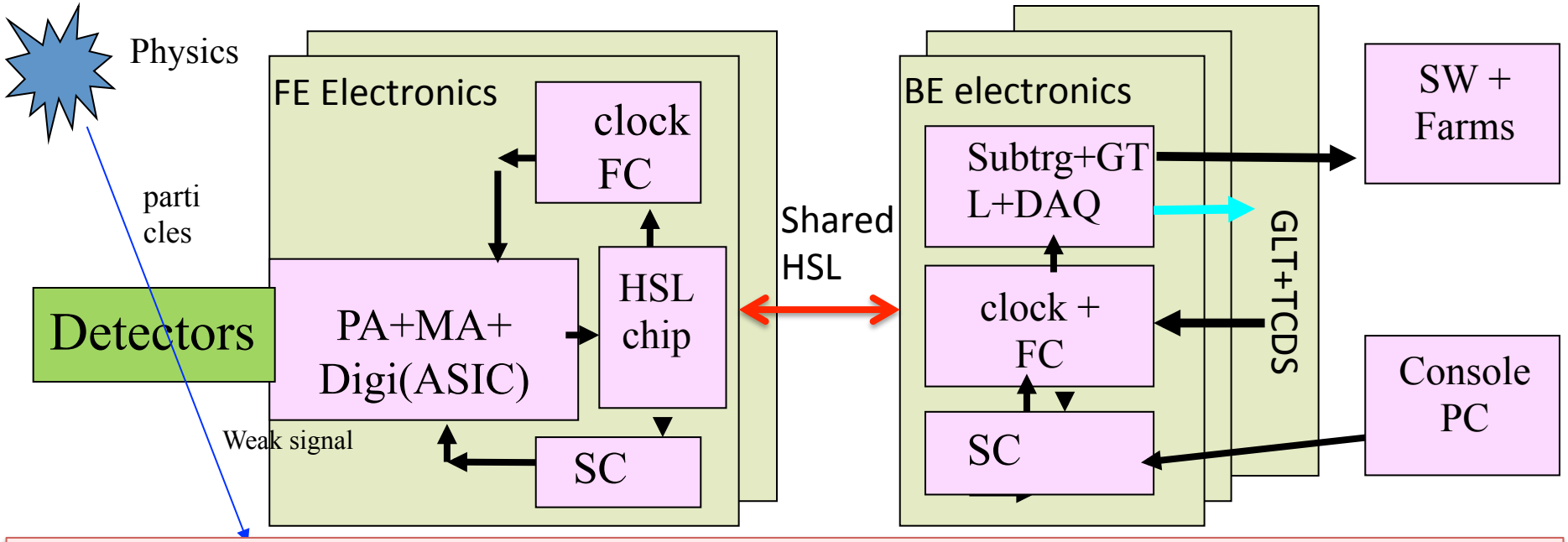
Modern Experiment Architecture



- FEE + TriDAS
- FEE(on Detector)
  - AM+Digi+triggerbasedROboard(8-12b、40-500MSps、800Mb/s-1.6Gb/sBW)
  - triggerPrimitive (signal+data transmitter)
  - digitizedParameterSetting (SC)

- Off-detector
  - FC
  - Remote SC
  - radiationMonitoring (SEU)

Future Trend of Experiment architecture



- FEE(ASIC)
  - 12-16b、500M-4GSps、MultiCH,highdensity(high RO BW)
  - picoSec timing,largedynamicRange (Hpclocks,synchronized)
- HS,MCHlinks:1.6G/4.8G/10Gbps (triggerless continuousRO)
- Unified BE (complexRO,trig,clk,FC,SC)

Questions to CEPC Sub-Detector Systems

- Any zero suppression or compression they might carry out at the front end
  - No
  - YES, then how
- Needs for control and timing signals in FEE
  - Clocks, Synch,BC0,L1A,SC,…
- Any views/preferences on readout style(triggered or trigger-less readout)
  - Trigger sequential readout
  - Continuous sequential readout
  - Non-sequential readout

New Ideas

- Introduce BE electronics vs FE electronics
- Continuous data transmission to BE, L1P based readout in BE
- High Speed Link(HSL) sharing between FE and BE
  - Fast Control(FC with TS) +
  - Slow Control(SC) +
  - Data link
- Time compensation/Phase alignment in HSL

Experience from:
1. BESIII Trigger FC
2. Belle2link Hslink Sharing
3. CERN GBT protocol

Proposals for TDAQ R&D

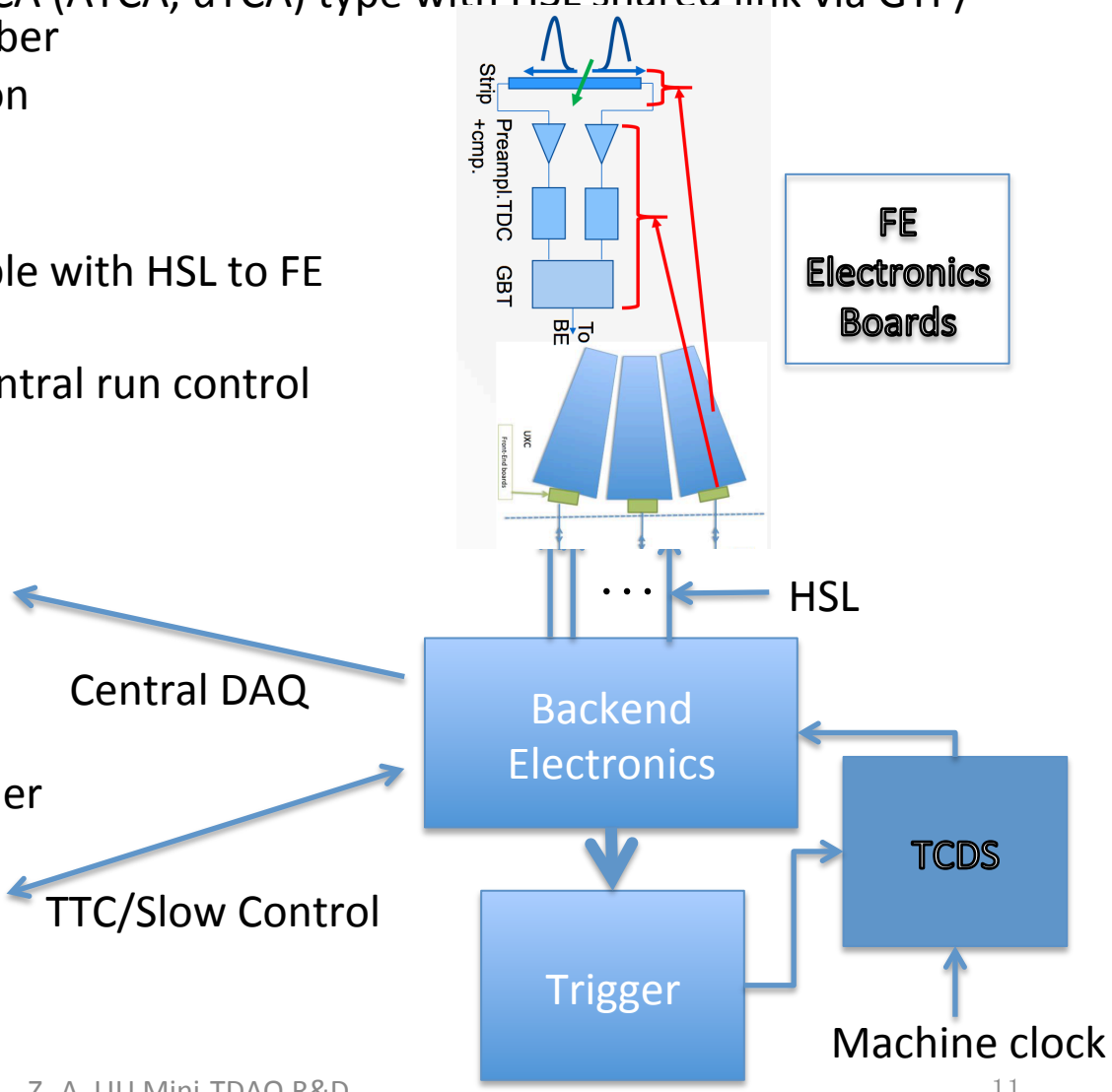
- Q1: Any zero suppression or compression they might carry out at the front end
  - No
  - YES, then how
- A1: ZS if possible with MUX/DEMUX between FE and BE Electronics
- Q2:Needs for control and timing signals in FEE
  - Clocks, Synch,BC0,L1A,SC,…
- A2:Fast Control(FC) + Time stamp by BX
- Q3:Any views/preferences on readout style(triggered or trigger-less readout)
  - Trigger sequential readout
  - Continuous sequential readout
  - Non-sequential readout
- A3: Trigger based, but triggerless FEE to FEB, Continuous, Sequential

Elements of the R&D

- Prototype/Mini system for a TDAQ with all elements
  - Trigger(TRG)
  - Readout(RO)
  - Fast control(FC)
  - Slow Control(SC/FEE Parameter setting)
  - DAQ/Event Building(EB, not covered this time, later with LiFei)

Unified Hardware

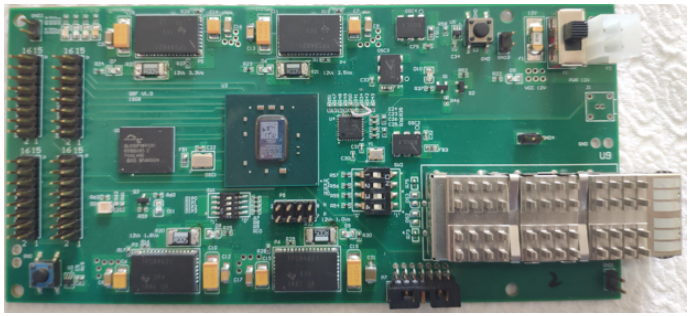
- FE
  - Single board, NIM, VME, xTCA (ATCA, uTCA) type with HSL shared link via GTP/ GTH/GTX port and optical fiber
  - Signal processing, digitization
  - Output to BE via HSL
- BE
  - xTCA (ATCA, uTCA) preferable with HSL to FE
  - Fast control to TCDS
  - Slow control interface to central run control
  - Output to trigger
  - Readout for DAQ
- Trigger
  - Inputs from BE
  - Output to TCDS
- DAQ/Network
  - 10/40 Gb link to Event Builder
  - Monitoering
  - Data storage
- TCDS



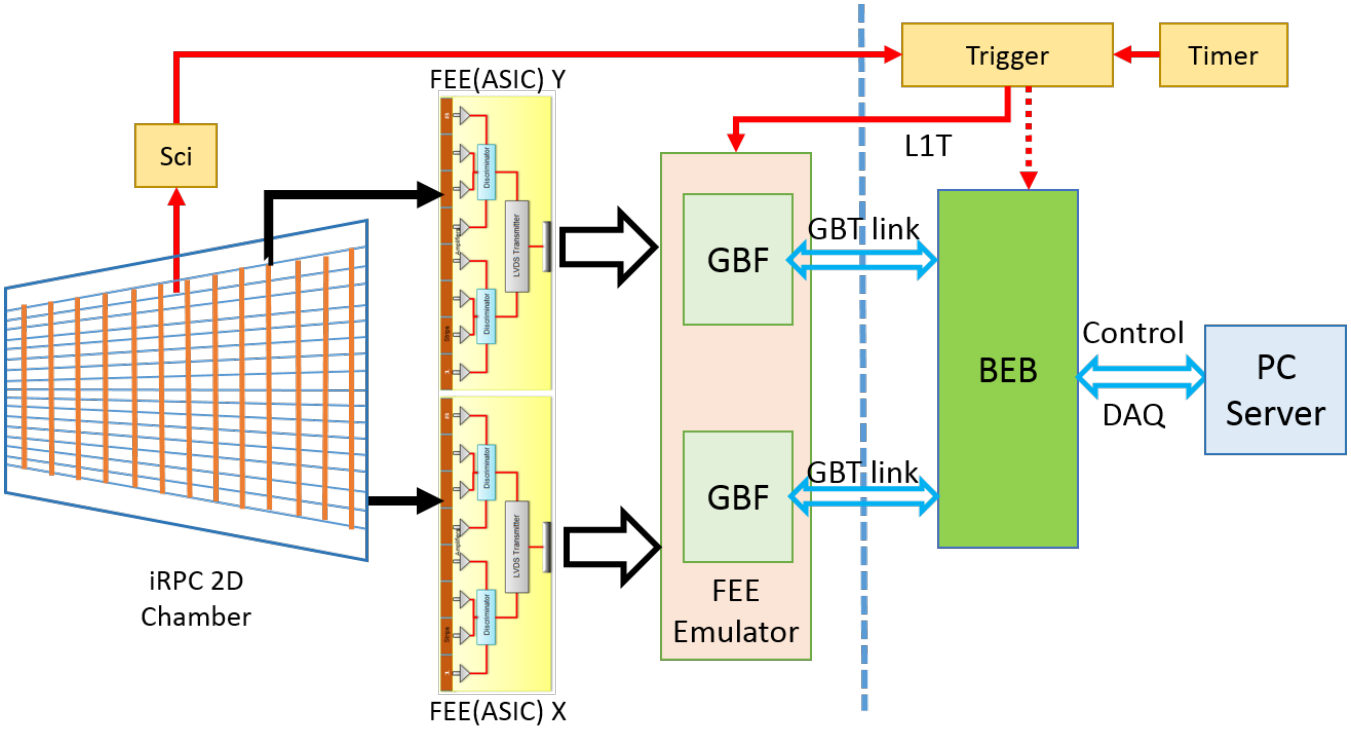
FEE

A common board for data collection (GBF)

- Kintex-7 FPGA: GBT-FPGA, TDC-FPGA, Rising&Falling Edge, 2.5ns
- E-link Interface: 32 pairs of LVDS input
- SMA Interface: External clock input from BEE
- Trigger Interface: Pulse Generator or Scintillator
- QSFP: 4-channel optical module, GBT link



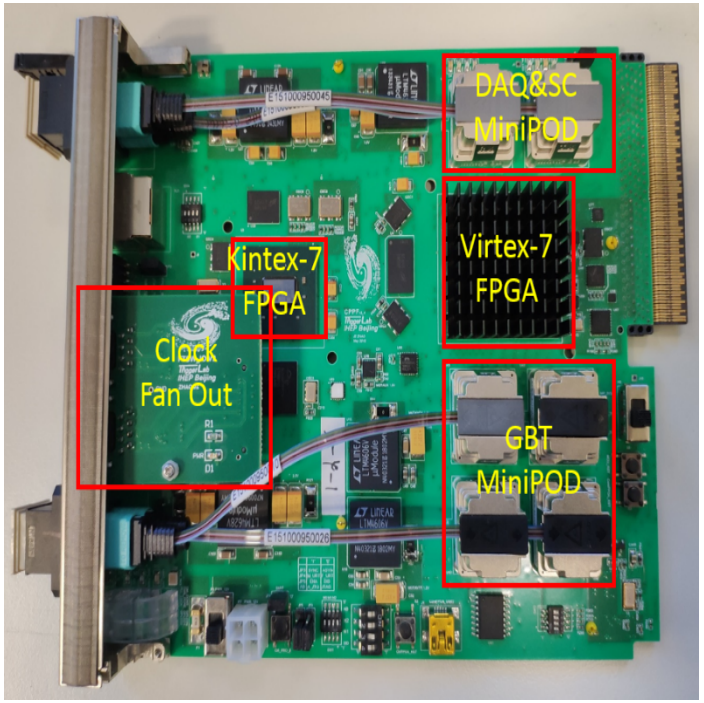
- Detector
  - ?
- FEE
  - ASIC/interface
  - GBF unified



Backend electronics

- BEB： uTCA/AMC card
  - Virtex-7 FPGA： Core FPGA, to realize GBT link transmission and data processing;
  - Kintex-7 FPGA： Control FPGA, clock configuration and BE hardware control;

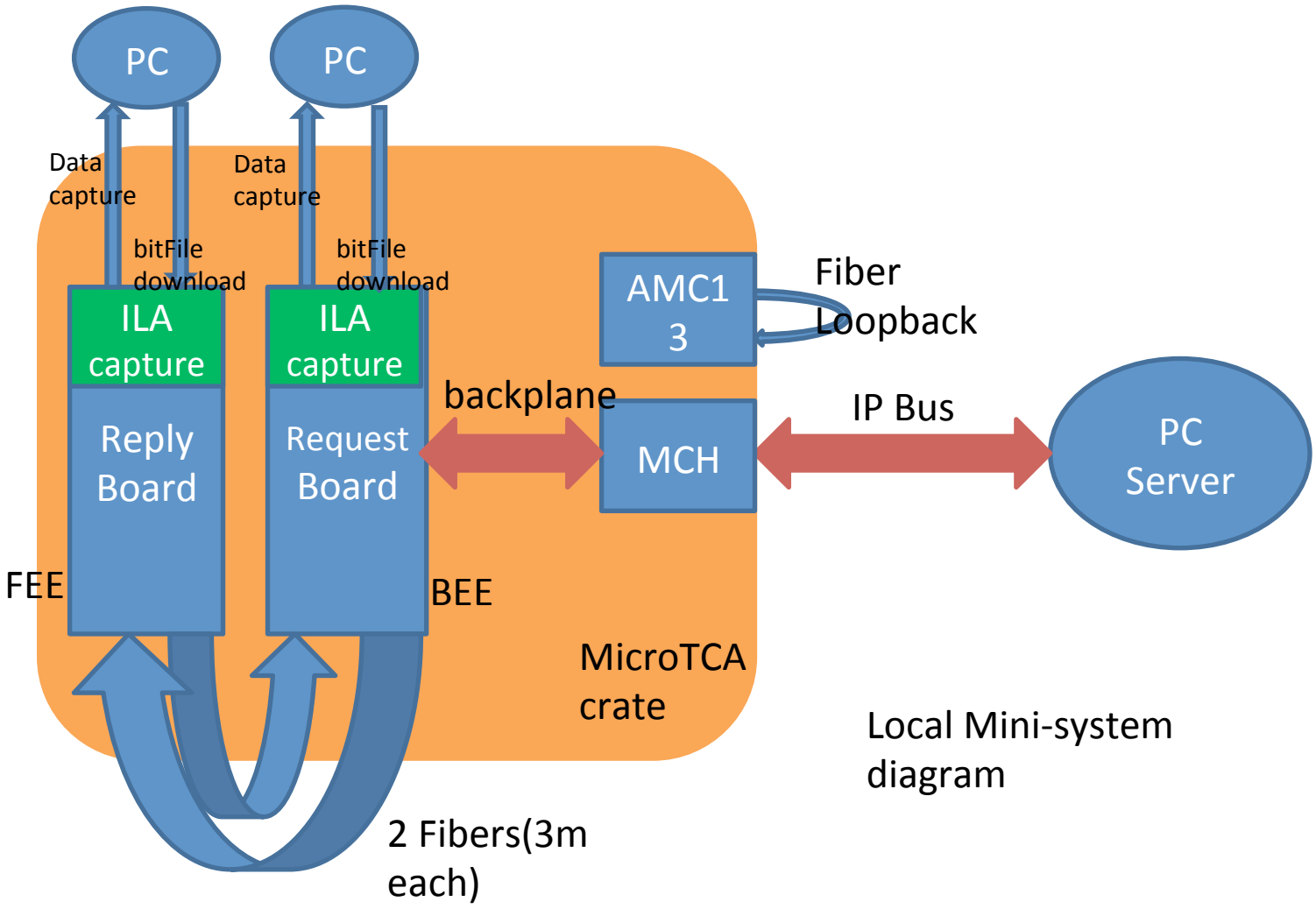
- BE System
  - µTCA compliant BEB
    - core board
  - a µTCA crate,
  - an AMC13 card,
    - system clock and fast control
  - a µTCA Carrier Hub(MCH),
    - manage the whole system
  - a sever PC.
    - slow control and DAQ



Roadmap

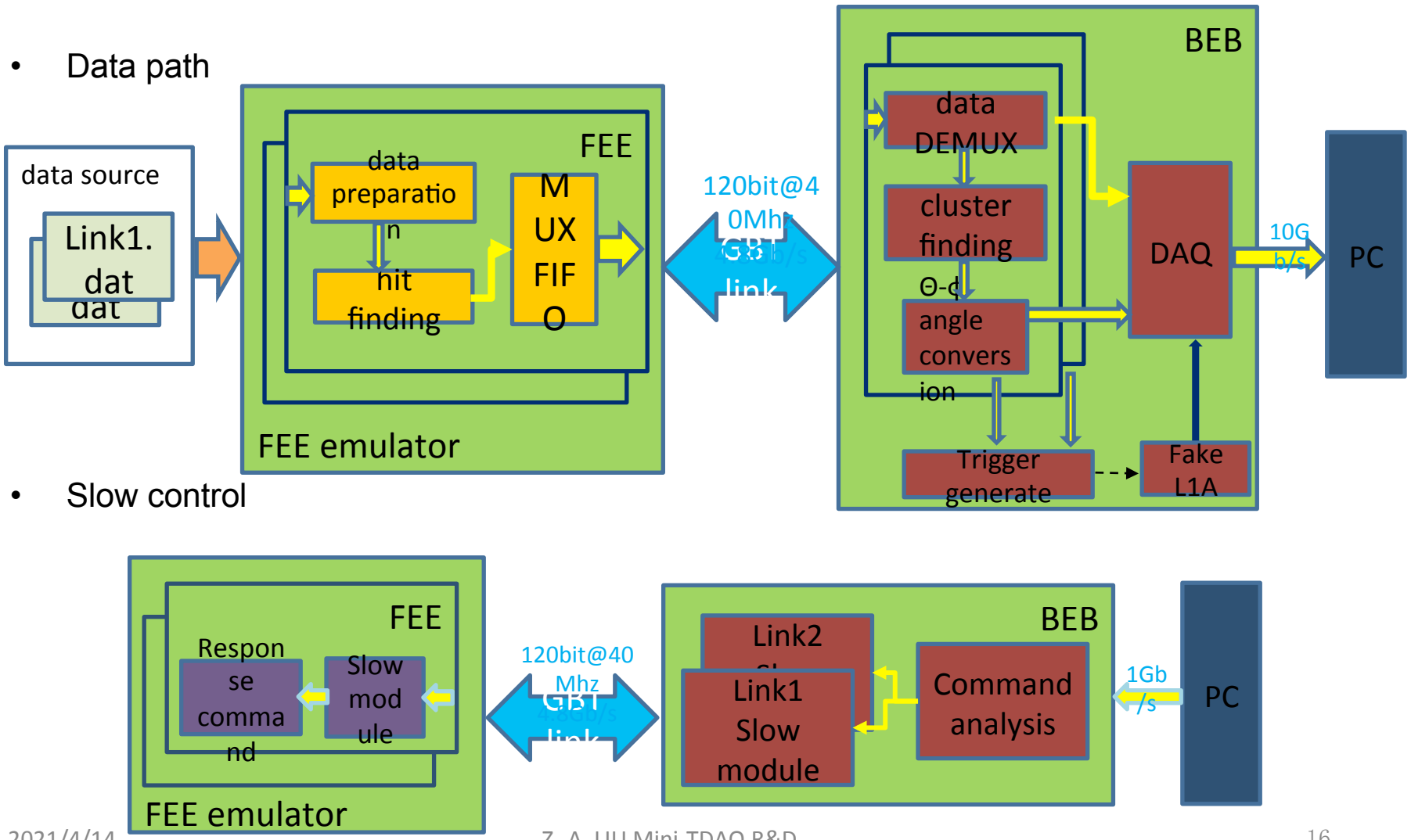
- Hardware Development(Key boards)
- Firmware/Software Development
  - Simulation
  - Emulator
  - Data transmission
  - FC/SC implementation(FEE/BEE sides)
  - Trigger (Detector specific)
  - DAQ/RO(general/detector specific)
- Demo System
- Application/verification with example Detector

Data flow in the Mini-system



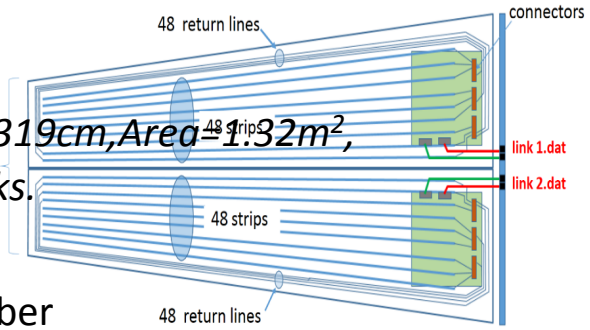
Demo system firmware blockdiagram

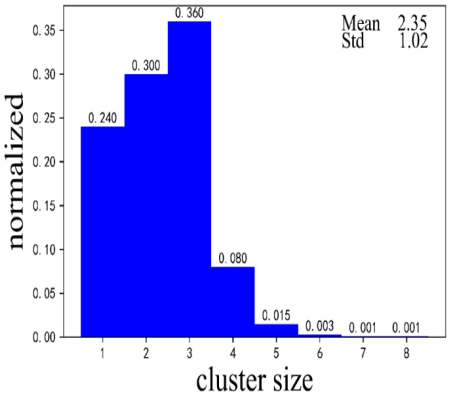
- Firmware design：
  - Data path
  - Slow control

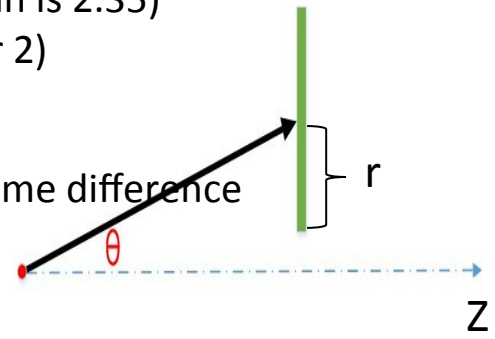


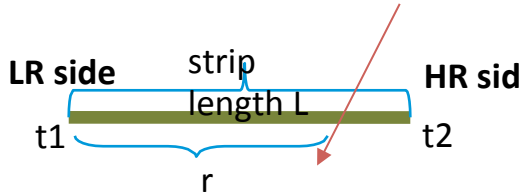
Detector hits Simulation

- data source generation：
  - Parameters setting
    - RE3/1: $R\downarrow in$ =153cm, $R\downarrow out$ =319cm, Area=1.32m^2, contains 96 strips， read out by 2 links.
  - Simulate detector hits
    - Random hit point(r, ϕ) in a chamber
    - Smear of ϕ direction
    - Cluster size randomization(1-8,mean is 2.35)
    - Cluster Number randomization(1 or 2)
  - FEE TDC data generation
    - Hit position: r is calculated by the time difference of signals from both
    - TDC Data unit(32 bits)
      - devAddr： FPGA ID
      - chanAddr : channel address
      - Coarse time: combine BCN(Preserved, 12
      - Fine time: responsible to the precision, 2
    - Digitization: For each fired strip, 2 *32-bit TD
      - Channel-HR TDC-data + Channel-LR TDC-data







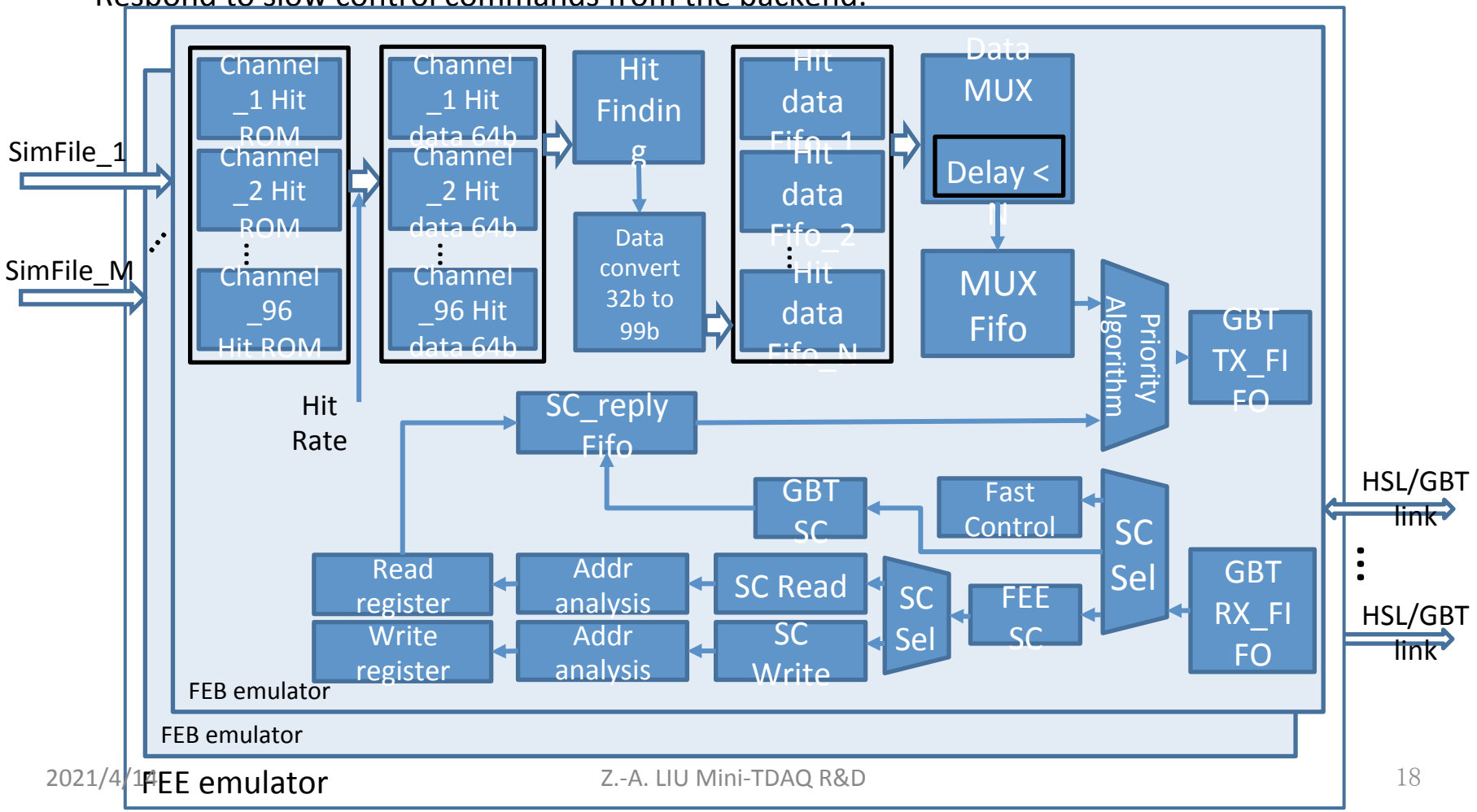


$$r = 1/2\ L - (t2 - t1)$$

devAddr	chanAddr	TDC data		
		Coarse time		Fine time
2	6	12	4	8

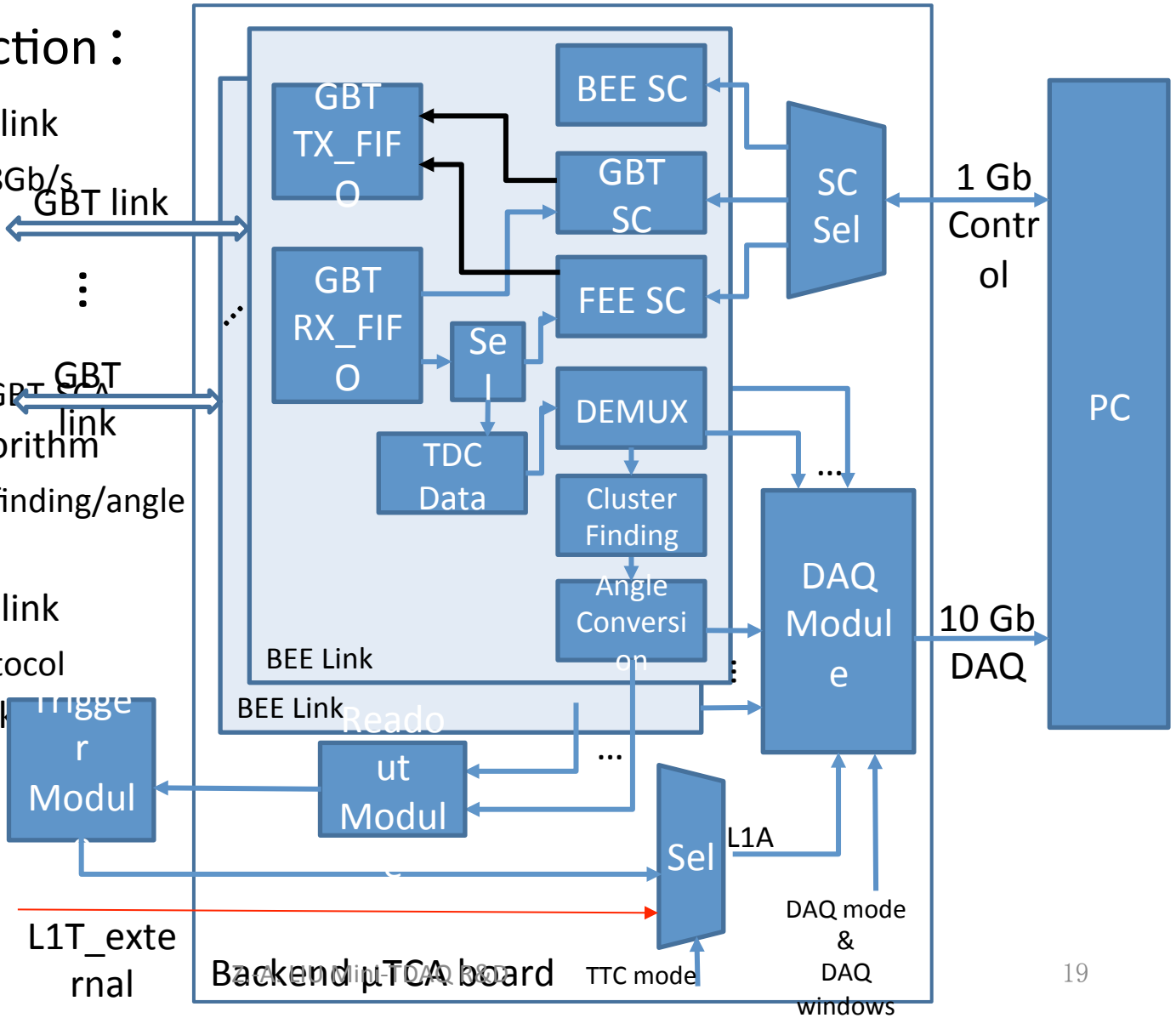
FEE emulator firmware Development

- Principle:
  - Encode the simulated TDC data to generate FEE uplink TDC-data frames, which are transmitted to the back end through the GBT link.
  - Respond to slow control commands from the backend.

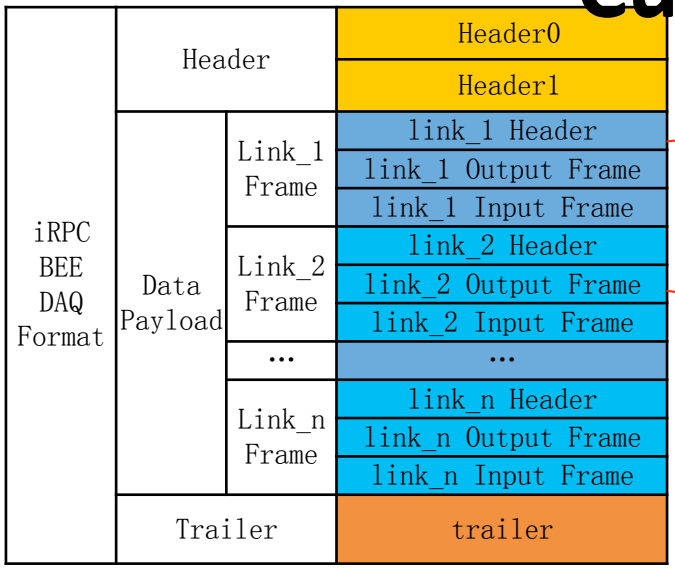


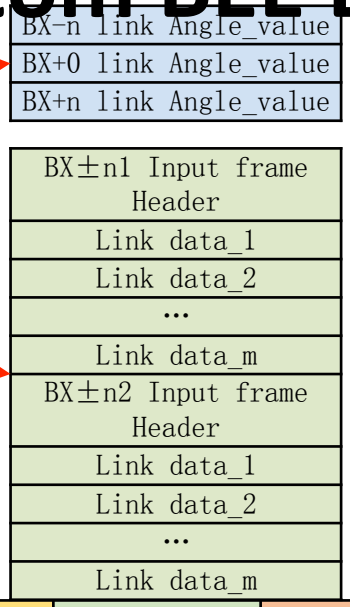
Backend electronics system

- BE firmware function：
  - GBT transmission link
    - Bidirectional, 4.8Gb/s
  - Fast control
    - BC0/resync
  - Slow control
    - BEE-SC/FEE-SC/GBT-SCA
  - Clusterization algorithm
    - DEMUX/cluster finding/angle
  - DAQ algorithm
  - PC to BEB control link
    - 1Gb/s, Sitcp protocol
  - BEB to PC DAQ link
    - 10Gb/s, TCP/ip



Custom BEE DAQ data format



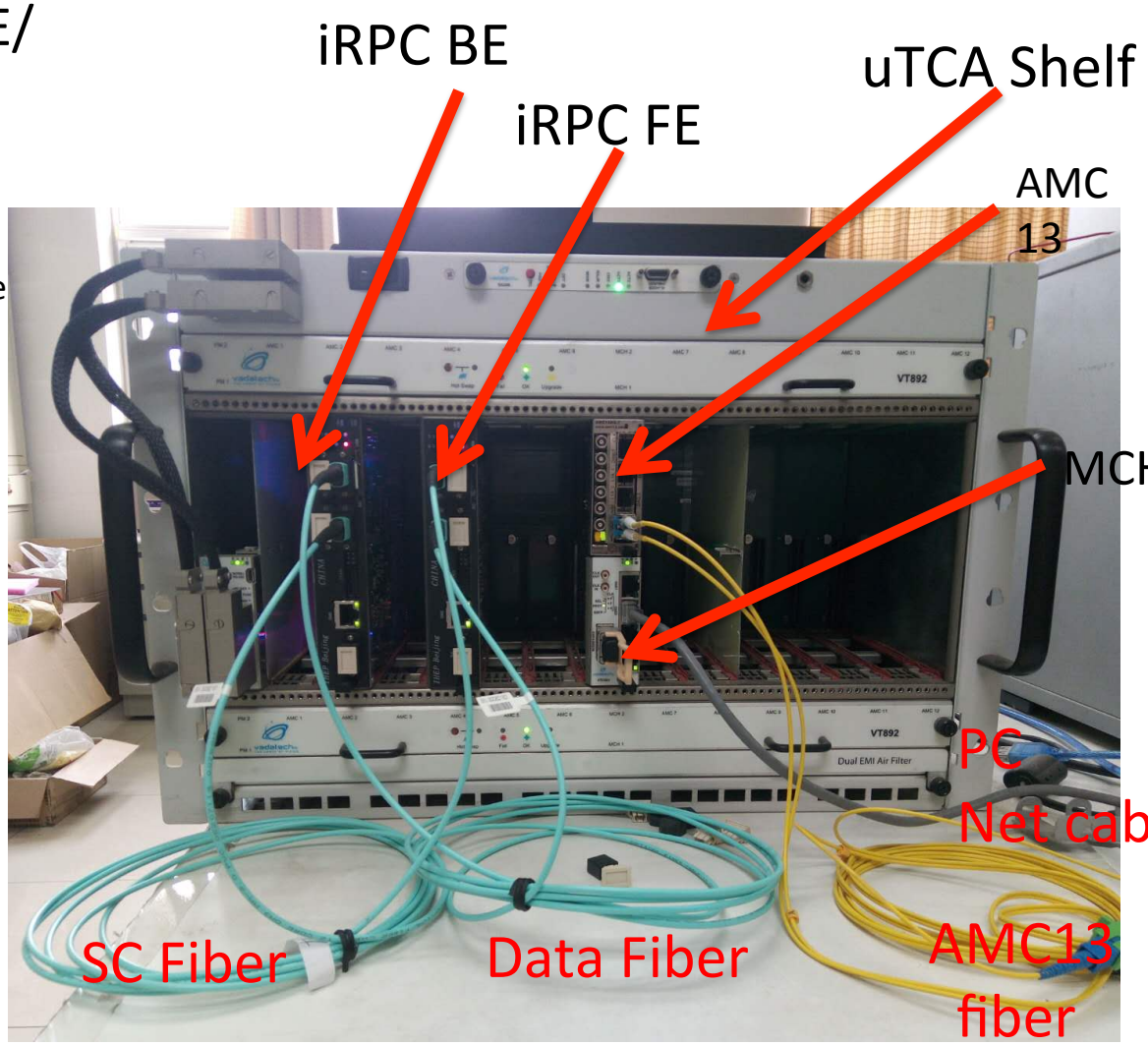


The DAQ data format is only used for the current BEE firmware development

	Byte 7								Byte 6								Byte 5								Byte 4								Byte 3								Byte 2								Byte 1								Byte 0							
	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Header0	x″DEADBEEF″																								BEE_version																Board_ID																			
Header1	Trigger Number																																Window(TX & RX)								Mode(RX/TX/ RX&TX)								Event Length															
Link Header	X” FFAA”																LinkID								Trigger Number																											link Length							
Link Angle_value	cluster_1 Theta(R value)																cluster_1 Phi																cluster_2 Theta(R value)																cluster_2 Phi							
Input Frame Header	X” FFBB”																LinkID								X” FFCC”																BX number								X” FF”								Length							
Link Data	HR1 rising_edge																																LR1 rising_edge																											
	HR2 rising_edge																																LR2 rising_edge																											
	…																																…																											
	HR_m rising_edge																																LR_n rising_edge																											
Trailer	CRC32																																x″BEEFDEAD″																											

DEMO System

- Complete DEMO System FE/ BE
  - 2 ixFP cards
    - 1 ixFP cards for slow control/ processor
    - 1 ixFP cards for iRPC data source
  - 1 AMC13
    - TTC/TTS
    - Management
  - 1 MCH + 1 PC
    - Slow control
    - Management + data storage
- Functions
  1. Emulation/Development System
  2. Hardware, GBT/GBT based
  3. Detector Simulator/data source
  4. Fast/Slow control, cluster finding, data saving on to disk



Emulator to BEE testing

Test List

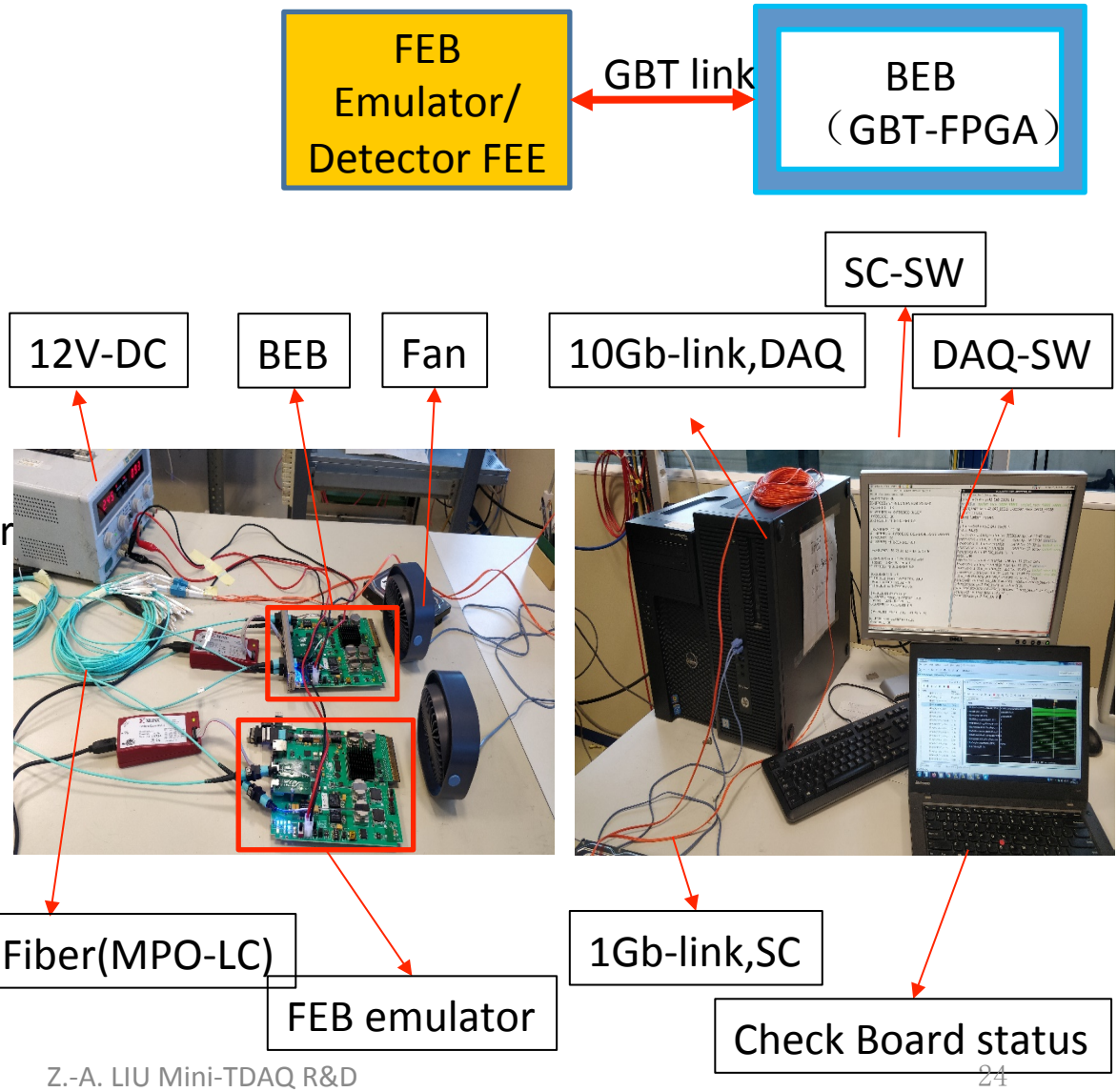
- Check GBT link establish status between FEE emulator and BE board
- GBT link Long time stability test(> 3 days)
- Data transmission Error rate test between FEE emulator and BE board
  - FEB send pseudo-random data and BE check the data
- Slow control frame write and read check
  - Write and read a custom address
  - Single frame mode
  - Burst mode
- Slow control frame repeatedly write and read check
- GBT SCA write/read test
- Data process algorithm check
  - Check DEMUX, cluster finding, and angle conversion algorithm
  - Check data package and upload algorithm

Verification with Demo Detector

- Which Detector as example?
  - To be decided

Possible Standalone Demo system

- System setup：
  - 2 boards
    - one acts as FEB emulator
    - one acts as BEB
  - Power supply
  - Fan
  - PC- desktop
    - 1Gb-link and 10Gb-link Har
    - Slow control software
    - DAQ software
  - PC- laptop
    - Check firmware algorithm



Summary

- Proposal for a Demo Mini-TDAQ System
- Key components in the Demo System described
- Roadmap/plan is proposed
- Firmware/Software development described
- Demo Emulator system is foreseen
- Relevant work is ungoing

Thanks for patience!