Status of the CEPC HCAL

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On behalf of the CEPC Calorimeter Group

CEPC Day, 3/25/2021

Outline

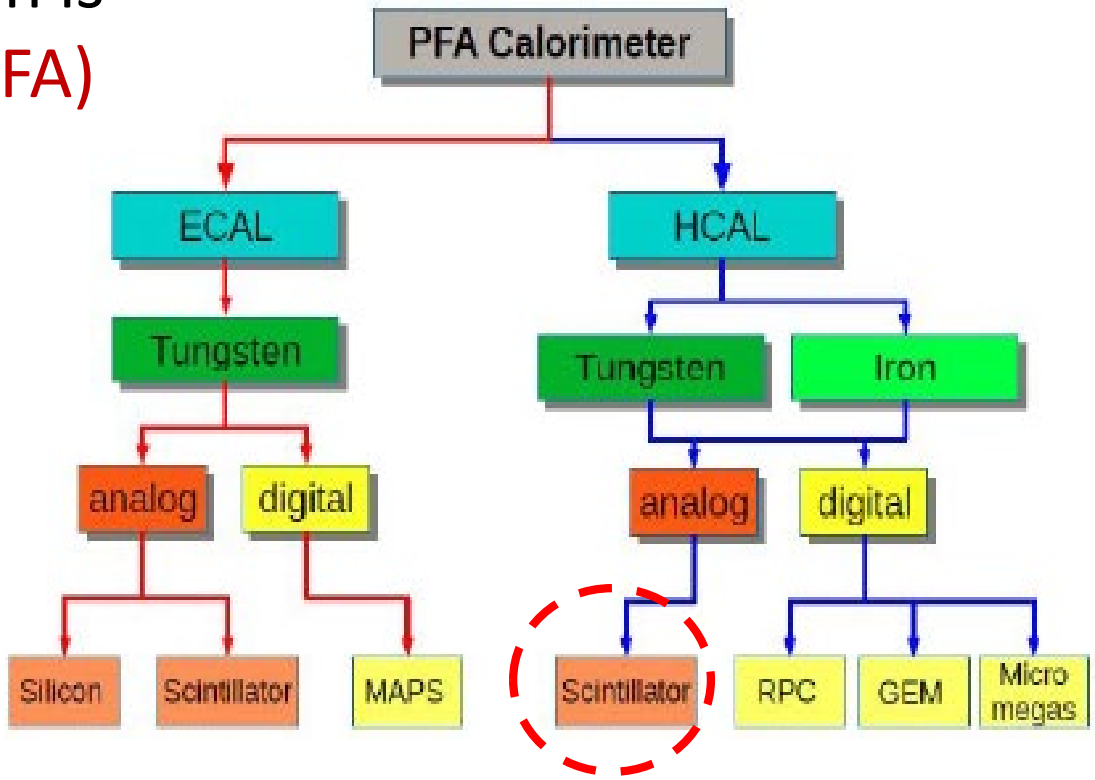
- Background introduction
- Progress of AHCAL prototype
- Progress of SDHCAL
- Summary

Background

- The baseline Calorimeter detector option is guided by the particle flow algorithm (PFA)
- Physics requirement
  - Linearity: $\pm 3\%$
  - Resolution: $\frac{60\%}{\sqrt{E(GeV)}} \oplus 3\,\%$
- AHCAL: Scintillator + SiPM

  → Progress of AHCAL Prototype
- SDHCAL: RPC

  → Progress of SDHCAL timing electronics

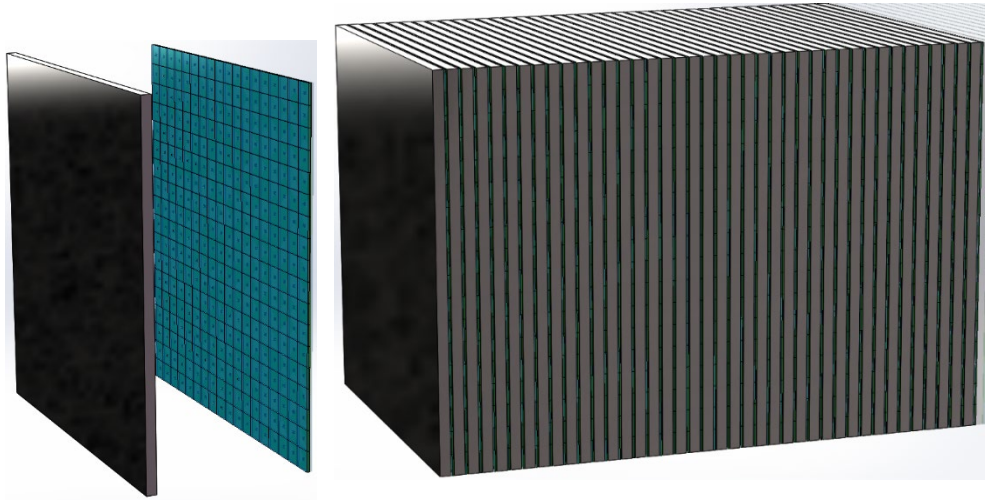


Outline

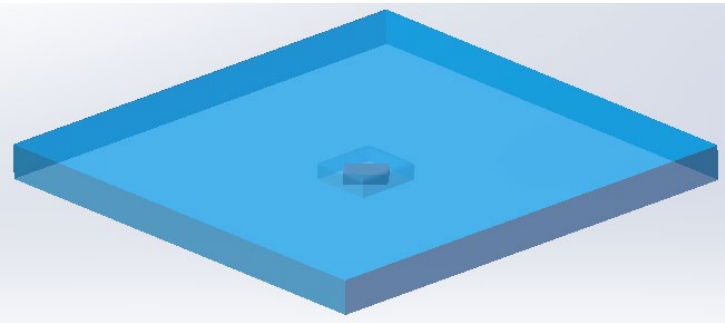
- Background introduction
- Progress of AHCAL prototype
  - Scintillator production and wrapping
  - Batch test of detector cells
  - HBU development
- Progress of SDHCAL
- Summary

Structure of AHCAL Prototype

- Task: BMR < 4% and $60\%/\sqrt{E} \oplus 3\%$
  - validate the CEPC AHCAL option by designing, building and testing a full AHCAL prototype
- Prototype
  - Transverse dimension: 72cm × 72cm
  - Number of layers: 40
- Single layer
  - Stainless steel as absorber: 20 mm
  - Scintillator as sensitive medium: 3 mm
  - SPIROC2E as baseline; KLAUS as another option
- Detector cells
  - Cell size: 40mm × 40mm
  - Sensor: SiPMs from HPK & NDL
  - Total number of channels: 12,960



Single layer and detector part



Detector cell of
40mm ×40mm ×3mm

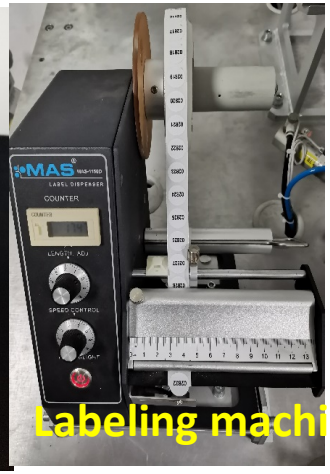
Scintillator Production and Wrapping

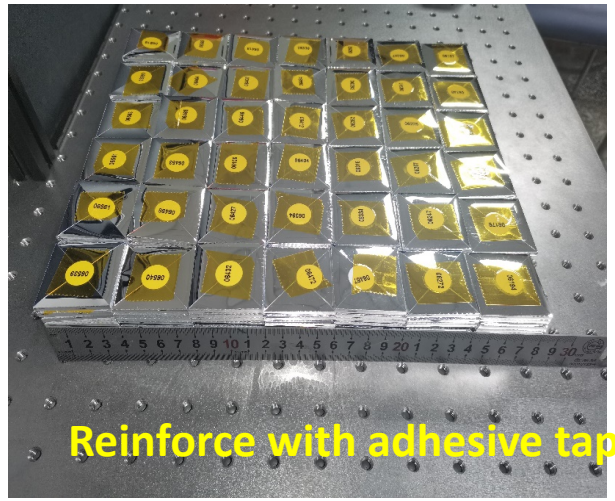
- **16000 scintillators have been produced** using the injection molding technique

1	2	3	4	5	6	7	8	9	10	11	Total
1800	2880	1600	1180	1640	1640	1540	430	2160	890	410	**16170**

- The light yield of each scintillator is about **40 p.e.**, tested by NDL-22-1313-15S

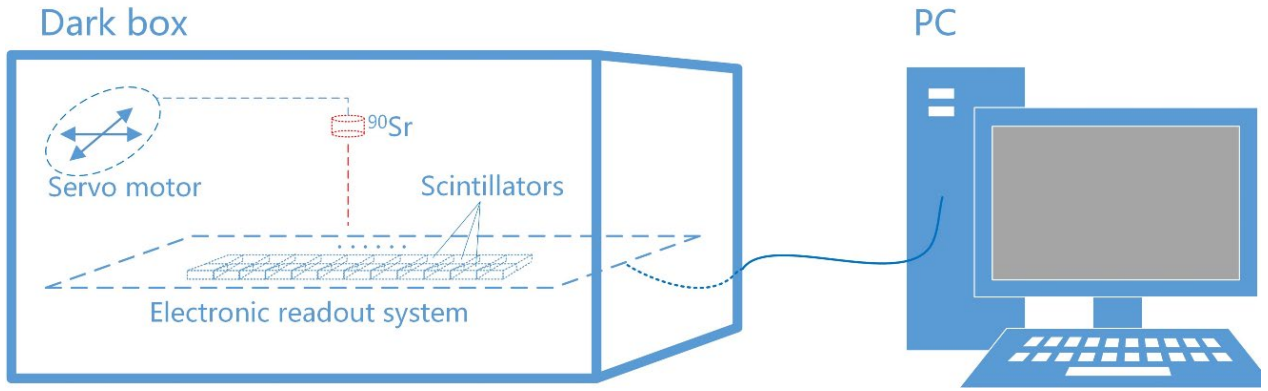
- **Automatic wrapping and labelling**
  - 100 scintillators cost 75min once
  - The remaining tiles is expected to be finished by the next month





Batch Test of Detector Cells

- Test the uniformity of all scintillators
- 13360-1325PE SiPM @5V overvoltage
- Auto-moving MIP source : Sr-90
  - 144 channels each run
- 3 batch testing platforms



Batch Testing Platform

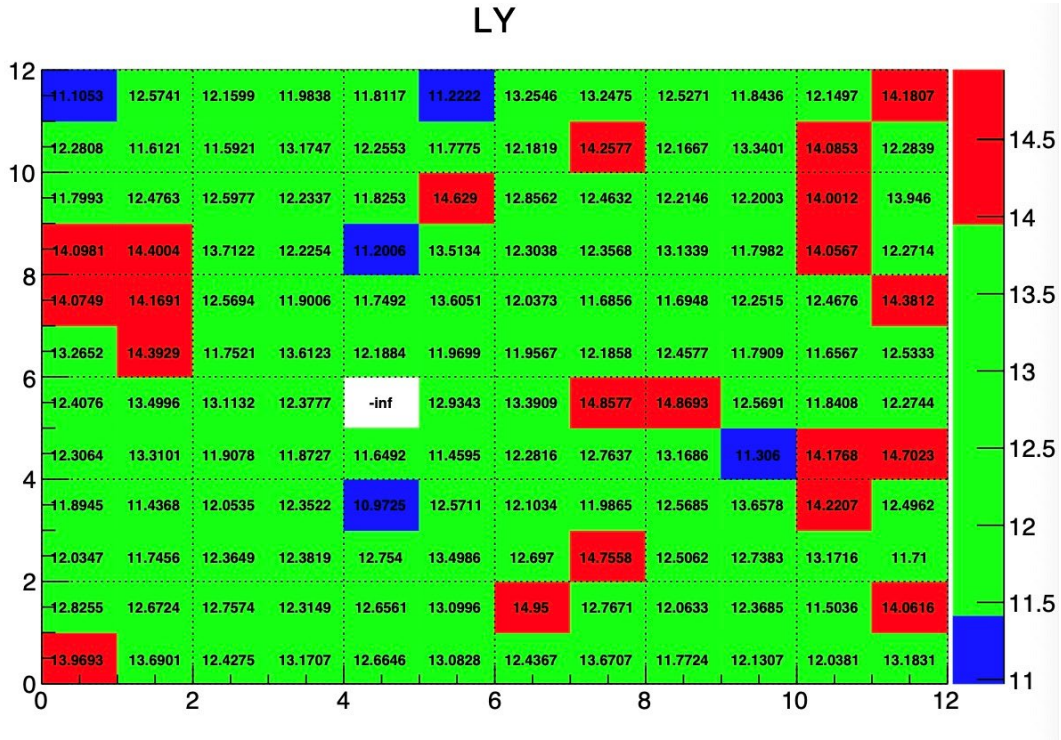
USTC

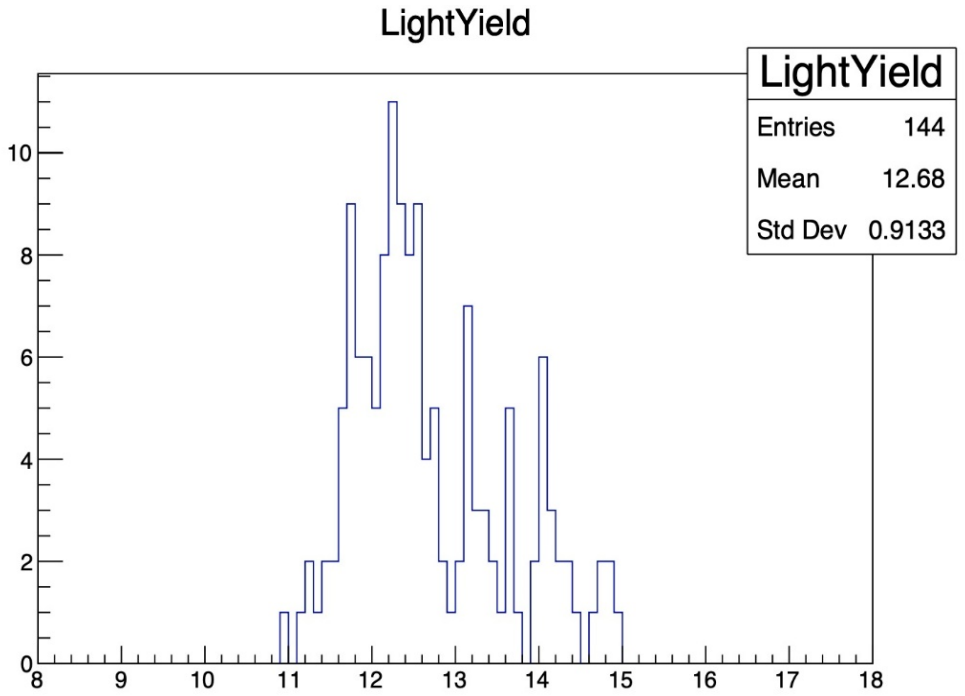
SJTU

IHEP

Batch Test of Detector Cells

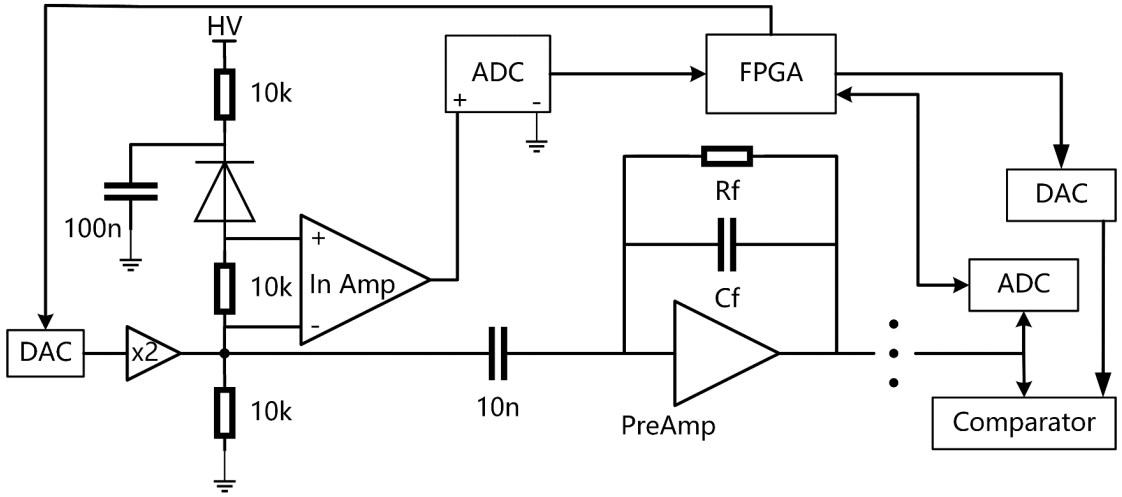
- Uniformity within ±15%
- The difference between channels will be calibrated
- The difference between 3 platforms will be calibrated

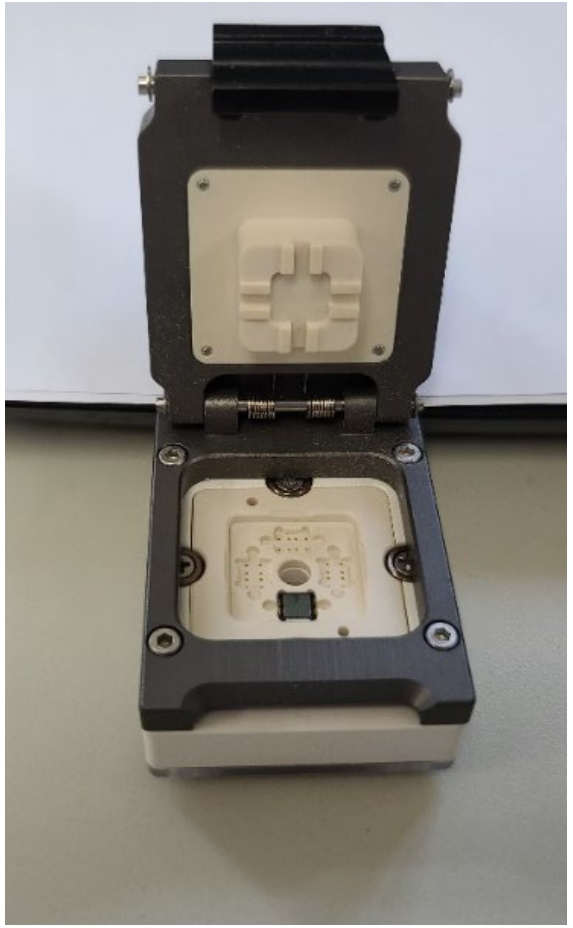




Batch Test of Detector Cells

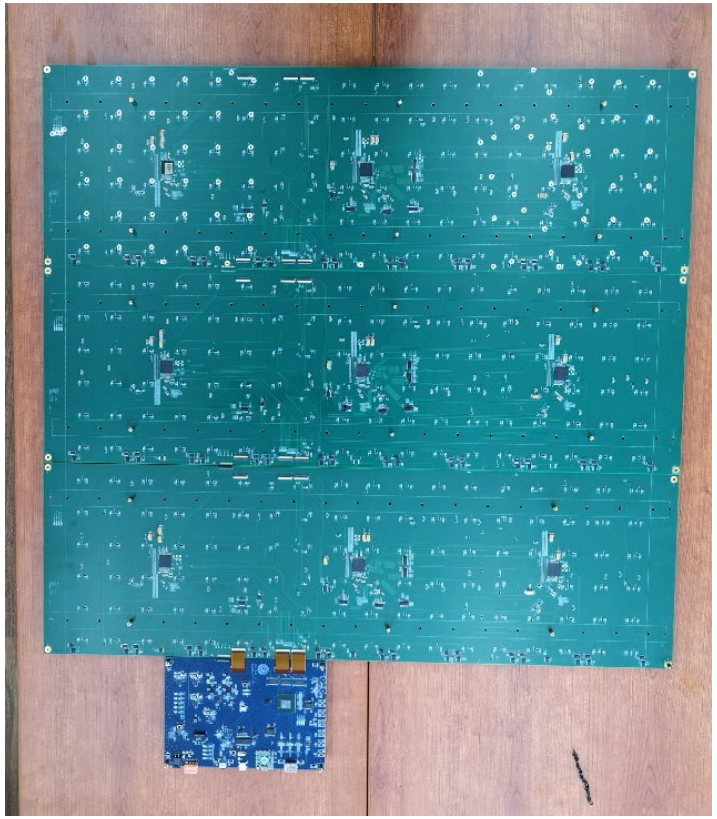
- 7000 SiPMs will be received in two months.
- A SiPM test platform has been designed.
  - A SiPM detachable fixer
  - SKIROC2a readout or discrete-circuit readout
  - Test quality: break down voltage, dark count, gain





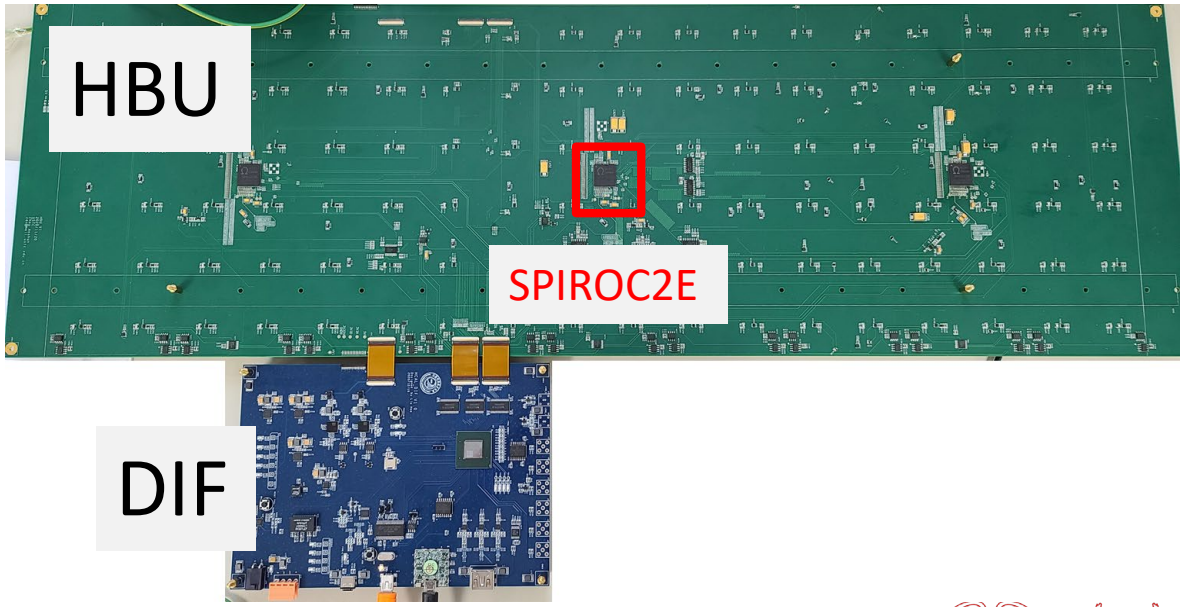
SiPM Test Platform

Development of HBU



HBU:HCAL Basic Unit

- The sensitive size of one layer: $72 \times 72 cm^2$
  - A single layer is equally divided into 3 boards
  - Each board is $78.5 \times 24 cm^2$ and has 108 channels
  - Every layer is controlled by one DIF board
- All electronics parts have been tested and verified.



Schedule of AHCAL Prototype

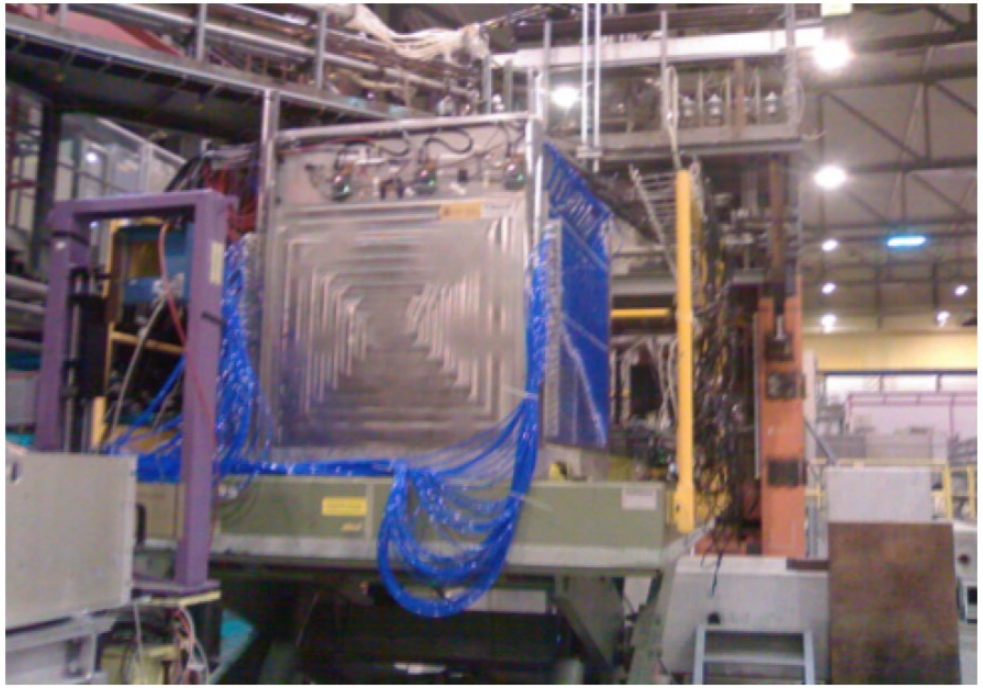
标识号	任务名称
1	成像型强子量能器技术验证
2	1）量能器原型机物理设计
3	1.1) 量能器关键参数的选取和优化
4	1.2) 量能器性能模拟研究
5	2）灵敏探测器的研制
6	2.1) 原材料、器件采购
7	2.2) 灵敏单元结构的设计和优化
8	2.3) 闪烁单元生产工艺的研究
9	2.4) 闪烁单元批量生产
10	2.5) 闪烁单元包装工艺的研究
11	2.6) 闪烁单元批量包装
12	2.7闪烁单元批量测试装置制作
13	2.8) 闪烁单元批量测试
14	2.9) 单层灵敏探测器工艺摸索
15	3）读出电子学和数据获取系统
16	3.1) 原材料、电子元器件的采购
17	3.2) 前端读出板和数据接口板的设计和开发
18	3.3) SPIROC芯片功能测试板开发
19	3.4) 前端读出板和数据接口板的批量制作与测试
20	3.5) 测试用数据获取板的开发与制作
21	3.6) 数据获取板的开发与制作
22	4）SiPM性能监测和刻度系统的研究
23	4.1) 基于LED的监测系统的开发
24	4.2) 基于光纤的监测刻度系统的研究
25	5）机械设计和制作
26	5.1) 探测器灵敏层结构
27	5.2) 原型机吸收体和支撑结构
28	5.3) 束流测试平台
29	5.4) 宇宙线测试平台
30	6）量能器原型机系统集成
31	6.1) 探测器灵敏层的组装和测试
32	6.2) 整体样机的集成
33	7）量能器原型机测试和性能研究
34	7.1) 数据分析软件的开发和准备
35	7.2) 原型机宇宙线测试及质量检验
36	7.3) 原型机束流测试前期准备和运输
37	7.4) 原型机束流测试及样机运回
38	7.5) 测试数据分析及原型机性能研究
39	8）项目总结

Outline

- Background introduction
- Progress of AHCAL prototype
- Progress of SDHCAL
  - Timing electronics development
  - GRPC construction
- Summary

SDHCAL Prototype

- **S**emi-**D**igital **H**adronic **CAL**orimeter technological prototype (SDHCAL)
- High granularity calorimeter based on Glass RPC (cell size 1cm × 1cm)
- **Hits associated to three thresholds**:
  - 1st threshold = 110fC
  - 2nd threshold = 5pC
  - 3rd threshold = 15pC



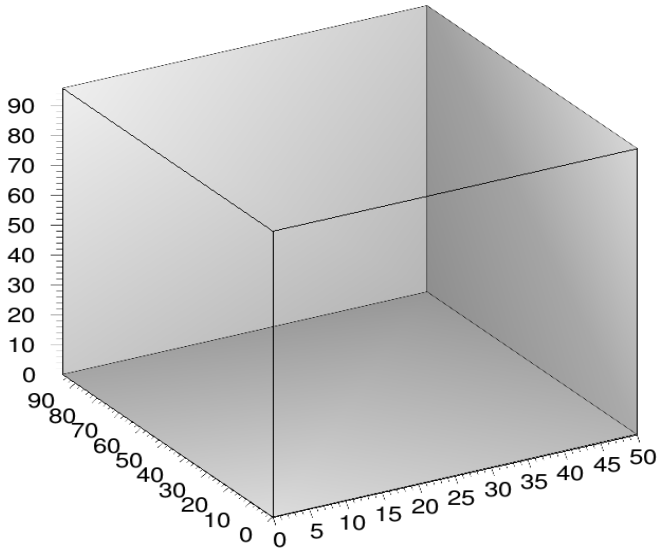
- 48 layers with GRPC as sensitive medium

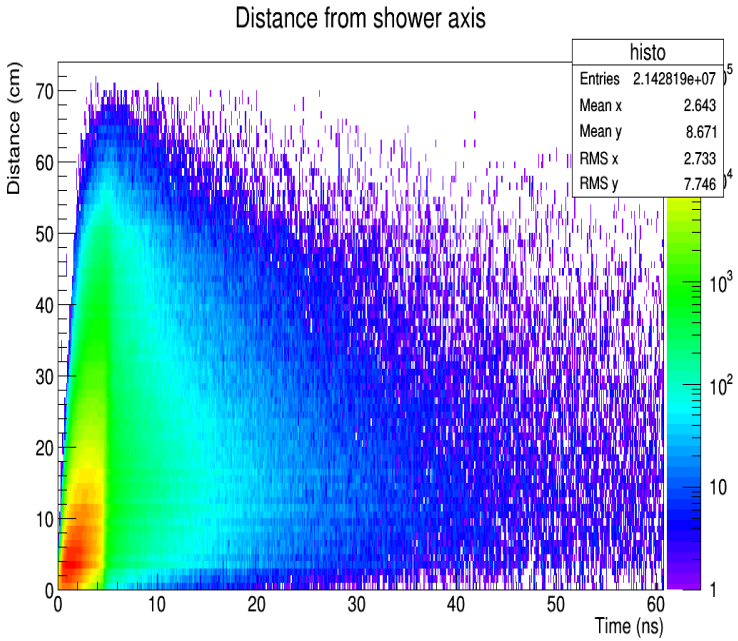
  → Dimensions: 1m × 1m × 1.3m
- 6 Interaction length ($6\lambda_I$)

  → Semi-digital readout

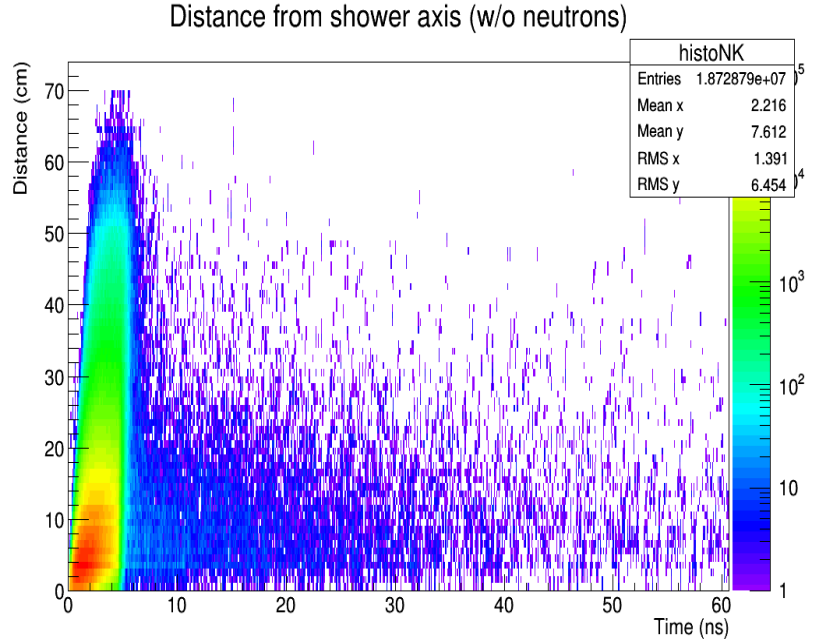
Motivation using Timing Information

- Timing could be an important factor to identify delayed neutron and **better reconstruct their energy**.





With Neutrons

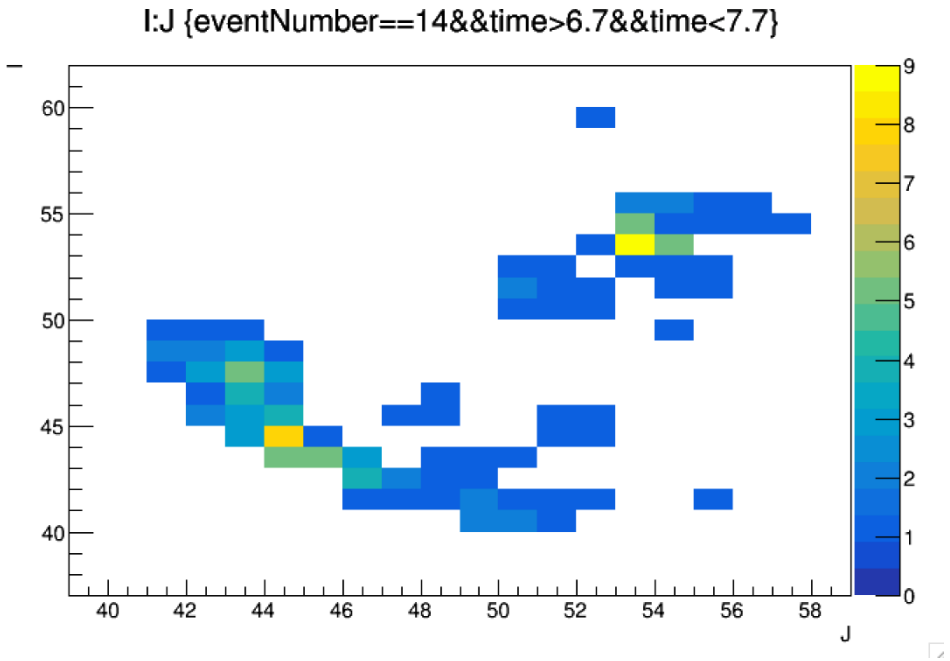


Without Neutrons

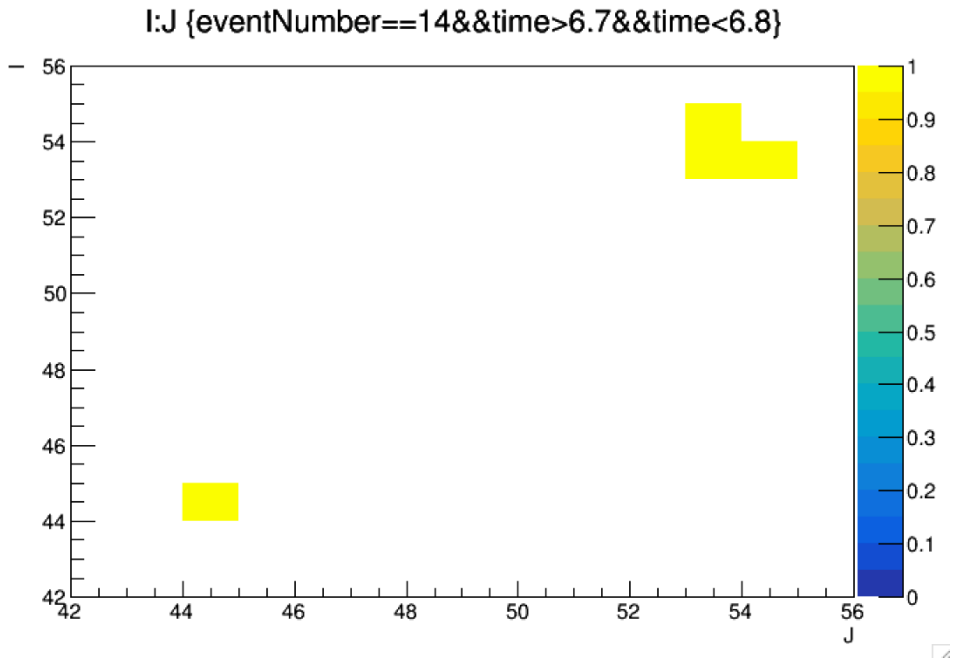
Motivation using Timing Information

- Time information can be very helpful to **separate close by showers** and **reduce the confusion** for a better PFA application.

1 ns resolution



100ps resolution

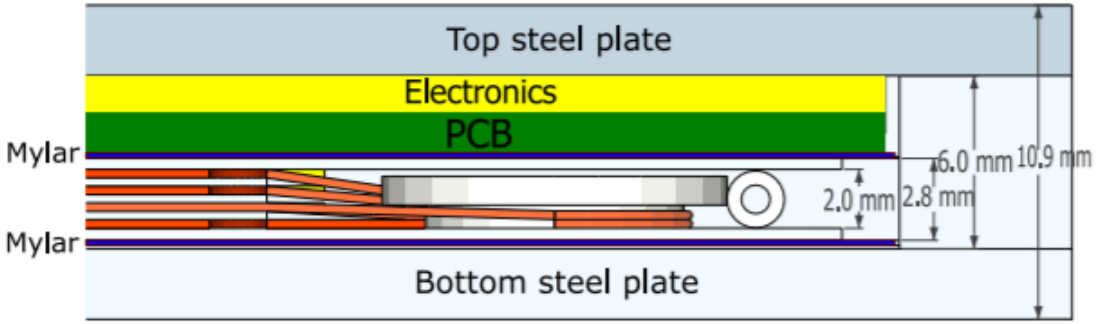


Fast Timing Measurement

- Purpose: => Identify neutral and charged hadrons
- Position, Energy and Timing => 5D HCAL

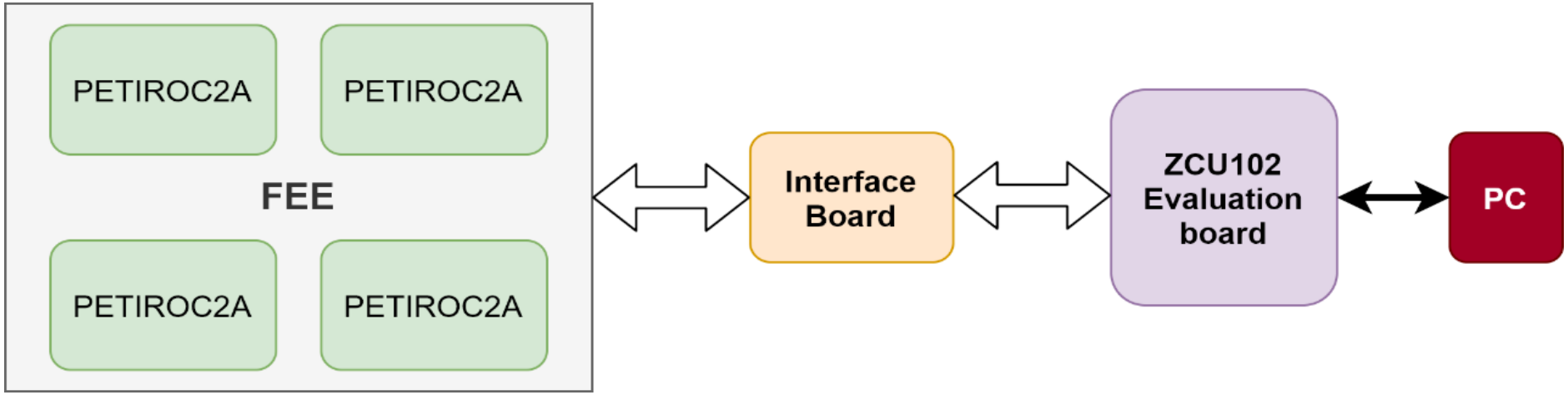
- Adding MRPC layers in the SDHCAL
- Fast timing readout electronics for MRPC readout
  - PETIROC from Omega group (resolution: ~40 ps)

- First step：
  - Design a FE prototype with four PETIROC2B chips



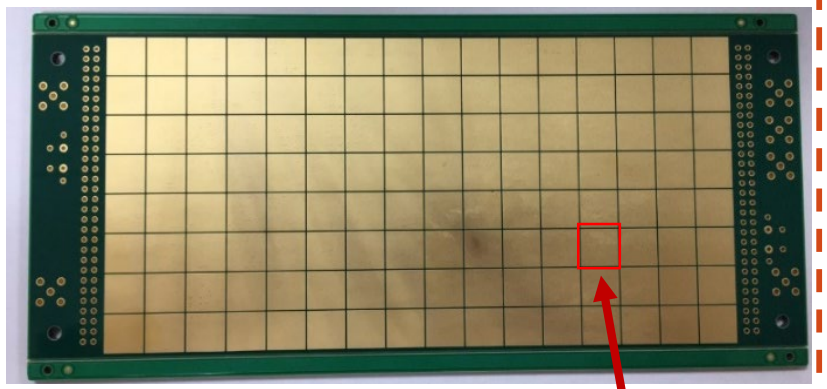
Prototype of Timing Electronics

- The FEE prototype includes four PETIROC chips, 128 readout pads on the PCB bottom side for MRPC induction signals.
- Detector Interface(DIF) card was designed to connect FEE and FPGA board
  - Data transmission, power rail and clock source.
- The DAQ system should be developed to transfer data between FEE and PC.



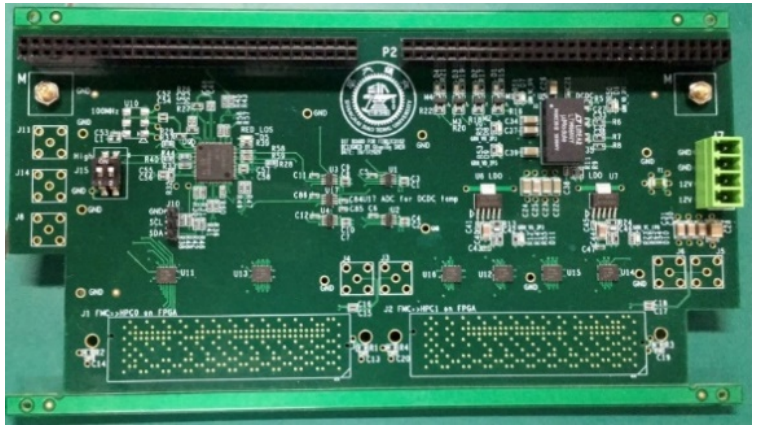
Block diagram of timing electronics prototype

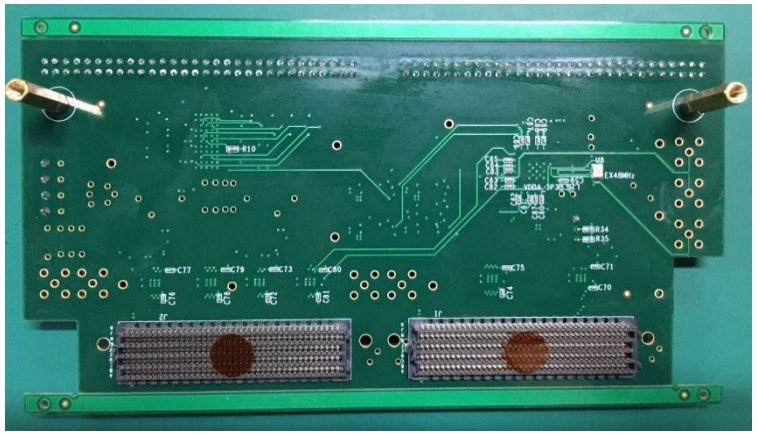
Hardware of Timing Electronics Prototype



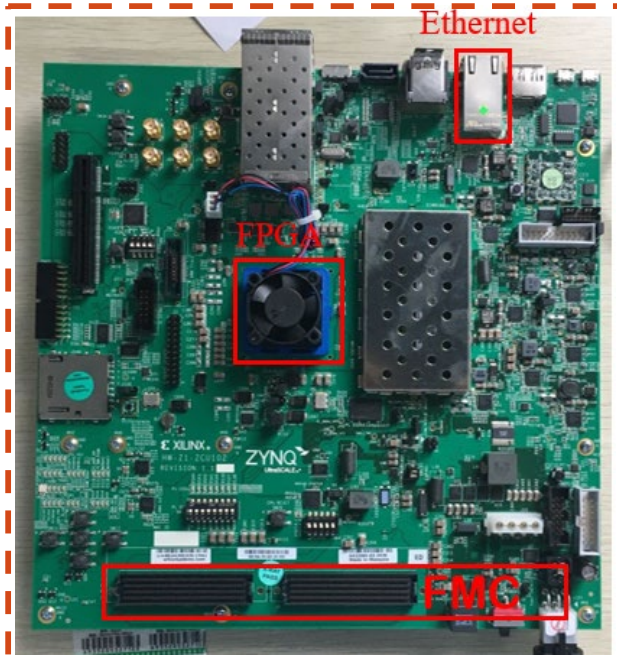
128 pads with the cell size 1cm × 1cm

FE Board





DIF Card

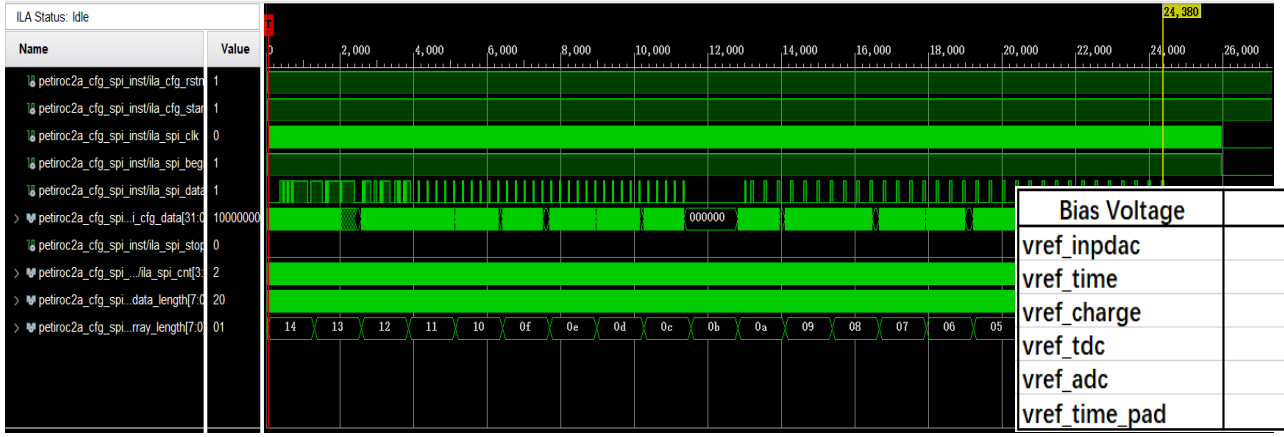


ZCU102

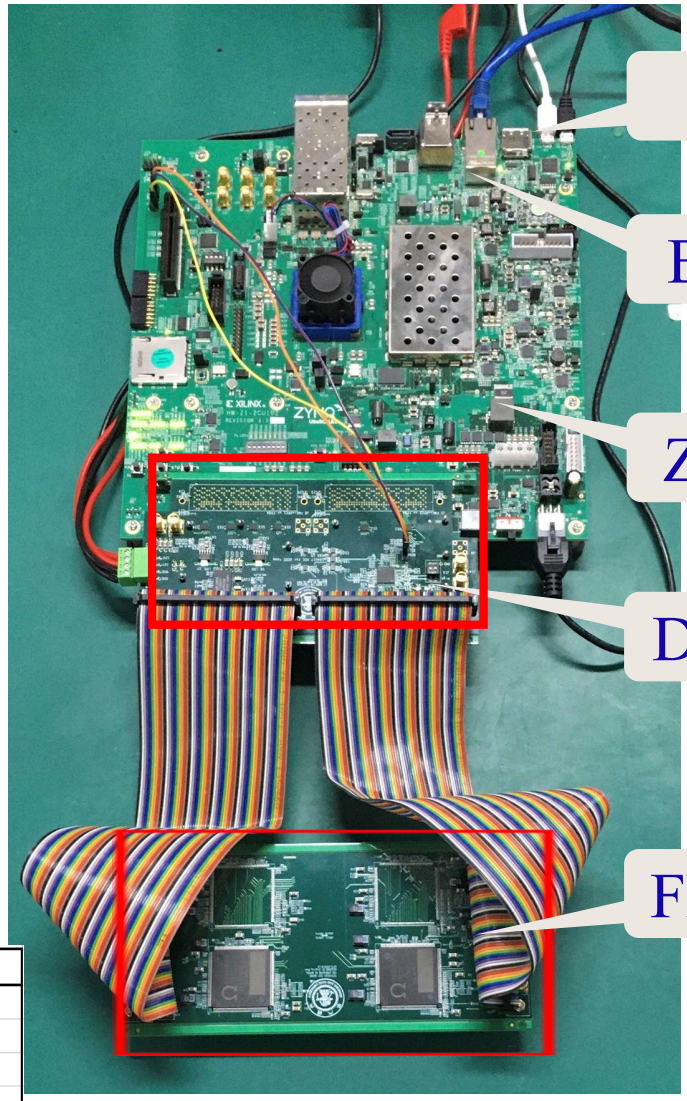
Status of System Test

- The test platform has been setup.
  - **FEB, DIF, DAQ** based on ZCU102

- PETIROC Configuration works well
  - All of bias voltage values are correct.
  - Output data has been checked, after sending trigger signals



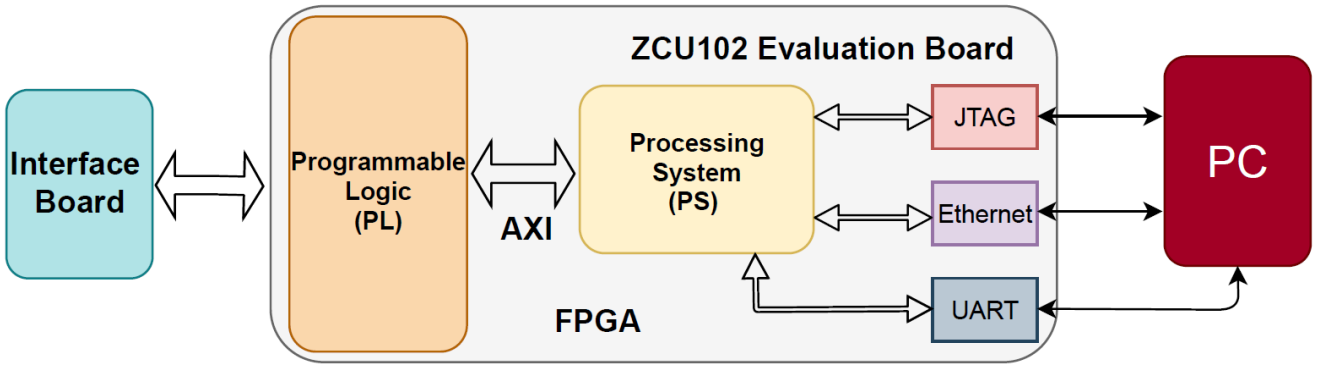
Bias Voltage	Value(V)
vref_inpdac	0.989
vref_time	1.664
vref_charge	0.976
vref_tdc	0.133
vref_adc	0.961
vref_time_pad	1.658



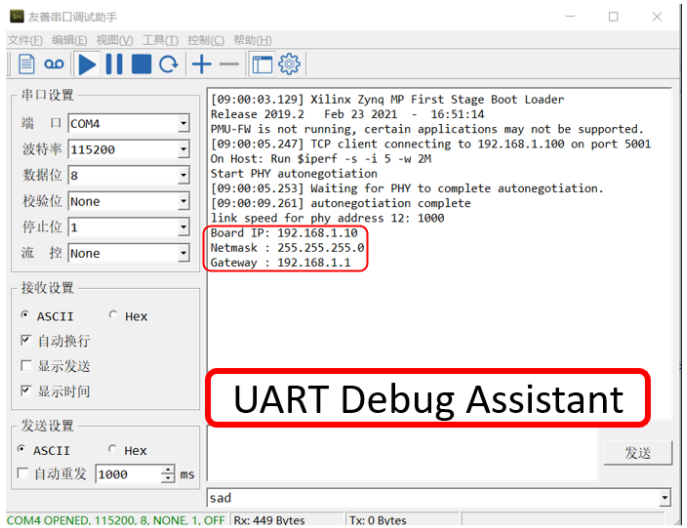
Test Platform

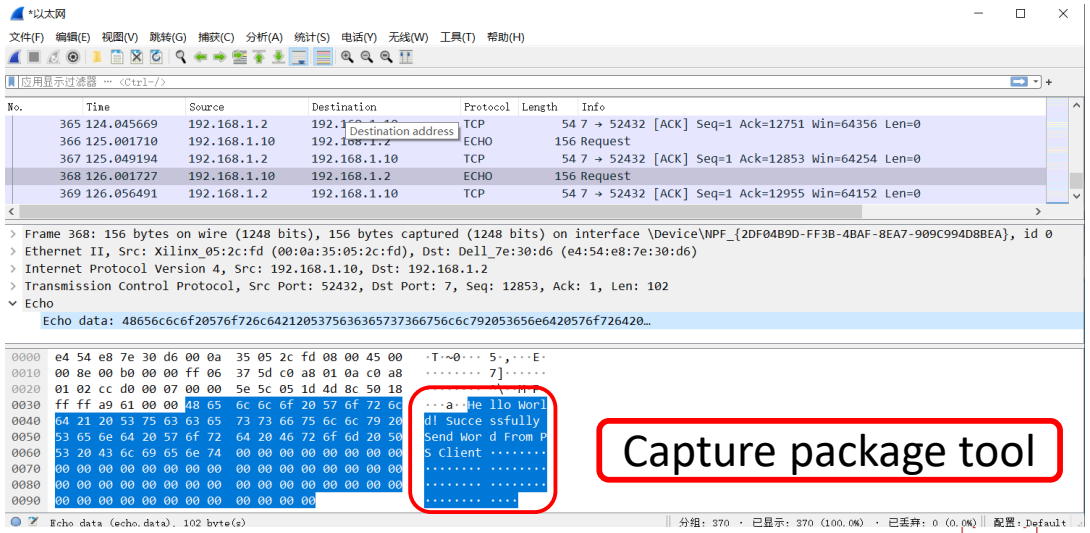
Status of System Test

- DAQ system is based on Xilinx ZCU102 that contains Processing System (PS) and Programmable Logic (PL).
- Embedded design (SDK) in ZCU102 (PS) is applied
  - UART communication works well
  - Ethernet communication works well



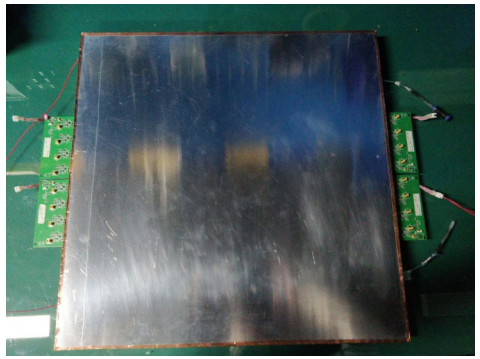
FPGA Logic Design Block Diagram

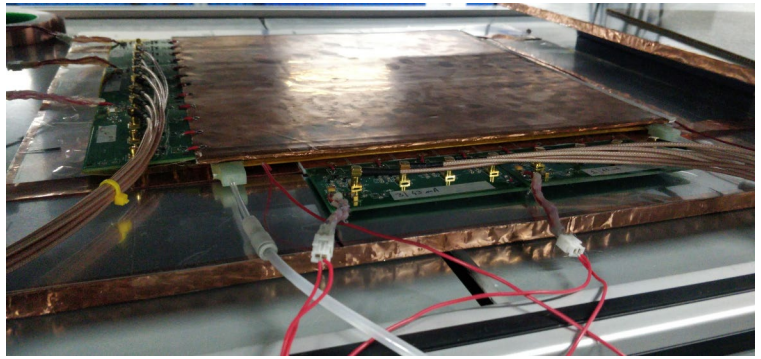




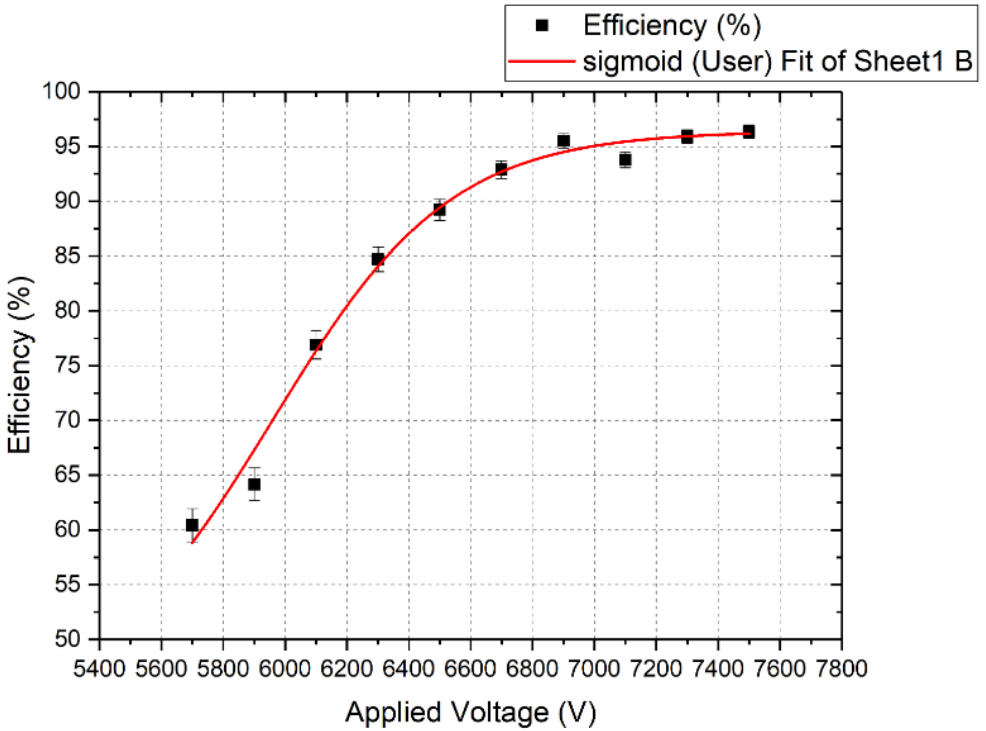
Progress of GRPC Construction

- SJTU group built 50cm x 35cm, 100cm x 100cm RPCs





We are now building 1m × 1m chambers.



Summary

AHCAL:

- The production and batch test of scintillators will be finished before summer.
- The SiPM test platform will be completed soon.
- HBU electronics can work now, the mechanics design has been started.
- Production of all 40 prototype layers will be finished this year.
- The prototype construction will start before the end of this year, and the cosmic and beam test are expected next year.

SDHCAL:

- The timing electronics including FEE and DIF, have been designed and manufactured.
- Test platform have been constructed.
  - PETIROC chips can be successfully configured.
  - Ethernet and UART communication have been completed.
- The DAQ system is still under development.

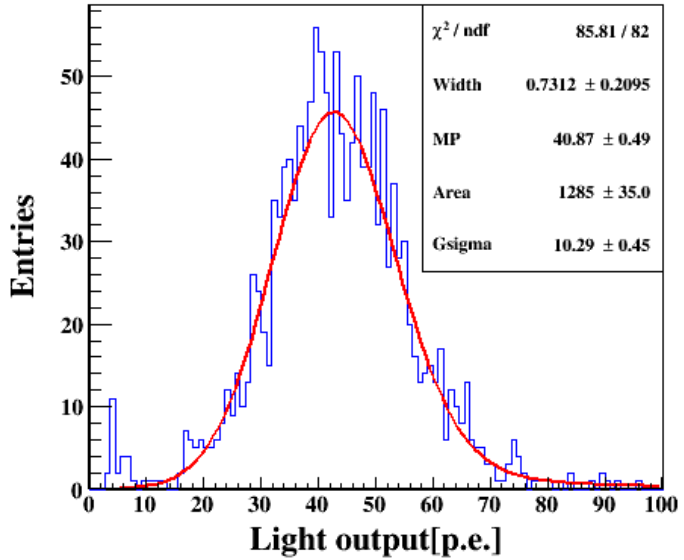
Thanks for your attention!

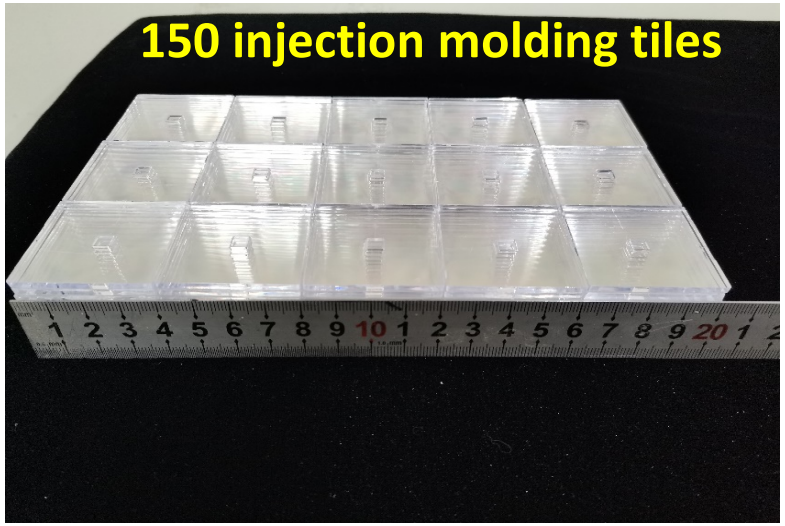
Backup Slides

Scintillator Production and Wrapping

- Massive production of scintillator tiles using the injection molding technique since November 2020 in GNKD
  - confirmation of craft: temperature, pressure, ratio of solute and solvent
  - Tiles of around 16,000 have been produced
- The light yield of one scintillator is about 40 p.e. test by NDL-22-1313-15S

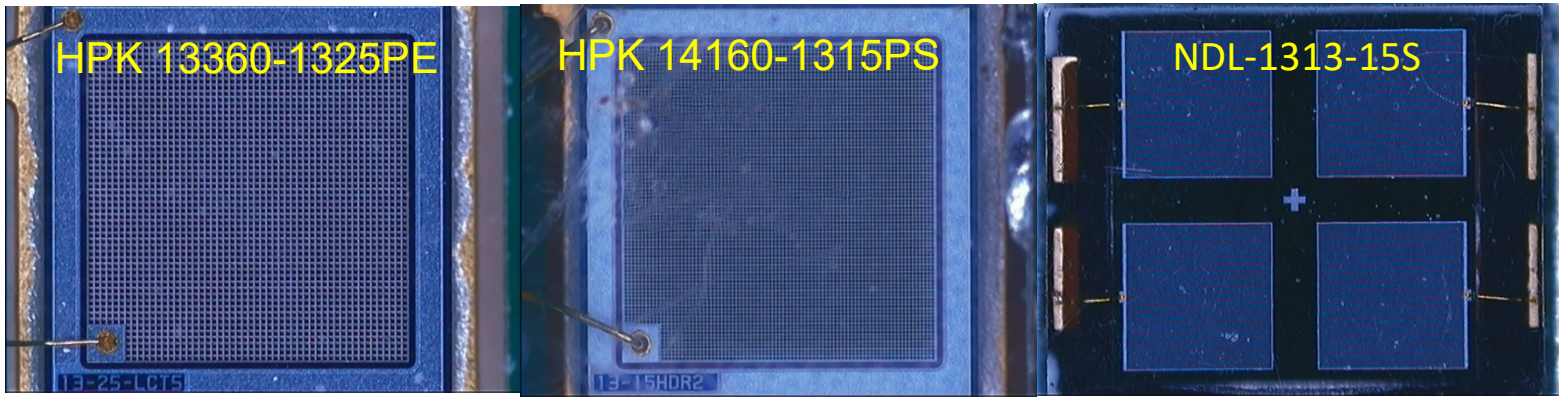
1	2	3	4	5	6	7	8	9	10	11	Total
1800	2880	1600	1180	1640	1640	1540	430	2160	890	410	16170





The SiPM comparison

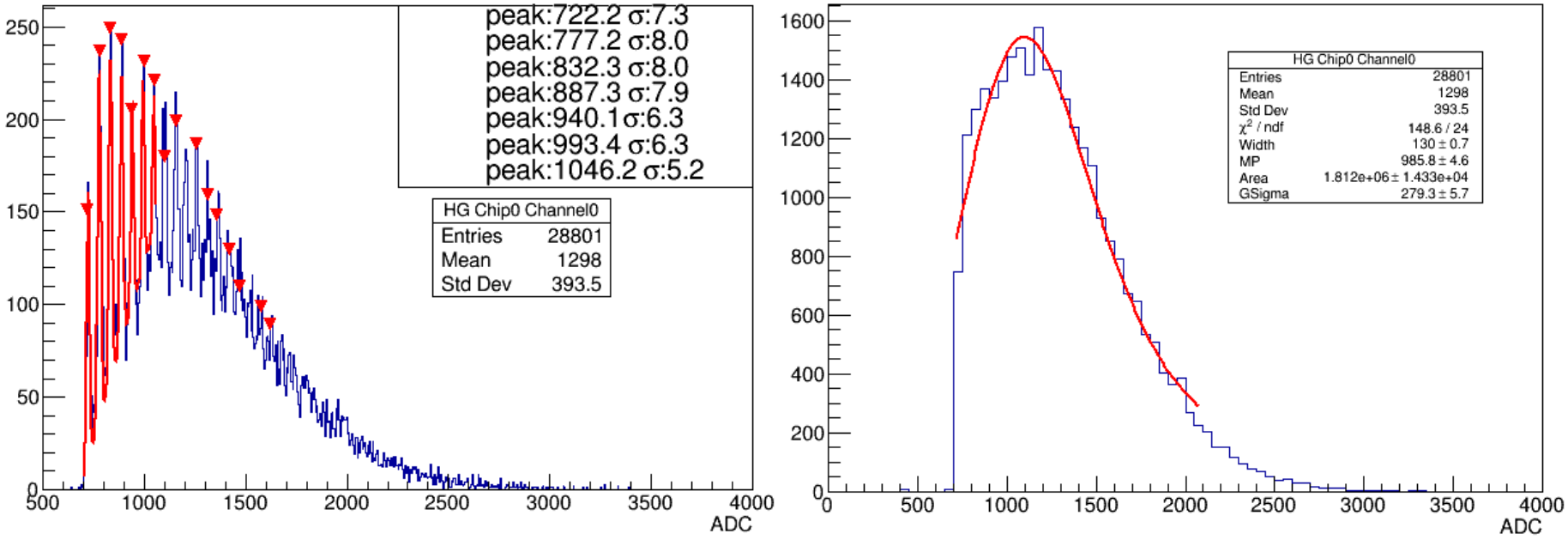
- NDL-SiPM:
  - High PDE, dark rate and crosstalk
  - Low breakdown
  - Low price
- HPK-SiPM
  - Low PDE,dark rate and crosstalk
  - High breakdown
  - Low price



Company	HPK		NDL
Type	13360-1325PE	14160-1315PS	22-1313-15S
Light output [p.e.]	13	17	40
Crosstalk[%]	1.59	1.17	4.4
Dark Counts [kHz]	120	290	550
Breakdown[V]	53	38	27.5

Batch test of scintillators

- MIP source : Sr 90
- The scintillator light is detected by the SiPM 13360-1325PE working at the 5V overvoltage
- The SiPM signal is read by the SPIROC2E chip



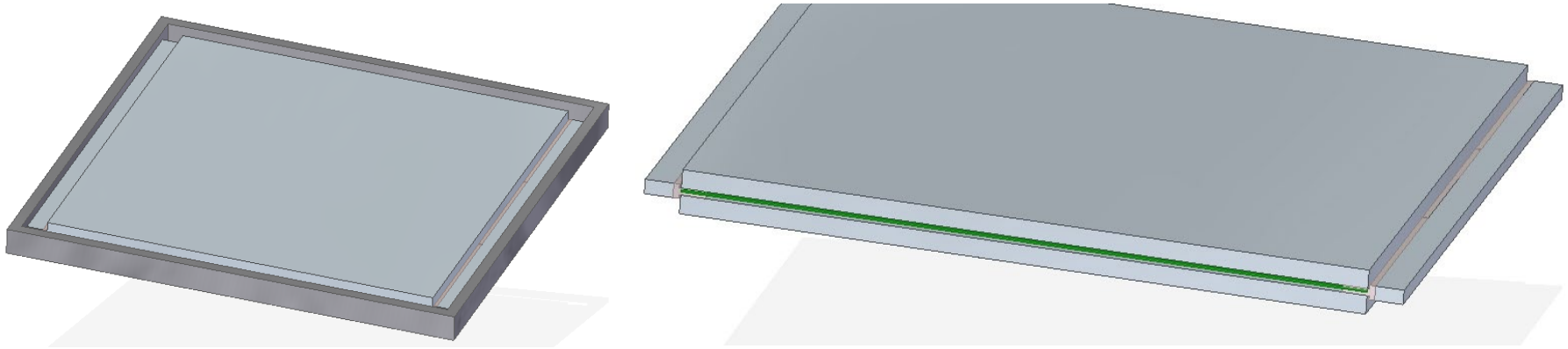
The MIP Spectrum

Introduction of PETIROC chip

- Time measurement with 10bits TDC interpolating 40MHz coarse time
- Charge measurement (Q>50fC) with 10bits DAC
- Voltage input amplifier, 200Ohm matching
- High bandwidth preamp (GBWP> 1.2 GHz)
- PETIROC parameters:
  - One chip with 32-channels and mixed analog/digital
  - The 32chs input connected with PAD (detector unit)
  - One channel split into two parts, respectively for charge and time measurement
  - Internal DAC for each channel to adjust the amplitude of the input signal
  - Lower power consumption (~6mW/channel)
  - Jitter ~18 ps RMS on trigger output (4 photoelectrons injected)

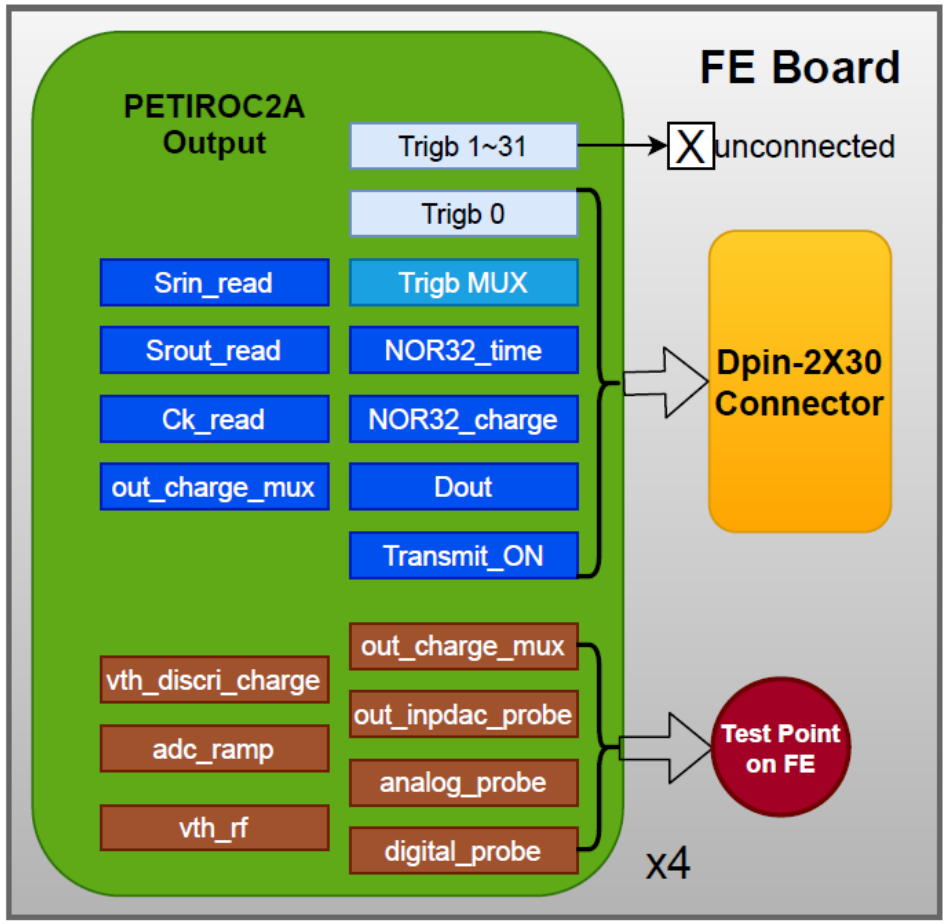
Development of HBU

- Challenge for HBU mechanics
  - The weight of 72 cm × 72 cm × 2cm steel board is 81.5KG
  - The connection between PCB boards
  - The warping of the PCB
- The concept design for AHCAL single layer structure
  - Use part of the absorber to make a box for PCB

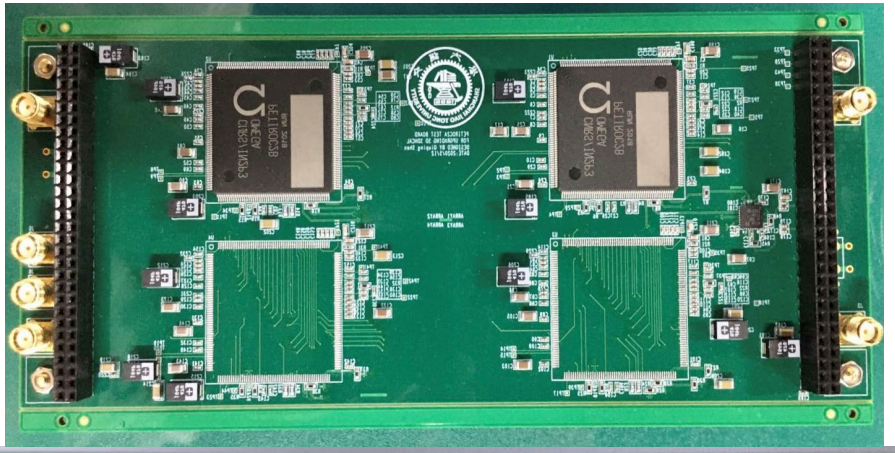


Sub-component Design and Testing

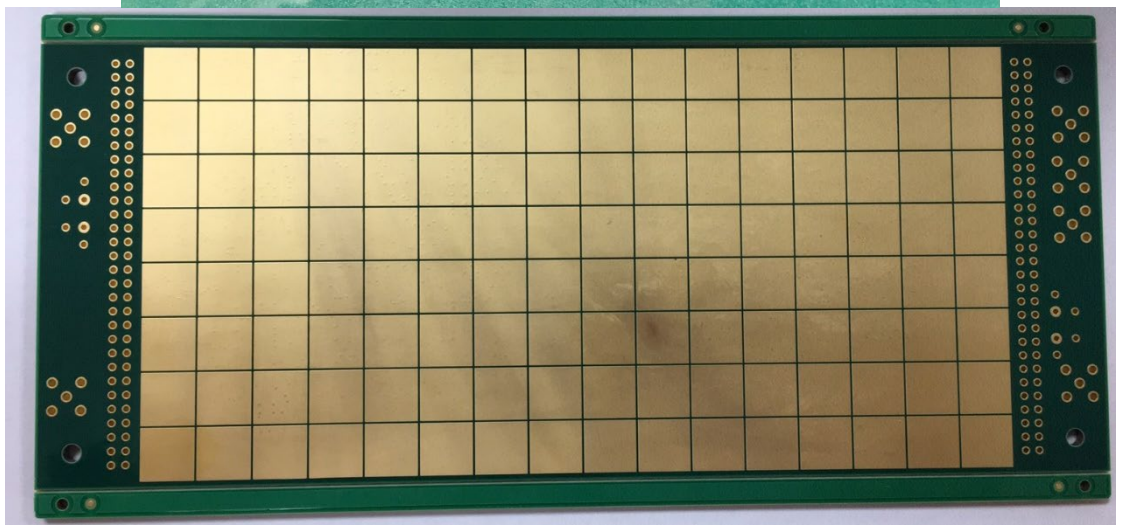
- Front-End readout Board Design with pads and four petiroc2b



Block diagram of front-end electronics



Front

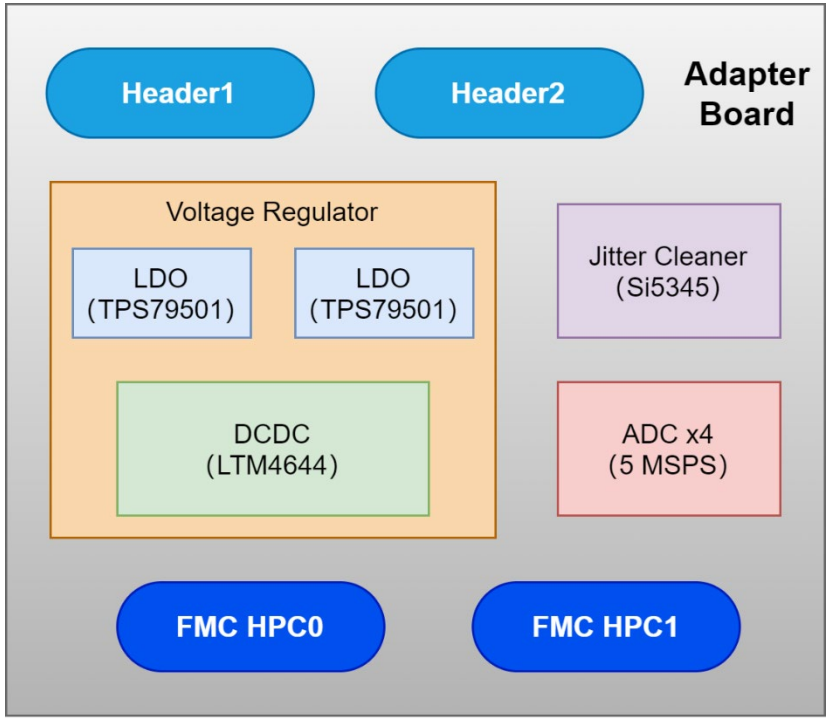


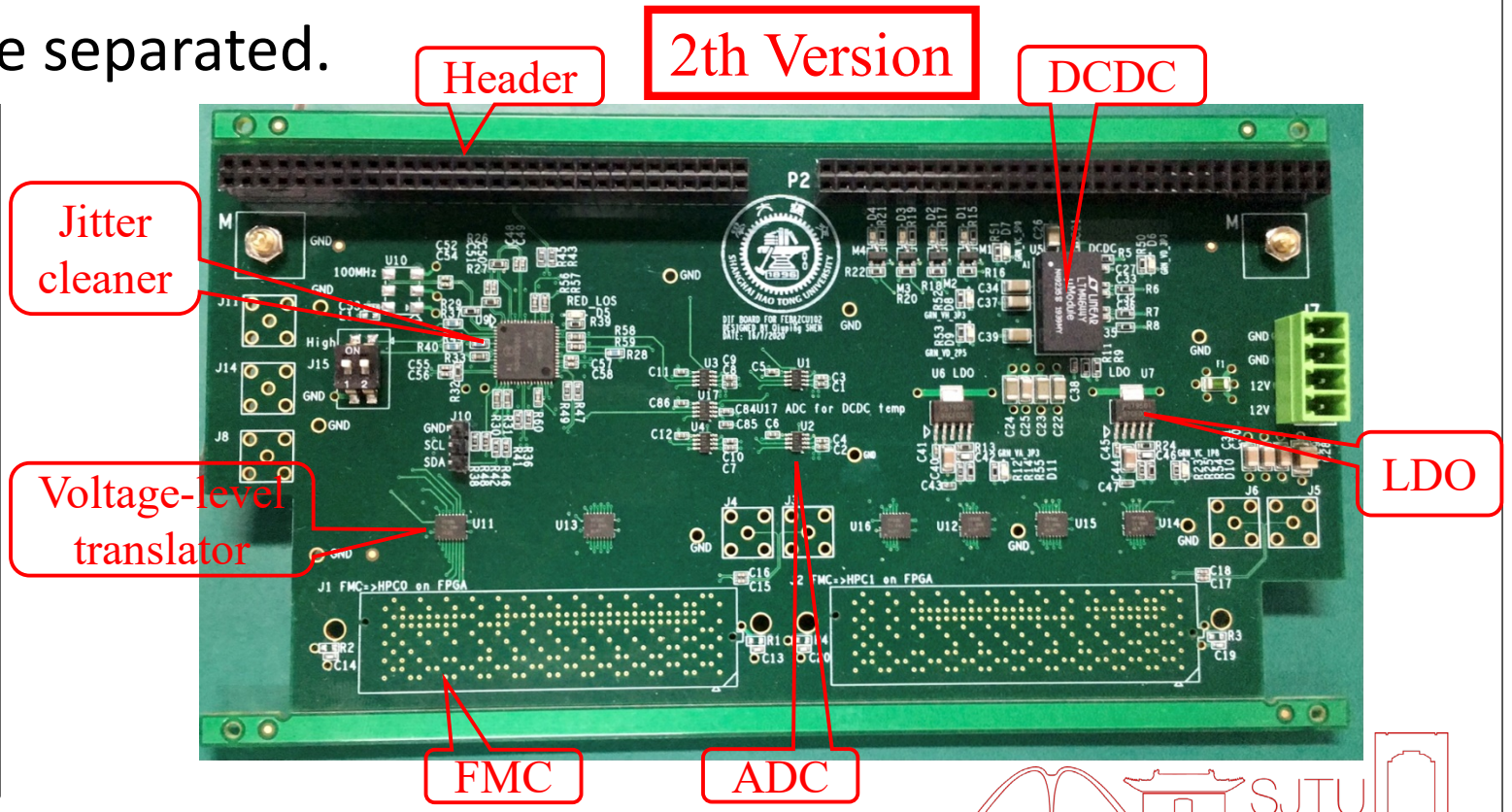
Back

Sub-component Design and Testing

- Detector Interface Card Design: mainly jitter cleaner and power system
- DIF card will be in charge of the communication and data transfer with the FE electronics(two headers) and ZCU102(two FMCs).
- Analog and digital power are separated.

More Details





Embedded design based on FPGA -- UART

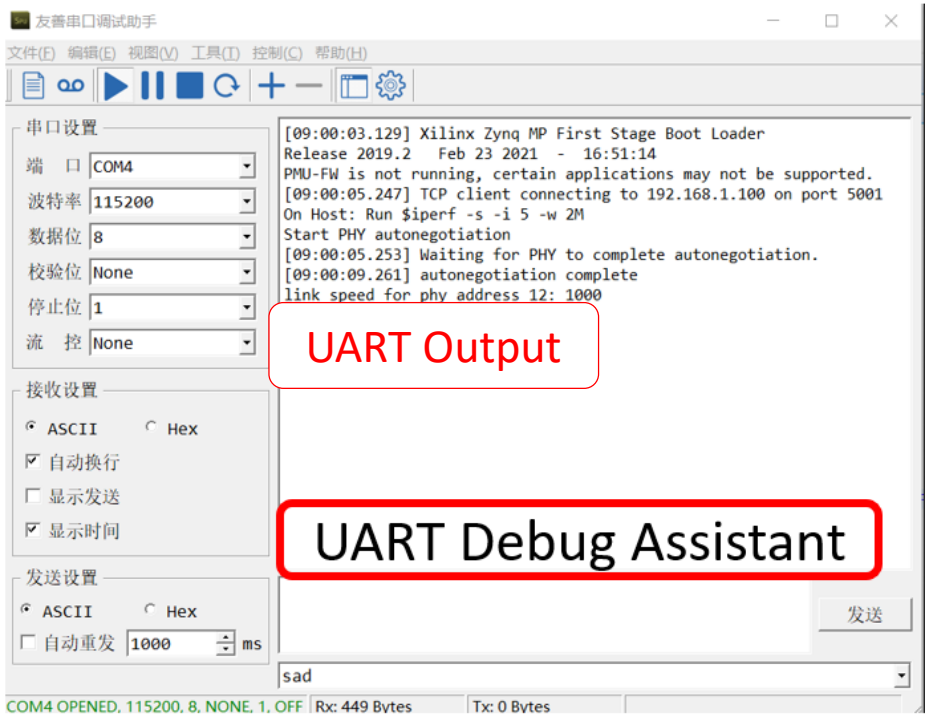
- The embedded design in ZCU102(PS side) mainly contains serial port communication(UART), ethernet communication(TCP/IP) and PETIROC configuration(Slow Control).

- UART test in PS side:
  - Hardware only needs Processing System part on ZCU102.
  - Write the C/C++ code and run on the hardware platform.
  - Information is printed on the tool window through UART port.

```c
#include <stdio.h>
#include <string.h>

#include "lwip/err.h"
#include "lwip/tcp.h"
#include "lwipopts.h"
#include "xil_cache.h"
#include "xil_printf.h"
#include "sleep.h"

#define TX_SIZE 102

static struct tcp_pcb*connected_pcb = NULL;
unsigned client_connected = 0;
//Static Global Function, blind for external file
uint tcp_trans_done = 0;

//u_char data[TX_SIZE] = {0, 1, 2, 3, 4, 5, 6, 7, 8, 9};
u_char data[TX_SIZE] = "Hello World! Successfully Send Word From PS Client";

int send_data()
{
    err_t err;
    struct tcp_pcb *tpcb = connected_pcb;

    if (!tpcb)
        return -1;

    //判断发送数据长度是否小于发送缓冲区剩余可用长度
    if (TX_SIZE < tcp_sndbuf(tpcb)) {
        //Write data for sending (but does not send it immediately).
        err = tcp_write(tpcb, data, TX_SIZE, 1);
        if (err != ERR_OK) {
            xil_printf("txperf: Error on tcp_write: %d\r\n", err);
            connected_pcb = NULL;
            return -1;
        }

        //Find out what we can send and send it
        err = tcp_output(tpcb);
        if (err != ERR_OK) {
            xil_printf("txperf: Error on tcp_output: %d\r\n",err);
            return -1;
        }
```

PS code

1



UART Output

UART Debug Assistant

UART communication test