Status update on the CMOS pixel sensor JadePix3

Yunpeng Lu

On behalf of the JadePix3 study group

2021/4/7

Timeline of status reports

2021.4

- This talk and the next talk by Jing Dong
  - Test results of JadePix3
  - Test results of CPV3

2020.12

- Application of SOI-3D in the Vertex detector, Yunpeng Lu, CEPC Day on December 28, 2020
  - Design of CPV4, first version of SOI-3D for the CEPC

2020.6

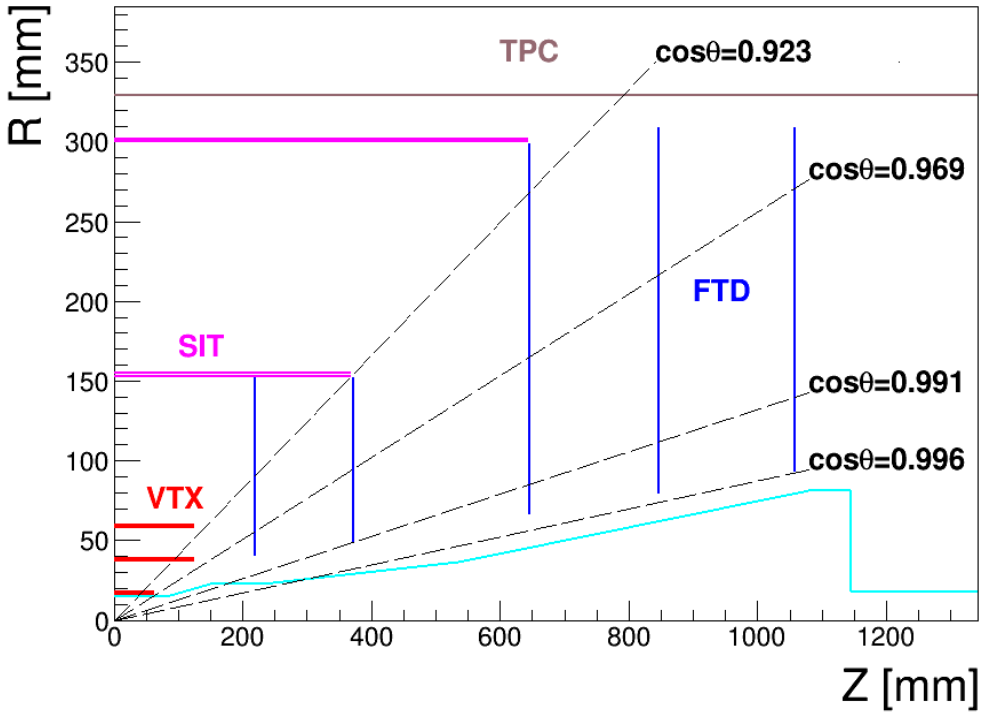
- Update on CMOS/MOST1 and SOI pixel R&D, Qun Ouyang, CEPC Day on June 15, 2020
  - Update on JadePix3 and CPV3
  - Perspective for the next 5 years

Outline

- Motivation
  - Baseline scheme for the Vertex Detector
- Revisit the JadePix3 design
- Update on the Test results
  - General overview
  - Highlights of performance study
- Summary

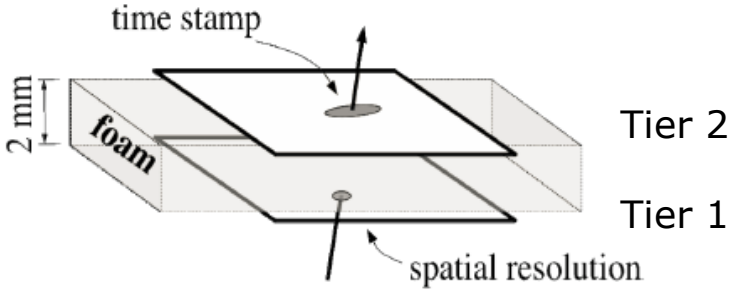
CEPC vertex detector : conceptual design

Silicon tracking system



- SIT: Silicon Internal Tracker
- FTD: Forward Tracking Detector
- SET: Silicon External Tracker
- ETD: End-cap Tracking Detector

- VTX:
  - 3 layers of double-sided pixels
  - σ_{SP} = **2.8 μm** in L1
  - Total number of pixels: 690M



Concept of double-sided structure

Baseline design parameters

	R(mm)	| Z |(mm)	$\sigma(\mu m)$	material budget
Tier 1	16	62.5	2.8	0.15%/X_0
Tier 2	18	62.5	6	0.15%/X_0
Tier 3	37	125.0	4	0.15%/X_0
Tier 4	39	125.0	4	0.15%/X_0
Tier 5	58	125.0	4	0.15%/X_0
Tier 6	60	125.0	4	0.15%/X_0

Complementary design of pixel sensor

- Tier 1: high resolution, low power and modest readout speed
  - JadePix3 targeting on: **3~5 μm**, 50~100 mW/cm^2, 100 μs
- Tier 2: Fast readout speed, low power and relaxed constraint of resolution
  - **1 μs**, 50 mW/cm^2, 4~6 μm is foreseen
- Radiation tolerance is common requirement to Tier 1 and 2

Impact parameter resolution

$$\sigma_{r\phi} = 5\mu m \oplus \frac{10}{p(GeV)\sin^{3/2}\theta}\mu m$$

Vertex detector specs

$\sigma_{s.p.}$ ~ 2.8um

Material budget ~ 0.15% X_0/layer

r of Inner most layer ~ 16mm

Pixel sensor specs

Tier 1

Small pixel ~ 16um

Thinning to ~ 50um

low power ~ 50mW/cm^2

fast readout ~ 1us

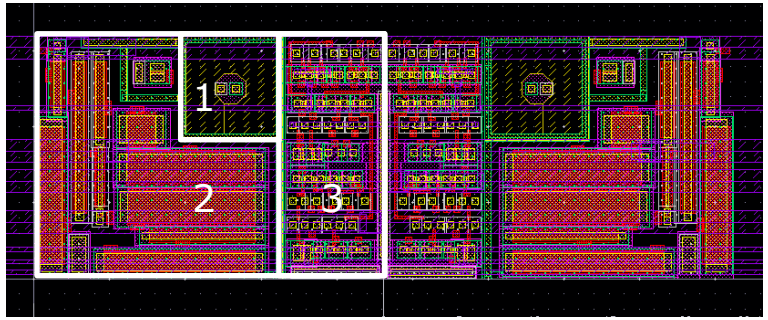
Tier 2

radiation tolerance ~

$\leq 3.4\ Mrad/year$

$\leq 6.2\times10^{12} n_{eq}/(cm^2\ year)$

Small pixel design in the JadePix3

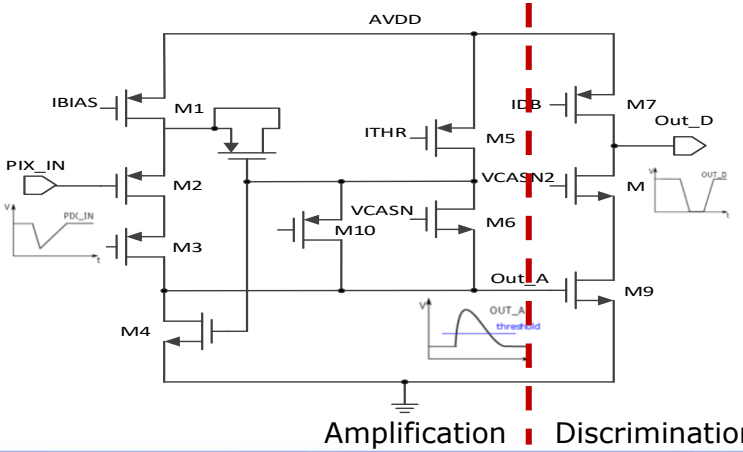


Minimal pixel footprint: **16 μm* 23.11 μm**
1: Sensing diode
2: Analog frontend
3: digital frontend

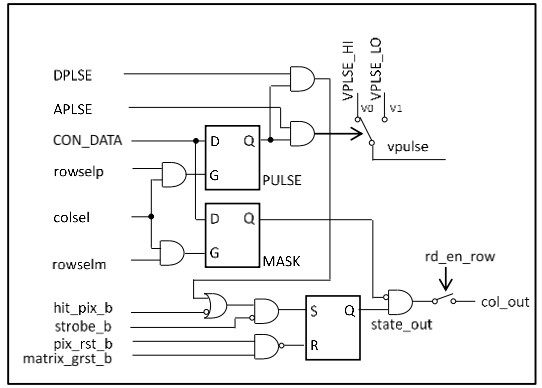
- Small footprint design
  - Sensing diode of minimized geometry verified on JadePix1
  - Frontend with **tradeoff** between layout area and FPN
- Fix φ direction* to **16 μm** and allow the z* to vary
  - Different configuration bits
  - D-FlipFlop vs RS-latch
- Mirrored layout to share bias lines between two columns

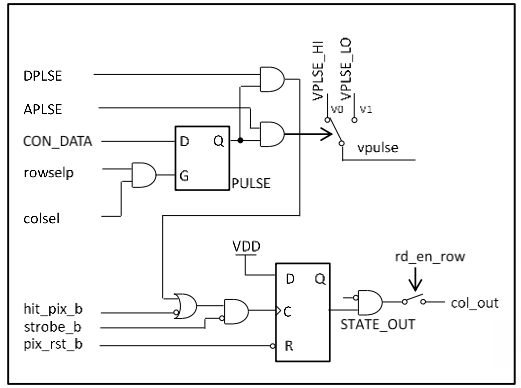
* Detector coordinates in page 4

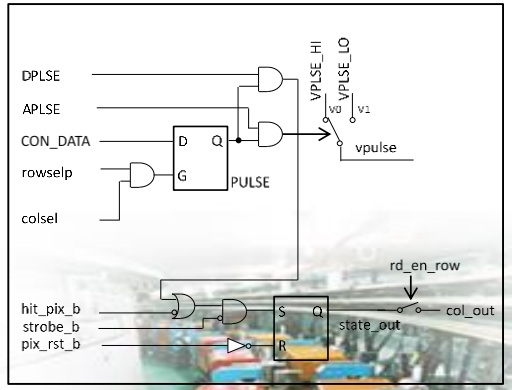
analog frontend



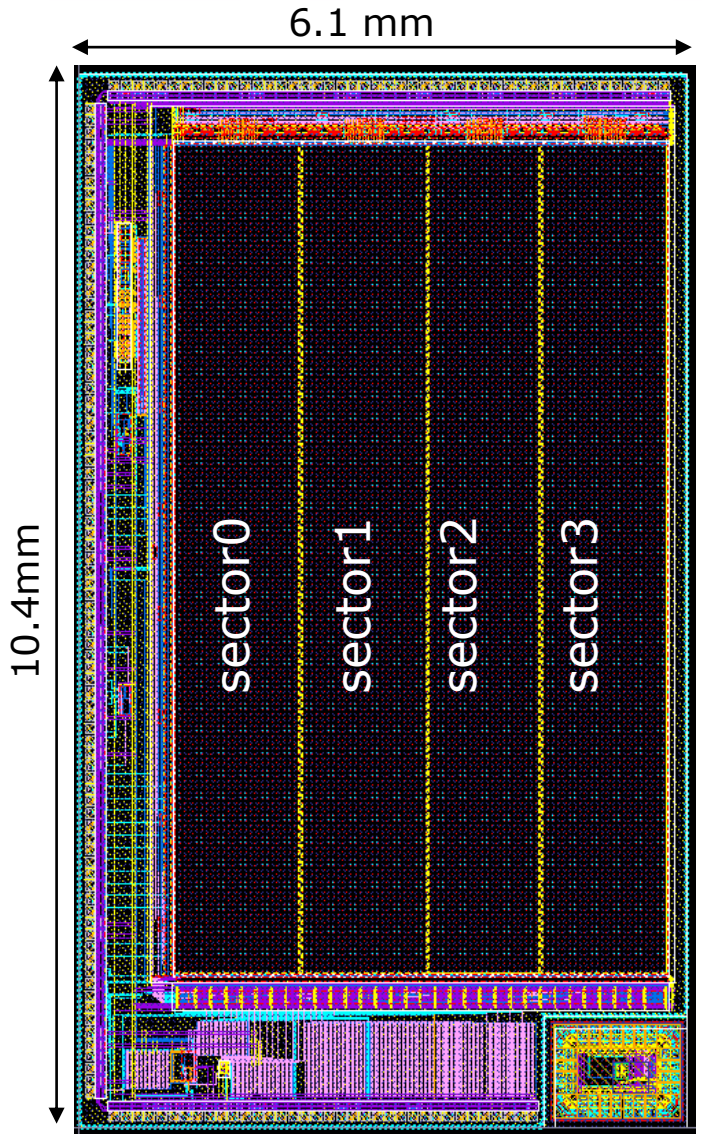
3 variants of digital frontend







Readout of the Matrix

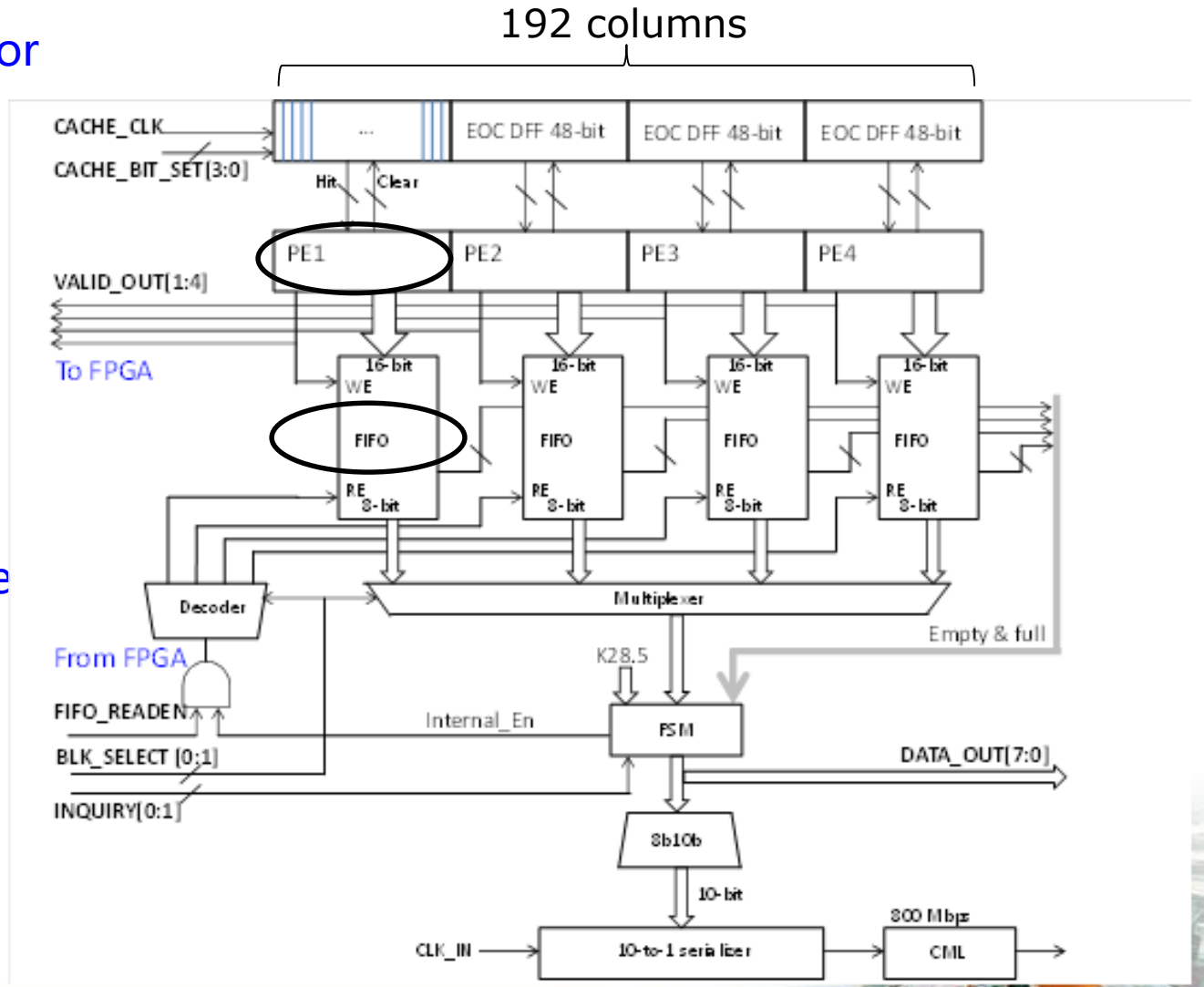


- **Rolling shutter** to avoid heavy logic and routing in the column-wise
  - Shrink the pixel size by ~ 7 μm
- **Full-sized** in the φ direction
  - Matrix coverage: 16 μm * 512 rows = 8.2 mm
  - Matrix readout time: 192ns/row * 512 rows = **98.3 μs/frame**
- **Extensible** in the z direction
  - 48 columns * 4 sectors

Sector	Diode	Analog	Digital	Pixel layout
0	2 + 2 μm	FE_V0	DGT_V0	16×26 μm²
1	2 + 2 μm	FE_V0	DGT_V1	16× 26 μm²
2	**2 + 2 μm**	**FE_V0**	**DGT_V2**	**16× 23.11 μm²**
3	2 + 2 μm	FE_V1	DGT_V0	16×26 μm²

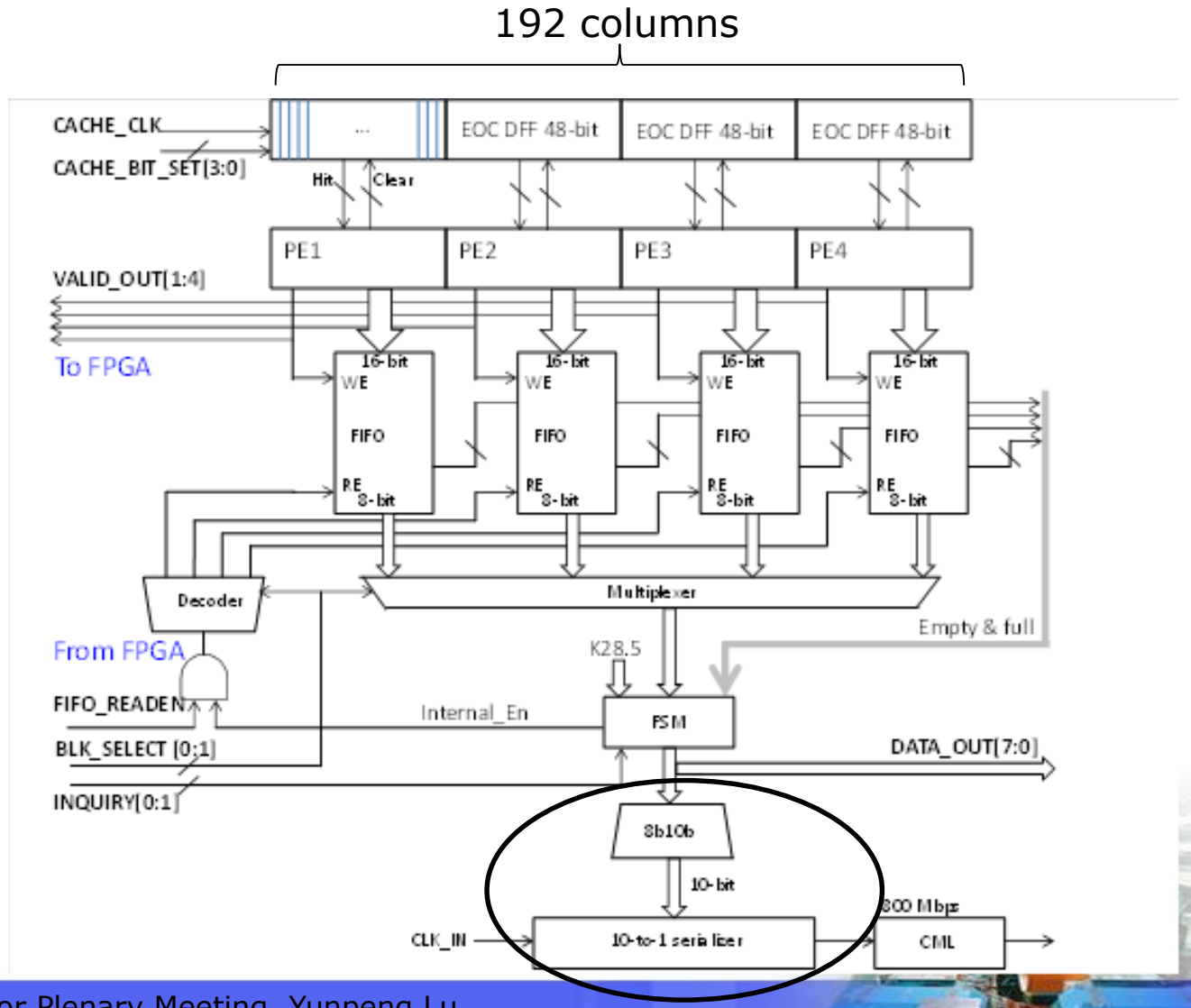
Lower power design in the JadePix3

- A low power frontend of **20 nA static current**, equivalent to 9 mW/cm^2
  - Except for the sector 4, where 60 nA used for the comparison of radiation tolerance
- Zero suppression at the end of column
  - **Priority Encoded (PE) address** of HIT pixel
- Data buffering
  - 4 parallel FIFOs * 48 depth
  - Multiplexed output @ 80MHz
  - Readout strategy can be tested to allow the **optimization of FIFO depth**
- Extensible along with the matrix sectors



Engineering consideration in the JadePix3

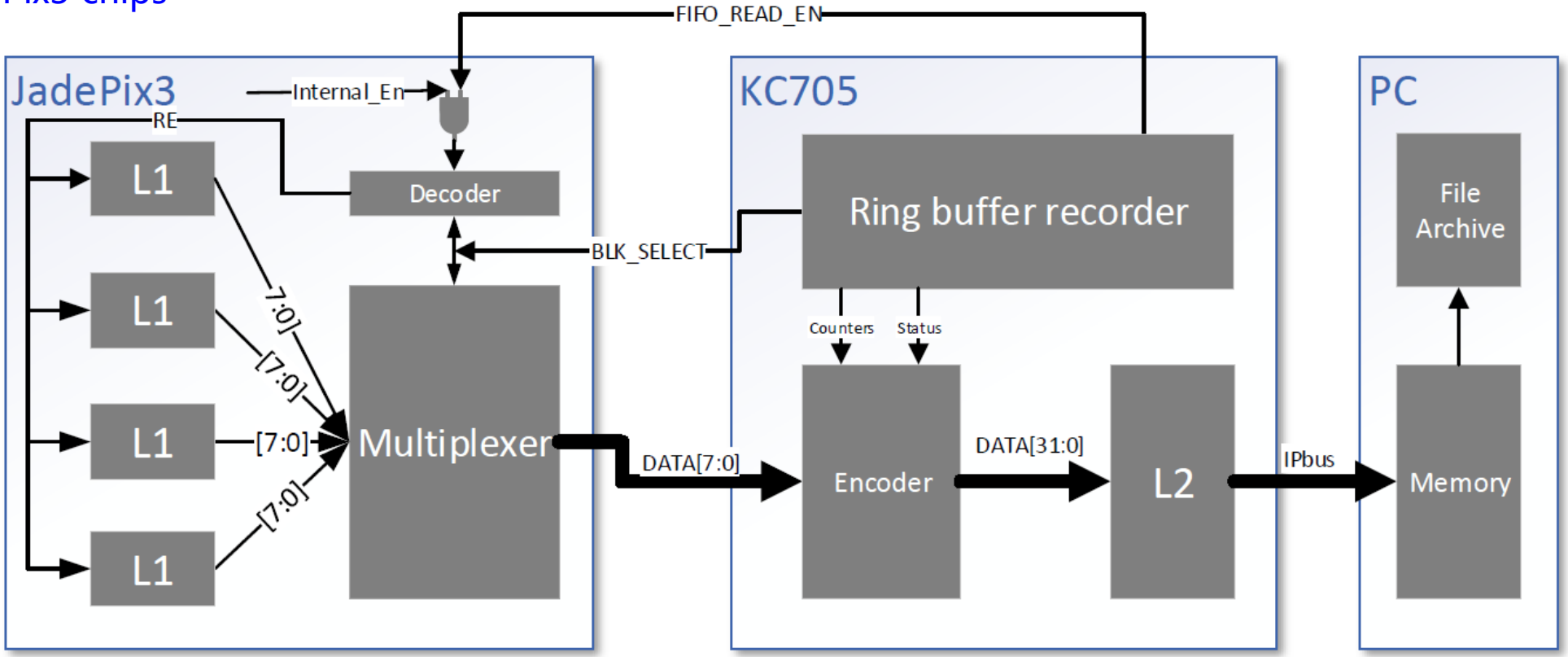
- High speed data transmission modules
  - 8b10b **Encoder**
  - 10-to-1 **Serializer**
  - **PLL**-based clock solution
- **DACs** for the analog biasing
  - 10-bit voltage DAC * 6 channels
  - 8-bit current DAC * 6 channels
- Adjustable **Bandgap** module
- Serial Program Interface (**SPI**)
- Reduced Swing Differential Signal (**RSDS**)
  - Low power differential transceiver



Test system

Sheng DONG, Hulin WANG, Yunpeng LU

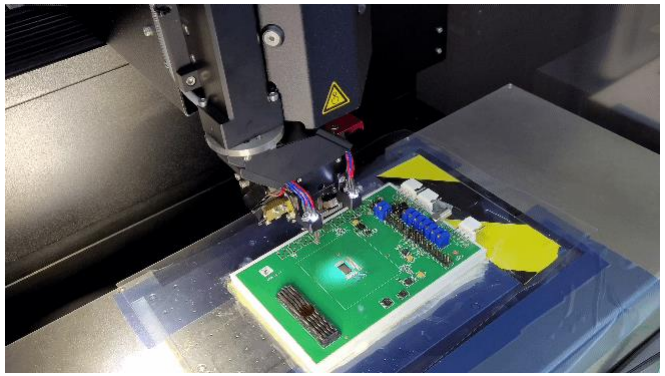
- General-purpose FPGA platform, KC705
  - Well-defined **FPGA firmware**
- Two test setup in IHEP and CCNU
  - Extensively debugged with the **interactive** JadePix3 chips
- IPBUS protocol
  - Reliable high-performance **control link** for particle physics electronics
  - **JUMBO PACKAGE feature** developed and added to the new release



Chip-board assembly

Daming SUN, Yunpeng LU

- 7 boards assembled with the Jadepix3 chips
  - Two chips confirmed broken and replaced
  - **All passed functional tests**
  - Counter measure of ESD proved effective
- Good **uniformity** observed on the assembled chips
  - Power supply current
  - Bandgap output
  - Analog waveform of frontend
  - Threshold and noise



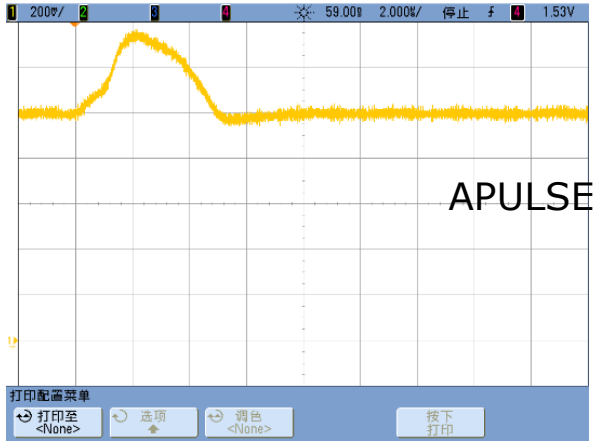
Wire bonding on the JadePix3 chip

Functional verification

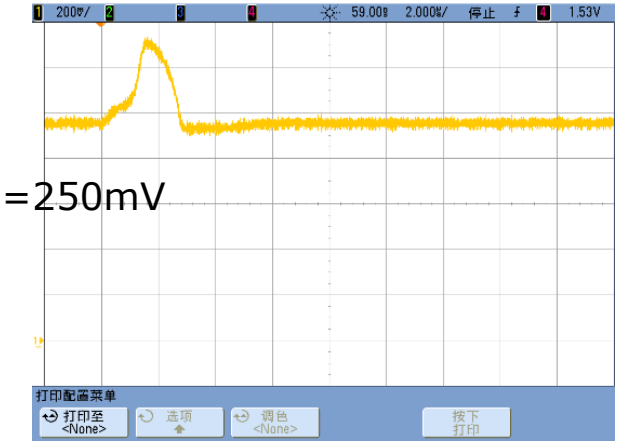
Sheng DONG, Yang ZHOU, Ying ZHANG, Zhan SHI, Yunpeng LU

- **All module** functions verified
  - Configuration of matrix registers
  - Configuration of DAC
  - Pulse test
  - Analog output waveform
  - Data readout
  - PLL clock
  - Serializer output pattern
- Response to the radiation as expected
  - Radiative source ^{55}Fe
  - Cosmic ray
  - **Pulsed laser beam**

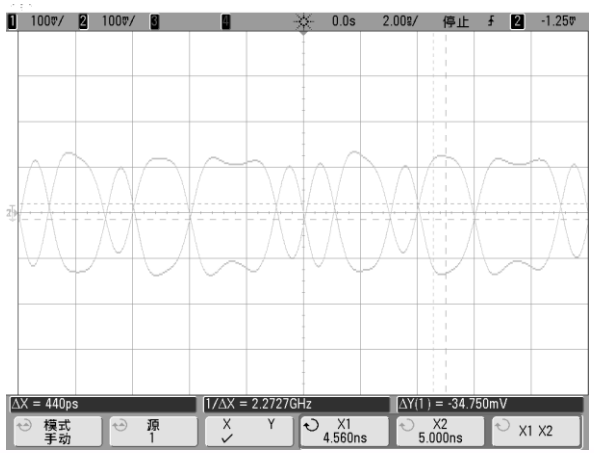
Low power frontend



Radiation-enhanced frontend



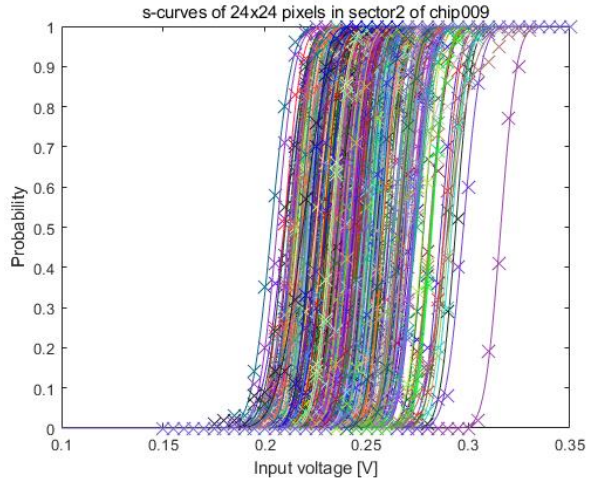
Output pattern of serializer @ 1Gbps

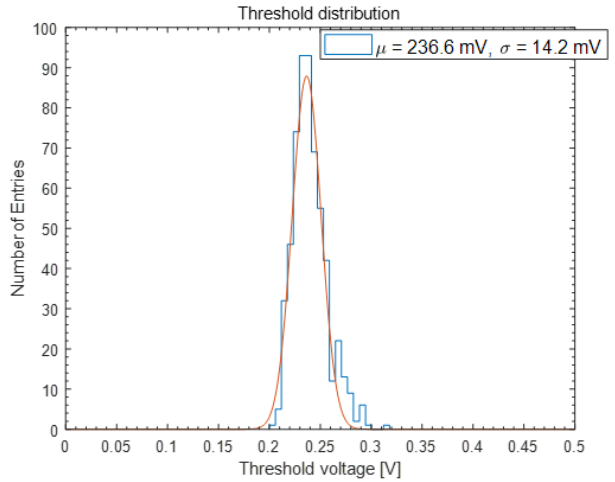


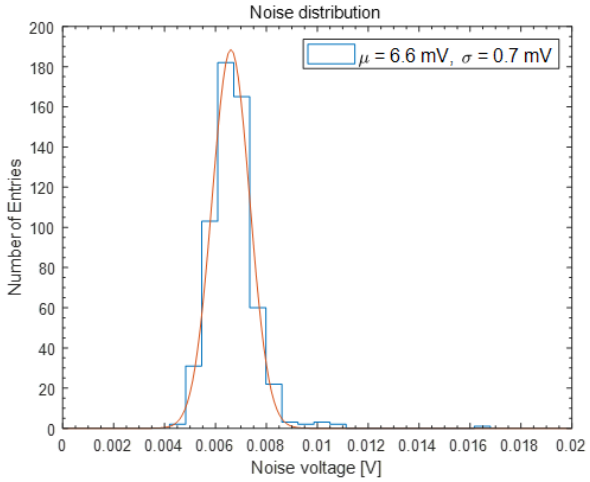
Threshold and Noise

Ying ZHANG, Yang ZHOU, Jing DONG, Yunpeng LU

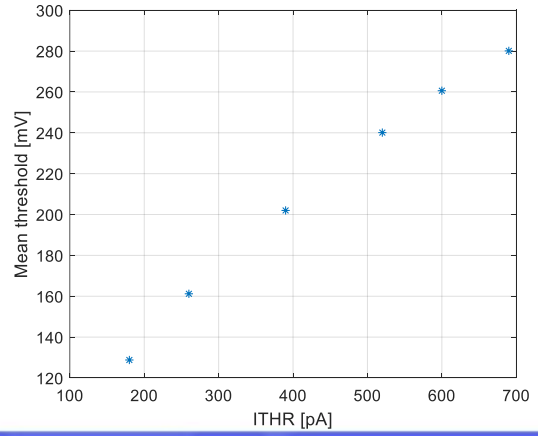
- Pulse amplitude scan and **S-curve** fit (1 mV ~ 0.9 e$^-$)

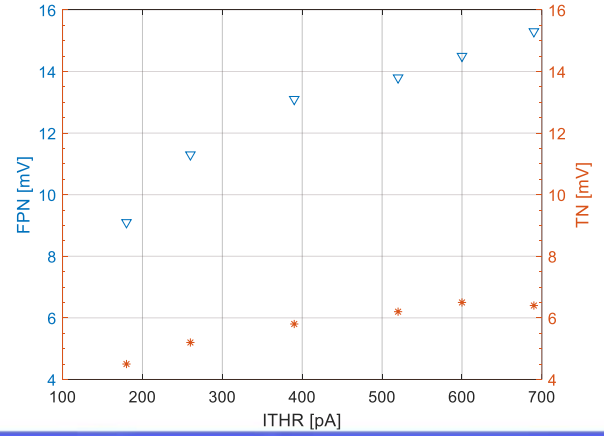


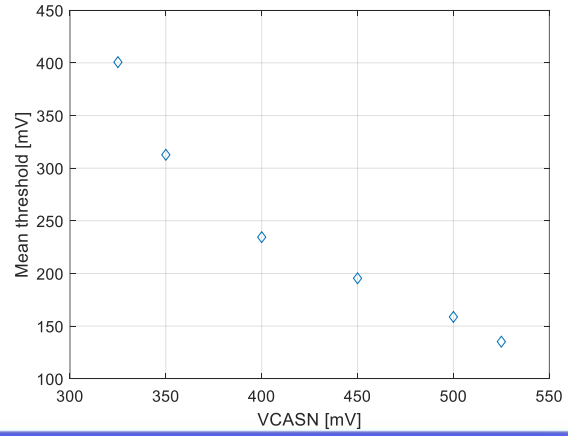


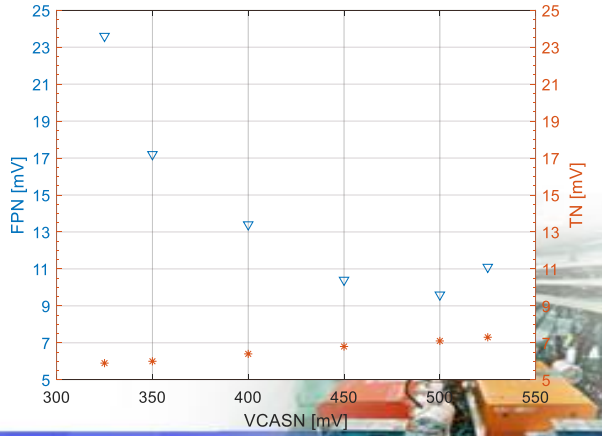


- Characterized with varing Ithr and Vthr
  - Optimized parameters: Ithr = 0.5 nA, Vthr= 400 mV



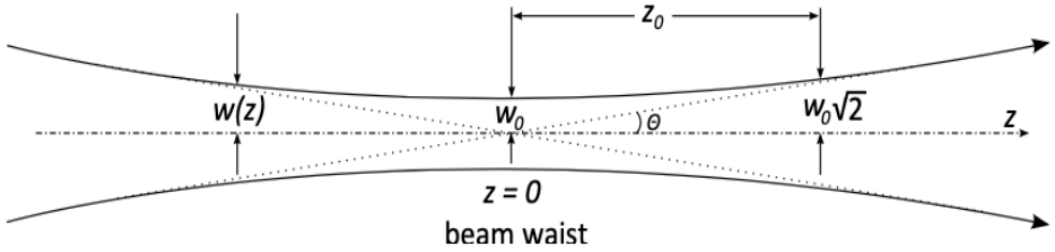


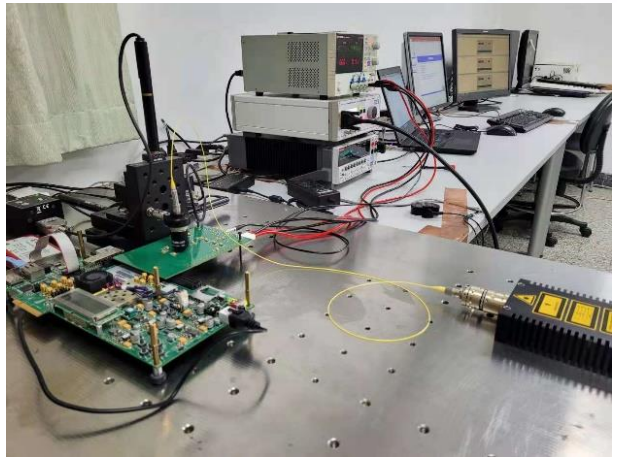




Pulsed laser test

Hulin WANG, Shen DONG, Yunpeng LU





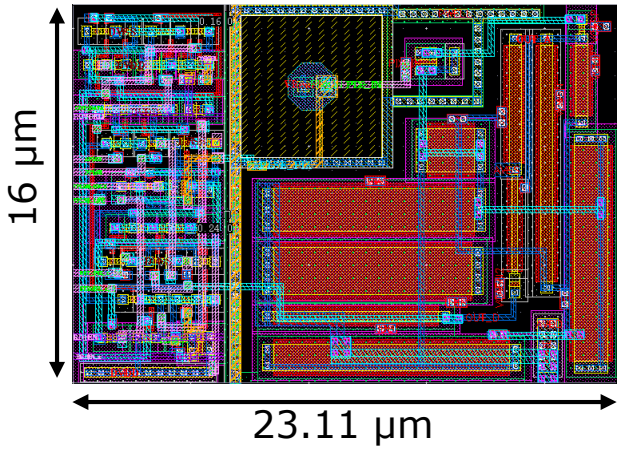
- Laser beam characterization
  - Wavelength: 1064 nm
  - Beam waist ω_0 ~ **1.7 μm**
  - Rayleigh range z_0 ~ 8.5 μm
  - Divergence Angle **θ = ~ 11°**
  - Laser pulse duration ~100 ps
- Laser power tune
  - 0% : maximum power; 100% : minimum power
  - For final results, use 92.7%, 92.9%, 93.3%, 93.5%, 93.7%
  - 92.7% ~ **4 × threshold** (threshold set to ~220 e-)
  - 93.7% ~ **2 × threshold**

Single point resolution

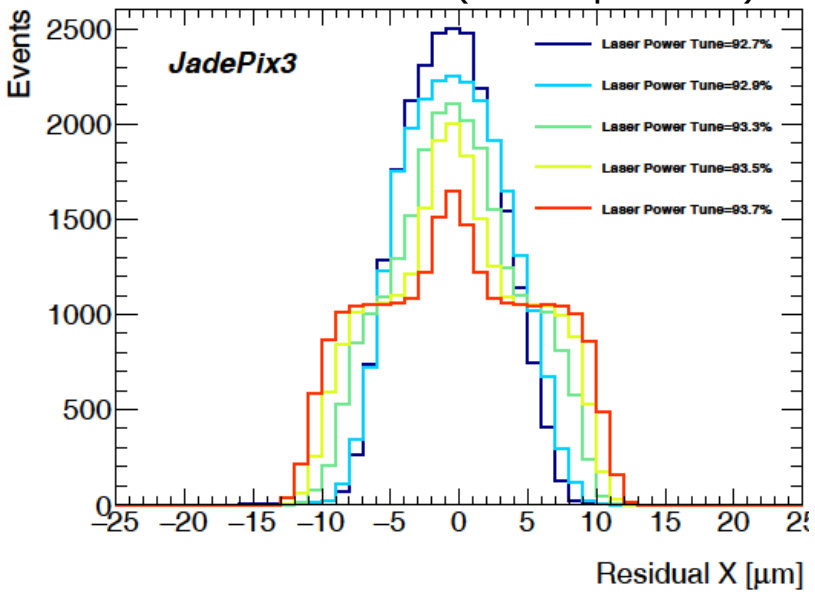
Hulin WANG, Shen DONG, Yunpeng LU

- Laser beam used to simulate the track of charged particle
  - A useful tool to reveal the **localized behavior** of single pixel
- **Theoretical minimum value** can be approached on both sides
  - 3.34 μm and 2.31 μm respectively
- Charged particle beam is required for a **realistic** measurement
  - Expected in between the Maximum and Minimum of laser results

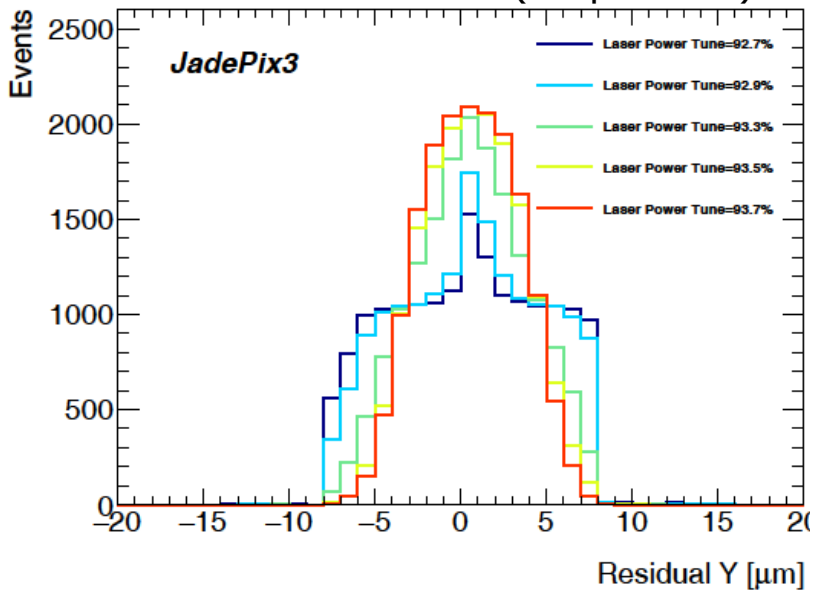
Layout of pixel undertest



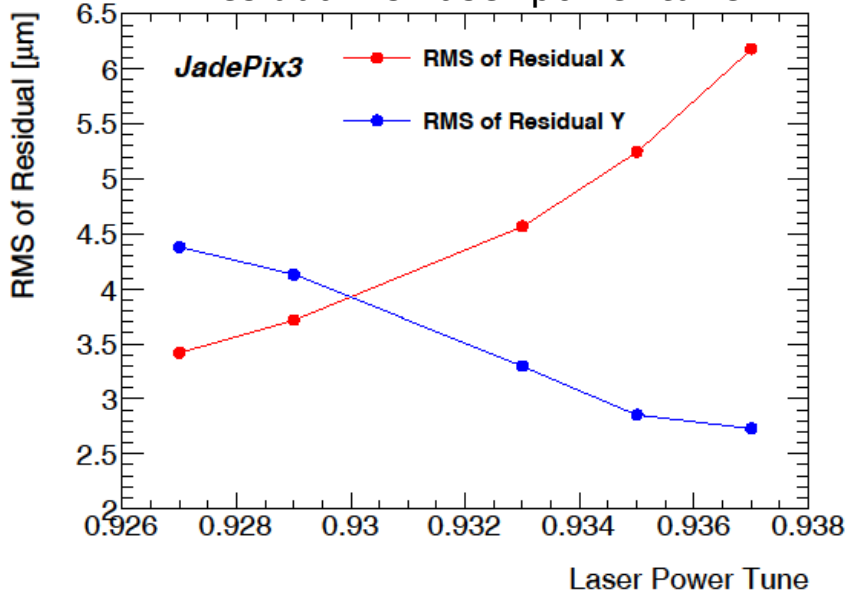
Residual in X (23.11 μm side)



Residual in Y (16 μm side)



Residual vs Laser power tune



Power consumption

Ying ZHANG, Zhan SHI, Yunpeng LU

- Average power consumption
  - (62.44-14.38-31.54 mA)*1.8V/(1.04*0.61 cm^2)=**46.9 mW/cm^2**
  - PLL and Serializer not included
- Extrapolated to a full size chip of **1 cm*2.56 cm**
  - Sensitive area 0.819 cm*2.56 cm
  - PLL and Serializer included
  - Average power **91.44 mW/cm^2**
- **Test-specific** function > 15 mA
  - Analog buffer (1.8mA)
  - LVDS receiver (1.74mA)
  - PLL test output (11.5mA)

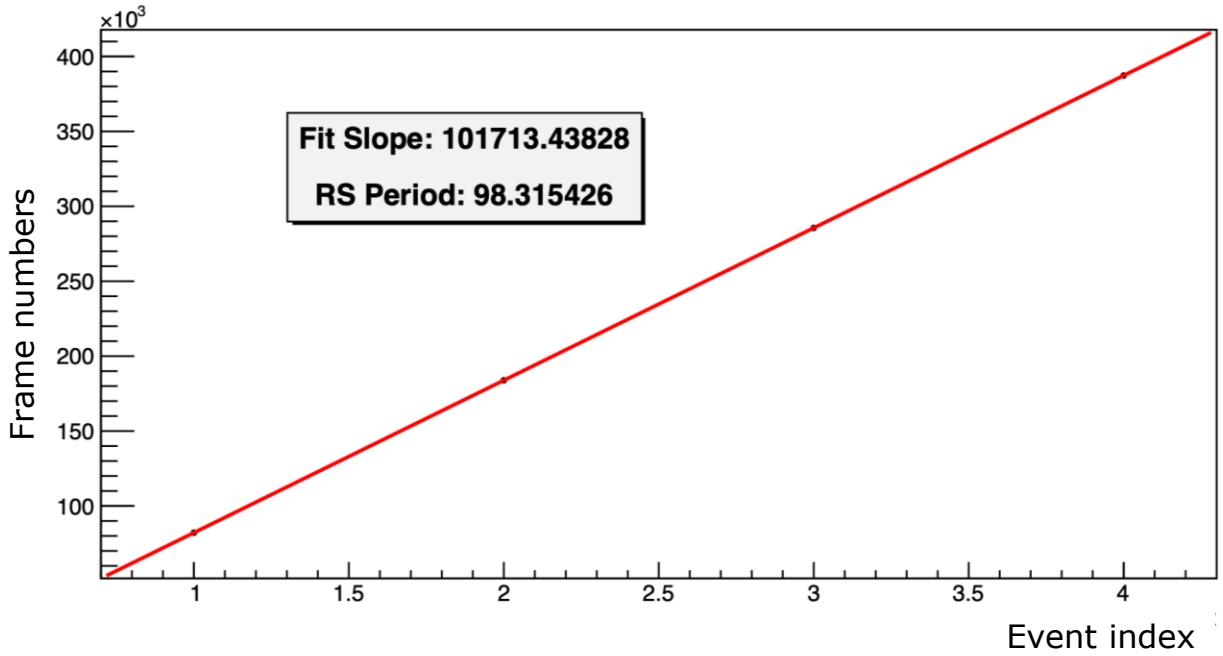
Extrapolation of average power consumption

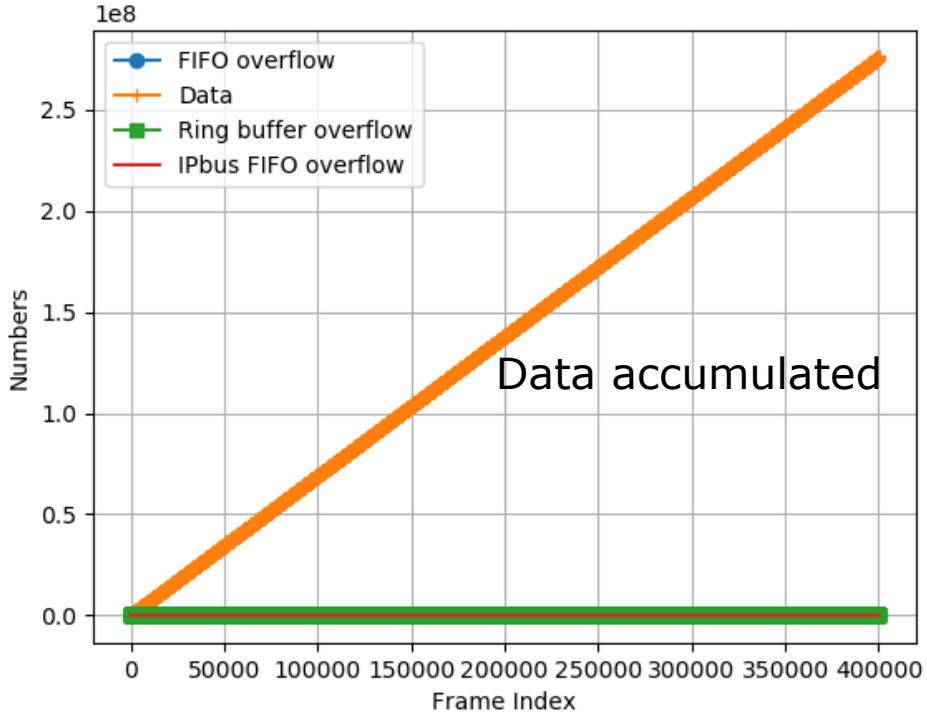
	512*192 (JadePix3)	512*1024 (Full-sized chip)
Matrix	3.15 mA	16.79 mA
Zero suppression and data buffering	12.47 mA	66.47 mA
Shared modules	46.82 mA	46.82 mA
Sum	62.44 mA	130.08 mA

Rolling Shutter Readout

Sheng DONG, Hulin WANG, Yunpeng LU

- Frame period (**Integration time**)
  - Event interval: 10 s
  - Count the frame numbers between 2 events
  - Frame period: **98.315 μs**
- Stability test
  - Hit number per event: 2048
  - Event interval: 110 μs
  - Data throughout: **595.8 Mbps * 39.3 s**

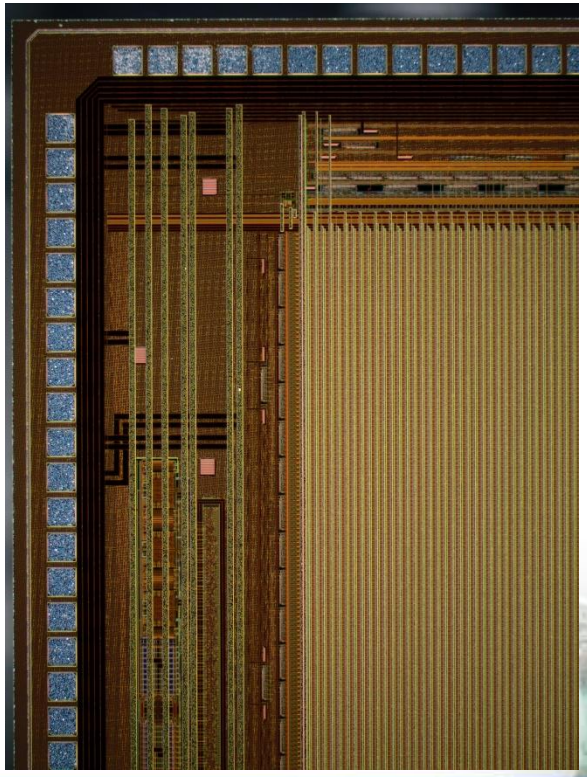




Summary

- JadePix3 is designed for the baseline scheme of **double-sided** structure
  - Optimized for high resolution, low power and modest readout speed
- Portable and reliable **test systems** in IHEP and CCNU
- Performance **consistent with the design** targets
  - Low threshold and noise
  - Single point resolution 3 ~ 5 μm
  - Low power < 100 mW/cm^2
  - Integration time < 100 μs
- A success of collaboration and teamwork
  - Still looking for beam test opportunity

Microscopic view of JadePix3
(Top-left corner)



JadePix3 study group

- IHEP: Ying Zhang, Yang Zhou, Zhigang Wu (graduated), Jing, Dong, Yunpeng Lu, Qun OuYang
- CCNU: Yang Ping, Weiping Ren, Le Xiao, Di Guo, Chenxing Meng (graduated), Anyang Xu (graduated), Sheng Dong, Hulin Wang, Xiangming Sun
- SDU: Liang Zhang
- Dalian Minzu Unv: Zhan Shi

Thank you for your time!