Plan for flex PCB design

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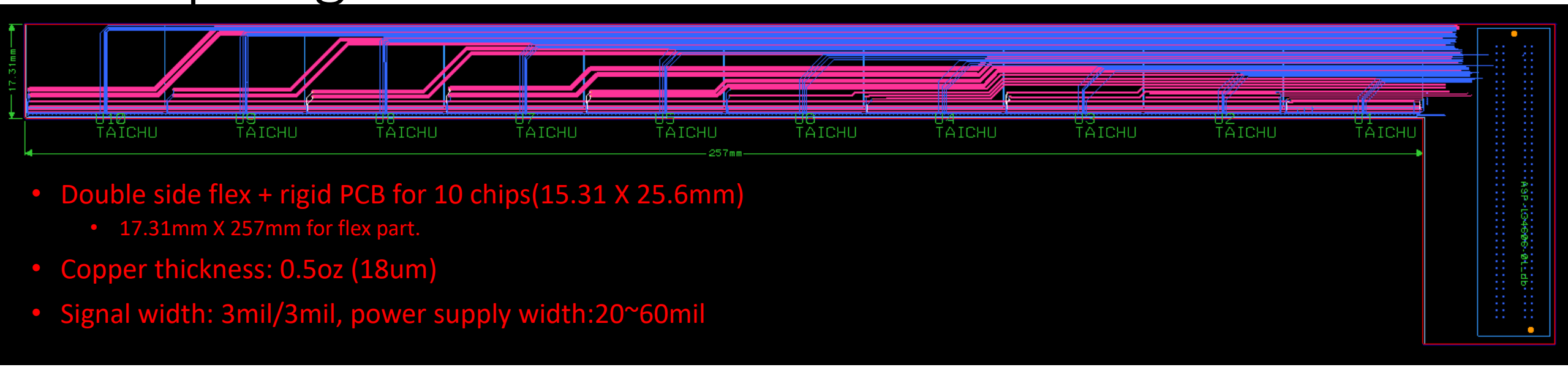
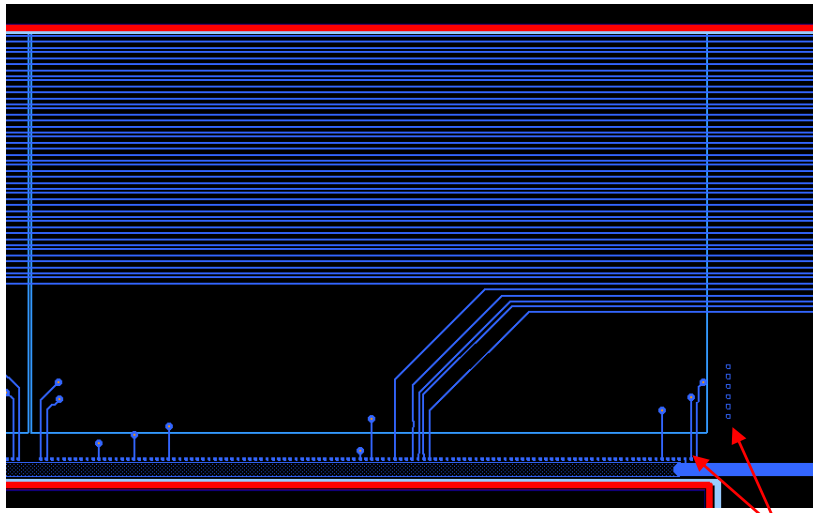
Topological

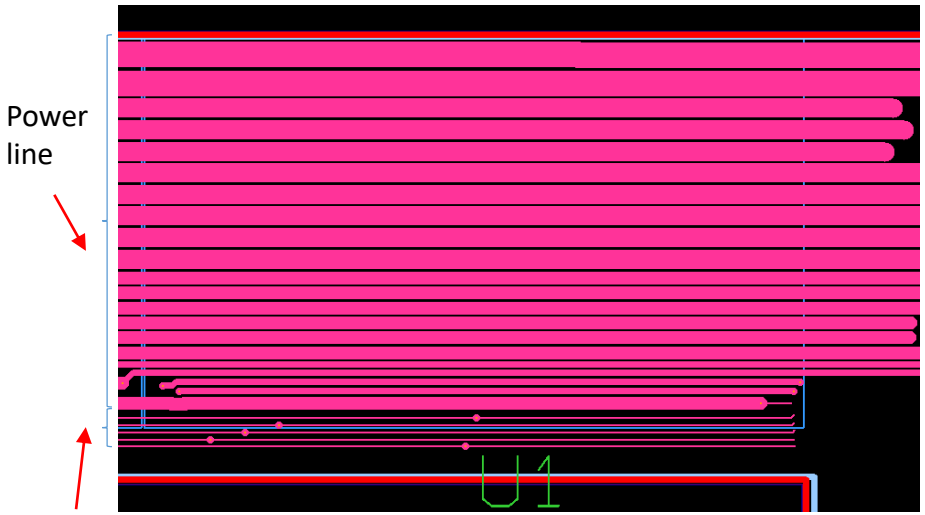


- Double side flex + rigid PCB for 10 chips(15.31 X 25.6mm)
  - 17.31mm X 257mm for flex part.
- Copper thickness: 0.5oz (18um)
- Signal width: 3mil/3mil, power supply width:20~60mil



Top side

Bonding pad



Bottom side

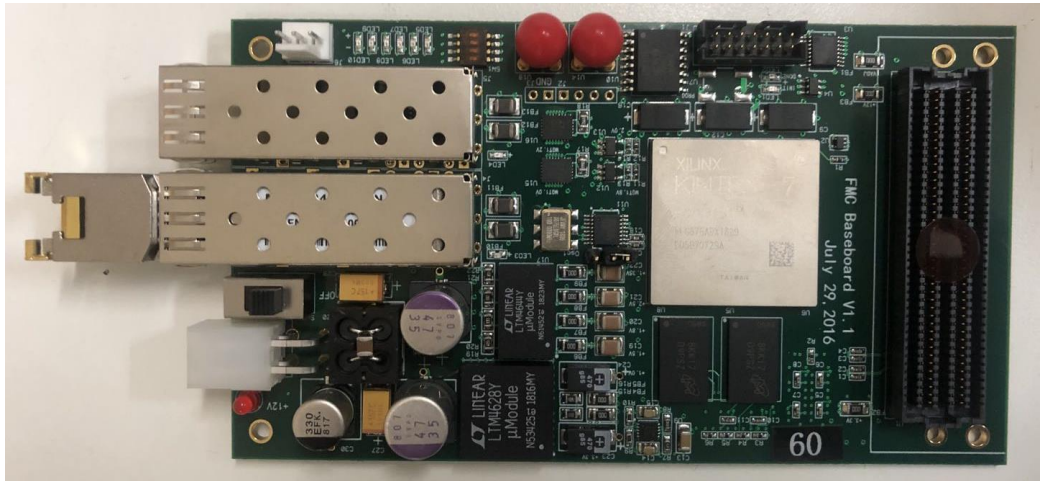
- Independent signals(3 single-end and 1 differentials):
  - CLK40M, SPI_CSB, DOUT_P, DOUT_N, SER_VALID
- Shared signals
  - APULSE, VRESET, VHIGH, VLOW, TRIGGER, SPI_MISO , *TP_IO* (6 single-end):
  - Inter-conn signal(6 single-end)
- Power supply
  - VDDD, VDDA, PWELL, GND

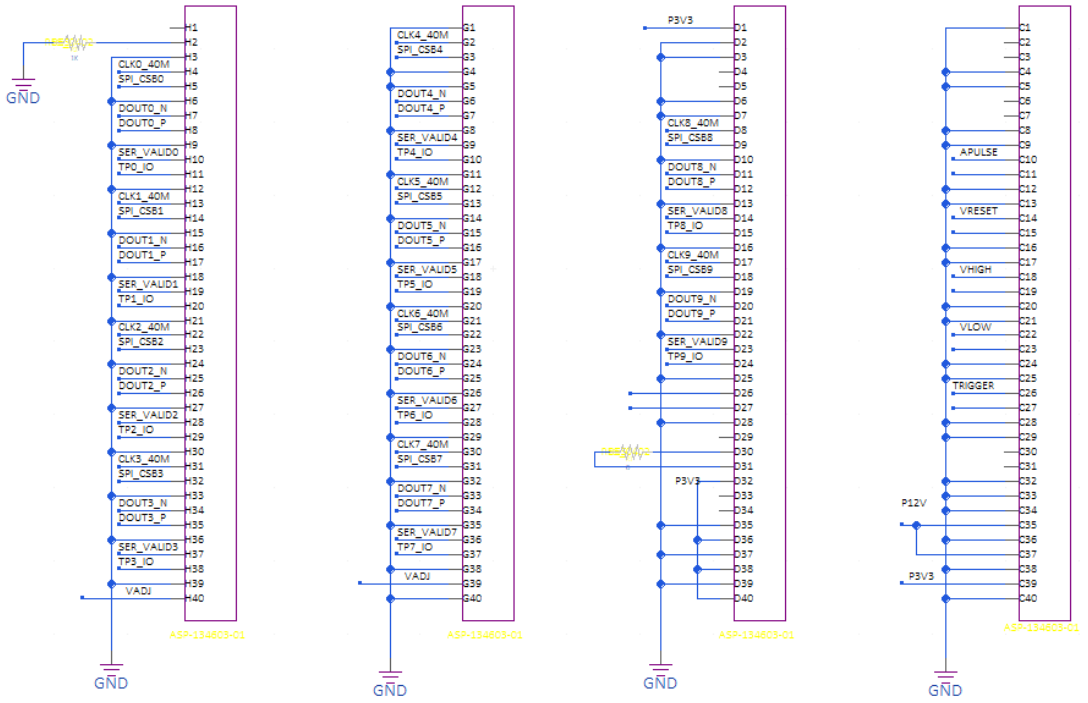
Some calculation

- Resistance of PCB power line
  - R = ρ L/S = 0.0175*0.0256/(0.015*1) = 0.03Ω for 1 chip length, 1mm width.
  - For VDDA and PWELL(0.5mm), I < 8.3mA
    - The 10th chip at the far-end of ladder, $V_{dropmax}$= 0.12 X 55 X 8.3mA= 54.78mV
  - For VDDD and GND(0.625mm), I ≈ 0.21A
    - $V_{dropmax}$ = 0.48*0.21A = 0.1V
- Dedicated power filter need to be designed on the rigid PCB which close to the chips
- Synchronized clocks for each chip

Readout test board

- General purpose FMC carry board
- FMC connector, ASP-124606,01 male LPC, 8.5mm height (34 pairs signals + 2 digital power)
- Ethernet readout: SiTCP IP to PC
- DDR 2GB on board





FMC interface

Plan

- 2021.4-2021.6: finish the design of first flex cable for multiple chips
- 2021.7-2021.10: Test and modification
- 2021.10-2021.12: Combine test with detector and DAQ.