Scintillator Setup

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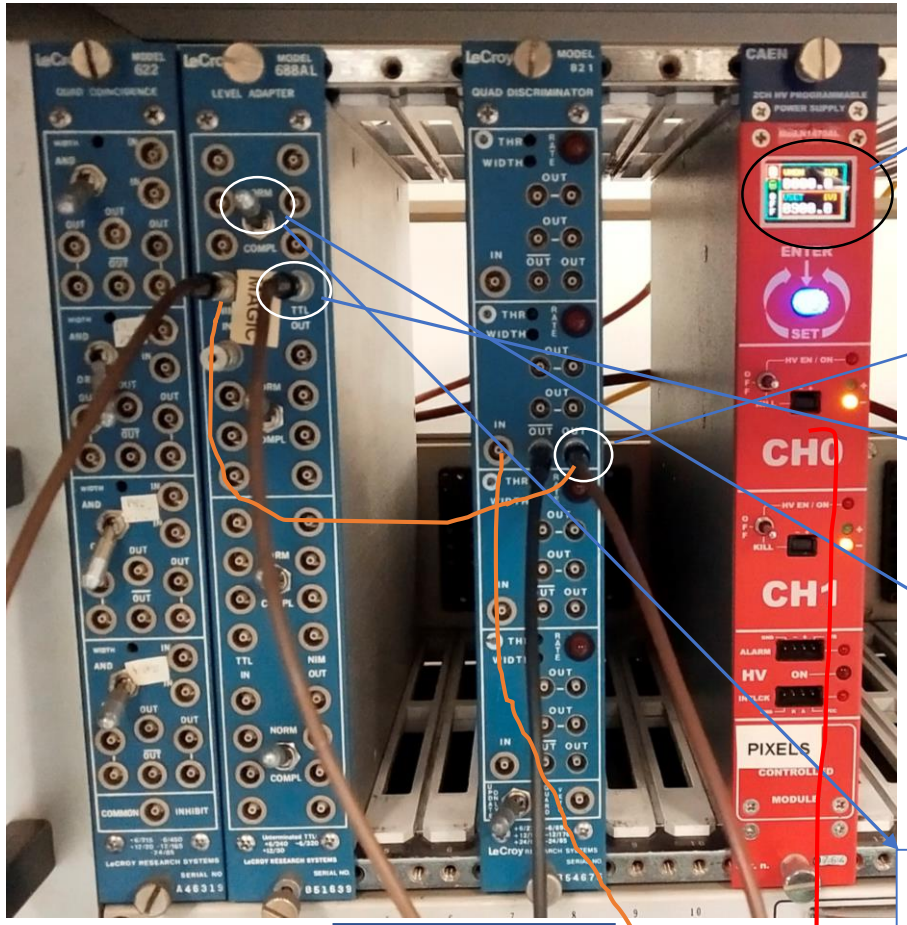
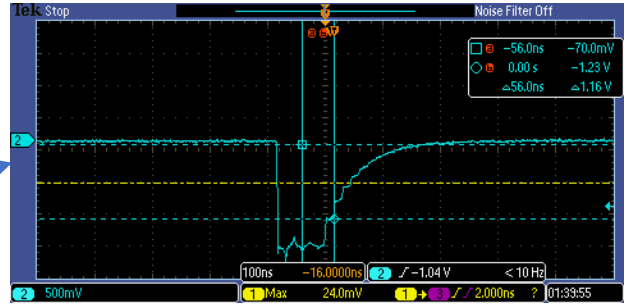
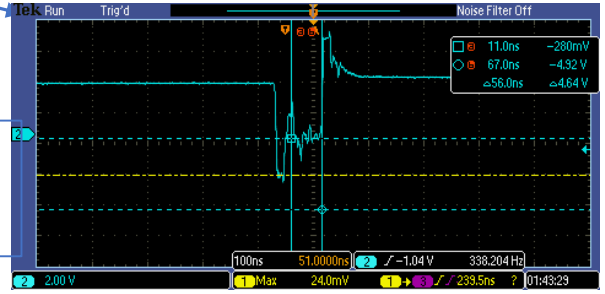
Scintillator setting



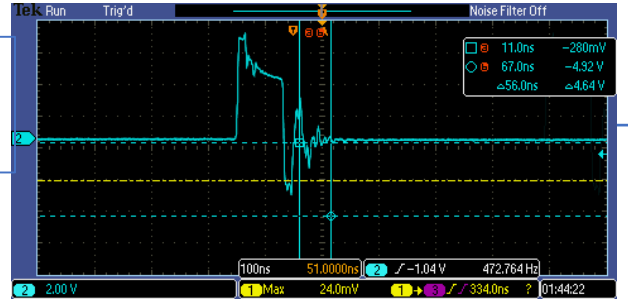
-900V

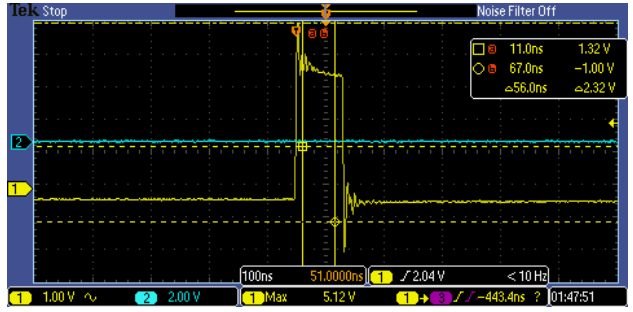


NORM TTL



COMPL TTL





- High Voltage source set to -900V
- Negative OUTD signal of 100 ns pulse with -1.5 V
- NIM to TTL, set to the COMPL to obtain the positive TTL
- The Lemo to BNC connector has a big signal ringing due to the impedance matching. With the oscilloscope probe seems better.

Sr.90

Readout in trigger mode

TaichuPix1

Scintillator

Internal trigger latency Configuration

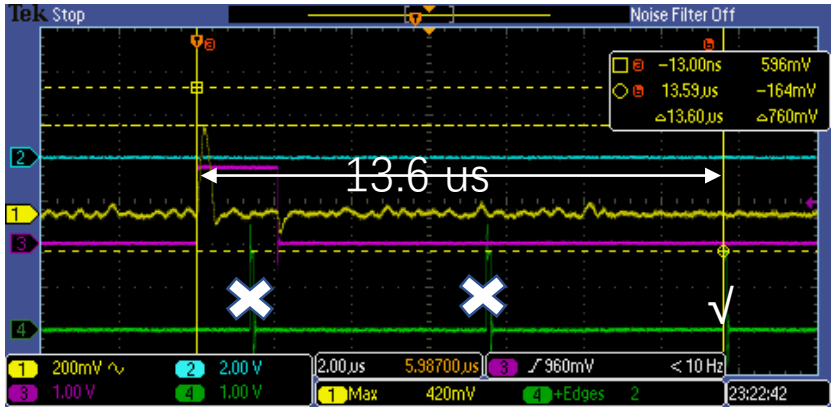


Fig 1 Internal trigger from FPGA

```
SPI_WRITE (1,0x7C);
SPI_WRITE (2,0x78);
SPI_WRITE (3,0xE0);

 for(k=0;k<300;k++)
          {
            SPI_WRITE(26,0);
          }
 SPI_WRITE (1,0x7C);
 delay  (10us)
APULSE;
Trigger_delay(13.2 us);
 SPI_WRITE (1,0x74);
```

```
for(j=0;j<260;j++)
        {
        SPI_WRITE(26,0);
data1= READ_DATA(data);
data2= READ_DATA(data);
data3= READ_DATA(data);
data4= READ_DATA(data);
 valid=(data1>>7)&0x00000001;
 ts=(((data1&0x7F)<<1)+((data2>>7)&0x01));
 col=(((data2&0x7F)<<2)+((data3>>6)&0x03));
 row=(((data3&0x07)<<4)+((data4>>4)&0x0F));
 pat=data4&0x0000000F;
 }
```

read out FIFO2

```
n=0
valid=  1,ts= 68,col= 30,row=  2,pat=  0
valid=  1,ts= 68,col= 30,row=  1,pat=  0
valid=  1,ts= 68,col= 30,row=  0,pat=  0
n=1
valid=  1,ts=192,col= 30,row=  2,pat=  0
valid=  1,ts=192,col= 30,row=  1,pat=  0
n=2
valid=  1,ts=164,col= 30,row=  2,pat=  0
valid=  1,ts=164,col= 30,row=  1,pat=  0
valid=  1,ts=164,col= 30,row=  0,pat=  0
n=3
valid=  1,ts= 76,col= 30,row=  2,pat=  0
valid=  1,ts= 76,col= 30,row=  1,pat=  0
n=4
valid=  1,ts= 56,col= 30,row=  2,pat=  0
valid=  1,ts= 56,col= 30,row=  1,pat=  0
valid=  1,ts= 56,col= 30,row=  0,pat=  0
n=5
valid=  1,ts=216,col= 30,row=  2,pat=  0
valid=  1,ts=216,col= 30,row=  1,pat=  0
n=6
valid=  1,ts= 84,col= 30,row=  2,pat=  0
valid=  1,ts= 84,col= 30,row=  1,pat=  0
valid=  1,ts= 84,col= 30,row=  0,pat=  0
```

- Injected a pulse signal to three pixels (Col30,Row 0/1/2)
- Set a trigger latency of 3 us, timestamp uncertain selection window of 175 ns (175/25=7)
- Scan the delay of the moment to read out the data. With this internal trigger setting, the delay between the injected pulse and trigger pulse should be 13.6 us

1) Set the initial value to register 1,2,3
2) Empty FIFO2
3) Set SMOD to “1” stop receive data from pixel array
4) Delay for a while(~10us)
5) Inject Apulse
6) Set a delay of the trigger pulse

7) Set SMOD to “0”to receive the data of the pixel array
8) Read the FIFO2 with register 26 and 27

External trigger latency Configuration

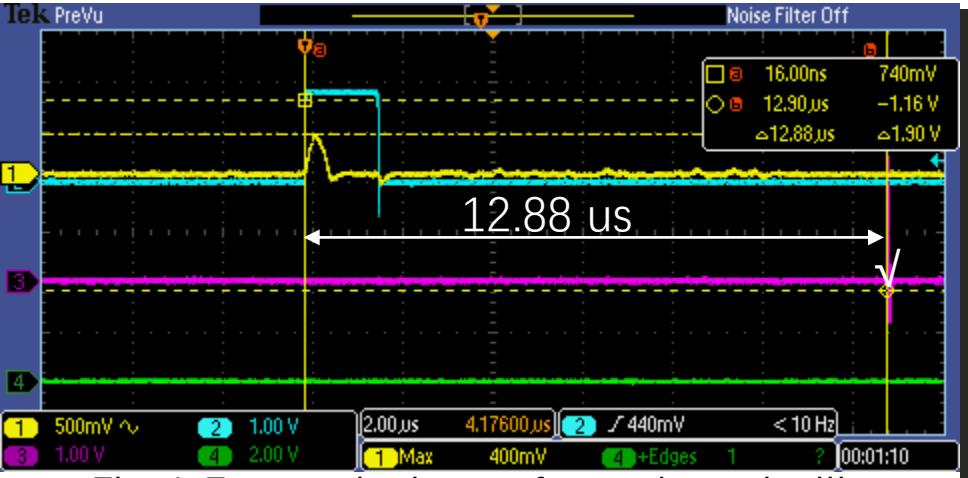
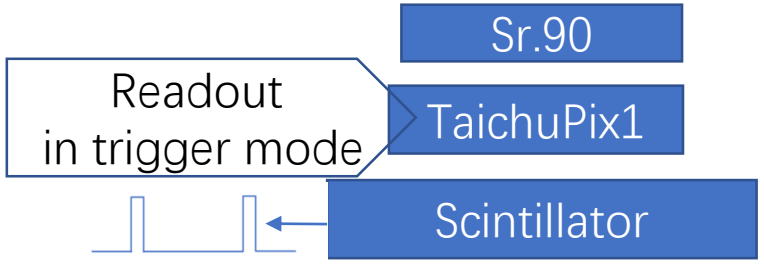


Fig 1 External trigger from the scintillator

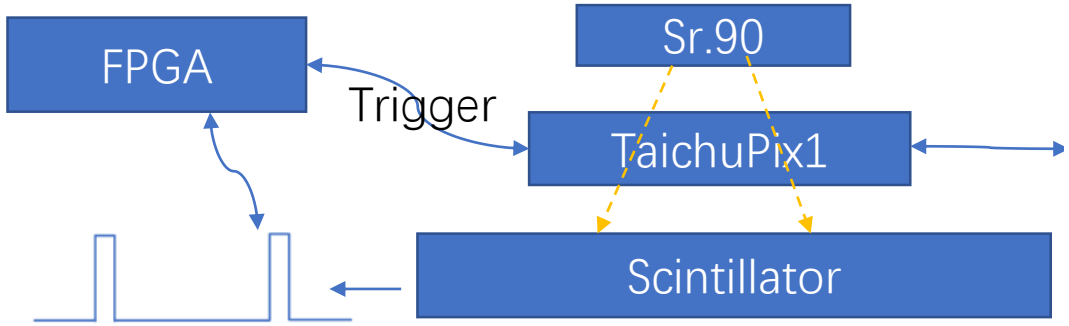



```
cnt1=538
cnt2=6517
valid=  1,ts= 87,col= 14,row= 71,pat=  0
cnt2=13541
valid=  1,ts= 87,col= 14,row= 70,pat=  0
cnt2=20720
valid=  1,ts= 87,col=  9,row= 43,pat=  0
cnt1=540
cnt1=539
cnt2=6526
valid=  1,ts=143,col= 16,row=108,pat=  0
cnt2=13502
valid=  1,ts=143,col= 16,row=107,pat=  0
cnt1=539
cnt1=540
cnt1=538
cnt1=539
cnt1=540
cnt2=6577
valid=  1,ts=167,col= 22,row=107,pat=  0
cnt2=13620
valid=  1,ts=167,col= 22,row=106,pat=  0
cnt2=20502
valid=  1,ts=167,col= 22,row=104,pat=  0
cnt2=27204
valid=  1,ts=167,col= 20,row=116,pat=  0
```

- Scintillator pulse is connected to the FPGA as a trigger to the system readout
- The Chip is placed in the middle between the Sr.90 and scintillator
- Calibrate the latency with the APULSE, an APULSE is generated as soon as the FPGA received a trigger
- Remove the APULSE ,then readout data with the Sr.90 injection.

1) The trigger will reset a 32bits counter inside FPGA, the counter is running at 20MHz
2) cnt1 is the 540(540x50ns =27 us) when the FIFO2 starts to readout, and cnt2 is the moment when the data is read out.

Hit map and cluster with external trigger




```
While(! Trigger Start)
    SPI_WRITE (1,0x7C);
    SPI_WRITE (2,0x78);
    SPI_WRITE (3,0xE0);

    for(k=0;k<300;k++)
            {
              SPI_WRITE(26,0);
            }
    SPI_WRITE (1,0x7C);
    delay  (10us)
   APULSE;
  Trigger_delay(13.2 us);
   SPI_WRITE (1,0x74);
```

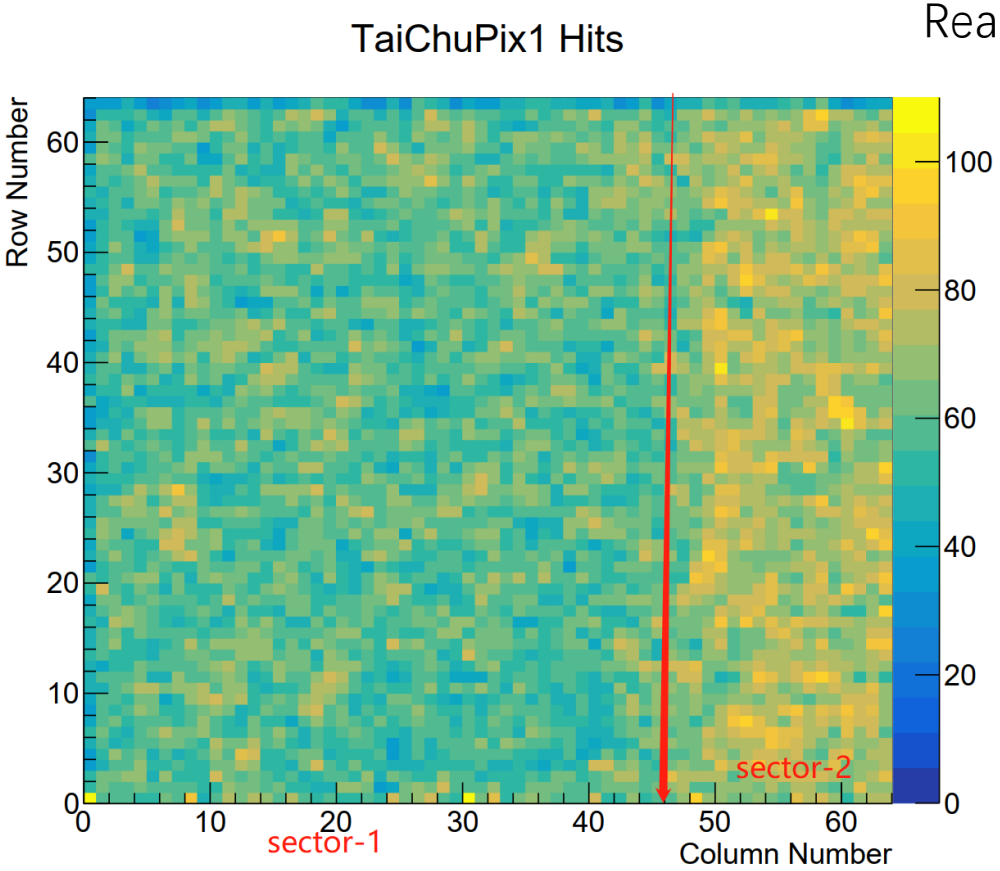
Step1

Readout

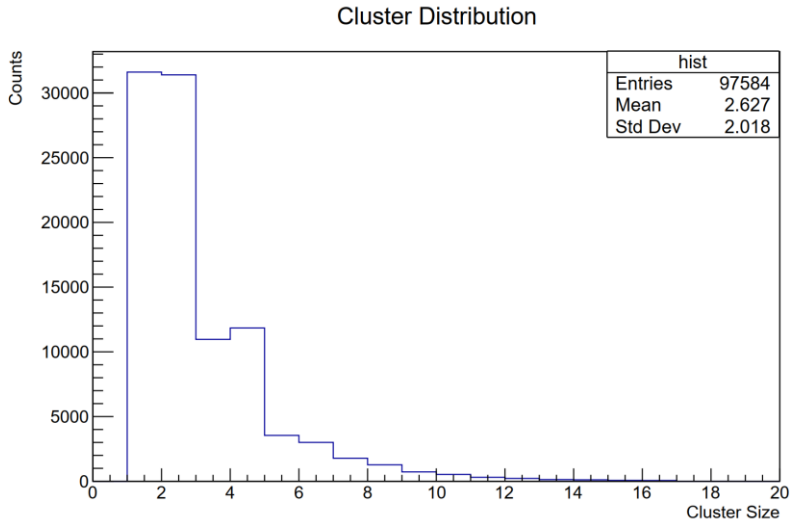
```
for(j=0;j<260;j++)
        {
        SPI_WRITE(26,0);
 data1= READ_DATA(data);
 data2= READ_DATA(data);
 data3= READ_DATA(data);
 data4= READ_DATA(data);
  valid=(data1>>7)&0x00000001;
  ts=(((data1&0x7F)<<1)+((data2>>7)&0x01));
  col=(((data2&0x7F)<<2)+((data3>>6)&0x03));
  row=(((data3&0x07)<<4)+((data4>>4)&0x0F));
  pat=data4&0x0000000F;
  }
```

read out FIFO2

Step2

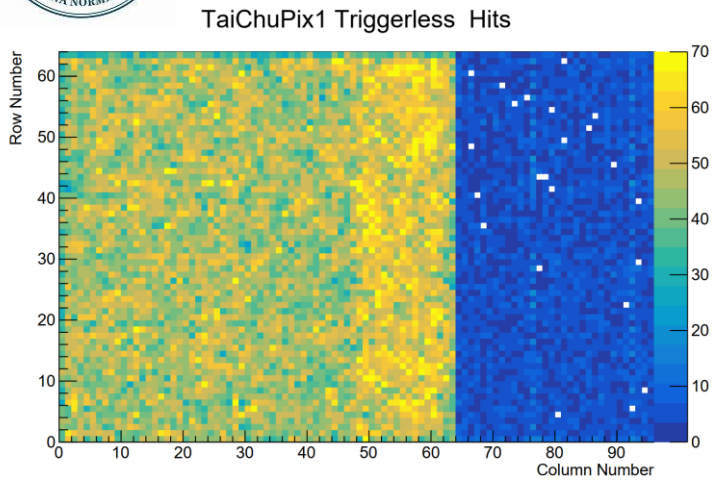


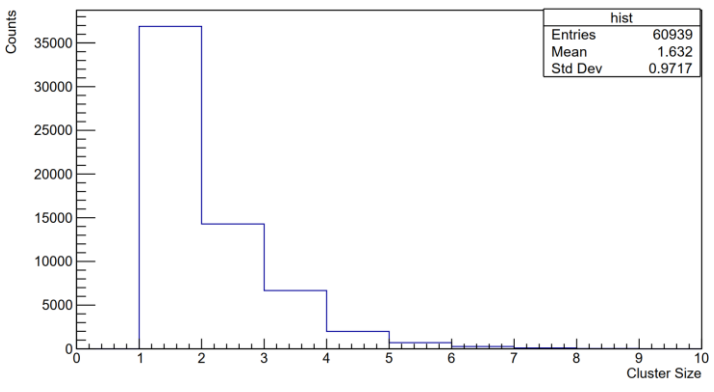

```
valid=1,  ts=53,   col=26,  row=27,  pat=0   4
valid=1,  ts=53,   col=25,  row=27,  pat=0   3
valid=1,  ts=53,   col=25,  row=26,  pat=0   2
valid=1,  ts=53,   col=25,  row=25,  pat=0   1
valid=1,  ts=253,  col=28,  row=32,  pat=0   1
valid=1,  ts=253,  col=28,  row=31,  pat=0   2
valid=1,  ts=253,  col=28,  row=30,  pat=0   1
valid=1,  ts=253,  col=10,  row=117, pat=0   2
valid=1,  ts=253,  col=10,  row=114, pat=0   1
valid=1,  ts=1,    col=21,  row=99,  pat=0   2
valid=1,  ts=125,  col=1,   row=126, pat=0   2
valid=1,  ts=101,  col=9,   row=57,  pat=0   2
valid=1,  ts=101,  col=9,   row=56,  pat=0   2
valid=1,  ts=93,   col=7,   row=108, pat=0   2
valid=1,  ts=93,   col=7,   row=96,  pat=0   2
valid=1,  ts=93,   col=6,   row=109, pat=0   2
valid=1,  ts=93,   col=30,  row=19,  pat=0   2
valid=1,  ts=93,   col=30,  row=16,  pat=0   2
valid=1,  ts=93,   col=19,  row=56,  pat=0   2
valid=1,  ts=93,   col=18,  row=57,  pat=0   2
valid=1,  ts=93,   col=11,  row=55,  pat=0   2
valid=1,  ts=93,   col=11,  row=54,  pat=0   2
```



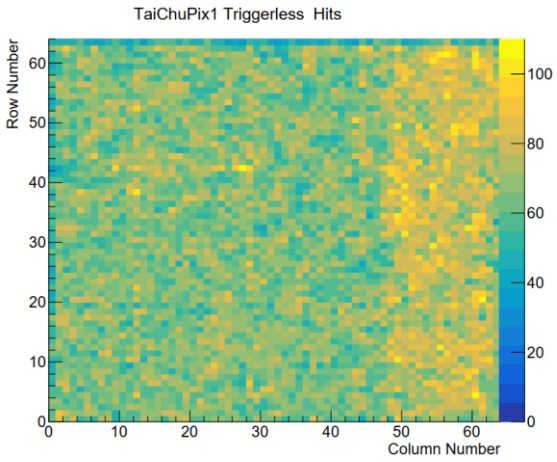
- Sector1/2 have different threshold cause the gradient view
- The data are triggered readout in debug mode.
- The average cluster size is 2.6.

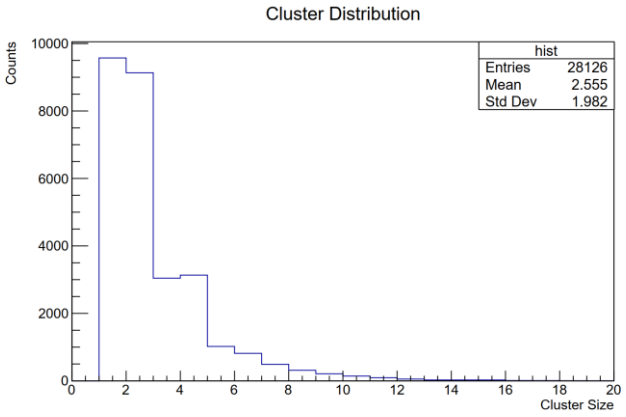
Data acquisition from LVDS interface



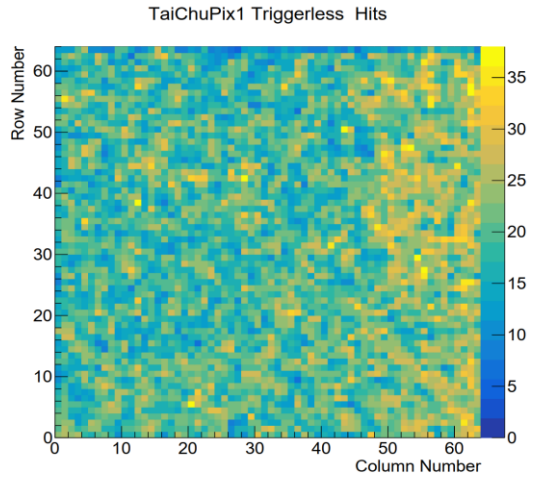


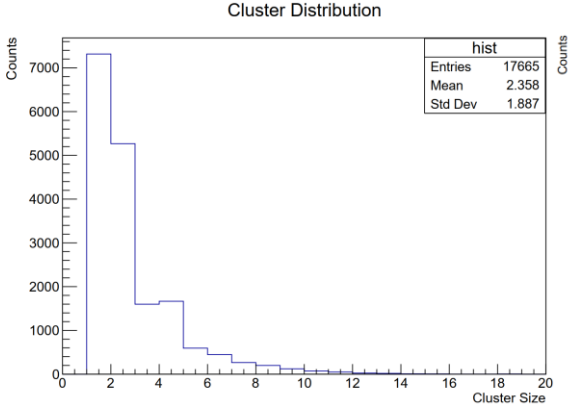
CPRN=0, compression
DOFREQ =01, 5MHz
Triggerless mode



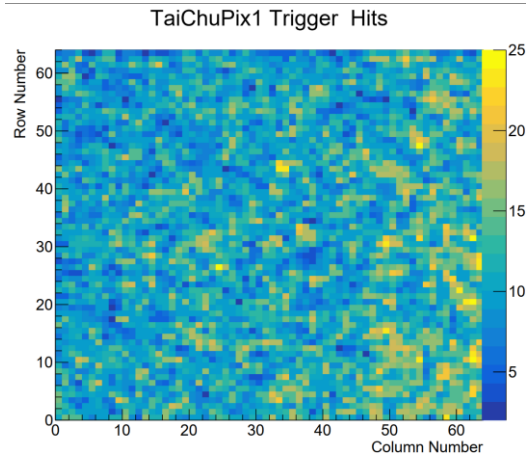


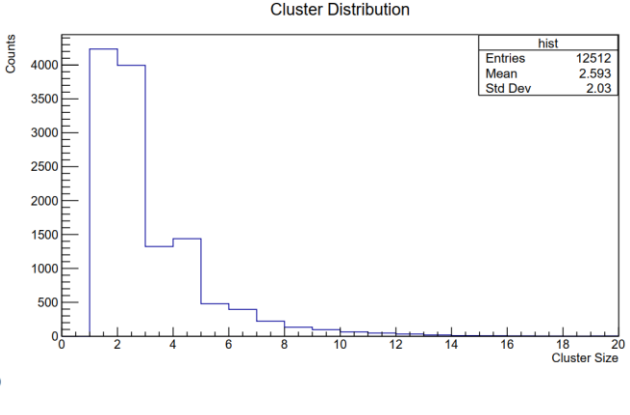
CPRN=1, no compression
DOFREQ =01, 5MHz
Triggerless mode





CPRN=1, no compression
DOFREQ =11, 20MHz
Triggerless mode





CPRN=1, no compression
DOFREQ =01, 5MHz
Trigger mode

Data acquisition from LVDS interface

DOFREQ =00, 2MHz

```
valid= 1,ts=210,col= 27,row= 94,pat= 0
valid= 1,ts=210,col= 27,row= 94,pat= 0
valid= 1,ts=210,col= 27,row= 94,pat= 0
valid= 1,ts=230,col= 19,row= 51,pat= 0
valid= 1,ts=230,col= 19,row= 51,pat= 0
valid= 1,ts=230,col= 19,row= 51,pat= 0
valid= 1,ts=230,col= 19,row= 48,pat= 0
valid= 1,ts=230,col= 19,row= 48,pat= 0
valid= 1,ts=230,col= 19,row= 48,pat= 0
valid= 1,ts=230,col= 18,row= 50,pat= 0
valid= 1,ts=230,col= 18,row= 50,pat= 0
valid= 1,ts=230,col= 18,row= 50,pat= 0
valid= 1,ts=230,col= 18,row= 49,pat= 0
valid= 1,ts=230,col= 18,row= 49,pat= 0
valid= 1,ts=230,col= 18,row= 49,pat= 0
valid= 1,ts= 50,col= 13,row= 43,pat= 0
valid= 1,ts= 50,col= 13,row= 43,pat= 0
valid= 1,ts= 50,col= 13,row= 42,pat= 0
valid= 1,ts= 50,col= 13,row= 42,pat= 0
valid= 1,ts= 98,col= 28,row= 82,pat= 0
valid= 1,ts= 98,col= 28,row= 82,pat= 0
valid= 1,ts= 98,col= 28,row= 82,pat= 0
valid= 1,ts= 22,col= 31,row= 74,pat= 0
valid= 1,ts= 22,col= 31,row= 74,pat= 0
valid= 1,ts= 22,col= 31,row= 74,pat= 0
```

DOFREQ =01, 5MHz

```
valid= 1,ts=225,col= 28,row= 84,pat= 0
valid= 1,ts=193,col= 28,row= 84,pat= 0
valid= 1,ts=129,col= 28,row= 84,pat= 0
valid= 1,ts= 97,col= 28,row= 84,pat= 0
valid= 1,ts= 1,col= 28,row= 84,pat= 0
valid= 1,ts=225,col= 28,row= 12,pat= 0
valid= 1,ts= 70,col= 31,row= 20,pat= 0
valid= 1,ts= 70,col= 31,row= 18,pat= 0
valid= 1,ts= 70,col= 22,row=121,pat= 0
valid= 1,ts= 70,col= 22,row=118,pat= 0
valid= 1,ts= 70,col= 13,row= 33,pat= 0
valid= 1,ts= 70,col= 13,row= 30,pat= 0
valid= 1,ts= 70,col= 2,row= 71,pat= 0
valid= 1,ts= 10,col= 27,row= 56,pat= 0
valid= 1,ts= 10,col= 27,row= 55,pat= 0
valid= 1,ts=182,col= 31,row= 40,pat= 0
valid= 1,ts=182,col= 31,row= 39,pat= 0
valid= 1,ts=182,col= 30,row= 41,pat= 0
valid= 1,ts=182,col= 30,row= 38,pat= 0
valid= 1,ts=182,col= 22,row= 99,pat= 0
valid= 1,ts=182,col= 22,row= 96,pat= 0
valid= 1,ts=182,col= 22,row= 95,pat= 0
valid= 1,ts=182,col= 21,row= 98,pat= 0
valid= 1,ts=182,col= 21,row= 97,pat= 0
valid= 1,ts=182,col= 21,row= 94,pat= 0
```

DOFREQ =10, 10MHz

```
valid= 1,ts=162,col= 12,row=123,pat= 0
valid= 1,ts=162,col= 12,row=122,pat= 0
valid= 1,ts=162,col= 12,row=120,pat= 0
valid= 1,ts=162,col= 11,row=122,pat= 0
valid= 1,ts=162,col= 11,row=121,pat= 0
valid= 1,ts=162,col= 1,row= 64,pat= 0
valid= 1,ts=162,col= 0,row= 65,pat= 0
valid= 1,ts=162,col= 0,row= 64,pat= 0
valid= 1,ts= 74,col= 29,row= 0,pat= 0
valid= 1,ts= 74,col= 28,row= 2,pat= 0
valid= 1,ts= 74,col= 26,row= 35,pat= 0
valid= 1,ts= 74,col= 26,row= 34,pat= 0
valid= 1,ts= 74,col= 26,row= 33,pat= 0
valid= 1,ts= 74,col= 9,row= 98,pat= 0
valid= 1,ts= 74,col= 9,row= 97,pat= 0
valid= 1,ts= 74,col= 9,row= 96,pat= 0
valid= 1,ts= 74,col= 7,row= 91,pat= 0
valid= 1,ts= 74,col= 6,row= 90,pat= 0
valid= 1,ts= 74,col= 4,row= 21,pat= 0
valid= 1,ts= 74,col= 4,row= 20,pat= 0
valid= 1,ts=146,col= 21,row= 6,pat= 0
valid= 1,ts= 18,col= 30,row=107,pat= 0
valid= 1,ts= 18,col= 10,row=125,pat= 0
valid= 1,ts= 18,col= 10,row=124,pat= 0
valid= 1,ts= 18,col= 10,row=123,pat= 0
valid= 1,ts= 18,col= 10,row= 64,pat= 0
valid= 1,ts= 18,col= 9,row= 65,pat= 0
```

DOFREQ =11, 20MHz

```
valid= 1,ts= 94,col= 28,row=121,pat= 0
valid= 1,ts= 94,col= 22,row= 27,pat= 0
valid= 1,ts= 94,col= 21,row=124,pat= 0
valid= 1,ts= 94,col= 16,row= 84,pat= 0
valid= 1,ts= 94,col= 16,row= 80,pat= 0
valid= 1,ts= 94,col= 2,row= 38,pat= 0
valid= 1,ts=238,col= 24,row= 35,pat= 0
valid= 1,ts=238,col= 24,row= 89,pat= 0
valid= 1,ts=238,col= 16,row=122,pat= 0
valid= 1,ts=238,col= 10,row= 12,pat= 0
valid= 1,ts=238,col= 9,row= 92,pat= 0
valid= 1,ts=238,col= 8,row= 94,pat= 0
valid= 1,ts=238,col= 4,row= 17,pat= 0
valid= 1,ts=206,col= 30,row= 94,pat= 0
valid= 1,ts=206,col= 30,row= 92,pat= 0
valid= 1,ts=206,col= 29,row= 48,pat= 0
valid= 1,ts=206,col= 29,row= 46,pat= 0
valid= 1,ts=206,col= 28,row= 50,pat= 0
valid= 1,ts=206,col= 28,row= 48,pat= 0
valid= 1,ts=206,col= 31,row= 61,pat= 0
valid= 1,ts=206,col= 9,row= 4,pat= 0
valid= 1,ts=206,col= 2,row=118,pat= 0
valid= 1,ts=206,col= 2,row=116,pat= 0
valid= 1,ts=206,col= 1,row=119,pat= 0
valid= 1,ts=206,col= 0,row= 5,pat= 0
```

- With the LVDS interface set to 160 MHz, when the data speed set to 2 MHz, every pixel will be read out 3 times.
- Since the matched speed of the interface is 5MHz*32bits=160Mbps, there are no obvious errors when the DOFREQ is set with 10MHz or 20MHz, but it may affect the cluster size distribution.